OTI-8511

DVB-S Compliant Demodulator

Technical Reference Manual

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DVB-S Compliant Demodulator
July 1998

Technical Reference Manual
Version 1.0

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v1.0

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CHAPTER 1 OVERVIEW

1.1 FEATURES

- Fully DVB compliant
- Continuously variable symbol rate from 2 to 45 MBaud
- Utilizes fixed frequency sampling clock
- Internal digital root raised cosine filter
- Less than 0.25 dB implementation loss
- Frequency multiplexing capability
- Automated frequency search
- Internal bias cancellation
- Both wideband and narrowband AGC
- Noise calibration for antenna steering
- Output data rate as high as 55 Mbps
- Interfaces directly with OTI-8211 MPEG-2 decoder
- Simple interface with tuner and analog processing
- 8-bit parallel or I^2C host interface
- Flags TEI bit in the event of uncorrectable errors
- Includes accumulators for corrected and uncorrected errors

1.2 DESCRIPTION

The OTI-8511 digital demodulator for direct broadcast satellite receivers is a single-chip solution fully compliant with the European Telecommunications Standards Institute (ETSI) specification ETS 300 421. This chip integrates a variable rate matched filter, variable rate QPSK demodulator with a Viterbi decoder, deinterleaver and Reed Solomon decoder in a 100-pin PQFP package.

The OTI-8511, which is implemented in a 0.5 micron CMOS, triple layer metal process, provides variable rate capability while operating with a fixed frequency sampling clock. Digital samples of baseband I and Q data are generated by external A/D converters, then provided to the chip at a fixed sample rate. The root raised cosine (RRC) filters are implemented internally with fully digital techniques. Similarly, the symbol timing recovery and carrier phase tracking functions are performed entirely in the digital domain. This approach provides minimum constraints on external circuits, thus reducing system costs.

The OTI-8511 may be configured by an external processor for a specific symbol rate and carrier frequency along with loop gain parameters. The OTI-8511 provides an external AGC signal, which is used to control the level of the analog signal applied to the A/D converters. It also employs a digital AGC internally, which controls the gain applied to the output of the RRC filters. In addition, the OTI-8511 provides fully programmable sweep circuitry to aid in initial acquisition when large frequency offsets may be present.

The digital frequency translation capability of the OTI-8511 permits this part to be used in the single and channel per carrier (SCPC) applications. In this application, an entire transponder bandwidth containing many signals is sampled at a fixed rate. The digital oscillator within the OTI-8511 is programmed to the specific desired carrier frequency within that band to permit the selected signal to be passed through the baseband filter and processed by the demodulator circuits.

The OTI-8511 is well suited to the Integrated Receiver Decoder (IRD) for DVB-services. Typically in this application, the demodulator may be clocked with a common fixed frequency of 50 MHz, which is shared with the OTI-8211. The demodulator is commanded to either 22 or 27.5 MBaud by microcontroller commands. The forward error correction (FEC) supports the five coding rates: 1/2, 2/3, 3/4, 5/6, and 7/8.

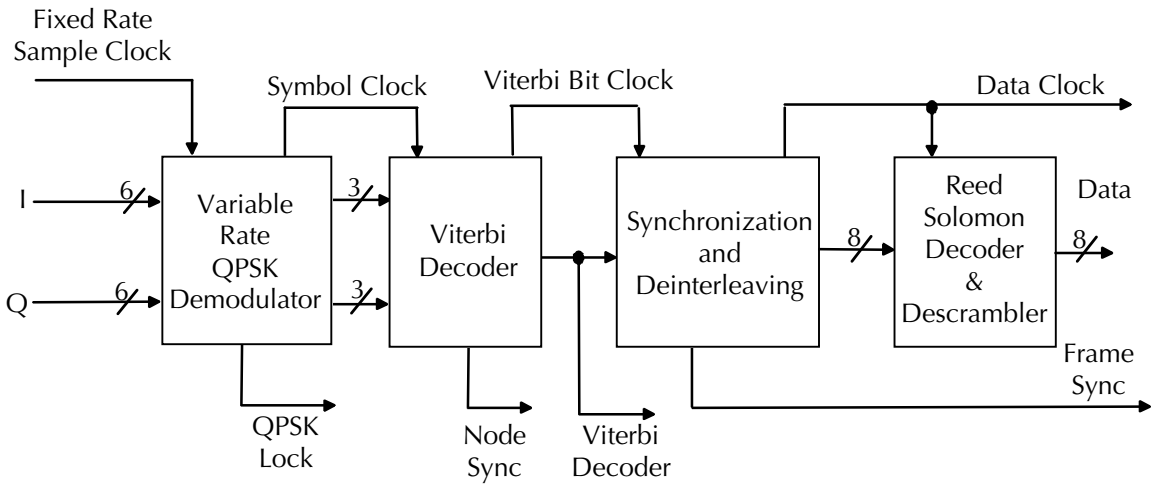

Figure 1-1: *Top-level Block Diagram*

CHAPTER 2 TECHNICAL OVERVIEW

2.1 TECHNICAL OVERVIEW

2.1.1 DEMODULATOR AND VITERBI DECODER

Variable Rate Demodulator

The block diagram below illustrates the overall configuration of the variable rate QPSK demodulator. Baseband in-phase (I) and quadrature (Q) inputs are applied to the demodulator at a fixed sampling rate. These digital samples are produced by A/D converters that employ AC coupling to minimize DC offset.

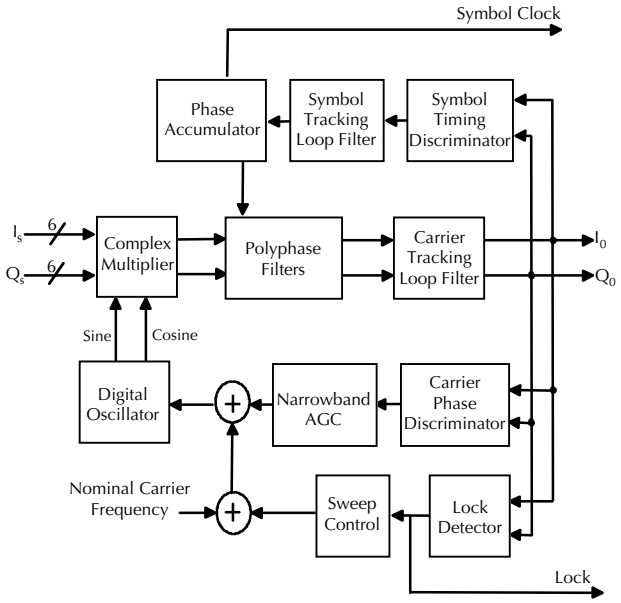

Figure 2-1: *Demodulator Block Diagram*

The carrier frequency error associated with these samples is removed digitally during tracking operations by a complex multiplier and a digitally controlled oscillator, sometimes called a numerically controlled oscillator (NCO).

A polyphase filter performs the RRC filtering of the frequency-corrected baseband samples. This filter is always configured to have an impulse response duration of 4 symbols regardless of the programmed symbol rate. For low symbol rates, a large number of samples are used, while for high symbol rates a relatively low number of samples are processed for each filter output. The outputs of the polyphase filters are applied to a digital narrowband AGC, which ensures that the signal is optimally scaled to the Viterbi decoder (to an accuracy of ±0.5 1) for optimum FEC performance.

In addition to optimizing performance of the Viterbi decoder, the digital narrowband AGC also ensures that the performance of the symbol timing and carrier tracking loops is independent of signal-level variations. An analog wideband AGC is also employed to ensure that the analog signal applied to the A/D converters is properly scaled.

Both the symbol timing and carrier tracking loops are implemented digitally, which eliminates the need for external connections to analog tuning components during steady state operation. This causes the requirements on the analog presampling filter to be relaxed, permitting a lower-cost analog front end. For systems that require a narrowband presampling filter and have the potential for significant frequency error in the LNB (several MHz), the OTI-8511 provides a high-resolution measure of carrier frequency to permit periodic readjustment of the front-end tuner frequency to compensate for drift. The host processor periodically reads the frequency register, then computes appropriate corrections to the tuner frequency.

Viterbi Decoder

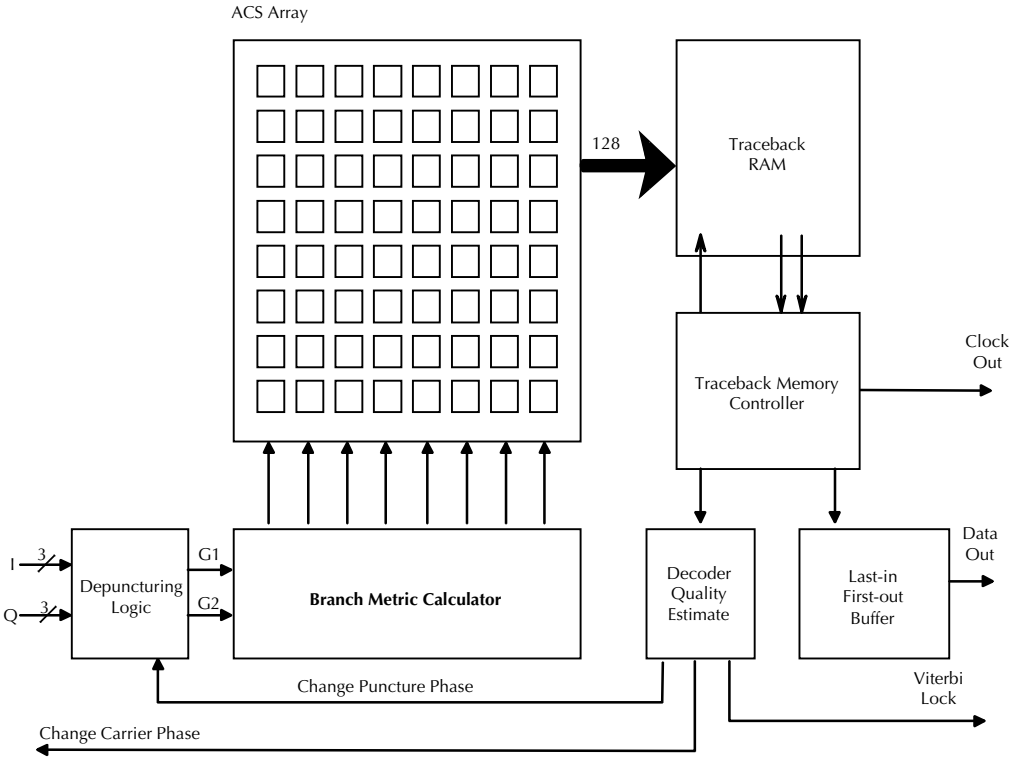

Figure 2-2: *Viterbi Decoder*

The Viterbi decoder accepts 3-bit soft decision samples of the I and Q components of the received signal. Once QPSK lock has been achieved, the decoder searches for the correct code rate, starting with rate 1/2, then proceeding to rate 2/3, 3/4, 5/6 and 7/8. Each of the possible synchronization phases at each rate is tested as well as the two possible carrier phase ambiguity conditions. Polarity reversal is corrected in the word synchronization logic. Viterbi lock is achieved when the trellis traceback algorithm converges, on the average, within a prescribed number of symbols.

Although the algorithm automatically tests for carrier phase ambiguity, there is no provision to automatically correct for spectral inversion. Spectral inversion can occur if the receiver chain, consisting of an LNB and tuner, provides an odd number of high side frequency translation operations. A system may be required to operate with different LNBs, some of which cause spectral inversion. This condition may be corrected by the host processor, which can set a bit in the OTI-8511 control register to correct for inversion.

The Viterbi decoder employs the radix four algorithm, which enables the decoder to process the maximum throughput with internal processing cycle time (twice the master clock cycle time). For symbol rates higher than half the sampling clock rate, some selections of code rate are invalid. The sufficient condition is that the data rate out of the Viterbi decoder must be less than the sample clock rate.

The output buffer reserializes the data that is made available, along with the Viterbi data clock, as external signals. These signals permit verification of the DVB specification, which is referenced to the Viterbi decoder output.

Autonomous Acquisition

The OTI-8511 provides several features to permit signal acquisition with minimal interaction with the host microcontroller. The host microcontroller must configure the OTI-8511 demodulator for a specific symbol rate, carrier frequency, carrier sweep conditions, and for tracking-loop bandwidths. The microcontroller should also monitor lock status to determine when acquisition is achieved. There are many provisions in the OTI-8511 to enable the system designer to implement custom algorithms for specific requirements.

The microcontroller first must set the lower edge of the carrier search range in the Carrier Frequency registers (04, 05, and 06). Then the processor configures the Carrier Sweep Step Size register (08, 09) to a value that is less than two times the carrier pull-in range. The number of symbols that dwell at each frequency is defined in registers 0A-0B and is typically set to a value of 500 to 2000. The total search range is set by the Number of Search Frequencies as defined in register 0C. The total sweep frequency range is this number times the Carrier Sweep Step Size. The sweep process stops automatically once QPSK carrier lock is detected by the OTI-8511. If no lock is detected, the sweep process continuously repeats. During the time when no signal is present, or when the carrier frequency is incorrect, the lock flag may intermittently switch between true and false, due to the nature of the lock detect algorithm. However, when a lock is achieved, the flag should remain valid continuously.

The QPSK demodulator may lock to any one of four different phase reference states, only one of which produces valid I and Q data as it was modulated at the transmitter. If the local phase reference is ±90° with respect to the true phase, the information provided to the Viterbi decoder will be unintelligible. If the Viterbi decoder is unable to achieve valid lock, it will reattempt lock with a 90° phase shift, without external intervention.

In the event that the local phase is 180° from the true phase, the data provided to the Viterbi decoder will be inverted, but otherwise valid. The code employed by the Viterbi decoder is transparent, thus the data from the Viterbi decoder will be inverted if the input is inverted. This situation is corrected in the word synchronization circuit. This circuit searches for the unscrambled sync word that occurs once per frame (every 204 bytes at the Viterbi output). Once correlation with the sync word is found, the data is reformatted as a series of bytes with the beginning of each 204 byte frame identified to provide the synchronization information required for the deinterleaver and the Reed Solomon decoder. If the polarity of the sync word is incorrect, the data is inverted before further processing without external interaction.

The OTI-8511 supports five different code rates: 1/2, 2/3, 3/4, 5/6, and 7/8. When rate 1/2 is employed, there is a one-to-one correspondence between incoming I and Q samples and G1 and G2 terms required by the Viterbi decoder. The higher rates employ punctured coding techniques, which periodically cause either a G1 or G2 term to be deleted. The puncturing pattern can have 6 possible ambiguity states for rate 2/3, four states for rate 3/4, six states for rate 5/6 and eight states for rate 7/8. As part of the Viterbi decoding acquisition process, each puncturing state of each code must be tested. Total acquisition requires search of 26 different combination conditions. The process starts with rate 1/2 coding and proceeds sequentially to rate 3/4, 2/3, 5/6, and 7/8.

The table below illustrates a typical acquisition process. For this example, the symbol rate is one half the clock rate. The code rate is set to 5/6, which requires 13 trial and errors before node sync is achieved. The carrier search logic requires 10 dwells at different frequencies (500 symbols per dwell) before demodulator lock is achieved.

Example: Acquisition Timing

	Bit Times	Symbols	Clock Cycles
Carrier Search	8,333	5,000	10,000
Viterbi Node Sync	2,652	1,591	3,182
Byte Sync	16,000	9,600	19,200
Deinterleaver Flush	19,584	11,750	23,500
Reed Solomon	1,632	979	1,958
	48,201	**26,950**	**57,840**

The total time required for acquisition could vary widely, depending upon the carrier search range and the time required for Viterbi node sync. For this example, however, the byte sync time and the time required to flush the deinterleaver dominates the total time. If a 50 MHz clock were employed, the total acquisition time would be 1.156 milliseconds for this example.

False Locks and Spectral Inversion

A QPSK signal will have inherent false lock states at carrier frequency offsets that are integer multiples of 1/4 of the symbol rate. At these carrier frequency offsets valid QPSK lock can be achieved, but Viterbi node synchronization cannot be achieved as the data is meaningless. Most DBS signals that have symbol rates of 20 MBaud or higher will not experience false lock because the carrier frequency uncertainty is less than 1/4 the symbol rate.

The OTI-8511 is designed to process low data rate signals, which may experience false lock, particularly at high signal-to-noise ratio conditions. The OTI-8511 will permit recovery from false lock with some added host processor interaction. Specifically, the processor must initialize the internal carrier frequency search hardware to search over a carrier frequency range of less than 1/4 the symbol rate. If QPSK lock is achieved, but no Viterbi lock is achieved, the processor should assume this is a false carrier lock, then program the OTI-8511 to search another carrier frequency range covering less than 1/4 of the symbol rate. When both QPSK and Viterbi lock have been achieved, the search is completed. This technique is reliable because the OTI-8511 utilizes a fixed-frequency clock, which is not subject to inaccuracies associated with analog VCOs. This accuracy ensures that the multiple search ranges are perfectly continuous with respect to each other and no overlap.

Spectral inversion occurs when the transmit-receive chain of the system uses an odd number of high-side frequency translations. The symptoms of spectral inversion are the same as for false lock, i.e. valid QPSK lock can be achieved but without Viterbi node synchronization. Hence, if after having swept the entire band of interest with the OTI-8511 only false lock conditions have been achieved, the host should assume that a spectral inversion exists and configure the OTI-8511 appropriately (see register 0Eh).

2.1.2 REED SOLOMON DECODER

The serial output from the Viterbi is provided to the Word Sync circuit, which searches for the 8-bit frame sync byte, which occurs every 204 bytes. By detecting the polarity of the sync byte, this module can correct polarity reversals in the data provided by the Viterbi decoder.

Byte parallel data is provided to the convolutional deinterleaver, which reorders the received symbols. This process causes errors, which typically occur in bursts from the Viterbi decoder, to be distributed randomly over many blocks. This deinterleaved data is then provided to the Reed Solomon decoder, which can reduce an error rate of 2x10-4 from the Viterbi decoder to less than 1x10-10 (quasi error-free). The Reed Solomon decoder accepts input data in blocks of 204 bytes and produces error corrected blocks of 188 bytes.

The final process is descrambling, not to be confused with the descrambling that is part of conditional access. The purpose of scrambling the transmitted data and performing the inverse in the receiver is to ensure that the spectrum of the transmitted waveform is always evenly distributed without significant discrete spectral lines. Without the scrambling/descrambling process, a regularly repeating transmitted sequence would result in strong spectral components and could interfere with other signals in the same satellite transponder.

Note: This also allows AC coupling in the receiver, which is important in zero-IF architectures.

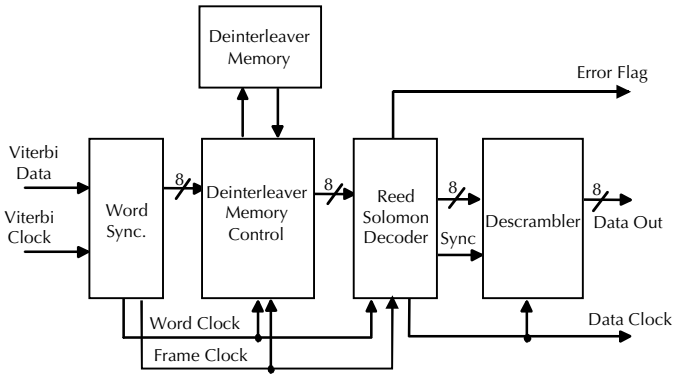

Figure 2-3: *Reed Solomon Decoder*

2.1.3 NOISE MEASUREMENT CIRCUIT

When the DBS system is being installed in the home, the most difficult part of the installation is accurate pointing of the antenna toward the satellite. Inaccurate pointing results in loss of margin and greater potential for outages in adverse weather conditions. Existing systems use information from the demodulator forward error correction circuits to provide a measure of antenna pointing. Unfortunately, this method is useful over a range of only several dB above system threshold.

The OTI-8511 employs a unique circuit for accurate measure of signal strength over a 20 dB range of signal-to-noise ratio. This method, illustrated in Figure 2-5, makes use of the fact that the demodulator provides 8 bits of resolution for each of the quadrature output components. This high resolution provides a means of measuring the noise component with great accuracy. The 8-bit in-phase demodulator filter output is detected by an absolute value circuit, then passed through a low pass IIR filter to provide a measure of average signal amplitude. Each sample is then subtracted from this average amplitude to provide an instantaneous noise sample. The absolute value of these noise samples are then averaged by a second filter to provide a measure of the noise, which is roughly proportional to the noise power and inversely proportional to signal-to-noise ratio. Figure 2-6 illustrates the results of simulations under different noise conditions. This figure illustrates that for signal-to-noise ratio as high as 19 dB, the noise measurement circuit provides a meaningful measure of signal power with worst case resolution of 1 dB.

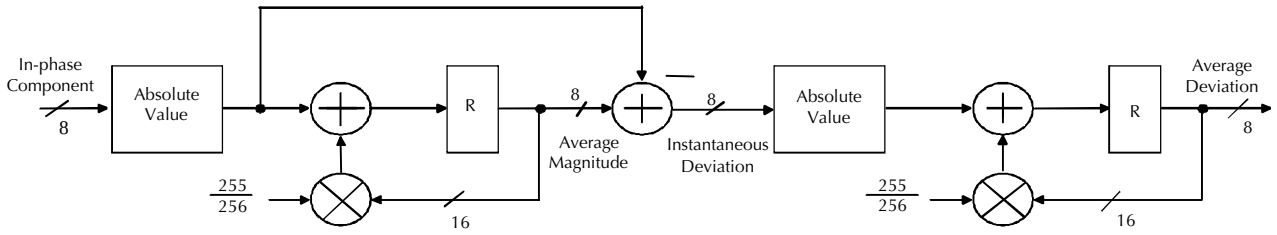

Figure 2-4: *Noise Measurement Circuit*

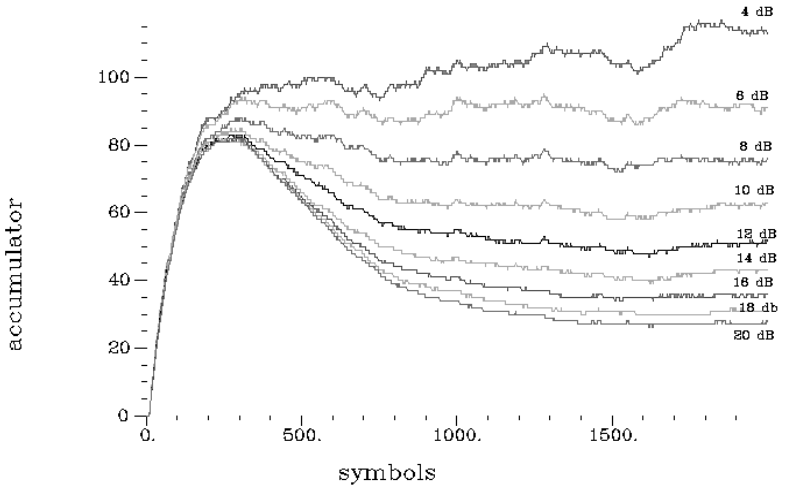

Figure 2-5: *Noise Accumulator as a Function of SNR and Time*

2.1.4 DBS RECEIVER

The OTI-8511 DVB demodulator and the OTI-8211 MPEG-2 decoder provide the core digital processing technology for a DBS receiver conforming with the DVB standard.

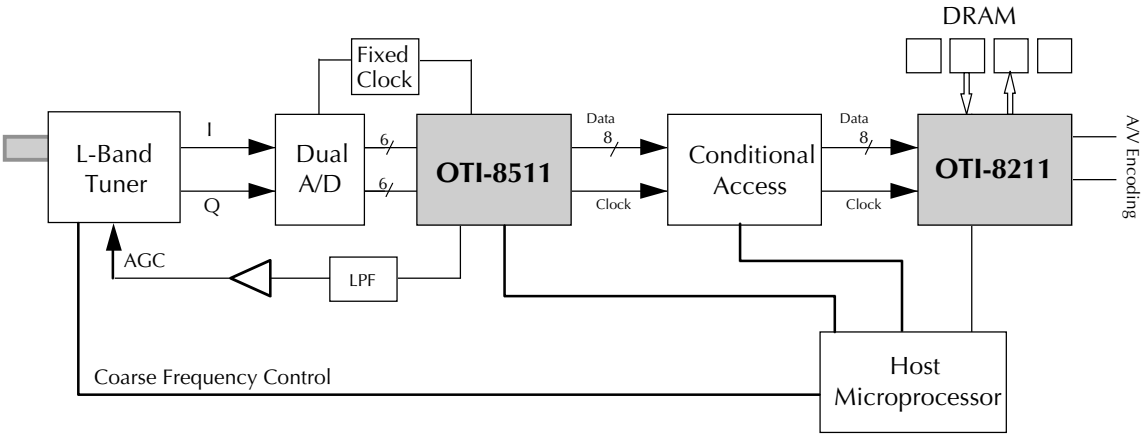

Figure 2-6: *Typical Set-top Box Architecture*

A tuner accepts an L-band RF input from the antenna/LNB assembly located outside the building. A host processor controls the tuner to the nominal center frequency of the target signal. Baseband I and Q outputs from the tuner are applied to an A/D converter pair, which samples at a fixed rate. The tuner is required to filter the received baseband signal to a bandwidth less than half the sampling rate, but is not required to perform matched filtering.

Once the OTI-8511 has locked to the target signal, the host processor may read the internal registers to determine the steady state frequency error. This error would be used to make periodic corrections to the programmed frequency of the tuner PLL.

The OTI-8511 provides an output that can be used to control the analog AGC in the tuner. This sigma delta output signal, which is clocked at the clock rate of the chip, is simply filtered and buffered before applying it to the AGC control element. When the loop is closed, the signal applied to the A/D converters is optimally scaled.

The output of the OTI-8511 is designed to be compatible with the OTI-8211 MPEG-2 decoder, with no required glue logic. The conditional access circuit may be required to modify the MPEG-2 data stream between the OTI-8511 and OTI-8211.

The OTI-8511 requires a 60 MHz clock to process the maximum symbol rate of 45 MBaud, while the OTI-8211 MPEG-2 decoder requires a 50 MHz clock. If the maximum symbol rate to be processed by the OTI-8511 is less than 28.5 MBaud, the OTI-8511 can share the 50 MHz clock that drives the OTI-8211 MPEG-2 systems, audio and video decoder, while still being able to decode all convolutional code rates. If only 1/2 and 2/3 rates are employed, the symbol rate may be increased to 35 MBaud with a 50 MHz clock.

2.1.5 PHASE NOISE CONSIDERATIONS

The OTI-8511 is designed to operate over a broad carrier frequency range and a broad range of symbol rates, while maintaining a simple RF front-end interface. The combined phase noise of all the frequency translation operations from Ku-band through the IF tuner can present the limiting performance factor for the demodulator, particularly at low symbol rates. In a conventional satellite set-top box, where varactor-tuned oscillators are employed, the phase noise may be prohibitive for low symbol rate applications. In a varactor-tuned oscillator, the phase noise close to the carrier may interfere with the demodulator carrier recovery loop, which typically would have a bandwidth in the range of 0.1 to 1.0% of the symbol rate.

For example, a signal that has a 1 MBaud symbol rate may have a carrier recovery loop that is in the range of 1 to 10 KHz. Phase noise close to the carrier, which is within the carrier loop bandwidth, will be reduced or effectively eliminated by the carrier tracking loop. The phase noise which is outside the loop bandwidth, will appear as additive noise in addition to thermal noise. For this reason, it is very important that the oscillator phase noise be well controlled at each down-conversion stage.

A set-top box designed for the OTI-8511 requires two L-band frequency translation operations in addition to the Ku band down converter. The final conversion, typically performed at 480 MHz, employs an oscillator phase locked to a crystal, or directly locked to a SAW resonator. This configuration provides minimum phase noise close to the carrier as compared with an open loop varactor controlled oscillator. For applications that do not employ very low baud rates, it is possible to use a varactor oscillator for the final conversion, but care should be taken to minimize the tuning bandwidth, which will also minimize phase noise.

The middle conversion is the tuner, which typically accepts a signal in the 950 to 2150 MHz range and produces an output centered near 480 MHz. This LO is phase locked to a crystal using indirect synthesis techniques. The phase noise of a typical indirect synthesizer near the carrier is inversely proportional to the synthesizer step size. Most synthesizer chips provide the flexibility to control step size in addition to center frequency. For this reason, in some cases it is advantageous to employ a coarse resolution synthesizer step size when low data rates are to be processed. This strategy, although contrary to intuition, is made possible by the fact that the OTI-8511 is capable of providing fine tuning over a range of close to ±1/2 the sample clock frequency. The tuning resolution is approximately one millionth of this frequency. Therefore, the combination of the fine tuning capability of the OTI-8511 and the coarse steps of the tuner are sufficient to cover the maximum bandwidth.

One exception to the above strategy is the case when the signal bandwidth is near the bandwidth of the SAW filter in the tuner. If the LNB causes frequency drift of several MHz, the signal may drift close to the band-edge of the filter. The resulting distortion could degrade the receiver performance. One strategy for overcoming this problem is for the host controller to monitor the frequency accumulator in the OTI-8511. When this frequency exceeds a limit, a correction is made to the frequency of the synthesizer, which drives the baseband frequency error toward zero and centers the signal in the passband.

One potential difficulty with this approach is that the synthesizer may introduce a frequency transient when this correction is made, depending on the design characteristics of the synthesizer and the carrier loop bandwidth of the demodulator. A transient could cause a temporary loss of demodulator lock resulting in an interruption of the MPEG-2 data and unwanted picture artifacts. An alternative strategy is to implement an analog coarse tuning varactor control in the tuner, which provides a frequency adjustment range equal to the maximum expected frequency drift of the LNB. The OTI-8511 provides two sigma delta converters (clocked at the clock rate of the chip), each with 8-bit control, which can be used for control of external devices. These converters require an external analog low pass filter, but provide an analog signal that ranges from near 0 to about 3 volts. In this case, the microcontroller would change the sigma delta converter instead of the synthesizer frequency to correct for detected baseband frequency drift. This approach has the benefit that the synthesizer will not create transients, but the phase noise will be somewhat degraded. For applications that do not require processing signals with very low baud rates, this may be a very practical approach.

CHAPTER 3 PIN DESCRIPTIONS

3.1 PIN ASSIGNMENTS

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	QPSK_LOCK	26	TEST_1	51	WE#/DS#	76	IOVDD
2	VSS	27	TEST_0	52	RE#/R/W#	77	DATA_3
3	WB_AGC	28	N/C	53	HI_DATA[7]	78	DATA_2
4	IOVDD	29	Sigma Delta2	54	HI_DATA[6]	79	DATA_1
5	I_IN_5	30	Sigma Delta1	55	HI_DATA[5]	80	DATA_0
6	I_IN_4	31	VDDS	56	HI_DATA[4]	81	VB_CLOCK
7	I_IN_3	32	N/C	57	IOVSS	82	VB_DATA
8	I_IN_2	33	N/C	58	IOVDD	83	IOVDD
9	I_IN_1	34	CLOCK_OUT	59	HI_DATA[3]	84	IOVSS
10	I_IN_0	35	IOVSS	60	HI_DATA[2]	85	SYMBOL_CLOCK
11	Q_IN_5	36	VSS	61	HI_DATA[1]	86	VB_NODESYNC
12	Q_IN_4	37	IOVDD	62	HI_DATA[0]	87	LOCK
13	Q_IN_3	38	CLOCK_IN	63	DTACK/Ready	88	TEST_15
14	Q_IN_2	39	VSS	64	VSS	89	TEST_14
15	Q_IN_1	40	VDD	65	VDD	90	VDD
16	Q_IN_0	41	RESET	66	FRAME_ERROR	91	VSS
17	VDD	42	HI_ADDR4	67	FRAME_SYNC	92	TEST_13
18	VSS	43	HI_ADDR3	68	DATA_VALID	93	TEST_12
19	TEST_6	44	HI_ADDR2	69	DATA_CLK	94	TEST_11
20	TEST_5	45	HI_ADDR1	70	DATA_STB	95	IOVDD
21	TEST_4	46	HI_ADDR0	71	DATA_7	96	IOVSS
22	IOVDD	47	BUSMODE	72	DATA_6	97	TEST_10
23	IOVSS	48	SCL_I^2C	73	DATA_5	98	TEST_9
24	TEST_3	49	SDA_I^2C	74	DATA_4	99	TEST_8
25	TEST_2	50	CE#/ CS#	75	IOVSS	100	TEST_7

3.2 PIN DESCRIPTIONS

3.2.1 INPUTS

Pin Name	Pin Description
I_IN[5:0]	6-bit in-phase (I) component input to the OTI-8511. This input is read at the sample clock rate.
Q_IN[5:0]	6-bit quadrature (Q) component input to the OTI-8511. This input is read at the sample clock rate.
CLOCK_IN	The sample clock input to the OTI-8511. The sample clock rate must be a minimum of 1.33 times the symbol rate of the signal to be processed and at least equal to the total bandwidth of the signal to be processed.
RESET#	A low on this signal causes the chip to be initialized. I/O registers are not cleared by this signal. This signal is asynchronous with respect to the clock.

3.2.2 OUTPUTS

Pin Name	Pin Description
DATA [7:0]	Transport stream data output. In parallel output mode, DATA [7:0] carry the 8-bit data. In serial output mode, DATA_0 is used as the serial data output.
DATA_CLK	The falling edge of this signal indicates that new data is available on the DATA [7:0] bus. This signal can be used in conjunction with DATA_VALID to transfer data from the OTI-8511. DATA_CLK will continue to toggle during the 16 FEC redundancy bytes.
DATA_VALID	This signal is high when the data on DATA [7:0] is from the useful 188 bytes of a transport stream packet. It will be low during the 16 FEC redundancy bytes.
FRAME_SYNC	This signal is true at the first byte of a block of 188 bytes.
DATA_STB	The rising edge of this signal indicates that new data is available on the DATA [7:0] bus. This signal is inactive during the 16 FEC redundancy bytes.
FRAME_ERROR	This signal goes high when the Reed Solomon decoder detects that an uncorrectable number of errors have occurred. The error flag (TEI) in the MPEG-2 output stream is also set when this flag goes high.
WB_AGC	This sigma delta output provides a measure of the external analog gain required for optimizing the signal applied to the analog to digital converters. This output is clocked at the OTI-8511 clock rate and must be filtered before applying to the front end analog gain control.
CLOCK_OUT	This is a buffered clock output signal, which may be used to drive other devices with the same clock that drives the OTI-8511, such as the dual A/D converter.
QPSK_LOCK	This signal goes high when the QPSK demodulator has achieved lock.
VB_NODESYNC	This signal goes high when the Viterbi decoder has achieved node synchronization.
LOCK	This signal goes high when the output data is valid and all synchronization functions have been performed.
SYMBOL_CLOCK	This signal, used for test purposes, goes high for a duration of one clock cycle for each received symbol. For symbol rates equal to or greater than half the clock frequency, this signal may remain high for two successive clock cycles to indicate that two symbols have occurred.
VB_DATA	The serial output of the Viterbi decoder is provided on this pin. This data is tapped prior to the polarity correction circuitry, so the data at this point may be inverted.
VB_CLOCK	The serial clock output from the Viterbi decoder. The rising edge of this signal indicates valid data on VB_DATA.
SIGMADELTA_1	The output of a sigma delta D/A converter, which has 8 bits of resolution. This output must be filtered with an analog low pass filter off the chip. This output may be used for any external analog control.
SIGMADELTA_2	The output of a second sigma delta D/A converter, which has 8 bits of resolution. This output must be filtered with an analog low pass filter off the chip. This output may be used for any external analog control.
TEST[15:0]	Test data output port. The data provided on these data lines is defined by the contents of register 13h.

3.2.3 HOST (MONITOR AND CONTROL) INTERFACE

Three different modes are supported for the monitor and control interface. Two of the modes are 8-bit parallel interfaces, one of which supports Intel microcontrollers and the other Motorola microcontrollers. The third mode is a serial interface conforming to the I^2C standard.

The I^2C mode is activated by placing CE# high at the same time RE# and WE# are low simultaneously. When this mode is active, the 7-bit I^2C slave address of the OTI-8511 is configured by the seven least significant bits of the HI_DATA[7:0] bus.

Note: ADDR signals are “don’t cares” in this mode.

Pin Name	Pin Description
HI_DATA [7:0]	This bi-directional data bus is used for communicating with the OTI-8511 internal register set.
CE#	Active low chip enable input.
RE#	Active low read enable input.
WE#	Active low write enable input. When BUSMODE is 0 (Motorola), this pin is not data strobe (see timing diagrams).
HI_ADDR [4:0]	The address bus defines which location within the device is to be accessed during a read or write operation.
BUSMODE	BUSMODE selects the type of microcontroller/processor used to setup the chip. When high, an Intel Processor/Microcontroller interface is used. When low, a Motorola Processor interface is used.
DTACK	Data acknowledge/data ready is a tristate output signal that informs the controlling processor that a data transfer has been acknowledged by the OTI-8511.
SCL_I^2C	I^2C clock input. When using I^2C mode, this input requires an external pull-up resistor per the I^2C specification.
SDA_I^2C	I^2C data line. When using I^2C mode, this line requires an external pull-up resistor per the I^2C specification.

3.2.4 I²C MODE

The OTI-8511 utilizes the subaddress technique when the I²C mode is employed. In all cases, the OTI-8511 behaves as the slave device (transmitter or receiver) while the host behaves as the master device. The 7-bit slave address of the OTI-8511 is user selectable, being defined by the inputs to HI_DATA[6:0] when the OTI-8511 is in I²C mode.

Further information on the I²C bus formats and protocols is contained in Philips Semiconductors I²C specification.

I²C Write to OTI-8511

The master initiates communication with the OTI-8511 by generating a start condition and then sending the OTI-8511 slave address defined by the 7-bit hardwired address on HI_DATA [6:0]. Per I²C convention, the eighth bit in the address byte is a read/not write bit, and should be set to zero. The OTI-8511 acknowledges the correctly sent slave address, following which the master sends an 8-bit word address. This is the address of the first OTI-8511 register to be written to. Once the word address has been acknowledged by the OTI-8511, the master can then transmit the byte to be written to the word address. Once this byte is acknowledged by the OTI-8511, the word address is automatically incremented and further data bytes may be transmitted by the master as necessary. Therefore, one transmission may contain a number of bytes of data to be written to a sequential set of addresses (dummy bytes should be written to addresses not defined in the OTI-8511 register set to continue this process). The process is terminated by the master generating a stop condition. Figure 3-1 depicts this protocol.

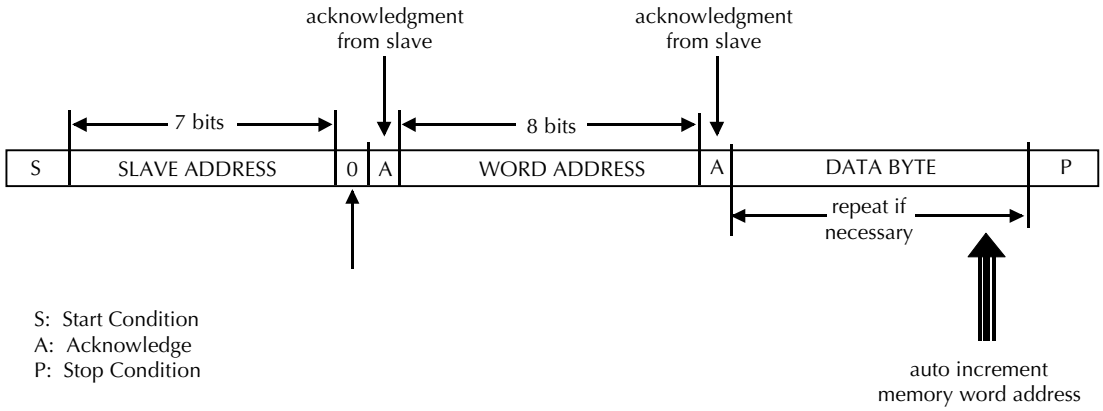

Figure 3-1: *I²C Write to the OTI-8511*

I²C Read from the OTI-8511

To read information from the OTI-8511, the master must first write the desired word address. Hence the master must first generate a start condition and transmit the 7-bit OTI-8511 slave address defined on HI_DATA[6:0], with the eighth bit (read/not write) set to zero. Once this has been acknowledged by the OTI-8511, the master transmits the first word address from which it wishes to read information. The master must then generate a second start condition and retransmit the OTI-8511 slave address, this time with the read/not write bit set to one (read). This will be acknowledged by the OTI-8511, which then assumes the role of slave transmitter and transmits the requested byte. This byte should be acknowledged by the master receiver. If no stop condition is generated by the master, the OTI-8511 will increment its word address pointer and transmit the next byte of information. This process is detailed in Figure 3-2.

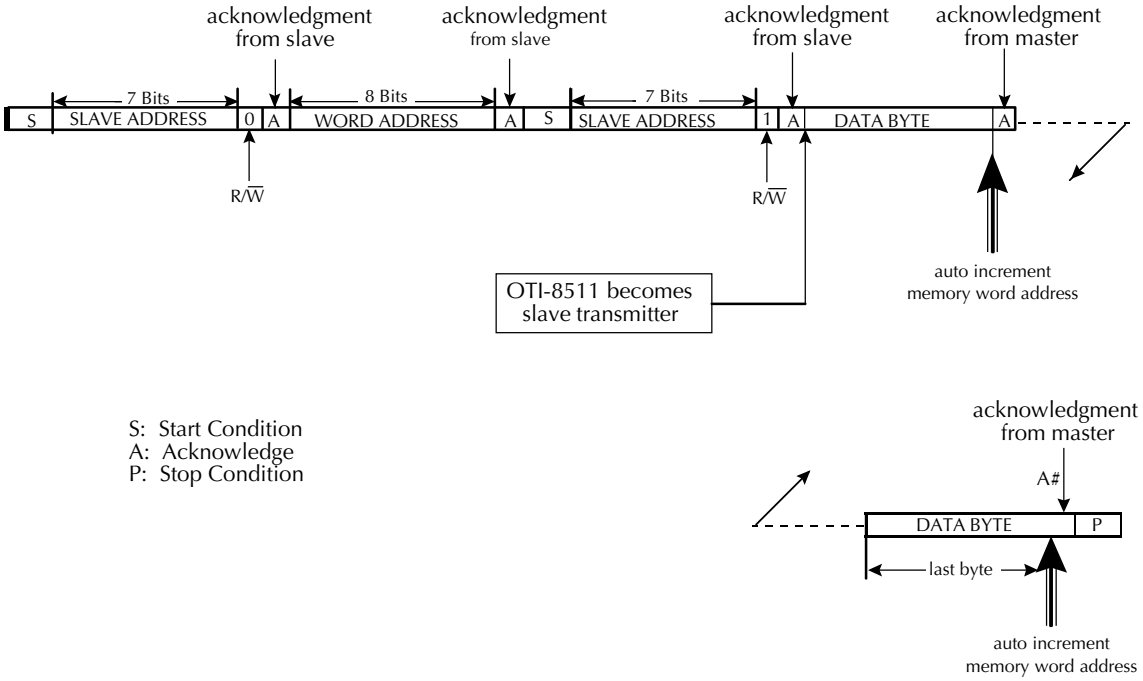

Figure 3-2: *I²C Read from the OTI-8511*

CHAPTER 4 AC AND DC SPECIFICATIONS

4.1 ABSOLUTE MAXIMUM RATINGS

Rating	Value	Unit
Ambient temperature under bias	0 to 70	C
Storage temperature	–65 to 150	C
Voltage on any pin	VSS – 0.5 to VDDS + 0.5	V
Operating power dissipation	1.6	W
VDD, IOVDD — voltage	7	V
VDDS voltage	7	V
Injection current	100	mA

4.2 DC CHARACTERISTICS

Symbol	Parameter	MIN	MAX	Units	Test Conditions
IOVDD	Interface Power Supply Voltage	3.00	3.60	Volts	Normal Operation
VDDS	Interface Bias Voltage	4.50	5.50	Volts	5V CMOS or TTL interface levels
		3.00	3.60	Volts	3.3V CMOS interface levels
VDD	Core Power Supply Voltage	3.00	3.60	Volts	Normal Operation
Vil	Input Low Voltage	0	0.8	Volts	
Vih	Input High Voltage	2.0	VDDS + 0.5	Volts	
Vol	Output Low Voltage		0.4	Volts	Iol = 4 mA
Voh	Output High Voltage	2.4		Volts	Ioh = 4 mA
Icc (DC)	Supply Current DC			mA	Vdd Nominal
Icc (AC)	Supply Current AC			mA/MHz	Vdd Nominal
Iih	Input High Current		10	uA	Vih = VDDS
Iil	Input Low Current	–10		uA	VDDS = 5.25V, Vil = 0.5V
Ioz	Output Leakage	–10		uA	0<Vout<VDDS
Cin	Input Capacitance		10	pF	
Cout	Output Capacitance		10	pF	

Note: Ta = 0° to 70°, unless otherwise noted.

4.3 DEMODULATOR SPECIFICATIONS

Parameter	Minimum	Maximum
Symbol Rate (Rs)	2 MBaud	45 MBaud
Viterbi Data Rate		< Clock Mbps
Reed Solomon Data Rate		< .92 Clock Mbps
Implementation Loss		0.25 db
Symbol Rate Uncertainty		±.0001 RS
Symbol Rate Resolution	Clock/(220)	
Carrier Frequency Resolution	Clock/(220)	
Carrier Tracking Range		±Clock/2
Acquisition Sweep Range		±Clock/2

4.4 AC CHARACTERISTICS OF DATA INPUT

Symbol	Parameter	Min.	Max.	Units
t_{su1}	Input data setup before clock	6		ns
t_{h1}	Input data hold after clock	2		ns
t_{pw1}	Low pulse width of clock	8.7		ns
t_{pw2}	High pulse width of clock	8.1		ns

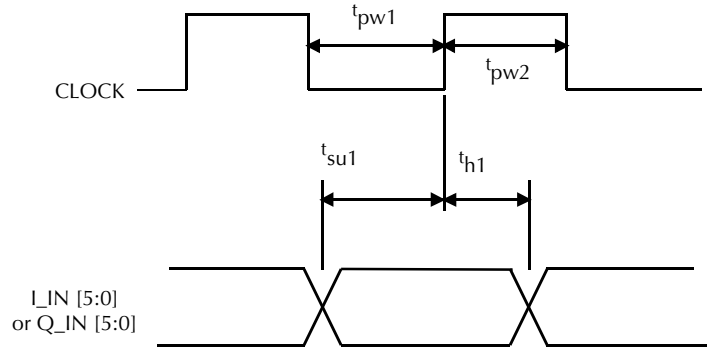

Figure 4-1: *Input Data Timing*

4.5 INTEL 80C88A READ CYCLE TIMING PARAMETERS (BUSMODE = 1)

Symbol	Parameter	Min.	Max.	Units
t_{su1}	Input address and CE# setup before RE# rising edge		35	ns
t_{h1}	Input address and CE# hold after RE# rising edge	5		ns
t_{pw1}	RE# low duration	200		ns
t_{d1}	Delay from CE# to DTACK/Ready active		35	ns
t_{doz1}	Delay from RE# rising edge to DTACK/Ready tristate mode		10	ns
t_{doz2}	Delay from RE# rising edge to HI_DATA [7:0] tristate mode	10		ns

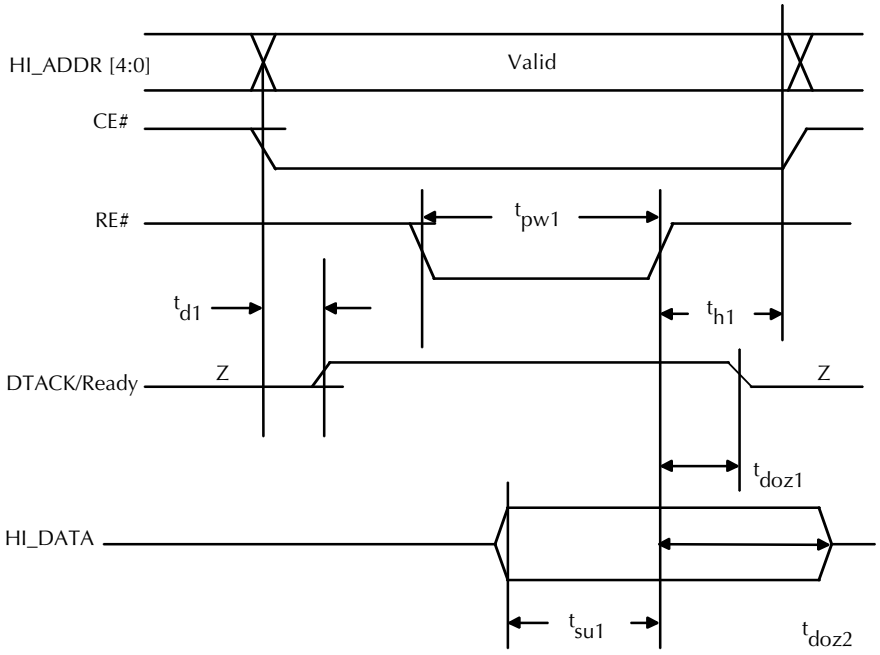

Figure 4-2: *Intel 80C88A Read Timing Diagram*

Note: HI_ADDR[4:0] is derived from the processor A15 — A8 bus and HI_DATA[7:0] is connected to the A7 — A0 bus.

4.6 INTEL 80C88A WRITE TIMING (BUSMODE = 1)

Symbol	Parameter	Min.	Max.	Units
t_{su1}	Input Data setup before WE# rising edge	20		ns
t_{h1}	Input address, data and CE# hold after WE# rising edge	8		ns
t_{pw1}	WE# low duration	200		ns
t_{d1}	Delay from CE# to DTACK/Ready active		35	ns
t_{doz1}	Delay from WE# rising edge to DTACK/Ready in tristate mode		15	ns

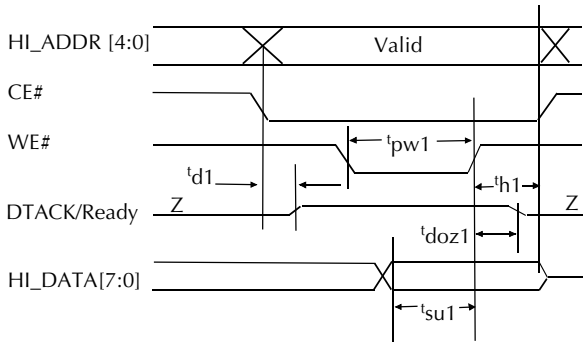

Figure 4-3: *Intel 80C88A Write Timing*

Note: HI_ADDR[4:0] is derived from the processor A15 — A8 bus and HI_DATA[7:0] is connected to the A7 — A0 bus.

4.7 INTEL 8051 READ TIMING (BUSMODE = 1)

Symbol	Parameter	Min.	Max.	Units
t_{su1}	Input address setup before CE# active	5		ns
t_{h1}	Input address and CE# hold after RE# trailing edge	5		ns
t_{pw1}	RE# active duration	400		ns
t_{pd1}	Delay from RE# active to HI_DATA [7:0] valid		40	ns
t_{doz1}	Delay from RE# trailing edge to HI_DATA[7:0] high impedance	10		ns

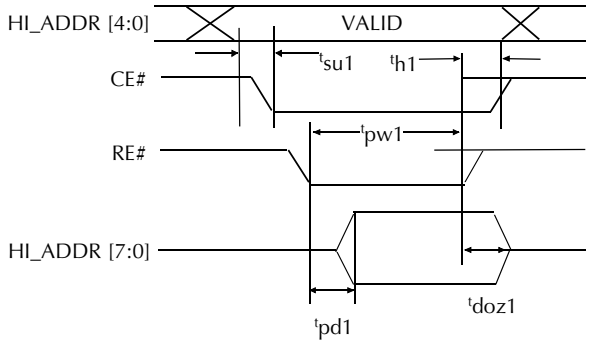

Figure 4-4: *Intel 8051 Read Timing*

4.8 INTEL 8051 WRITE TIMING (BUSMODE = 1)

Symbol	Parameter	Min.	Max.	Units
t_{su1}	Input address and data setup before WE# active	5		ns
t_{h1}	Input address and data hold after WE# trailing edge	5		ns
t_{pw1}	WE# active duration	400		ns
t_{su2}	CE# setup to WE# active	5		ns
t_{h2}	CE# hold after WE# active	5		ns

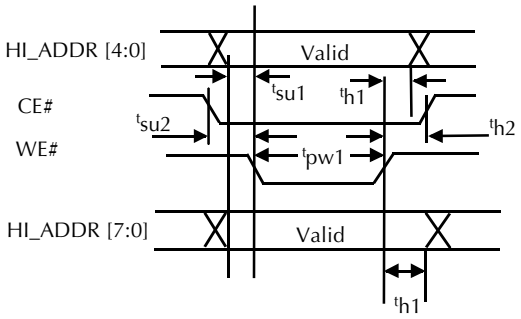

Figure 4-5: *Intel 8051 Write Timing*

4.9 MOTOROLA READ TIMING (BUSMODE = 0)

Symbol	Parameter	Min.	Max.	Units
t_{su1}	Setup time of R/W# with respect to CE#	5		ns
t_{su2}	Address setup with respect to DS#	5		ns
t_{d1}	Delay from DTACK/Ready active to data valid		30	ns
t_{h1}	R/W# hold with respect to DS#	5		ns
t_{h2}	Address hold with respect to DS#	5		ns
t_{h3}	Data hold with respect to DS# trailing edge	10		ns

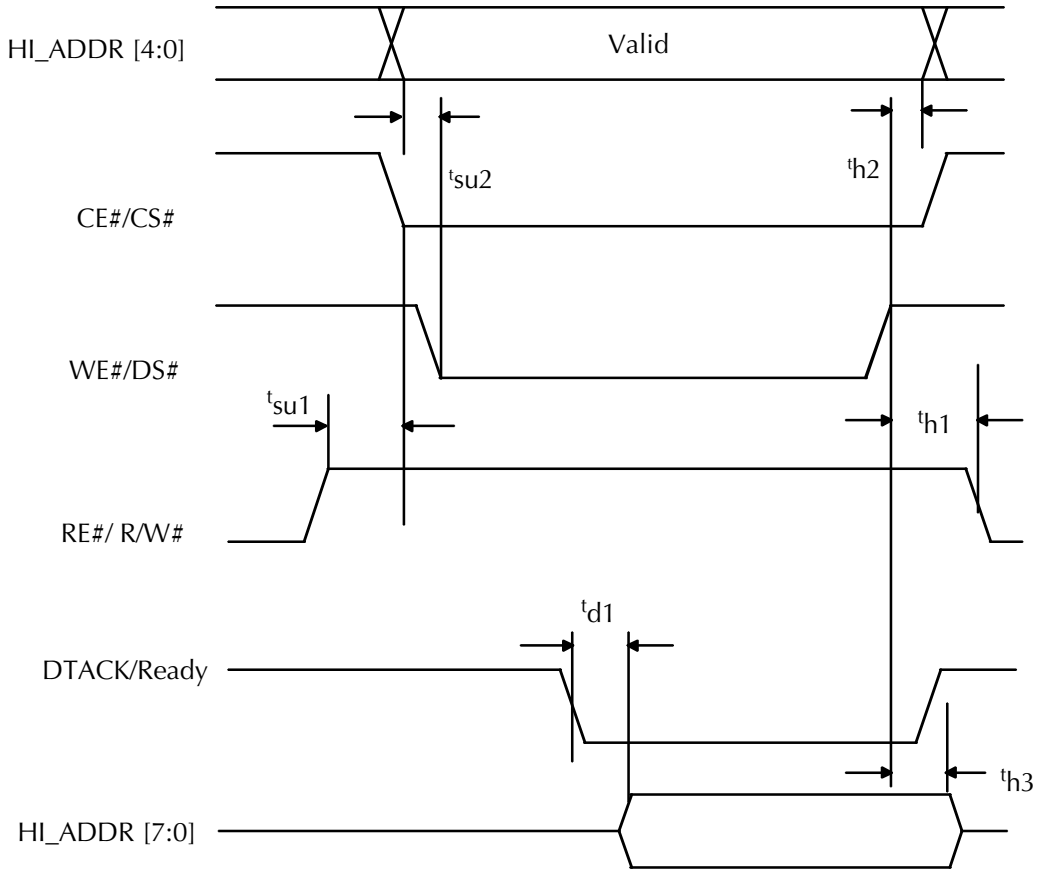

Figure 4-6: *Motorola Read Timing*

Note: External pull-up resistor required on DTACK/Ready

4.10 MOTOROLA WRITE TIMING (BUSMODE = 0)

Symbol	Parameter	Min.	Max.	Units
t_{su1}	Data setup to DS# leading edge	5		ns
t_{su2}	R/W# setup to CS# and address	3		ns
t_{d1}	DS# delay from R/W#	5		ns
t_{d2}	DTACK delay from DS# active		40	ns
t_{d3}	DTACK delay from DS# inactive		10	ns
t_{pw1}	DS# active duration	5		ns
t_{h1}	Address, CS# and R/W# hold from DS# trailing edge	5		ns
t_{h2}	Data hold from DS# trailing edge	5		ns

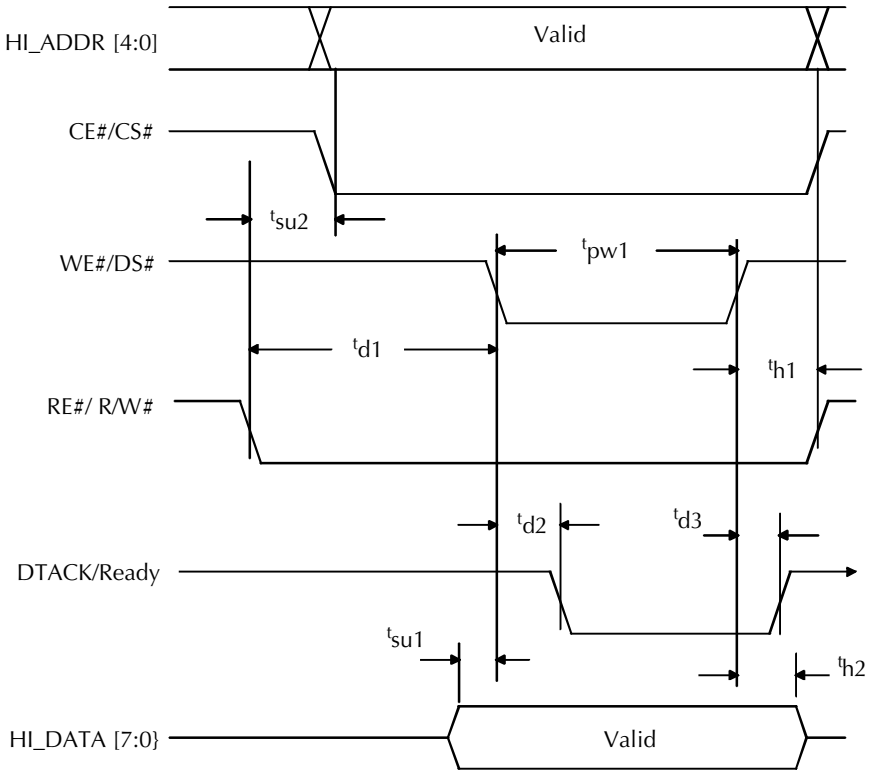

Figure 4-7: *Motorola Write Timing*

Note: DTACK requires an external pull-up resistor.

4.11 PARALLEL OUTPUT TIMING

Symbol	Parameter	Min.	Max.	Units
t_{su}	Output data setup before DATA_CLK and DATA_STB	5		ns
t_{hd}	Output data hold after DATA_CLK and DATA_STB	10		ns

When configured for parallel transport stream output, all 204 bytes (188 useful bytes plus 16 redundancy bytes from the FEC) of each transport stream packet appear sequentially on the parallel data lines DATA [7:0]. Each of these 204 bytes is clocked out by a falling edge on DATA_CLK. Each of the 188 useful bytes is clocked out by a rising edge on DATA_STB, which remains inactive during the 16 redundancy bytes. In addition, frame synchronization (FRAME_SYNC) and valid data (DATA_VALID) outputs are provided, as detailed in Figure 4-8.

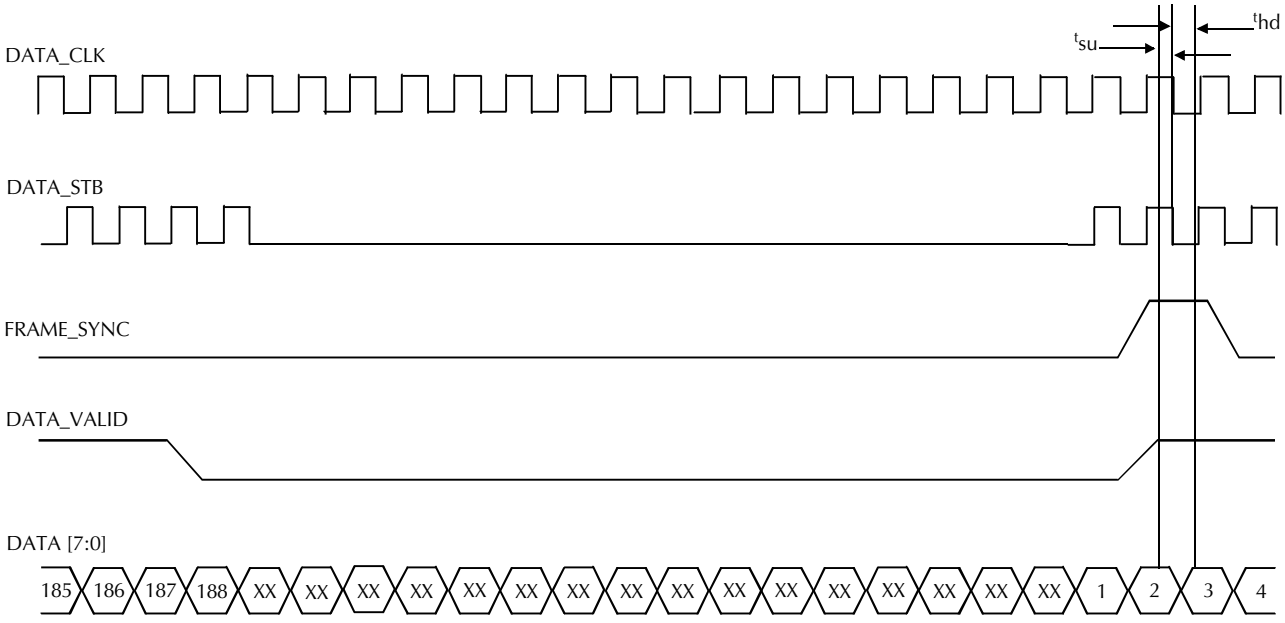

Figure 4-8: *Parallel Output Timing Diagram*

4.12 SERIAL OUTPUT TIMING

Symbol	Parameter	Min.	Max.	Units
t_{ssu}	Output data setup before DATA_CLK	5		ns
t_{shd}	Output data hold after DATA_CLK	5		ns

The OTI-8511 can present the transport stream output in serial format. In this output mode, all 204 bytes (188 useful bytes plus 16 redundancy bytes from the FEC) of each transport stream packet appear sequentially on the serial data output line, DATA_0. The bytes are presented MSB first. Each bit of the 188 useful bytes is clocked out by a rising edge on DATA_STB, which remains inactive during the 16 redundancy bytes; each bit of all 204 bytes is clocked out by a falling edge on DATA_CLK. Both DATA_STB and DATA_CLK are burst in nature, with the maximum burst frequency being the CLOCK frequency of the OTI-8511. The exact burst structure is a function of the FEC code rate. Figure 4-9 shows the timing relationships of the serial output signals.

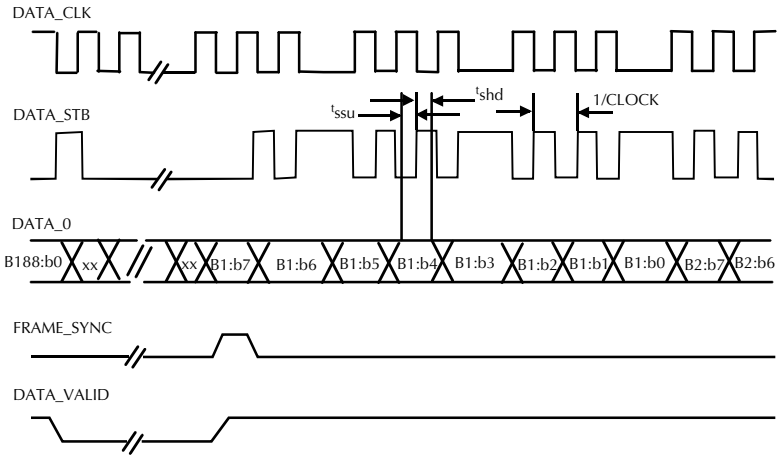

Figure 4-9: *Serial Output Timing Diagram*

CHAPTER 5 REGISTER DEFINITIONS

5.1 WRITE REGISTERS

5.1.1 SYMBOL TIMING FREQUENCY (Index 00h, 01h, and 02h)

The 20 bit straight binary number in this field establishes the symbol timing frequency utilized within the demodulator. Bit 7 of address 00 is the MSB and bit 4 of address 02 is the LSB. If R_s is the symbol rate and f_c is the clock frequency, the value to be stored in this 20-bit field is the integer portion of $R_s(220)/f_c$.

5.1.2 SYMBOL TIMING LOOP GAIN CONTROL (Index 03h)

This field establishes the K1 and K2 gain values for the second order loop filter of the symbol tracking loop. Bits 0,1, and 2 determine the straight-through gain, and bits 4, 5, 6, and 7 determine the integration path gain. The nominal value of this parameter in Hex, is expressed below for different ranges of symbol rate to clock rate ratios:

0.75 — 0.40	B6
0.40 — 0.20	A5
0.20 — 0.10	94
0.10 — 0.05	83
0.05 — 0.025	72
0.025 — 0.016	61

Note: The optimal value of gain may vary with different systems, depending on tuner phase noise characteristics.

5.1.3 CARRIER OFFSET FREQUENCY (Index 04h, 05h, and 06h)

The 20 bit, two's complement number in this field establishes the nominal carrier frequency of the demodulator. Bit 7 of address 04 is the MSB and bit 4 of address 06 is the LSB. The number in this 20-bit field multiplied by the clock frequency divided by 2^{20} is the carrier frequency in Hertz. When the carrier sweep function is active, this value defines the starting frequency.

5.1.4 CARRIER LOOP FILTER CONTROL (Index 07h)

This field establishes the K1 and K2 gain values for the second order loop filter of the carrier tracking loop. Bits 0,1, and 2 determine the straight-through gain, and bits 4,5,6, and 7 determine the integration path gain. The nominal value of this parameter in Hex is expressed below for different ranges of symbol rate to clock rate ratios. Two loop-filter configurations are provided at each symbol rate, one for steady state operation and one, which is used only for acquisition, to permit greater frequency pull in.

Symbol Rate/Clock	Steady State	Acquisition
0.75 — 0.40	A5	B6
0.40 — 0.20	94	A5
0.20 — 0.10	73	84
0.10 — 0.05	62	83
0.05 — 0.025	41	62
0.025 — 0.016	30	51

5.1.5 CARRIER SWEEP STEP SIZE (Index 08h, 09h)

This 16 bit value defines the size of the step of each carrier frequency dwell. Bit 7 of address 08 is the MSB and bit 0 of address 09 is the LSB. The number in this register is divided by 2^{16} and multiplied by the clock frequency to determine the frequency step increment.

5.1.6 SYMBOLS PER DWELL (Index 0Ah, 0Bh)

This 16-bit value defines the time, in symbol periods, for which the demodulator will dwell before making the next frequency step in a sweep. Bit 7 of address 0A is the MSB and bit 0 of address 0B is the LSB.

5.1.7 NUMBER OF SEARCH FREQUENCIES (Index 0Ch)

This 8-bit field determines the number of frequency steps, which occur during the frequency sweeping process. Combined with the frequency step-size (08 & 09), this determines the frequency span of the carrier sweep.

5.1.8 NARROWBAND AGC INITIAL VALUE (Index 0Dh)

The six most significant bits of this field establish the initial gain of the AGC. High numbers correspond to low gain associated with low symbol rates. If the narrowband AGC function is enabled, this number is used as a starting point and the closed loop will seek the optimum setting without processor interaction.

5.1.9 CONTROL PARAMETERS (Index 0Eh)

Bit 0 — Binary/Twos

When this bit is a zero, the system expects the 6-bit modulation input samples in two's complement format, otherwise the input should be in offset binary format.

Bit 1 — Spectrum Invert

When this bit is set to zero, the spectrum of the received signal is inverted. This is achieved by complementing the in-phase channel.

Bit 2 — Bias Cancel Enable

When this bit is set to one, the internal circuit that cancels DC bias on the I and Q inputs is enabled.

Bit 3 — Symbol Track Enable

When this bit is set to one, the symbol tracking function is enabled. When this bit is zero the symbol tracking frequency is forced to the nominal 20 bit programmed value.

Bit 4 — Carrier Track Enable

When this bit is set to one, the carrier phase tracking function is enabled. When this bit is zero, the carrier frequency is forced to the 20 bit programmed value.

Bit 5 — Sweep Hold

When this bit is set to one, the sweeping process is inhibited, and the nominal carrier frequency remains at the last value.

Bit 6 — Narrowband AGC Mode 1 Enable

When this bit is set to one and the narrowband AGC is in Mode 1, the narrowband AGC self adjusts to the optimum gain setting. When the bit is set to zero, the most recent value is held without updating.

5.1.10 RESET FUNCTIONS (Index 0Fh)

Bit 0 — Symbol Timing Recovery Accumulator

When this bit is set to zero, the frequency accumulator in the symbol tracking loop is cleared to zero. This bit must be set to one in normal tracking operation to implement a second order tracking loop, otherwise the loop is first order.

Bit 1 — Carrier Phase Accumulator

When this bit is set to zero, the carrier phase accumulator is cleared to zero. For normal operation, this bit should be set to one.

Bit 2 — Wideband (WB) AGC Accumulator

When this bit is set to one, the accumulator in the wideband AGC is cleared to zero. In normal operation, this bit is set to zero. When the WB AGC is set to Mode 1, this bit has no effect as the integrator must be implemented in the external analog circuits.

Bit 3 — Narrowband AGC Accumulator

When this bit is set to zero, the accumulator in the narrowband AGC is cleared to the initial value defined in location 0D. In normal operation, this bit is set to one.

Bit 5 — Carrier Sweep Function

When this bit is set to zero, the sweep function is disabled and the carrier frequency is forced to the preset value defined in register locations 04, 05, and 06.

Bit 6 — Viterbi Signal Quality

When this bit is set to zero, the Viterbi signal quality read register (18h) is forced to zero.

Bit 7 — Reed Solomon Error Count

When this bit is set to zero, the counter that identifies the number of corrected errors (read register 1C - 1D) and uncorrected errors (read register 1E) are cleared to zero.

5.1.11 WB AGC CONTROL (Index 10h)

Bit 0 — WB AGC Mode

When this bit is set to zero (Mode 0), the WB AGC output must be filtered with an external integrating analog filter to implement a first order feedback loop. When this bit is one (Mode 1), a digital integrator within the OTI-8511 performs this function and the only external analog function required is a low pass filter to remove the high frequency components of the sigma delta converter output.

Bit 1 — WB AGC Invert

When this bit is set to zero a high duty factor on the WB AGC output corresponds to too much gain. When the control bit is set to one, high duty factor corresponds to too little gain.

Bit 2 — WB AGC Hold

During normal tracking operation, this bit is set to one. When this bit is set to zero and the wideband AGC is in Mode 1, the digital integrator is held to the most recent value.

Bits [5:7] — WB AGC Gain

This 3-bit field defines the time constant of the WB AGC in Mode 1. A value of zero corresponds to the shortest time constant and 7 corresponds to the slowest time constant.

5.1.12 SIGMA DELTA ONE (Index 11h)

8-bit input to sigma delta D/A converter one. This function is independent of other demodulator functions and is provided as control for external analog components.

5.1.13 SIGMA DELTA TWO (Index 12h)

8-bit input to sigma delta D/A converter two. This function is independent of other demodulator functions and is provided as control for external analog components.

5.1.14 TEST PORT CONFIGURATION (Index 13h)

The value written to this location defines the data that will be presented on the 16-bit test output port, TEST[15:0]. For configurations where the data is updated once per symbol period, the data changes at the rising edge of SYMBOL_CLOCK (in the case that SYMBOL_CLOCK remains high for consecutive CLOCK cycles, the test port data will also change accordingly during the high period of SYMBOL_CLOCK due to the arrival of another symbol).

Value	Test Port Data
00h	Output is tristate.
01h	Test bits [15:8] provide the output from the I channel demodulator RRC filter; bits [7:0] provide the Q channel filter output. This information is updated once per symbol period.
02h	Test bits [15:0] provide the 16 most significant bits of the demodulator carrier 20-bit phase accumulator. This information is updated once per symbol period.
03h	Test bits [15:0] provide the 16 most significant bits of the demodulator symbol timing 20-bit phase accumulator. This information is updated once per symbol period.
04h	Test bits [15:8] provide the Reed Solomon output data. Test bits [7:0] provide the deinterleaved output data. This information is updated at the Reed Solomon clock rate; when the transport stream output is configured to parallel output mode, DATA_CLK may be used as an output clock for this data.
05h	Test bits [11:6] provide the 6-bit narrowband AGC accumulator value. Test bits [5:2] provide the 4-bit value of symbol phase. Test bits [1:0] provide the 2-bit symbol count value. This information is updated once per symbol period.

5.1.15 VITERBI LOCK CONTROL (Index 14h)

This 4-bit up/down counter monitors the measure of data convergence at each Viterbi code rate. The lock and unlock threshold can be defined.

Bits [7:4] — Lock Threshold

This 4-bit number defines the lock threshold at which the Viterbi decoder decides that the correct code rate has been found. Larger values require more time to achieve Viterbi lock. The nominal value is 12 and the value should be greater than 7.

Bits [3:0] — Lock Fail Threshold

This 4-bit number defines the lock fail threshold point at which the Viterbi decoder rejects a code rate and moves on to the next code rate. Smaller values instruct the Viterbi decoder to seek more data before trying the next code rate. The nominal value is 2 and the value should be less than 7.

5.1.16 VITERBI UNLOCK CONTROL (Index 15h)

This 4-bit up/down counter monitors state of lock at a given Viterbi code rate.

5.1.17 VITERBI AND REED SOLOMON CONTROL PARAMETERS (Index 17h)

Bit 0

Controls the transport stream output of the OTI-8511 to serial or parallel mode. When this bit is set to zero, the OTI-8511 MPEG output is set to parallel mode (default). When this bit is set to one, the OTI-8511 MPEG output is set to serial output mode.

Bit 1

Describes the input data stream to the OTI-8511. With this bit set to zero (default), the OTI-8511 expects a valid MPEG-2 synchronization byte at the start of each packet; without the synchronization byte, Viterbi lock will not be achieved. With this bit set to one, node synchronization can be achieved without a valid synchronization byte; this mode is provided primarily for test purposes.

5.1.18 VITERBI THRESHOLD REGISTERS (Index 18h and 1Ch)

These 6-bit registers define the thresholds used in the Viterbi decoder node synchronization process. In general, the default values provide optimal Viterbi decoder performance.

Register	Code Rate	Default Value
18h	1/2	18h
19h	2/3	24h
1Ah	3/4	24h
1Bh	5/6	24h
1Ch	7/8	24h

These registers provide a means of forcing the Viterbi decoder to search a limited subset of potential code rates. If a threshold value of zero is written into the register corresponding to a specific rate, that rate is essentially bypassed in the search algorithm. If four of the five registers contain zero, and the fifth register is programmed with the nominal threshold value, then the node synchronization circuit will only lock to the rate corresponding to the register with the nominal threshold value.

5.2 READ REGISTERS

5.2.1 NARROWBAND AGC ACCUMULATOR (Index 00h)

The current value of the 6-bit AGC accumulator may be read from this location.

5.2.2 SYMBOL TIMING FREQUENCY ACCUMULATOR (Index 01h, 02h, and 03h)

The current value of the 20-bit frequency accumulator in the symbol timing loop filter may be read from these three locations. Bit 7 of address 01 is the MSB and bit 4 of address 03 is the LSB.

5.2.3 PHASE TRACKING FREQUENCY ACCUMULATOR (Index 04h, 05h, and 06h)

The current value of the 20-bit frequency accumulator in the carrier phase loop filter may be read from these 3 locations. Bit 7 of address 04 is the MSB and bit 4 of address 06 is the LSB.

5.2.4 QPSK LOCK STATUS (Index 07h)

Bit 0

QPSK Lock Flag. When this bit is set to one, the QPSK demodulator is phase locked.

5.2.5 WIDEBAND AGC ACCUMULATOR (Index 08h)

This 8-bit value represents the most significant bits of the accumulator in the first order wideband AGC loop. This data only has meaning when the wideband AGC is in Mode 0.

5.2.6 SWEEP FREQUENCY (Index 09h, 0Ah)

The 16-bit sweep accumulator is available at this location. Bit 7 of address 09h is the MSB and bit 0 of address 0A is the LSB. The receiver frequency is determined by adding the Sweep Frequency with the carrier frequency accumulator (read addresses 04, 05 and 06) and the nominal carrier start frequency (write addresses 04, 05, and 06).

5.2.7 IN-PHASE (I) (Index 0Bh)

The 8-bit output of the I baseband filter is available at this location. This data is updated once per symbol.

5.2.8 QUADRATURE (Q) (Index 0Ch)

The 8-bit output of the Q baseband filter is available at this location. This data is updated once per symbol.

5.2.9 NOISE POWER (Index 0Dh)

This 8-bit output provides a measure of the noise component of the signal when QPSK lock is achieved. Higher numbers correspond to lower signal-to-noise ratio conditions. The quality of the this metric is improved if the narrowband AGC is disabled a minimum of 1000 symbol periods before this parameter is read.

5.2.10 UNUSED (Index 0Eh, 0Fh)

This 7-bit signal provides a measure of quality of the signal processed by the Viterbi decoder. This parameter can be used to infer bit error rate and input signal-to-noise ratio for signals which are within a few dB of threshold.

5.2.11 VITERBI RATE (Index 19h)

This 3-bit number represents the code rate of the Viterbi decoder.

Rate 1/2	0
Rate 2/3	1
Rate 3/4	2
Rate 5/6	3
Rate 7/8	4

5.2.12 REED SOLOMON ERRORS (Index 1Ah)

The 4-bit number at this location indicates the number of errors corrected in the most current block of 188 bytes. This number may range from 0 to 8.

5.2.13 FEC LOCK (Index 1Bh)

Bit 0 — Viterbi Node Sync

When this bit is set to one, the Viterbi decoder has successfully established node synchronization.

Bit 1 — Frame Sync

When this bit is set to one, the FEC chip has successfully established word and frame sync.

Bit 2 — Viterbi Byte Sync

When this bit is set to one, the Viterbi decoder has successfully established byte-synchronization.

Bit 3 — Pi Ambiguity

When this bit is set to one, the Viterbi decoder has successfully resolved pi ambiguity in the input data. (i.e. inverted data)

Bit 4 — Pi/2 Ambiguity

When this bit is set to one, the Viterbi decoder has successfully resolved pi/2 ambiguity in the input data.

5.2.14 ACCUMULATED REED SOLOMON ERRORS (Index 1Ch, 1Dh)

The 16-bit number at this location indicates the number of errors corrected since the last reset. Bit 7 of address 1C is the MSB and bit 0 of address 1D is the LSB.

Note: Counting will cease when the maximum count of 65535 is reached. For information on resetting these registers, see write register definitions for address 0F.

5.2.15 ACCUMULATED REED SOLOMON DATA (Index 1Eh)

The 8-bit number at this location indicates the uncorrected code words passed since the last reset. When the maximum value of 255 is reached, the counter value returns to zero and resumes counting. For information on resetting these registers, see write register definitions for address 0F.

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CHAPTER 6 APPENDICES

6.1 LOOP FILTER PROGRAMMING APPLICATION NOTE

To illustrate that both the symbol timing recovery loop and carrier phase recovery loop are programmable, several simulations were performed with different loop parameter conditions. These simulations were performed with a symbol rate of two samples per symbol, corresponding to 30M symbols-per-second if a 60 MHz clock were utilized.

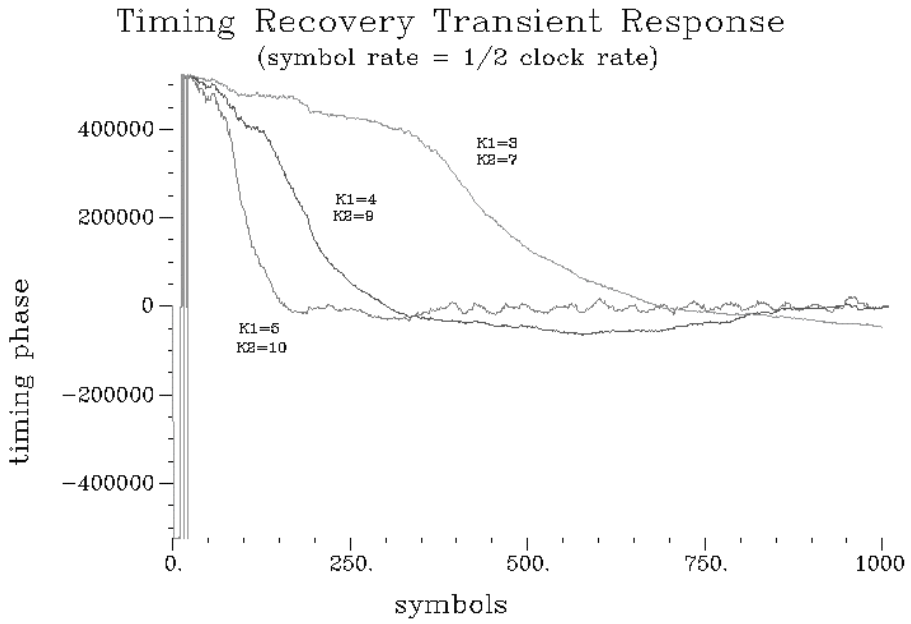

Figure 6-1: *Symbol Timing Recovery Transient Response*

Figure 6-1 illustrates the transient response of the symbol phase with three different loop conditions (K1=5, K2=10; K1=4, K2=9; and K1=8, K2=7). The vertical scale represents phase over a 360° range (524,287 to –524,288). All test cases were run at high signal-to-noise ratio. The highest gain condition could be used for fast acquisition as well as for steady state with high code rate conditions, while the intermediate gain is a suitable steady state setting for rate 1/2 codes (minimum E_b/N_0 of 4 dB). The lowest gain setting corresponds to ultra low-loop bandwidth and may be considered for maintaining lock without phase jumps during deep signal fades.

Figure 6-2 illustrates the transient response of the carrier tracking loop with the same loop bandwidth settings at high signal-to-noise ratio. The phase step for this test corresponds to 45°. The actual bandwidth of the carrier loop is greater than that of the symbol loop for the same settings because the carrier loop must cope with greater dynamics (such as frequency offset and drift). Figure 6-3 illustrates the transient response of the carrier phase tracking loop under the same conditions at minimum signal-to-noise ratio (E_b/N_0 of 4 dB with rate 1/2 coding). The highest bandwidth case will pull in with a carrier frequency error of ±.005 of the symbol rate at this minimum signal level. Higher loop bandwidth may be programmed to provide greater pull-in with higher signal-to-noise ratio conditions.

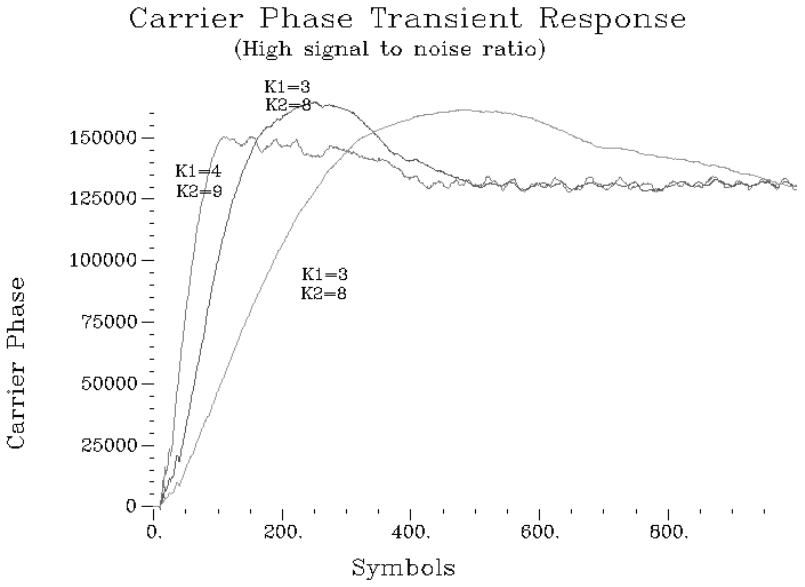

Figure 6-2: *Carrier Phase Recovery Transient Response*

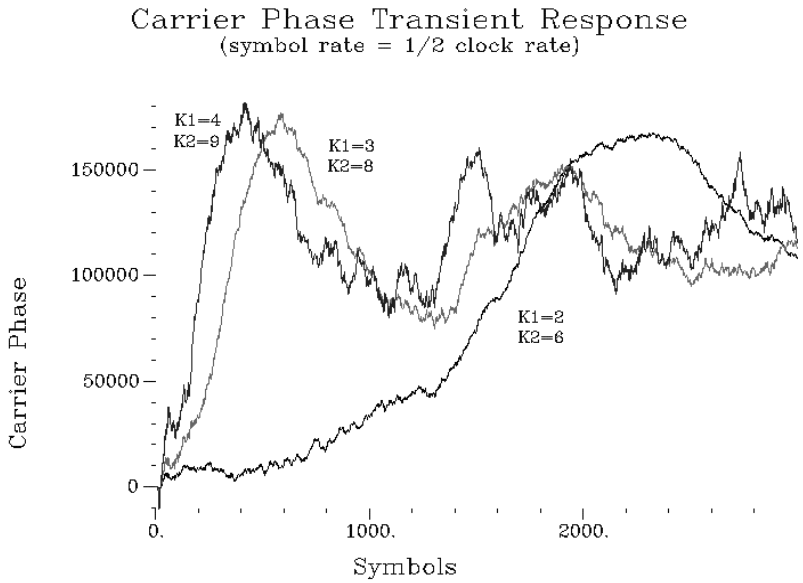

Figure 6-3: *Carrier Phase Recovery Transient Response with Low SNR*

6.2 PERFORMANCE WITH INTERFERENCE

In order to evaluate the filter employed within the OTI-8511 with respect to attenuating out-of-band interference, a test was performed utilizing the COSSAP simulator. The desired signal, at zero frequency, was configured to utilize 16 samples-per-symbol (corresponding to 3.75 MHz symbol rate if a 60 MHz clock is employed). An interfering signal was added with the same characteristics, except that the amplitude was made to be 10 dB higher than that of the desired signal, the data pattern was different and the carrier frequency was offset from that of the desired signal. Several offset frequencies were evaluated for this case. Figure 6-4 illustrates the spectrum of the test condition when the offset frequency is 1.35 times the symbol rate.

Figure 6-5 illustrates the measured bit error rate for various conditions. The error rate on the I channel was measured separately from that of the Q channel, and the horizontal axis is scaled in dB for one component, I or Q of the signal. For example, the point labeled 1 dB corresponds to SNR (noise bandwidth = symbol rate) of 4 dB or E_b/N_0 of 4 dB if rate 1/2 coding is employed.

The theoretical performance for coherent PSK is shown with the solid line. The curve closest to theoretical is the demodulator performance with no other interferers and corresponds to an implementation loss of about 0.2 dB. When the interferer was placed at a frequency of either 2.0 or 1.35 times the symbol rate away from the desired carrier, there is an additional degradation ranging from 0 dB to 0.1 dB. The worst case occurs when the interferer is placed at only 1.28 times the symbol rate from the carrier of the desired signal. In this case, the performance has degraded with respect to the no interference case by 0.3 to 0.5 dB.

Figure 6-6 illustrates performance with an interferer that is 20 dB higher than the desired signal and separated in frequency by 2 times the symbol rate. In this case, the performance has degraded by 0.7 to 0.8 dB from the case with no interferer.

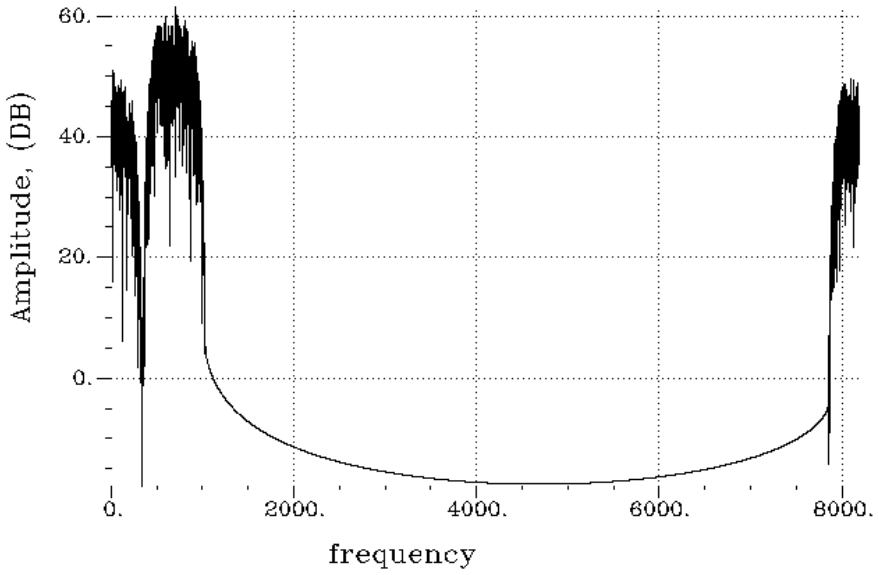

Figure 6-4: *Adjacent Channel Interference of 10 dB, 1.35 Spacing*

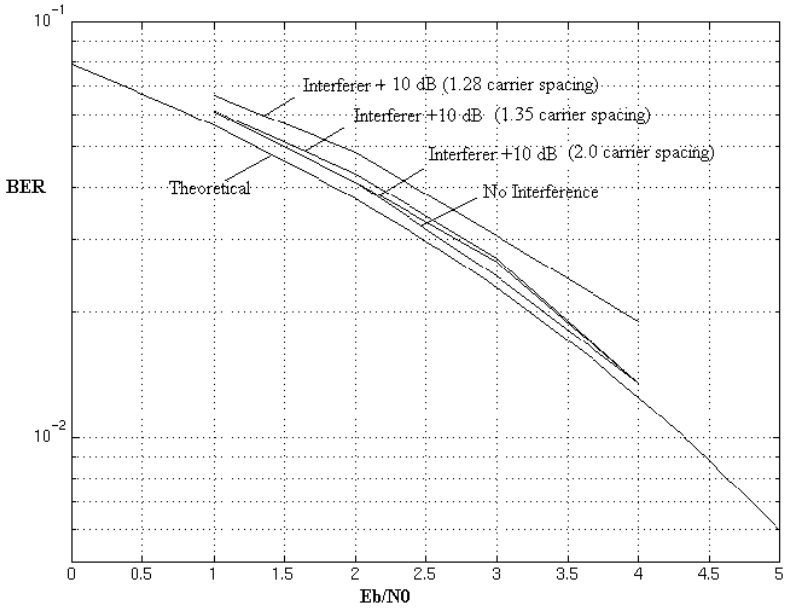

Figure 6-5: *Performance with Interferer at Different Carrier Spacing*

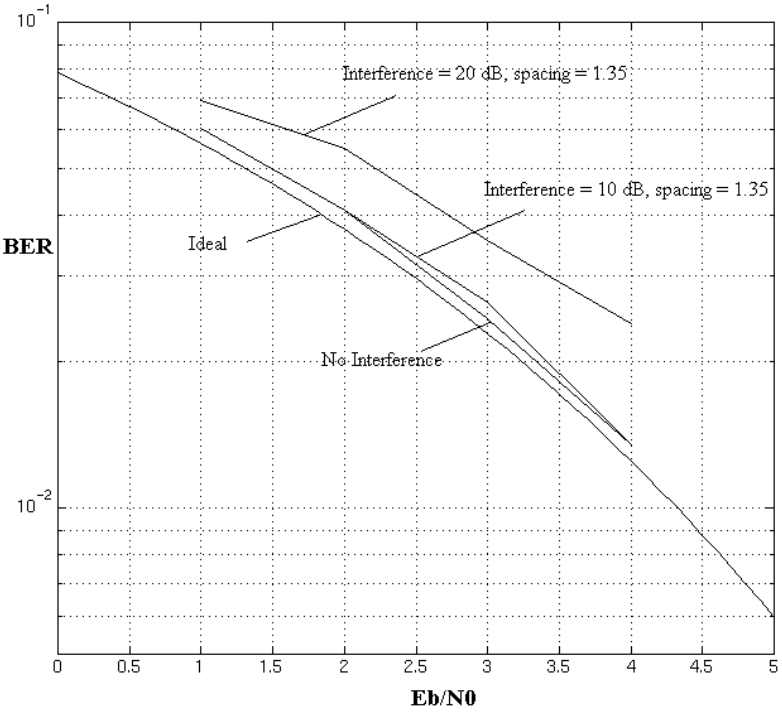

Figure 6-6: *Performance with a +10 dB Interferer*

6.3 NYQUIST CRITERIA CONSIDERATIONS

The OTI-8511 is clocked at 60 MHz, yet processes signals with symbol rates as high as 45M symbols-per-second. Initially, this might appear to be violating the Nyquist criteria, which states that the sampling rate must be at least twice the highest frequency component. The total bandwidth of the 45 MBaud signal, with 35% excess bandwidth, is about 60 MHz.

The samples provided to the OTI-8511 are complex samples, which is equivalent to 120M samples-per-second and does satisfy the Nyquist criteria. Another way of looking at this, is to examine the baseband signal. The signal bandwidth covers 60 MHz, but the baseband spectrum covers from –30 to +30 MHz. There are no baseband frequency components greater than 30 MHz, and the 60 MHz clock is adequate as long as complex samples are taken.

6.4 PACKAGE DIMENSIONS

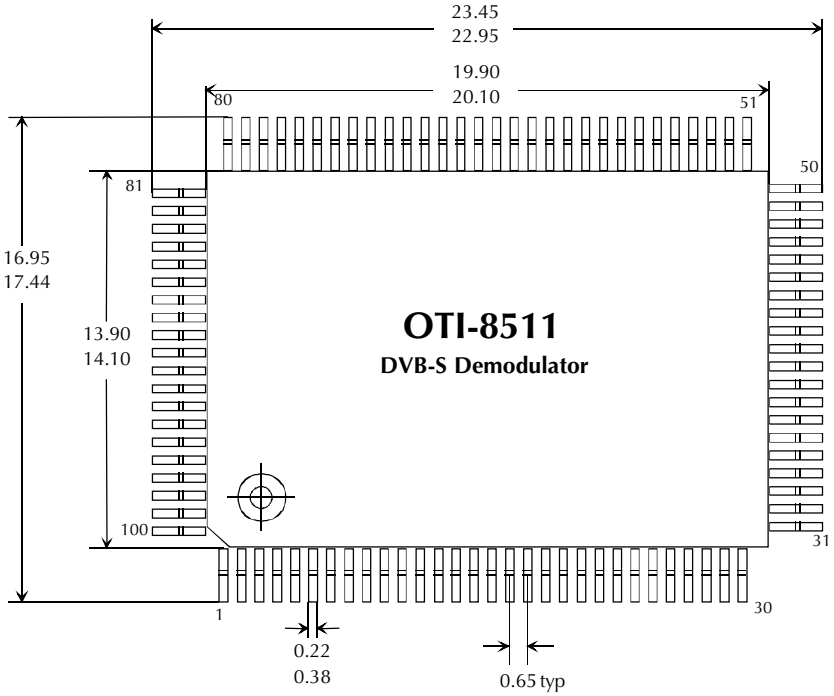

Figure 6-7: *Package Dimensions (in millimeters)*

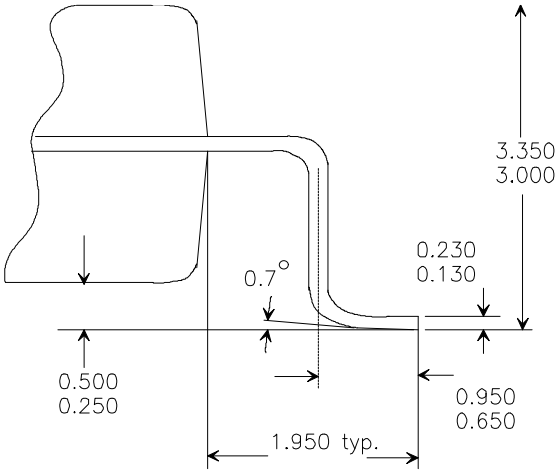

Figure 6-8: *Mechanical Configuration*

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