Universal Logic Circuits

Description

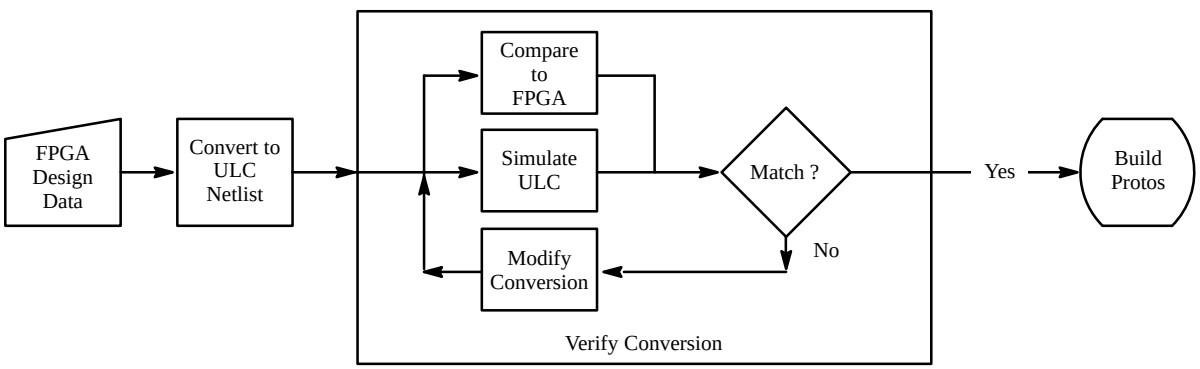
FPGAs and PLDs are excellent tools for design development and lower-volume production. They provide a quick design cycle for fast time to market, low development costs and low risk. In higher-volume production, with proven and stable designs, where cost, quality, power consumption, and manu- facturablilty are important considerations, ULC™ devices are a preferred alternative with significant improvements in each of these characteristics.

ULCs (Universal Logic Circuits) are factory-customized circuits that are pin-for-pin drop-in replacements for a wide range of FPGAs and programmable logic devices. MHS has developed a proprietary design flow that enables ULC conversions to be completed on a turnkey basis in most cases. This design flow, called ***Verify-Before-Silicon***, allows MHS to validate the correctness of any conversion directly against the original FPGA or PLD design without requiring a time- consuming simulation signoff by the customer. ***Verify-Before-Silicon*** also means that for a proven FPGA or PLD design, MHS assumes the risk that the ULC conversion is correct, unlike the typical ASIC conversion process where the customer assumes all of the risk that it is correct by virtue of a simulation sign-off.

Features

- Mask Programmed drop-in replacements for Field-Programmable Gate Arrays (FPGAs) and Programmable Logic Devices (PLDs)
- Cost reduction for volume applications
  - 20%, 50%, even 75% or more is possible
  - Function of density, volume and speed
- Easy, low-cost, low-risk conversion
  - Turnkey conversion and verification
  - No simulation sign-off required
  - No NRE in most cases for commercial ULCs
  - Guaranteed to work in the application, rather than to simulation
  - No obligation if parts don’t work in the application
- Quality improvement
  - Each ULC™ device tested for functional, dc and ac specifications
- Reduced power consumption
  - 85-95% reduction for most PLD and EPLD devices
- Wide range of architectures and speeds
  - 10- and 15-ns PLDs – 22V10, etc.
  - 10- through 20-ns EPLDs (MACH™, Altera® MAX®)
  - Most FPGAs (Xilinx™, Actel™, Altera®)
- Simplified manufacturing
  - Eliminates programming, testing or labeling
- Production flows available for most devices:
  - Commercial, Industrial and Military temperatures
  - Military and Radiation Tolerant flows

Verify-Before Silicon Technique



The design requirements for a ULC conversion are straightforward and are detailed in Section 2. The documentation required, such as design files, schematic or block diagrams, is frequently already available, such as design files, schematic or block diagram, etc. MHS can frequently complete ULC conversion without test vectors or simulation vectors from the customer although this can add substantially to the conversion time.

ULCs combine the design-cycle advantages of FPGAs and PLDs, with the production advantages of an ASIC to provide the best of both worlds.

Technology

ULCs are manufactured with advanced sub-micron CMOS technology. Several different series are used to meet the constraints of different PLD and FPGA types as well as unique customer requirements. The UD series of ULCs uses 0.8-mm (drawn) single-level metal CMOS. The UC series uses 0.85-mm (drawn) double-level metal CMOS. These technologies offer toggle rates in excess of 200 MHz and input-output propagation delays as fast as 7 ns. They are designed for cost-effective volume production, and thus offer state-of-the-art performance combined with highly predictable and cost-effective manufacturability. The UD series has been in production since late 1988, and the UC series has been in production since 1989.

New for 1995 is the UG series of ULCs. This series uses 0.6-mm (drawn) double-metal or triple-metal CMOS. UG ULCs offer toggle rates up to 350 MHz and input-output propagation delays as fast as 5 ns.

Field Programmable Devices Supported

Architectures

A wide range of architectures and vendors are supported for conversions. This includes most 10- and 15-ns PLDs, such as 22V10, 26V12, and 20RA10. It includes MACH™ family of EPLDs from AMD®. From Altera®, conversions are supported on EP “Classic” EPLDs, MAX® EPM5000™, and EPM7000™ family EPLDs and the FLEX®EPF8000™ series of FPGAs. From Actel™, ACT1™, ACT2™ and ACT3™ FPGAs. From Xilinx™, XC2000™, XC3000™, and XC4000™ as well as the XC7000 family of EPLDs. Conversions are also supported for Lattice™ pLSI™ EPLDs and Quicklogic pASIC™ FPGAs.

A cross-reference list of devices supported for ULC conversion is shown in Section 7. This list is not exhaustive, as new devices are added regularly. Additional devices not shown in this list may also be supported.

Benefits Of ULC Devices

Cost Reduction

Through advanced logic synthesis techniques, ULCs replicate an FPGA or EPLD design into a much more cost-effective semi-custom implementation than is possible with field-programmable devices. Field-programmable devices typically have substantial silicon resources devoted to programming and routing capabilities, which are eliminated in ULCs. The resulting cost-reduction ranges between 25% for smaller EPLDs to 50% for medium-density FPGAs and as much as 90% for very large FPGAs. The amount of the saving depends on the size of the device being converted, its speed, and the production volume level.

Easy, Low-Cost and Low-Risk Conversion

Conversion to ULC is an easy process because MHS does most of the work. The design hand-off consists of documentation, files, and master parts. Most of these are likely to exist already after completion of the FPGA or EPLD design, or they can be generated with a relatively small time commitment. After the design hand-off, MHS takes over. MHS handles the netlist conversion and all of the back-end engineering. There are no lengthy simulation runs nor any need to spend hours verifying that the conversion has been done correctly. A ULC customer can use valuable engineering resources where they will bring the greatest benefit: on new product designs, rather than on cost reduction.

For commercial flow ULCs, the typical volume vs. tooling cost calculations that come with traditional ASIC development do not have to be applied, as there is no NRE with a production order which meets minimum order requirements. ULCs can be treated as a pure production cost-reduction solution. On military and space level conversions, however, there will be an NRE.

MHS promises that the converted ULC will work in the customer’s application as a functional equivalent to the FPGA, PLD, or EPLD being replaced. This is unlike a typical ASIC design, where a simulation run sign-off is required, and the ASIC vendor commits to delivering parts which meet the simulation independent of whether they work in the board. This commitment is backed by MHS’ proprietary “***Verify-Before-Silicon***” technology that provides the highest level of assurance for first-time success.

Quality Improvement

One-time field-programmable devices are tested only partially by the manufacturer since complete verification requires programming. As a result, one-time field-programmable devices can exhibit high PPM defect levels. ULC devices are 100% tested to functional, dc, and ac specifications by MHS. This dramatically reduces defect levels compared to OTP devices.

Further, most field-programmable devices are typically tested after programming only for correct programming (fuse map verification), which does not necessarily guarantee correct operation. Any functional testing is typically limited by the: (1) testing capability of the programming environments, and (2) the number of test patterns typically generated to perform the tests. As a result boards manufactured with these devices are susceptible to failure at final test. This reduces manufacturing yield of the board or system, and raises product cost. Rework increases the overall cycle time, and, if done in line, further reduces manufacturing throughput.

ULC devices undergo extensive tests generated by automatic test vector generation (ATVG) software. (See Section 2 for design flow.) The software develops patterns to achieve a high degree of test coverage, typically over 90% on smaller devices, which ensures that the circuit is substantially exercised in the testing process. On larger devices, which cannot achieve such high test coverage, SCAN paths can be added during the conversion process to achieve a high level of coverage. With customer involvement, program limits and levels can be adjusted and additional test vectors can be added to eliminate test escapes.

This difference provides benefits to systems manufacturers for improving system yields, manufacturing cost and manufacturing throughput factors.

Power Consumption Reduction

The power consumption for PLD and EPLD devices is typically rated from 90 to 200 mA depending on the size of the device. ULC power consumption, is a strong function of device clock rates, but ranges between 5 and 25 mA for conversions of this type. This cuts power by a factor of 5 to 10 compared to field-programmable devices. Further, this is accomplished without putting the device in a standby mode, and thus without the latencies and extra logic associated with standby operation. A factor of two for operating power reduction on FPGA conversions at higher speeds is not unusual.

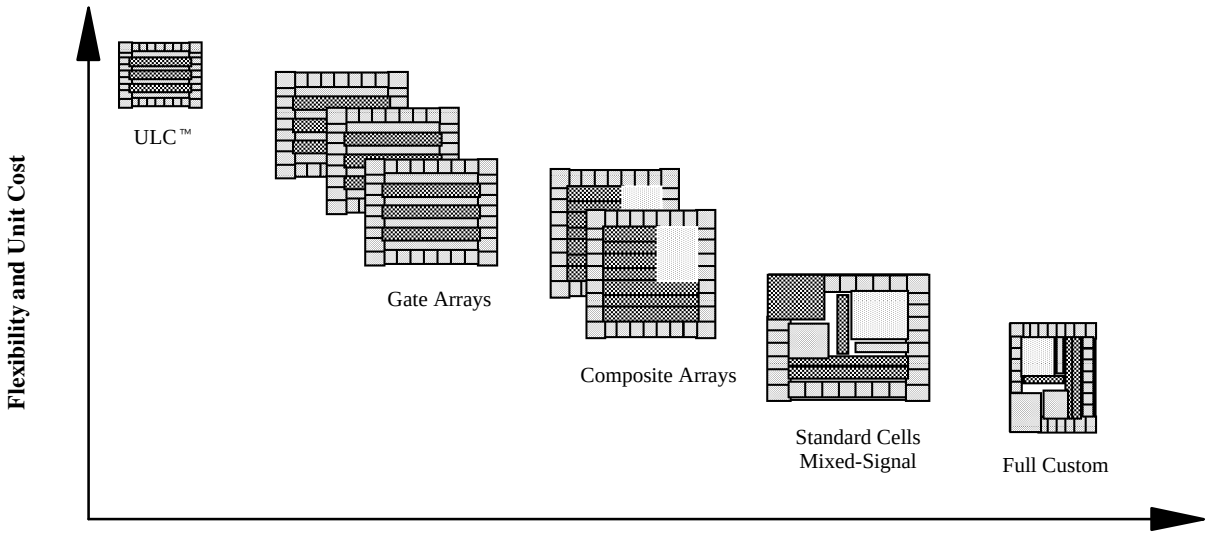
Simplified Manufacturing

Elimination of the need for in-house programming, testing and labeling, substantially reduces system manufacturing cost. Elimination of sockets in environments where the field-programmed devices are not tested prior to placement on the board can provide further savings.

The Risk-Free Solution

With no NRE in commercial applications, and MHS' guarantee to work in the application, ULCs truly are the **Risk-Free** solution to cutting high FPGA and EPLD costs. There is little effort required to prepare for the conversion. The customer simply identifies stable programs, sends in the completed design checklist(s), and prepares to enjoy the savings.

A Full Range of Solutions for Integration



ULCs are one of many semi-custom and full-custom solutions for system integration and cost-reduction offered by TEMIC. These different architectural solutions, offered in a number of different process technologies, provide a high level of flexibility in meeting varied and changing customer requirements. Capabilities include both pure digital and mixed digital and analog.

ULC to Standard Cell

One of the unique capabilities within TEMIC is the ability to provide a phased cost reduction process for applications with very high volume potential. This is done through the ULC to Standard Cell program wherein the original FPGA or PLD based design is first converted to a ULC for the initial production, which may have more moderate volumes and greater risk of program change. Then, as the volumes become very large, and the program absolutely defined, the ULC is then converted by MHS to a standard cell in the same process technology at a lower cost. Customer engineering involvement is substantially reduced from the normal development process for this second-level conversion, and a smooth production transition is provided by MHS.