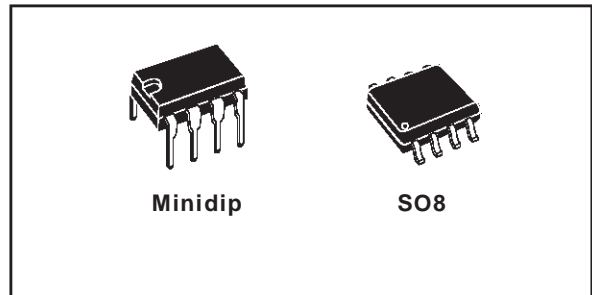




# UC2842A/3A/4A/5A UC3842A/3A/4A/5A

## HIGH PERFORMANCE CURRENT MODE PWM CONTROLLER

- TRIMMED OSCILLATOR DISCHARGE CURRENT
- CURRENT MODE OPERATION TO 500kHz
- AUTOMATIC FEED FORWARD COMPENSATION
- LATCHING PWM FOR CYCLE-BY-CYCLE CURRENT LIMITING
- INTERNALLY TRIMMED REFERENCE WITH UNDERVOLTAGE LOCKOUT
- HIGH CURRENT TOTEM POLE OUTPUT
- UNDERVOLTAGE LOCKOUT WITH HYSTERESIS
- LOW START-UP CURRENT (< 0.5mA)
- DOUBLE PULSE SUPPRESSION



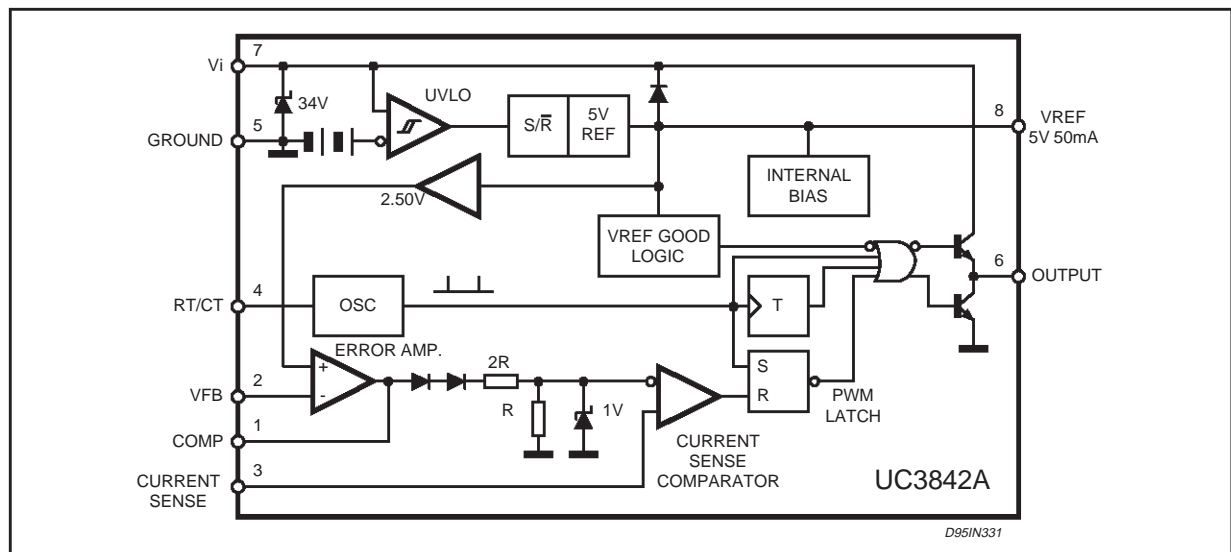
comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off-state.

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC3842A and UC3844A have UVLO thresholds of 16V (on) and 10V (off), ideally suited off-line applications. The corresponding thresholds for the UC3843A and UC3845A are 8.5 V and 7.9V. The UC3842A and UC3843A can operate to duty cycles approaching 100%. A range of the zero to < 50 % is obtained by the UC3844A and UC3845A by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.

### DESCRIPTION

The UC384xA family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include a trimmed oscillator for precise DUTY CYCLE CONTROL under voltage lockout featuring start-up current less than 0.5mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM

### BLOCK DIAGRAM (toggle flip flop used only in UC3844A and UC3845A)



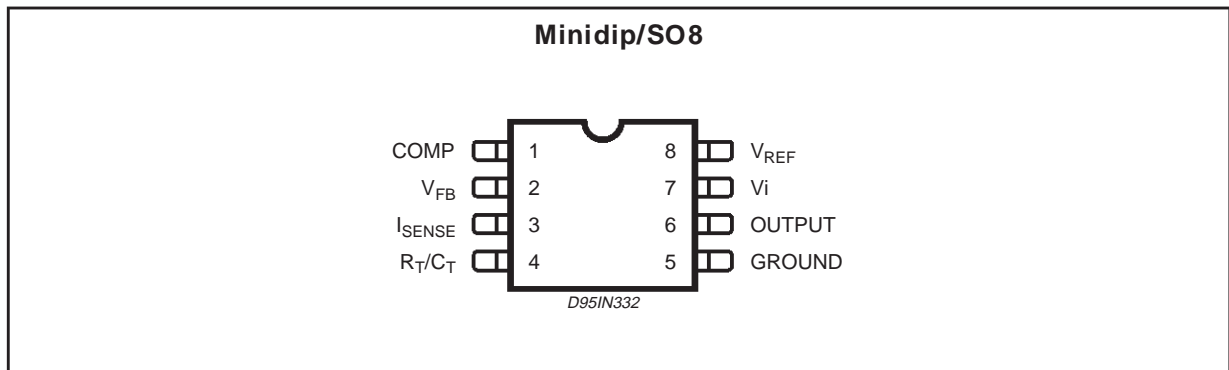
## UC2842A/3A/4A/5A - UC3842A/3A/4A/5A

### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_i$	Supply Voltage (low impedance source)	30	V
$V_i$	Supply Voltage ( $I_i < 30\text{mA}$ )	Self Limiting	
$I_o$	Output Current	$\pm 1$	A
$E_o$	Output Energy (capacitive load)	5	$\mu\text{J}$
	Analog Inputs (pins 2, 3)	- 0.3 to 5.5	V
	Error Amplifier Output Sink Current	10	mA
$P_{\text{tot}}$	Power Dissipation at $T_{\text{amb}} \leq 25^\circ\text{C}$ (Minidip)	1.25	W
$P_{\text{tot}}$	Power Dissipation at $T_{\text{amb}} \leq 25^\circ\text{C}$ (SO8)	800	mW
$T_{\text{stg}}$	Storage Temperature Range	- 65 to 150	$^\circ\text{C}$
$T_L$	Lead Temperature (soldering 10s)	300	$^\circ\text{C}$

\* All voltages are with respect to pin 5, all currents are positive into the specified terminal.

### PIN CONNECTION (top view)



### PIN FUNCTIONS

No	Function	Description
1	COMP	This pin is the Error Amplifier output and is made available for loop compensation.
2	$V_{\text{FB}}$	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	$I_{\text{SENSE}}$	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	$R_T/C_T$	The oscillator frequency and maximum Output duty cycle are programmed by connecting resistor $R_T$ to $V_{\text{ref}}$ and capacitor $C_T$ to ground. Operation to 500kHz is possible.
5	GROUND	This pin is the combined control circuitry and power ground.
6	OUTPUT	This output directly drives the gate of a power MOSFET. Peak currents up to 1A are sourced and sunk by this pin.
7	$V_{\text{CC}}$	This pin is the positive supply of the control IC.
8	$V_{\text{ref}}$	This is the reference output. It provides charging current for capacitor $C_T$ through resistor $R_T$ .

### ORDERING NUMBERS

SO8	Minidip
UC2842AD1; UC3842AD1	UC2842AN; UC3842AN
UC2843AD1; UC3843AD1	UC2843AN; UC3843AN
UC2844AD1; UC3844AD1	UC2844AN; UC3844AN
UC2845AD1; UC3845AD1	UC2845AN; UC3845AN

## THERMAL DATA

Symbol	Description	Minidip	SO8	Unit
$R_{th\ j-amb}$	Thermal Resistance Junction-ambient.	max. 100	150	$^{\circ}C/W$

**ELECTRICAL CHARACTERISTICS** ( [note 1] Unless otherwise stated, these specifications apply for  $-25 \leq T_{amb} \leq 85^{\circ}C$  for UC284XA;  $0 \leq T_{amb} \leq 70^{\circ}C$  for UC384XA;  $V_i = 15V$  (note 5);  $R_T = 10K$ ;  $C_T = 3.3nF$ )

Symbol	Parameter	Test Conditions	UC284XA			UC384XA			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
<b>REFERENCE SECTION</b>									
$V_{REF}$	Output Voltage	$T_j = 25^{\circ}C$ $I_o = 1mA$	4.95	5.00	5.05	4.90	5.00	5.10	V
$\Delta V_{REF}$	Line Regulation	$12V \leq V_i \leq 25V$		2	20		2	20	mV
$\Delta V_{REF}$	Load Regulation	$1 \leq I_o \leq 20mA$		3	25		3	25	mV
$\Delta V_{REF}/\Delta T$	Temperature Stability	(Note 2)		0.2			0.2		$mV/^{\circ}C$
	Total Output Variation	Line, Load, Temperature	4.9		5.1	4.82		5.18	V
$e_N$	Output Noise Voltage	$10Hz \leq f \leq 10KHz$ $T_j = 25^{\circ}C$ (note 2)		50			50		$\mu V$
	Long Term Stability	$T_{amb} = 125^{\circ}C$ , 1000Hrs (note 2)		5	25		5	25	mV
$I_{SC}$	Output Short Circuit		-30	-100	-180	-30	-100	-180	mA
<b>OSCILLATOR SECTION</b>									
$f_{OSC}$	Frequency	$T_j = 25^{\circ}C$	47	52	57	47	52	57	KHz
$\Delta f_{OSC}/\Delta V$	Frequency Change with Volt.	$V_{CC} = 12V$ to $25V$	-	0.2	1	-	0.2	1	%
$\Delta f_{OSC}/\Delta T$	Frequency Change with Temp.	$T_A = T_{low}$ to $T_{high}$	-	5	-	-	5	-	%
$V_{OSC}$	Oscillator Voltage Swing	(peak to peak)	-	1.6	-	-	1.6	-	V
$I_{dischg}$	Discharge Current ( $V_{OSC} = 2V$ )	$T_j = 25^{\circ}C$	7.8	8.3	8.8	7.8	8.3	8.8	mA
<b>ERROR AMP SECTION</b>									
$V_2$	Input Voltage	$V_{PIN1} = 2.5V$	2.45	2.50	2.55	2.42	2.50	2.58	V
$I_b$	Input Bias Current	$V_{FB} = 5V$		-0.1	-1		-0.1	-2	$\mu A$
	$A_{VOL}$	$2V \leq V_o \leq 4V$	65	90		65	90		dB
BW	Unity Gain Bandwidth	$T_j = 25^{\circ}C$	0.7	1		0.7	1		MHz
PSRR	Power Supply Rejec. Ratio	$12V \leq V_i \leq 25V$	60	70		60	70		dB
$I_o$	Output Sink Current	$V_{PIN2} = 2.7V$ $V_{PIN1} = 1.1V$	2	12		2	12		mA
$I_o$	Output Source Current	$V_{PIN2} = 2.3V$ $V_{PIN1} = 5V$	-0.5	-1		-0.5	-1		mA
	$V_{OUT}$ High	$V_{PIN2} = 2.3V$ ; $R_L = 15K\Omega$ to Ground	5	6.2		5	6.2		V
	$V_{OUT}$ Low	$V_{PIN2} = 2.7V$ ; $R_L = 15K\Omega$ to Pin 8		0.8	1.1		0.8	1.1	V
<b>CURRENT SENSE SECTION</b>									
$G_V$	Gain	(note 3 & 4)	2.85	3	3.15	2.85	3	3.15	V/V
$V_3$	Maximum Input Signal	$V_{PIN1} = 5V$ (note 3)	0.9	1	1.1	0.9	1	1.1	V
SVR	Supply Voltage Rejection	$12 \leq V_i \leq 25V$ (note 3)		70			70		dB
$I_b$	Input Bias Current			-2	-10		-2	-10	$\mu A$
	Delay to Output			150	300		150	300	ns

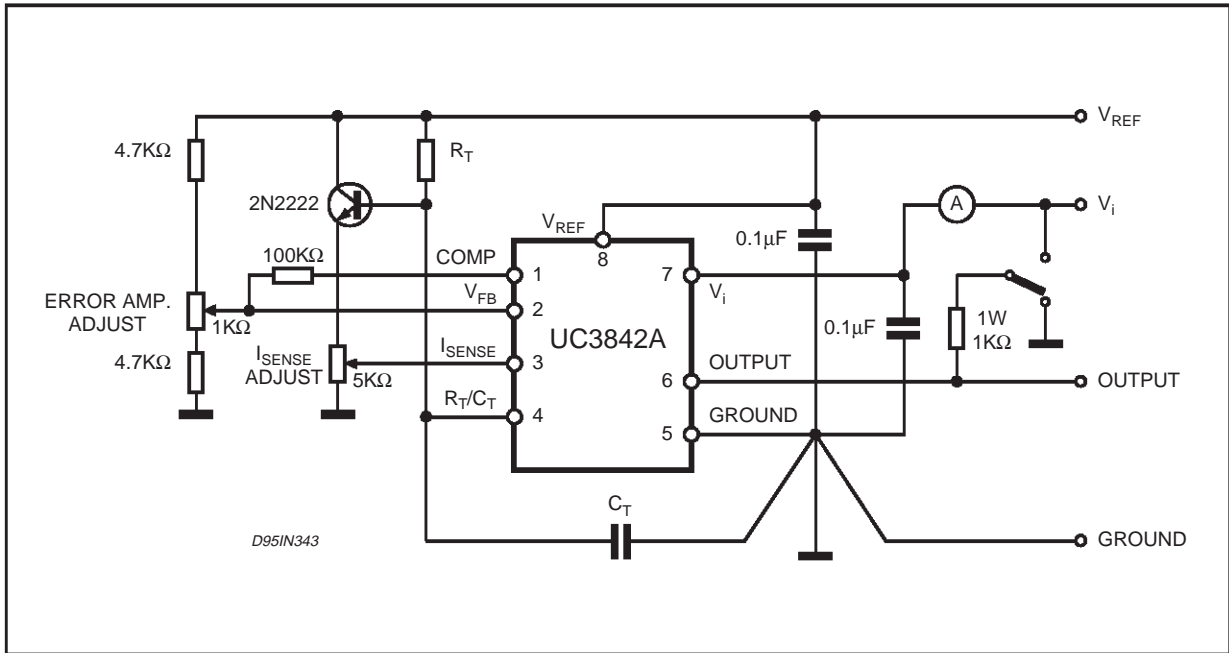
## UC2842A/3A/4A/5A - UC3842A/3A/4A/5A

### ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	UC284XA			UC384XA			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
<b>OUTPUT SECTION</b>									
V <sub>OL</sub>	Output Low Level	I <sub>SINK</sub> = 20mA		0.1	0.4		0.1	0.4	V
		I <sub>SINK</sub> = 200mA		1.6	2.2		1.6	2.2	V
V <sub>OH</sub>	Output High Level	I <sub>SOURCE</sub> = 20mA	13	13.5		13	13.5		V
		I <sub>SOURCE</sub> = 200mA	12	13.5		12	13.5		V
V <sub>OLS</sub>	UVLO Saturation	V <sub>CC</sub> = 6V; I <sub>SINK</sub> = 1mA		0.7	1.2		0.7	1.2	V
t <sub>r</sub>	Rise Time	T <sub>j</sub> = 25°C C <sub>L</sub> = 1nF (2)		50	150		50	150	ns
t <sub>f</sub>	Fall Time	T <sub>j</sub> = 25°C C <sub>L</sub> = 1nF (2)		50	150		50	150	ns
<b>UNDER-VOLTAGE LOCKOUT SECTION</b>									
	Start Threshold	X842A/4A	15	16	17	14.5	16	17.5	V
		X843A/5A	7.8	8.4	9.0	7.8	8.4	9.0	V
	Min Operating Voltage After Turn-on	X842A/4A	9	10	11	8.5	10	11.5	V
		X843A/5A	7.0	7.6	8.2	7.0	7.6	8.2	V
<b>PWM SECTION</b>									
	Maximum Duty Cycle	X842A/3A	94	96	100	94	96	100	%
		X844A/5A	47	48	50	47	48	50	%
	Minimum Duty Cycle				0			0	%
<b>TOTAL STANDBY CURRENT</b>									
I <sub>st</sub>	Start-up Current	V <sub>i</sub> = 6.5V for UCX843A/45A		0.3	0.5		0.3	0.5	mA
		V <sub>i</sub> = 14V for UCX842A/44A		0.3	0.5		0.3	0.5	mA
I <sub>i</sub>	Operating Supply Current	V <sub>PIN2</sub> = V <sub>PIN3</sub> = 0V		12	17		12	17	mA
V <sub>iz</sub>	Zener Voltage	I <sub>i</sub> = 25mA	30	36		30	36		V

- Notes :**
1. Max package power dissipation limits must be respected; low duty cycle pulse techniques are used during test maintain T<sub>j</sub> as close to T<sub>amb</sub> as possible.
  2. These parameters, although guaranteed, are not 100% tested in production.
  3. Parameter measured at trip point of latch with V<sub>PIN2</sub> = 0.
  4. Gain defined as :
 
$$A = \frac{\Delta V_{PIN1}}{\Delta V_{PIN3}} ; 0 \leq V_{PIN3} \leq 0.8V$$
  5. Adjust V<sub>i</sub> above the start threshold before setting at 15 V.

Figure 1: Open Loop Test Circuit.



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close

to pin 5 in a single point ground. The transistor and 5 KΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

Figure 2: Oscillator Frequency vs Timing Resistance

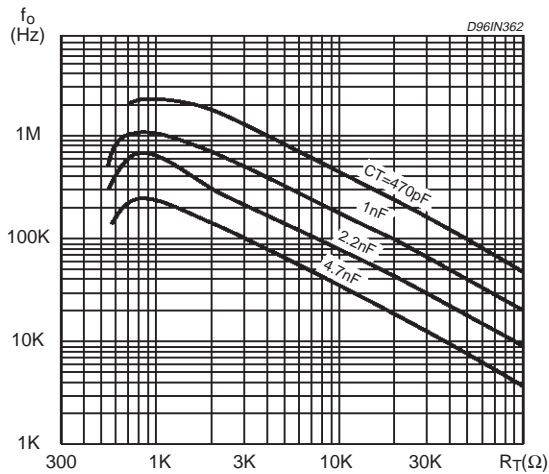
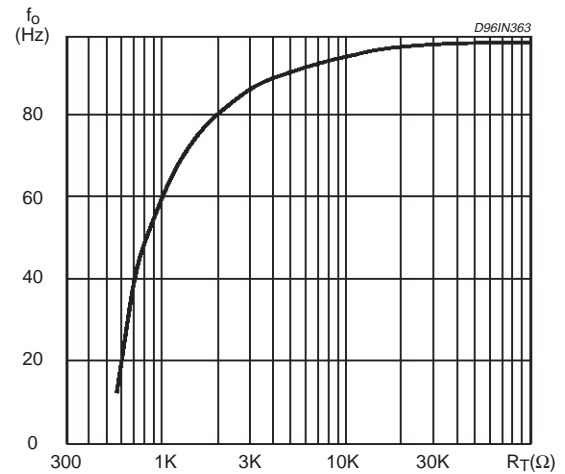
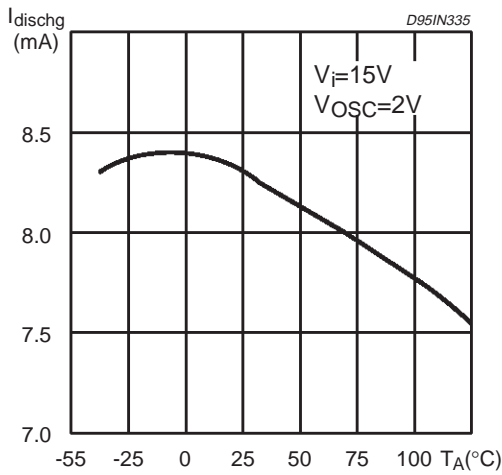


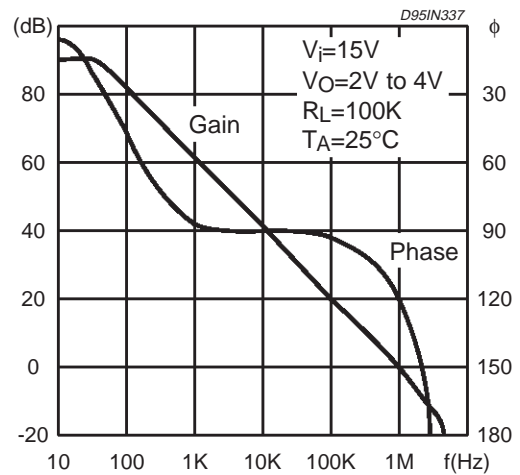
Figure 3: Maximum Duty Cycle vs Timing Resistor



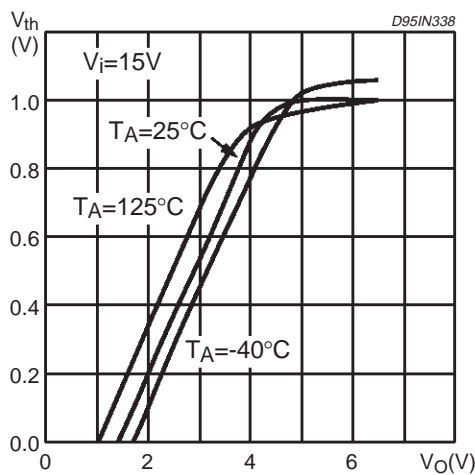
**Figure 4:** Oscillator Discharge Current vs. Temperature.



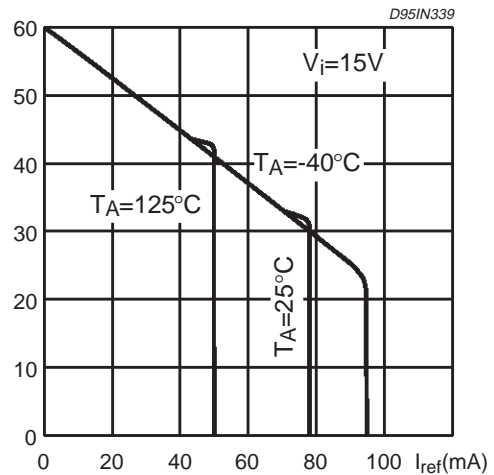
**Figure 5:** Error Amp Open-Loop Gain and Phase vs. Frequency.



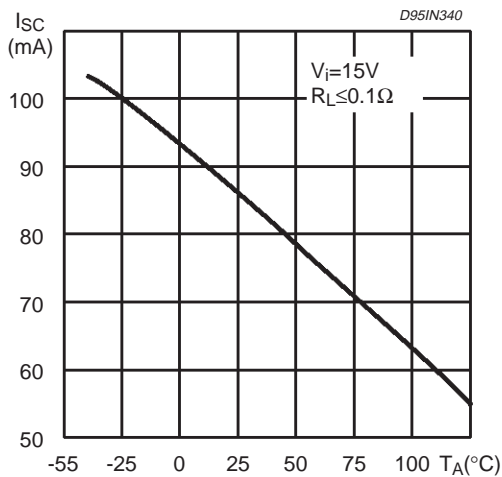
**Figure 6:** Current Sense Input Threshold vs. Error Amp Output Voltage.



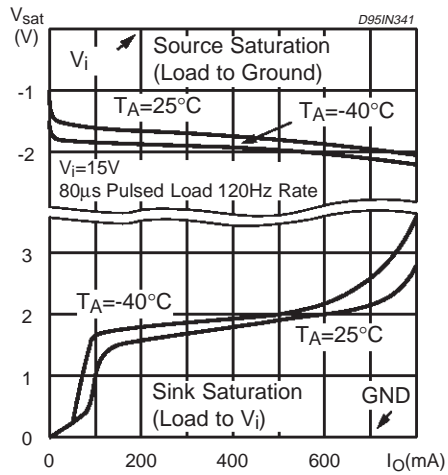
**Figure 7:** Reference Voltage Change vs. Source Current.



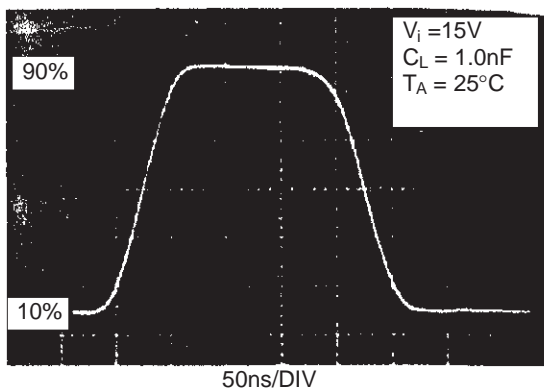
**Figure 8:** Reference Short Circuit Current vs. Temperature.



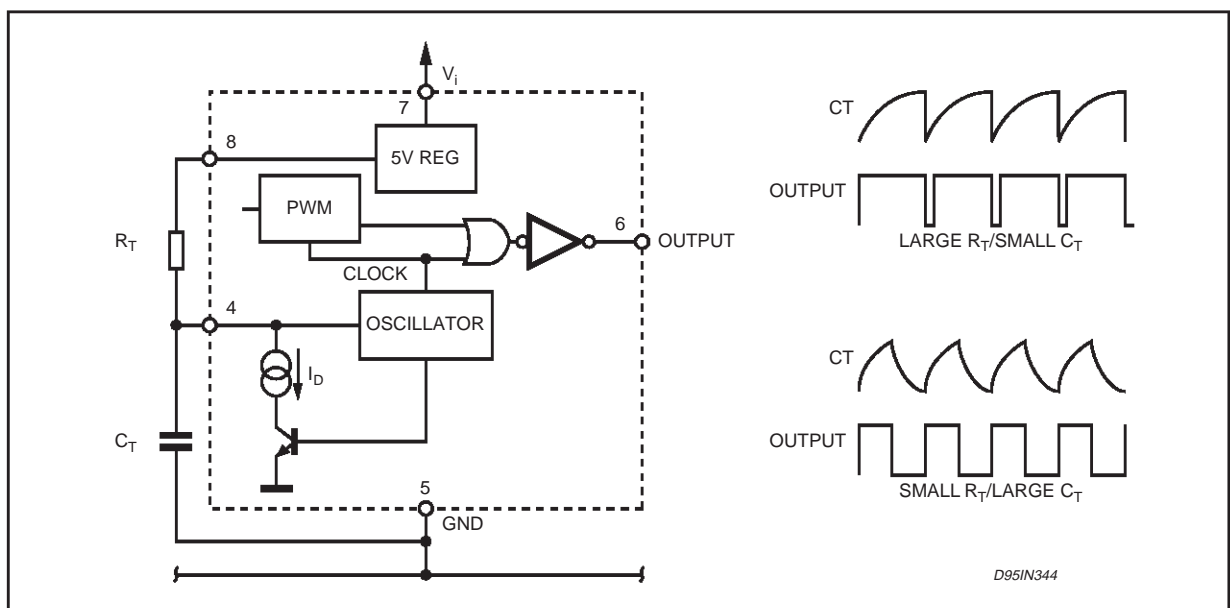
**Figure 9:** Output Saturation Voltage vs. Load Current.



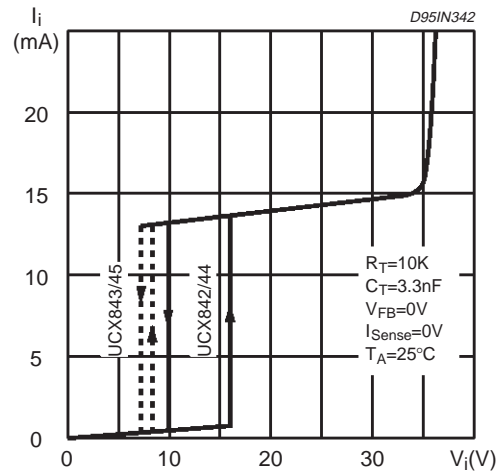
**Figure 11:** Output Waveform.



**Figure 13:** Oscillator and Output Waveforms.



**Figure 10:** Supply Current vs. Supply Voltage.



**Figure 12:** Output Cross Conduction

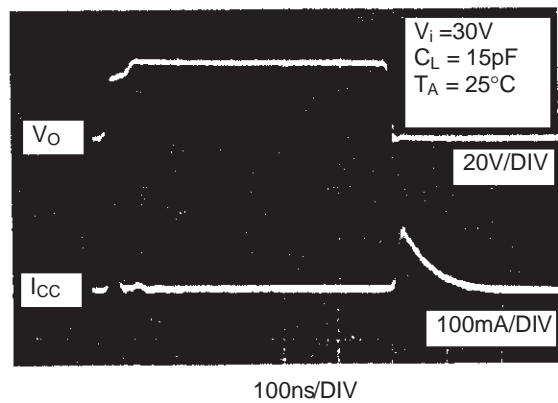


Figure 14 : Error Amp Configuration.

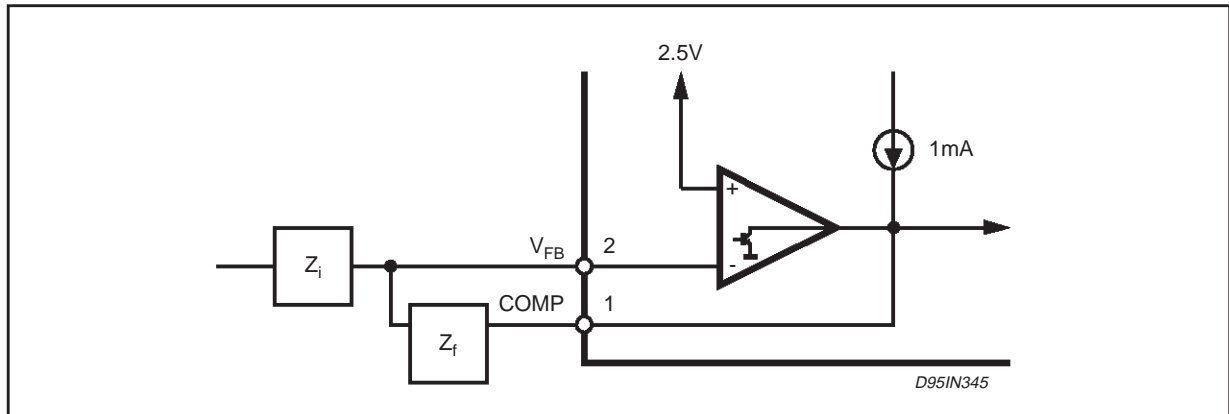


Figure 15 : Under Voltage Lockout.

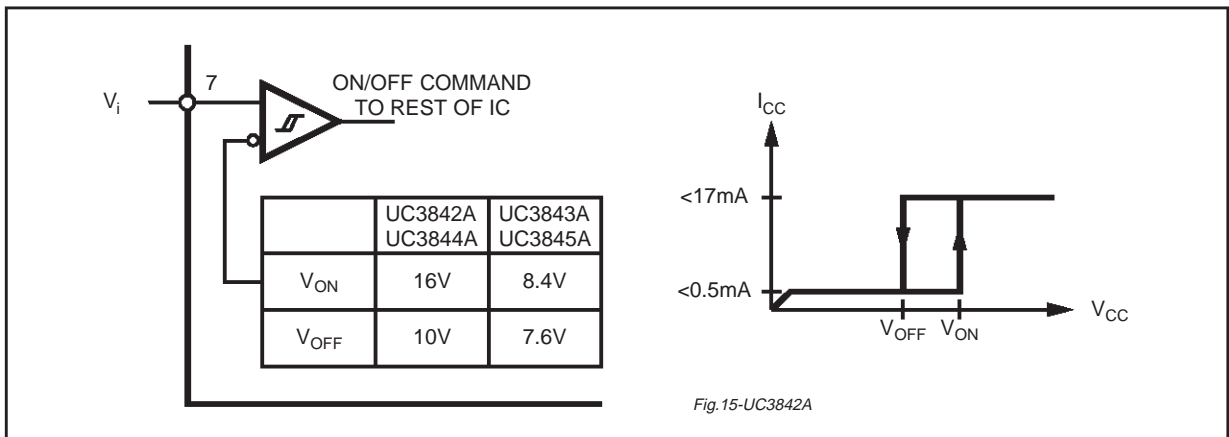
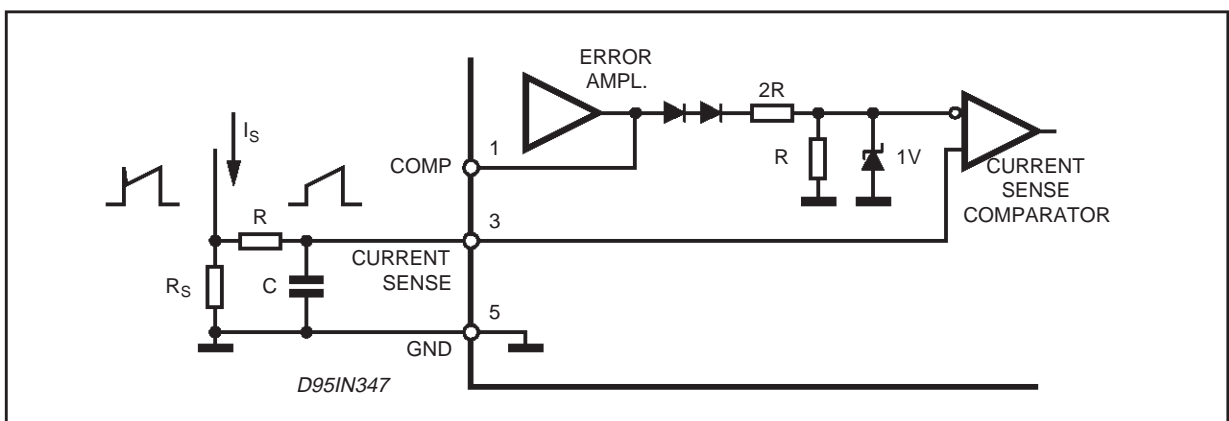


Figure 16 : Current Sense Circuit .



Peak current ( $i_s$ ) is determined by the formula

$$I_{s \max} \approx \frac{1.0 \text{ V}}{R_s}$$

A small RC filter may be required to suppress switch transients.



Figure 17 : Slope Compensation Techniques.

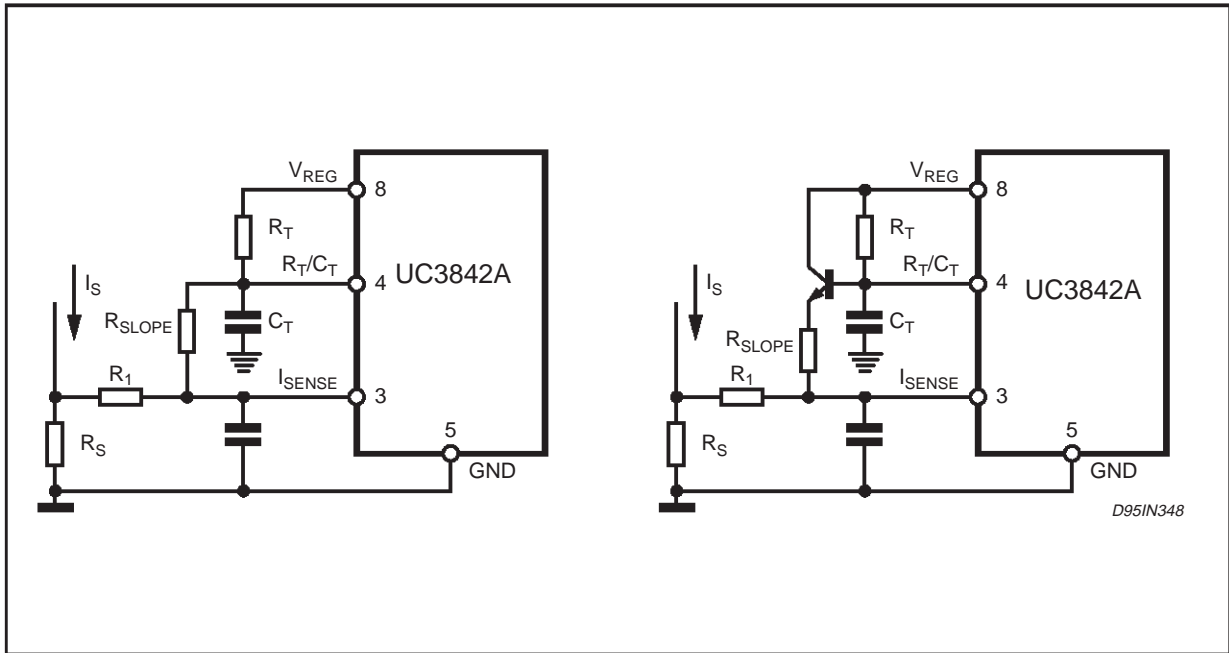


Figure 18 : Isolated MOSFET Drive and Current Transformer Sensing.

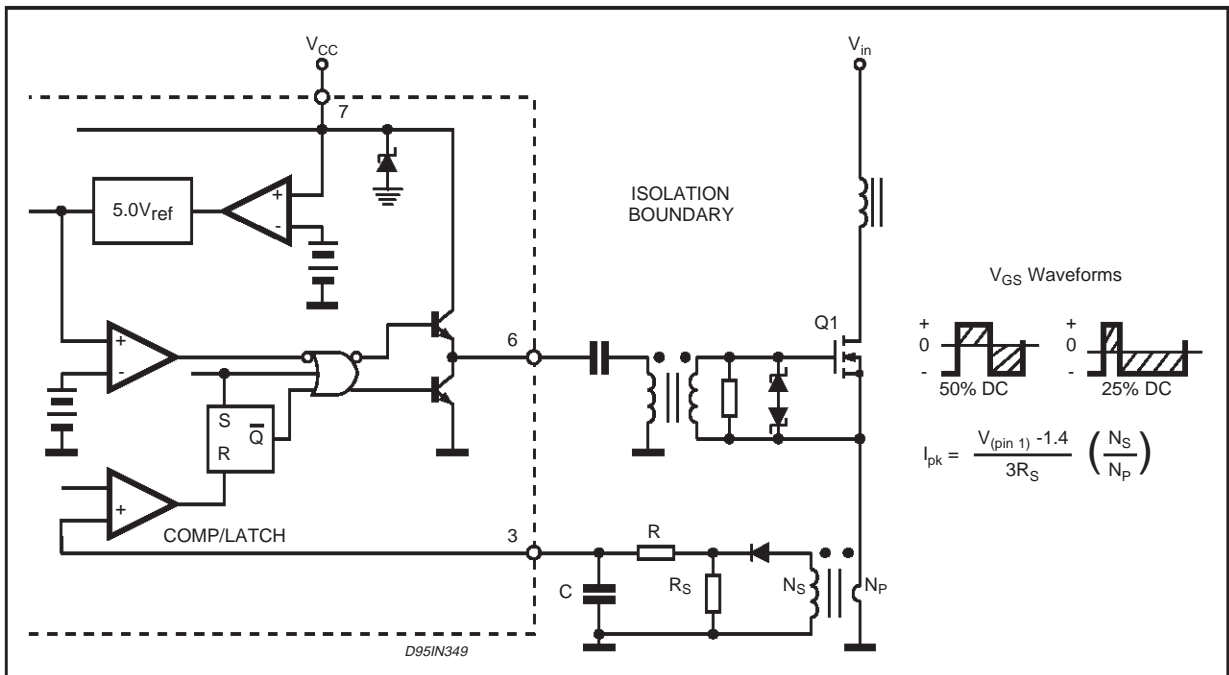


Figure 19 : Latched Shutdown.

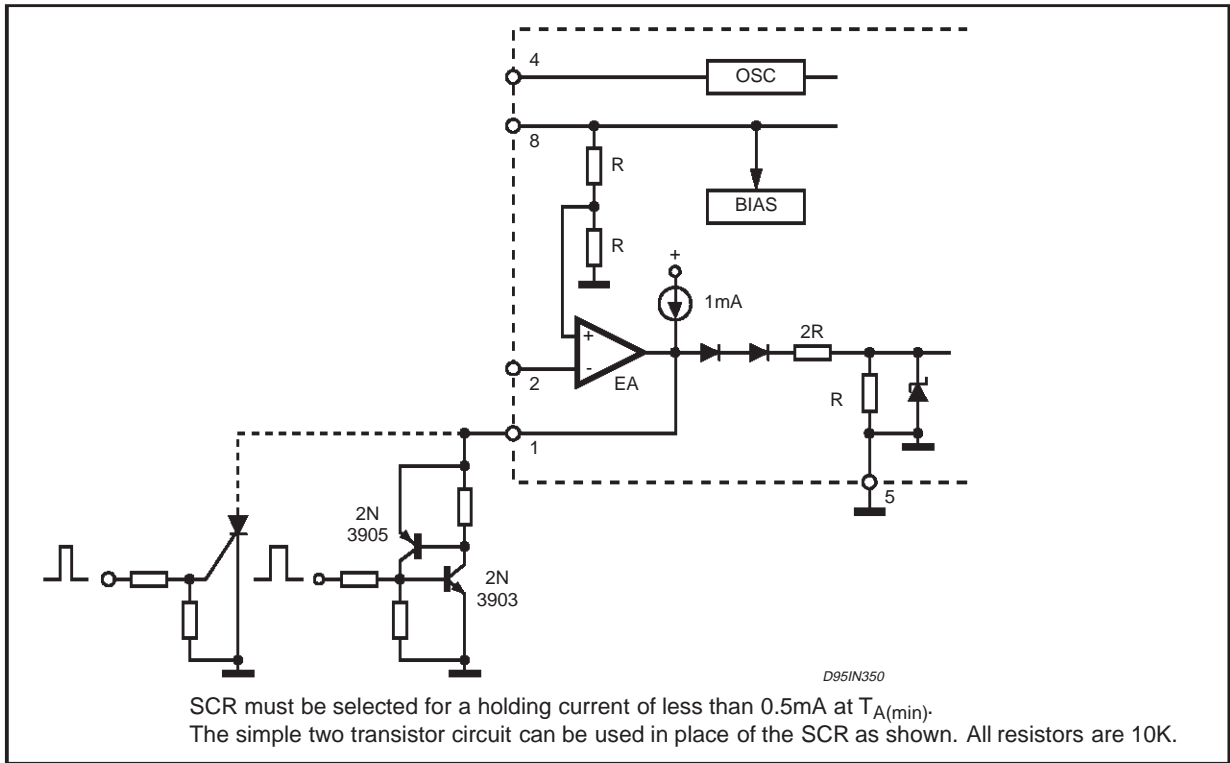


Figure 20: Error Amplifier Compensation

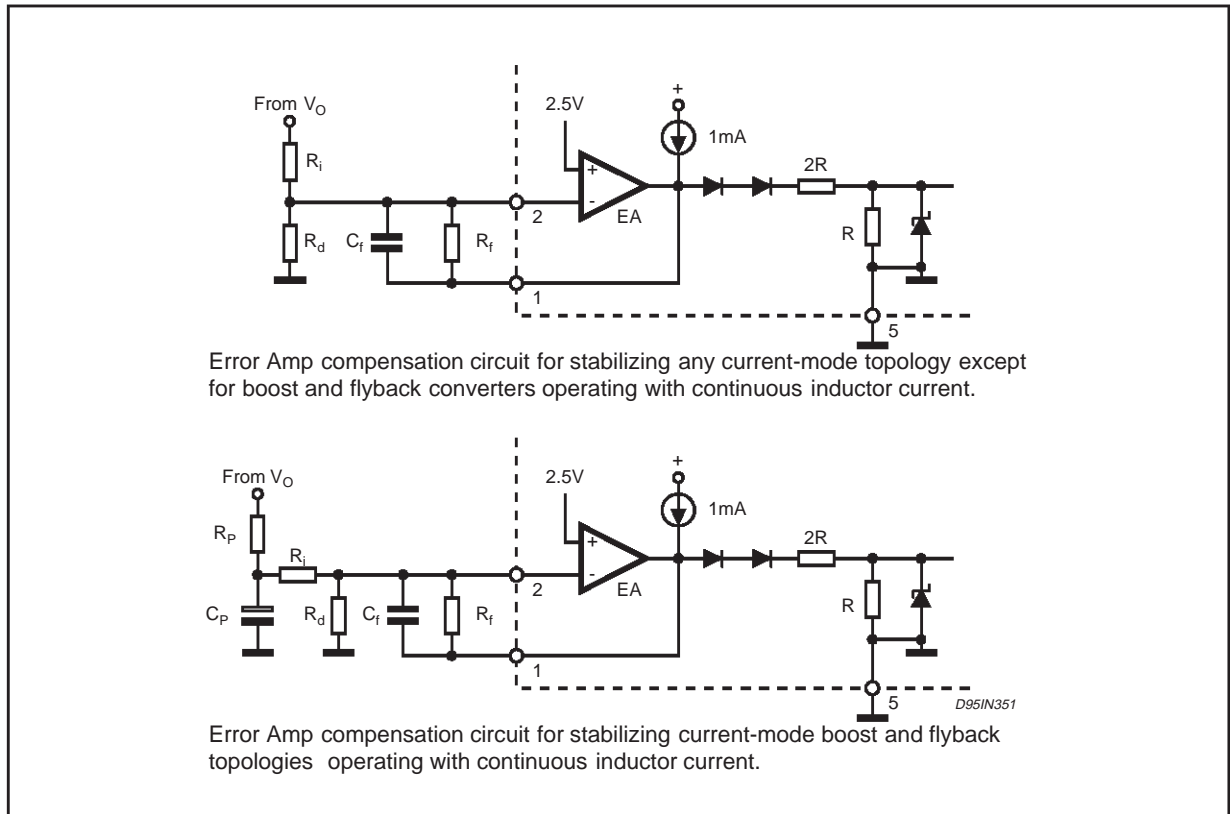


Figure 21: External Clock Synchronization.

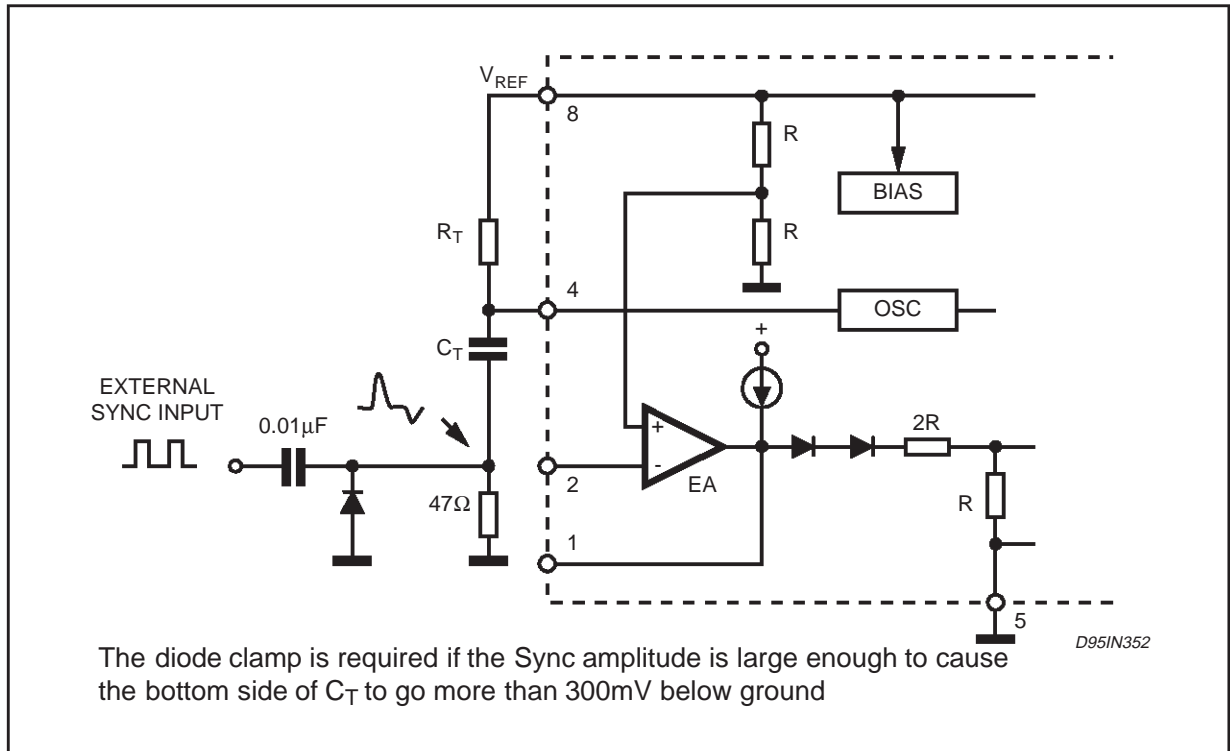


Figure 22: External Duty Cycle Clamp and Multi Unit Synchronization.

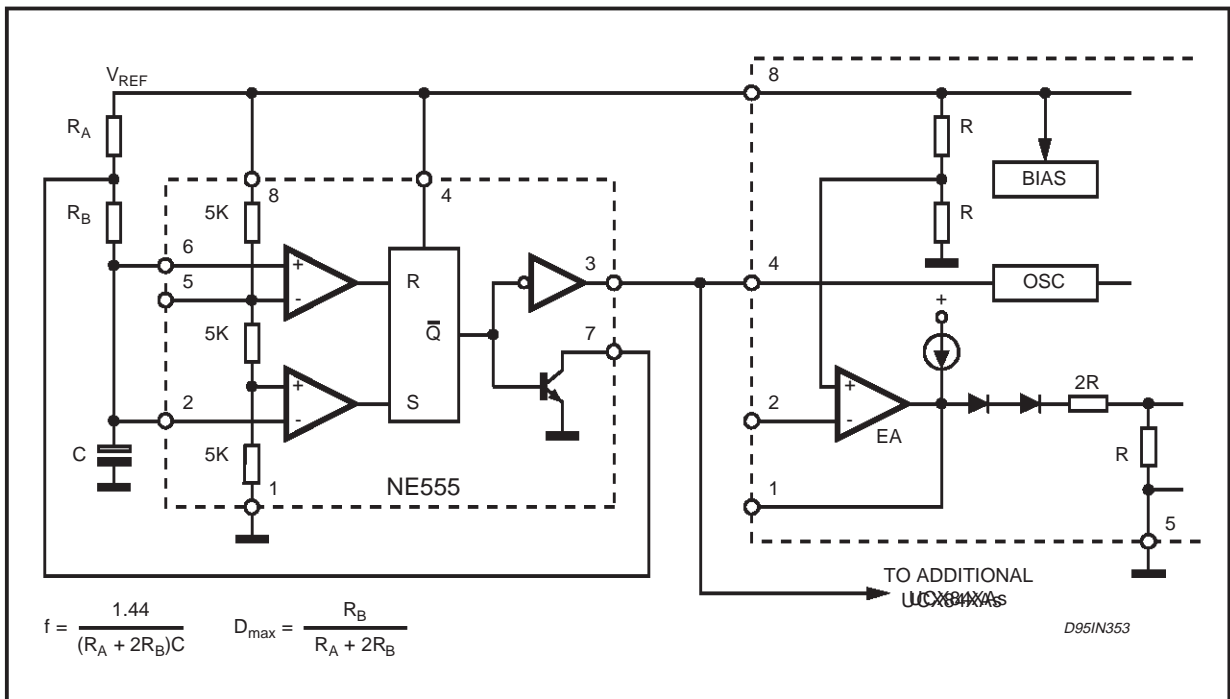


Figure 23: Soft-Start Circuit

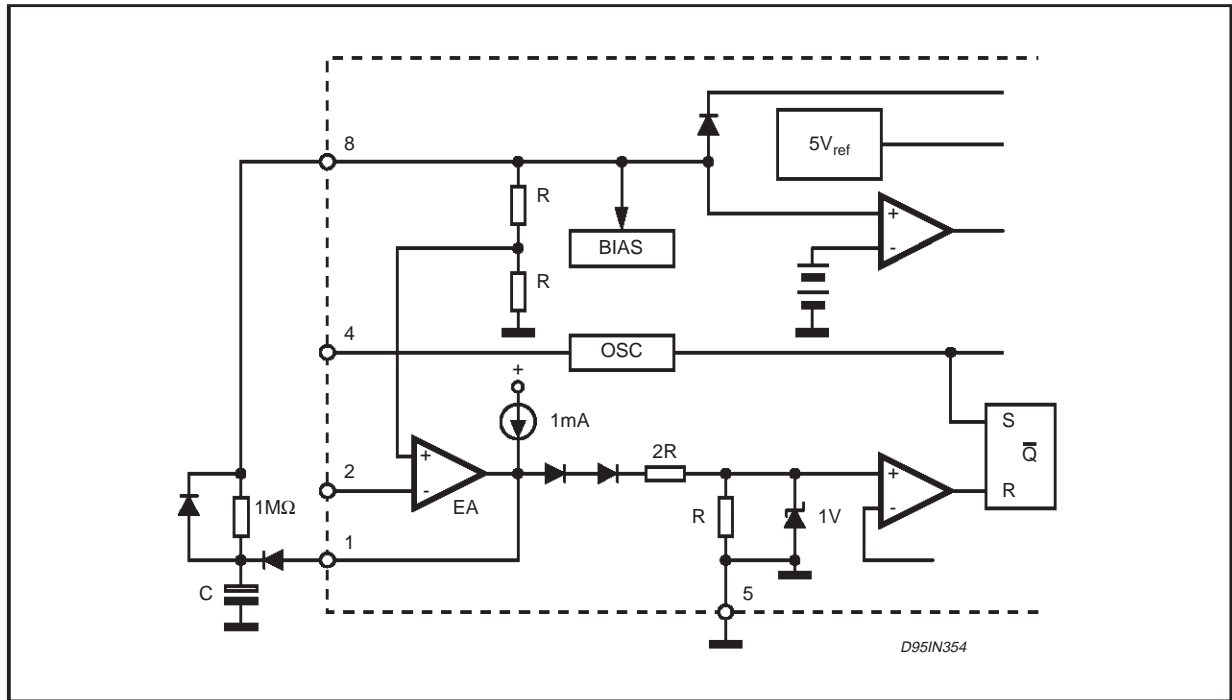
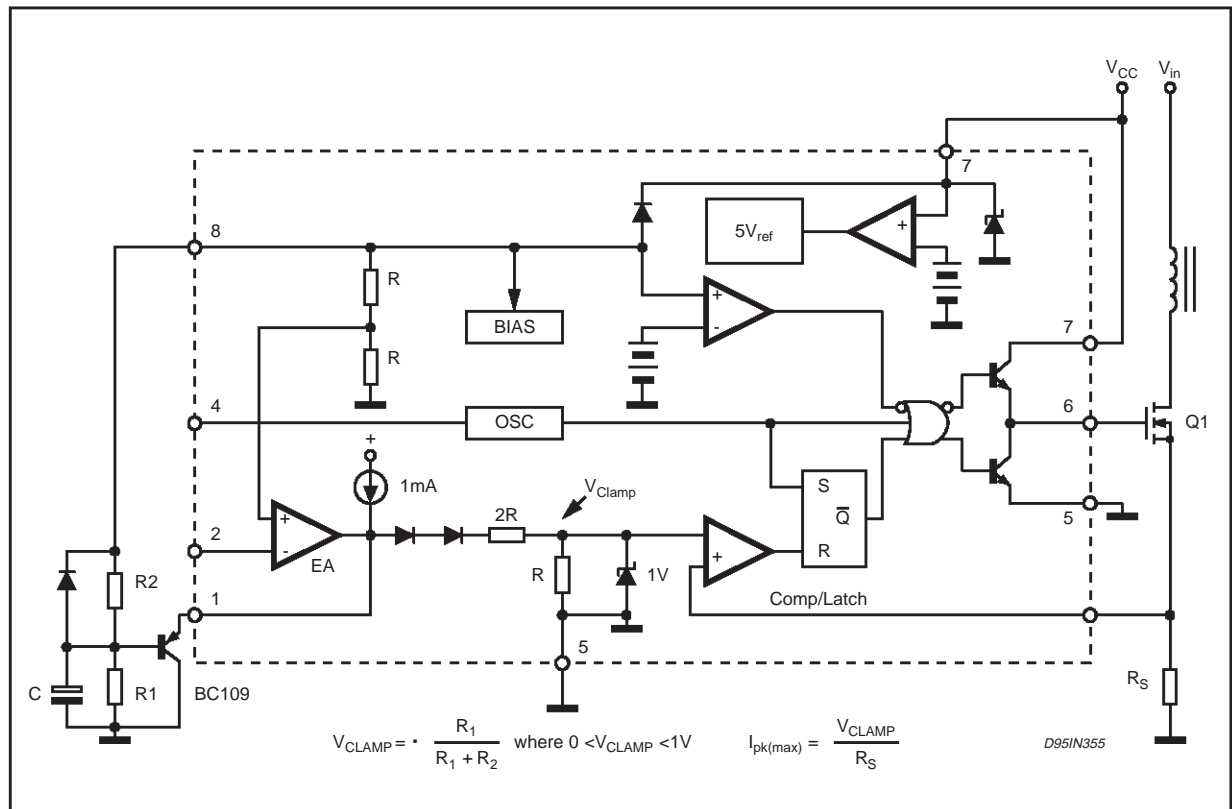


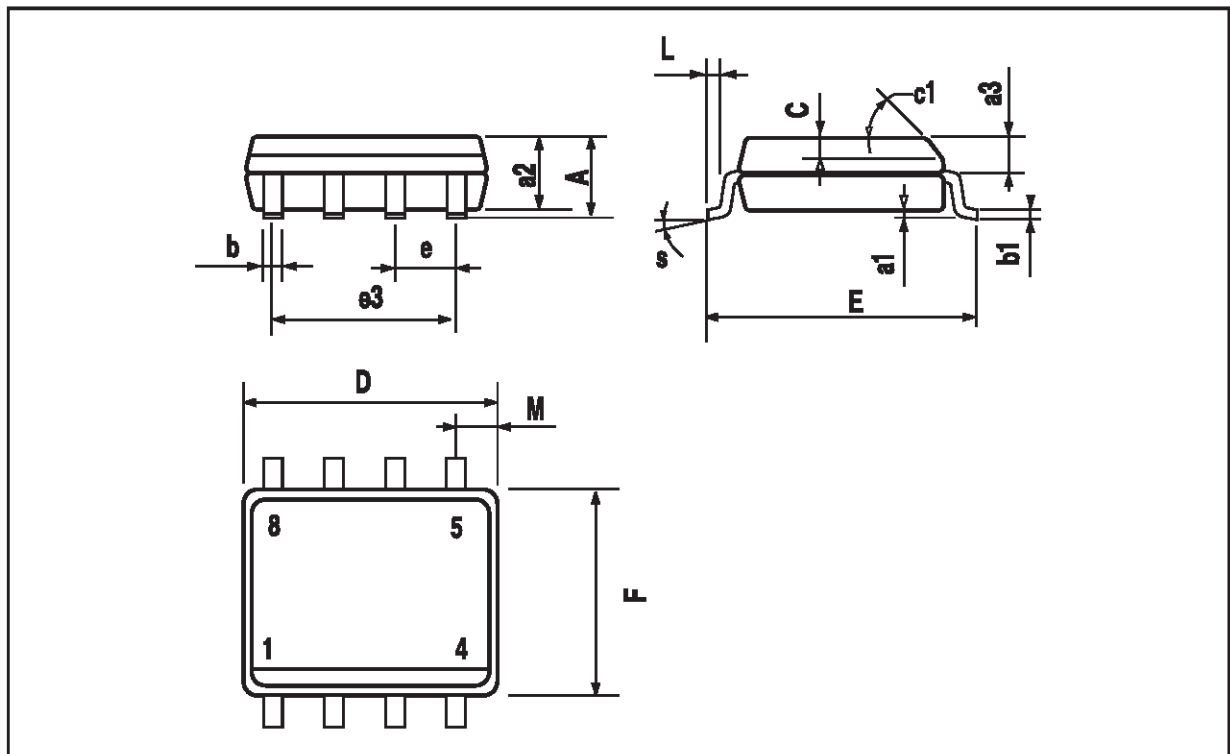
Figure 24: Soft-Start and Error Amplifier Output Duty Cycle Clamp.



**SO8 PACKAGE MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D (1)	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F (1)	3.8		4.0	0.15		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

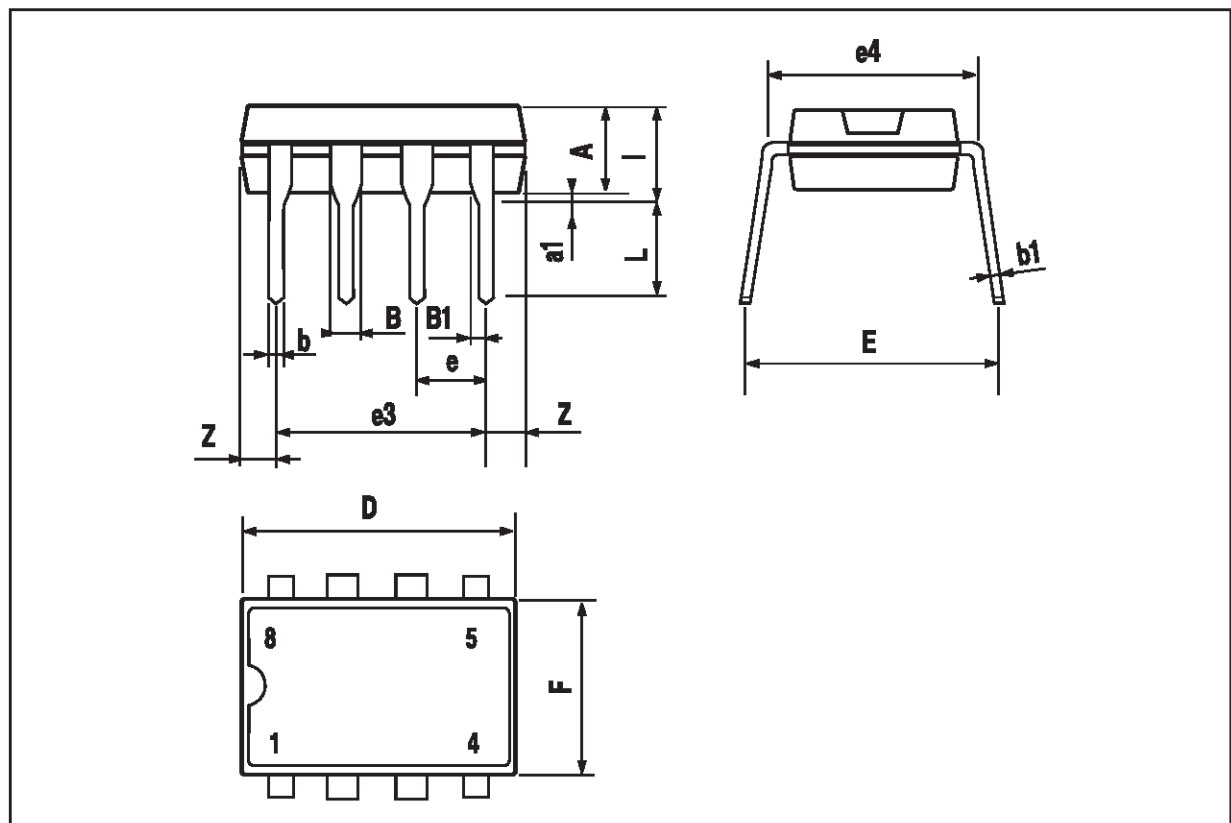
(1) D and F do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.006inch).



# UC2842A/3A/4A/5A - UC3842A/3A/4A/5A

## MINIDIP PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060



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