1.3 GHz PLL for TV- and VCR- Tuner

Description

The U6220B is a single chip frequency synthesizer with I²C bus and 3-wire bus control (universal bus). This IC contains a high frequency prescaler, a crystal oscillator, a switchable reference divider, 5 open collector switching outputs and an additional mixer switch output for band switching. The U6220B is especially designed for low cost, high performance 2-band and EasyLink tuners (please see application note ANT017 ‘Semiconductors for TV Tuners - The New EasyLink Concept’).

Features

- 1.3 GHz divide-by-8 prescaler integrated
- EasyLink interface to MOSMIC and mixer IC
- Universal bus:
  I²C bus or 3-wire bus
  I²C bus software compatible to U6204B
  3-wire bus software compatible to U6359B (18 bit)
- I²C bus mode:
  5 port outputs (open collector)
  4 addresses selectable at Pin 3 for multituner application
- 3-wire bus mode:
  4 port outputs (open collector)
  Lock-signal output (open collector)
- Low power consumption (typ. 5 V / 20 mA)
- Electrostatic protection according to MIL-STD 883
- SO16 small package

Block Diagram

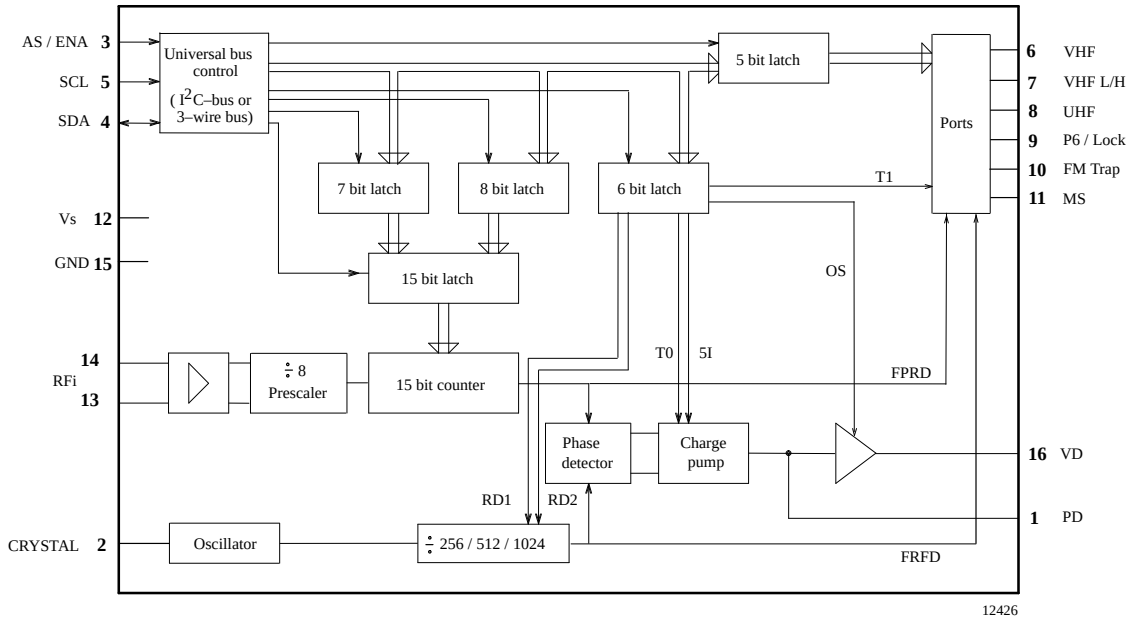


Figure 1. Block diagram

Ordering Information

Extended Type Number	Package	Remarks
U6220B-APG3	SO16 plastic	Taped and reeled

Pin Description

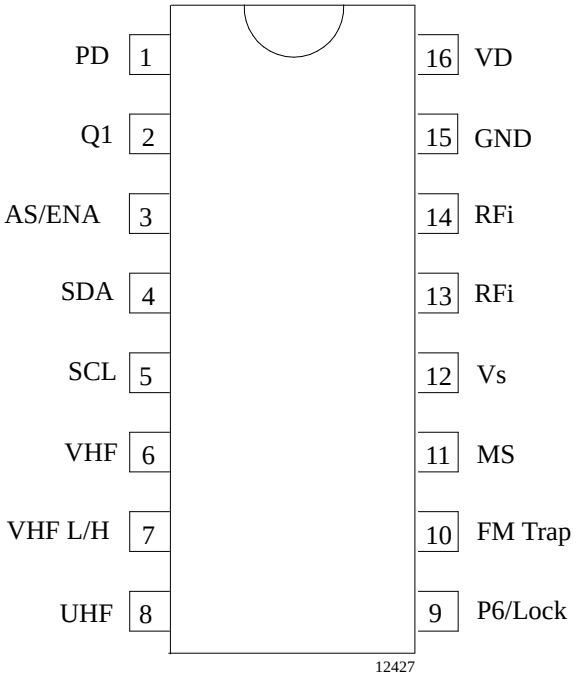


Figure 2. Pinning

Pin	Symbol	Function
1	PD	Charge pump output
2	Q1	Crystal input
3	AS/ ENA	Address select input Enable input
4	SDA	Data input/ output
5	SCL	Clock input
6	VHF	VHF switch
7	VHF L/H	VHF low/ high switch
8	UHF	UHF switch
9	P6/ Lock	Port output (I^2C bus mode) Lock output (3-wire bus mode)
10	FM Trap	Channel 6 FM Trap switch
11	MS	Mixer switch output
12	V_S	Supply voltage
13	RFi	RF input
14	RFi	RF input
15	END	Ground
16	VD	Active filter output

Description

The U6220B is a single cip PLL designed for TV and VCR receiver systems. It consists of a divide-by-8 prescaler (up to 1.3 GHz) with an integrated preamplifier, a 15bit programmable divider, a crystal oscillator and a reference divider with three selectable divider ratios ($\div 256$ / $\div 512$ / $\div 1024$), a phase/frequency detector together with a charge-pump, which drives the tuning amplifier. Only one external transistor is required for varactor line driving. The device can be controlled via a I^2C bus format or 3-wire bus format. It detects automatically which bus format has been received, therefore there is no need for a bus selection pin. In I^2C bus mode the device has four programmable addresses, programmed by applying a specific input voltage to the address select input, enabling the use of up to four synthesizers in a system. The same pin serves in 3-wire bus mode as the enable signal input. Five open collector outputs for band switching functions are included, four of them are capable of sinking at least 10 mA and the VHF L/H output can sink 30 mA. One of these open collector outputs serves as a lock-signal output in the 3-wire bus mode. The MS output is provided to control directly a mixer-oscillator IC according to the band switching information.

Absolute Maximum Ratings

All voltages are referred to GND (Pin 15)

Parameters	Test Conditions / Pins	Symbol	Min.	Max.	Unit
Supply voltage	Pin 12	V_S	–0.3	6	V
RF input voltage	Pins 13 and 14	RFi	–0.3	V_S + 0.3	V
Crystal oscillator voltage	Pin 2	Q1	–0.3	V_S + 0.3	V
Charge pump output voltage	Pin 1	PD	–0.3	V_S + 0.3	V
Active filter output voltage	Pin 16	VD	–0.3	V_S + 0.3	V
Bus input/ output voltage	Pins 4 and 5	VSDA,SCL	–0.3	6	V
SDA output current	Open collector Pin 4	ISDA	–1	5	mA
Address select / ENA voltage	Pin 3	VAS/ENA	–0.3	V_S + 0.3	V
Mixer switch voltage	Pin 11	MS	–0.3	V_S + 0.3	V
Port output current	Open collector, Pins 6, 8-10		–1	15	mA
Port output current	Open collector, Pin 7	VHF L/H	–1	40	mA
Total port output current	Open collector, Pins 6 to 10			50	mA
Port output voltage	In off state, Pins 6 to 10		–0.3 –0.3	14 6	V V
Junction temperature	In on state	T_{jmax}	–40	150	°C
Storage temperature		T_{stg}	–40	150	°C

Operating Range

All voltages are referred to GND (Pin 15)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Pin 12	V_S	4.5	5	5.5	V
Ambient temperature		T_{amb}	–20		85	°C
Input frequency	Pins 13 and 14	Rfi	80		1300	MHz
Programmable divider	I^2C bus mode 3-wire bus mode	SF	256 256		32767 16383	

Thermal Resistance

Parameters	Symbol	Test conditions	Value	Unit
Junction ambient	R_{thJA}	Soldered to PCB	110	K/W

Electrical Characteristics

Test conditions (unless otherwise specified): V_S = 5 V, T_{amb} = 25°C

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply current	VHF, UHF: on VHF L/H, FM Trap: off Pin 12	I_S	15	20	25	mA
Input sensitivity						
f_{RFi} = 80 - 1000 MHz	Pin 13	V_{RFi} [1]	10		315	mVrms
f_{RFi} = 1300 MHz	Pin 13	V_{RFi} [1]	40		315	mVrms
Crystal oscillator						
Recommended crystal series resistance			10		200	Ω
Crystal oscillator drive level	Pin 2			50		mVrms
Crystal oscillator source impedance	Nominal spread ± 15%, Pin 2			–650		Ω
External reference input frequency	AC coupled sinewave Pin 2		2		8	MHz
External reference input amplitude	AC coupled sinewave Pin 2	V_i [1]	70		200	mVrms
Switching output / lock output (open collector, VHF (Pin 6), UHF (Pin 8), P6/Lock (Pin 9), FMtrap (Pin 10), Lock condition: LOW)						
Leakage current	VH = 13.5 V	IL			10	µA
Saturation voltage	IL = 10 mA	VSL [2]			0.5	V
VHF L/H switching output (open collector, VHF L/H (Pin 7))						
Leakage current	VH = 13.5 V	IL			10	µA
Saturation voltage	IL = 30 mA	VSL [2]			0.5	V

Notes: [1] RMS - voltage calculated from the measured available power om 50 Ω
[2] Tested with one switch active. The collector voltage may not exceed 6 V

Electrical Characteristics (continued)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Charge pump output, PD						
Charge pump current 'H' (I^2C and 3-wire bus mode)	5l = 1, VPD = 1.7 V Pin 1	IPDH		± 180		µA
Charge pump current 'L' (only I^2C bus mode)	5l = 1, VPD = 1.7 V Pin 1	IPDL		± 50		nA
Charge pump leakage current	T0 = 0, VPD = 1.7 V Pin 1	IPDTRI		± 5		nA
Charge pump amplifier gain	Pins 1 and 16			6400		
Bus inputs, SDA, SCL						
Input voltage high	Pins 4 and 5	Vi'H'	3		5.5	V
Input voltage low	Pin 4 and 5	Vi'L'			1.5	V
Input current high	Vi'H' = V_S Pins 4 and 5	Ii'H'			10	µA
Input current low	Vi'L' = 0 V Pins 4 and 5	Ii'L'	–10			µA
Leakage current	V_S = 0 V Pins 4 and 5	IL			10	µA
Output voltage SDA (open collector)	ISDA'L' = 3 mA Pin 4	VSDA'L'			0.4	V
Address selection / Enable input, AS / ENA						
Input current high	Vi'H' = V_S Pin 3	Ii'H'			10	µA
Input current low	Vi'L' = 0 V Pin 3	Ii'L'	–100			µA
Mixer switch output, MS						
Output voltage VHF	I_{MS} = –20 uA Pin 11	$V_{MS\ VHF}$	0	0.25	1	V
Output voltage UHF	I_{MS} = –20 uA Pin 11	$V_{MS\ UHF}$	3.5	V_S–0.75	V_S	µA

Functional Description

The U6220B is programmed via a 2-wire I^2C bus or 3-wire bus depending on the received data format. The three bus inputs Pins 3, 4 and 5 are used as address select, SDA and SCL inputs in I^2C bus mode and as ENABLE, DATA and CLOCK inputs in 3-wire bus mode. The data includes the scaling factor SF (15/14bit) and switching output information. In I^2C bus mode, there are some additional functions included for testing of the device.

Oscillator frequency calculation:

$$f_{VCO} = 8 \times SPF \times f_{refOSC} / SRF$$

f_{VCO}: Locked frequency of voltage controlled oscillator

SPF: Scaling factor of programmable divider (15bit in I^2C- or 14bit in 3-wire bus mode)

SRF: Scaling factor of reference divider ($\div 256$/ $\div 512$/ $\div 1024$/ in I^2C bus mode or $\div 512$ in 3-wire bus mode)

f_{refOSC}: Reference oscillator frequency: 3.2/ 4 MHz crystal or external reference frequency

This input amplifier together with a divide-by-8 prescaler provides excellent sensitivity (see 'TYPICAL PRESCALER INPUT SENSITIVITY'. The input impedance is shown in the diagram 'TYPICAL IMPEDANCE'. When a new divider ratio according to the requested f_{VCO} is entered, the phase detector and charge pump together with the tuning amplifier adjusts the control voltage of the VCO until the output signals of the programmable divider and the reference divider are in frequency locked and phase locked. The reference frequency may be provided by an external source capacitively coupled into Pin 2, or by using an on-board crystal with an 18 pF capacitor in series. The crystal operates in the series resonance mode. In I^2C bus mode the reference divider division ratio is selectable to $\div 256$/ $\div 512$/ $\div 1024$ to two bits of the control byte 2. In 3-wire bus mode it is fixed to $\div 512$. Therefore, with a 4 MHz crystal and the nominal division ratio of $\div 512$ of the reference divider, the comparison frequency is 7.8125 kHz, which gives 62.5 kHz steps for the VCO, or with a 3.2 kHz crystal respectively 6.25 kHz comparison frequency and 50 kHz VCO step size. In addition, there are switching outputs available for band switching and other purposes.

Application

A typical application is shown on page 13. All input/ output interface circuits are shown on page 11.

Some special features which are related to test- and alignment procedures for tuner production are explained together within the following bus mode description.

I^2C Bus Description

When the U6220B is controlled via a 2-wire I^2C bus format, then data and clock signals are fed into the SDA and SCL lines respectively. The table 'I^2C BUS DATA FORMAT' describes the format of the data and shows how to select the device address by applying a voltage at Pin 3. When the correct address byte has been received., the SDA line is pulled low by the device during the acknowledge period, and then also during the acknowledge periods, when additional data bytes are programmed. After the address transmission (first byte), data bytes can be sent to the device. There are four data bytes requested to fully program the device. The table 'I^2C BUS PULSE DIAGRAM' shows some possible data transfer examples.

Programmable divider bytes PDB1 and PDB2 are stored in a 15 bit latch and control the division ratio of the 15 bit programmable divider. The control byte CB1 enables the control of the following special functions:

– 5l-bit switches between low and high charge pump current

– T1-bit enables divider test mode when it is set to logic 1

– T0-bit allows to disable the charge pump when it is set to logic 1

– RD1-bit and RD2-bit allow to select the reference divider factor.

– Os-bit disables the charge pump drive amplifier output when it is set to logic 1.

The charge pump current can only be controlled in I^2C bus mode. In 3-wire bus mode, there is always the high charge pump current active. The OS-bit function disables the complete PLL function. This enables the tuner alignment by supplying the tuning voltage directly through the 33 V supply voltage of the tuner. The control byte CB2 programs the switching outputs VHF, VHF L/H, UHF, P6, FM Trap according the band switching logic table on page 8.

I²C Bus Description (continued)

Description	I2C Bus Data Format								
	MSB								
Address byte	1	1	0	0	0	AS1	AS2	0	A
Programmable divider, byte 1	0	n14	n13	n12	n11	n10	n9	n8	A
Programmable divider, byte 2	n7	n6	n5	n4	n3	n2	n1	n0	A
Control byte 1	1	5l	T1	T0	x	RD2	Rd1	OS	A
Control byte 2	x	P6	x	P4	x	P2	P1	P0	A

A = Acknowledge, X = not used

n0...n14: Scaling factor (SF) SF = 16384 x n14 + 8192 x n13 +...+2 x n1 + n0
T0, T1: Testmode selection T1 = 1: divider test mode on T1 = 0: divider test mode off
FPRD at Pin 6/ FRFD at Pin 7
T0 = 1: charge pump disable T0 = 0: charge pump enable
P0, 1, 2, 4 Band switching according logic table page 8
P6 Port output P6 = 1; open collector active
5I: Charge pump current switch 5l = 1: high current 5l = 0: low current
OS: Output switch OS = 1: varicap drive disable OS = 0: varicap drive enable

RD1, RD2: Reference divider selection

RD2	RD1	Reference divider ratio
0	0	off
0	1	1024
1	0	256
1	1	512

AS1, AS2: Address selection Pin 3

AS1	AS2	Address	Dec. value	Voltage at Pin 3
0	1	1	194	open
0	0	2	192	0 to 10% V_S
1	0	3	196	40 to 60% V_S
1	1	4	198	90 to 100% V_S

I²C Bus Description (continued)

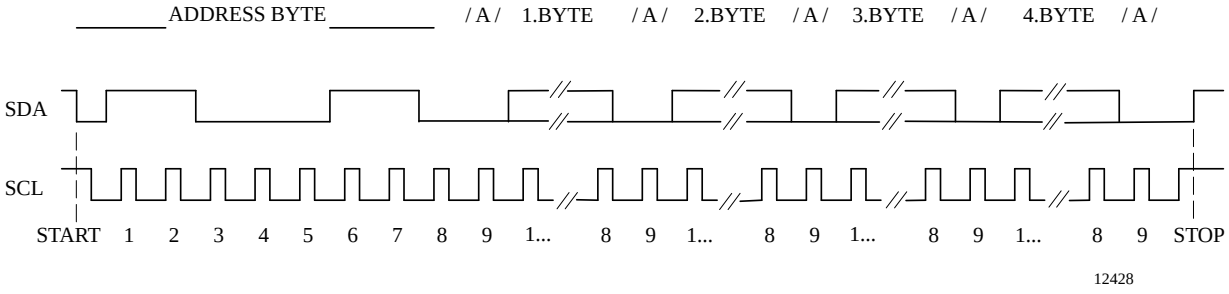
Band Switching Logic in I²C Bus Mode

(2 mixer EasyLink with MOSMIC gate1 switch off logic)

	P0	P4	P2	P1	VHF Pin6	VHF L/H Pin 7	UHF Pin 8	FM Trap Pin 10	MS Pin 11
UHF	1	0	0	0	on	off	off	off	4 V
VHF high	0	0	1	0	off	on	on	off	0 V
VHF low (except channel 6)	0	0	0	1	off	off	on	off	0 V
VHF channel 6	0	1	0	1	off	off	on	on	0 V

– Port VHF switches the VHF MOSMIC (inverse logic)
– Port VHF L/H switches the VHF switching-diode (high output current output)
– Port UHF switches the UHF MOSMIC (inverse logic)
– Port FM Trap switches the FM Trap in channel 6
– Port MS switches the MX band switch input (e.g. U2326B)

I²C Bus Pulse Diagram

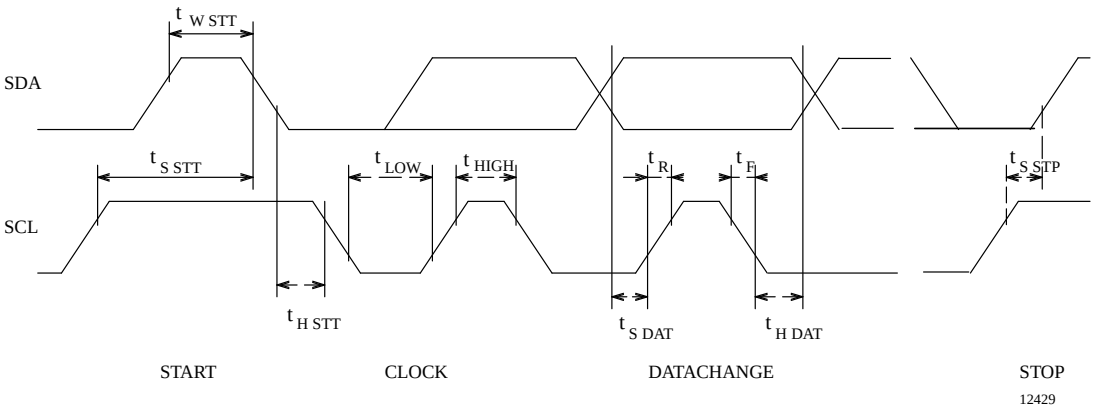


Data transfer examples
START - ADR - PDB1 -PDB2 - CB1 - CB2 - STOP
START - ADR - CB1 - CB2 -PDB1 - PDB2 - STOP
START - ADR - PDB1 - PDB2 - CB1 - STOP
START - ADR - CB1 - CB2 - PDB1 - STOP
START - ADR - PDB1 - PSB2 - STOP
START - ADR -CB1 - CB2 - STOP
START - ADR - CB1 - STOP

Description
START = Start condition
ADR = Address byte
PDB1 = Programmable divider byte 1
PDB2 = Programmable divider byte 2
CB1 = Control byte 1
CB2 = Control byte 2
STOP = Stop condition

I²C Bus Description (continued)

I²C Bus Timing



Parameter	Symbol	Conditions	Min.	Max.	Unit
Rise time SDA, SCL	tR			15	µs
Fall time SDA, SCL	tF			15	µs
Clock frequency SCL	FSCL		0	100	kHz
Clock ‘H’ pulse	tHIGH		4		µs
Clock ‘L’ pulse	tLOW		4		µs
Hold time start	tH STT		4		µs
Waiting time start	tW STT		4		µs
Setup time start	tS STT		4		µs
Setup time stop	tS STP		4		µs
Setup time data	tS DAT		0.3		µs
Hold time data	tH DAT		0		µs

3-Wire Bus Description

When the U6220B is controlled via a 3-wire bus format, then data, clock and enable signals are fed into the SDA, SCL and AS/ENA lines respectively. The diagram ‘3-WIRE BUS PULSE DIAGRAM’ shows the data format. The data consist of a single word, which contains the programmable divider (14bit) and switch information (4 bit). The data is only clocked into the internal data shift register on the negative clock transition during the enable high period. During enable low periods, the clock input is disabled. New data words are only accepted by the internal data latches from the shift register on a negative transition of the enable signal, if exactly eighteen clock pulses were sent during the high period of the enable. The data sequence and the timing is described in the following diagrams.

In 3-wire bus mode Pin 9 becomes automatically the lock-signal output. an improved lock detect circuit generates a flag when the loop has attained lock. ‘In lock’ is indicated by a low impedance state (on) of the open collector output.

In 3-wire bus mode, the high charge pump current is always. Only in I²C bus mode can the charge pump current be controlled.

The complete PLL function can be disabled by programming a division ratio of zero, which is normally not used. This enables the tuner alignment by supplying the tuning voltage directly through the 33-V supply voltage of the tuner.

In 3-wire bus mode the division ratio of the reference divider is fixed to divide by 512. It can be controlled only in I²C bus mode.

3-Wire Bus Description (continued)

Band Switching Logic in 3-Wire Bus Mode

(2-mixer EasyLink with MOSMIC gate 1 switch off logic)

	B1	B2	B3	B4	VHF Pin 6	VHF L/H Pin 7	UHF Pin 8	FM Trap Pin 10	MS Pin 11
UHF	1	0	0	0	on	off	off	off	4 V
VHF high	0	0	1	0	off	on	on	off	0 V
VHF low (except channel 6)	0	0	0	1	off	off	on	off	0 V
VHF channel 6	0	1	0	1	off	off	on	on	0 V

– Port VHF switches the VHF-MOSMIC (inverse logic)
– Port VHF L/H switches the VHF-switching diode (high output current output)
– Port UHF switches the UHF-MOSMIC (inverse logic)
– Port FM Trap switches the FM Trap in channel 6
– Port MS switches the MX band switch input (e.g. U2326B)

3-Wire Bus Pulse Diagram

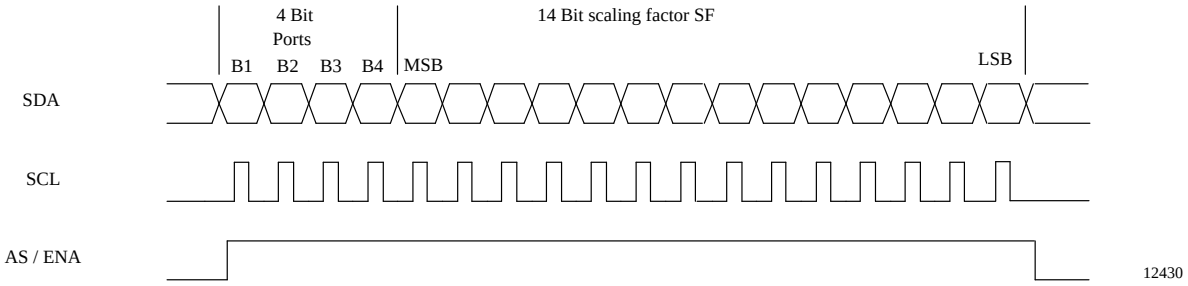


Figure 3.

3-Wire Bus Timing

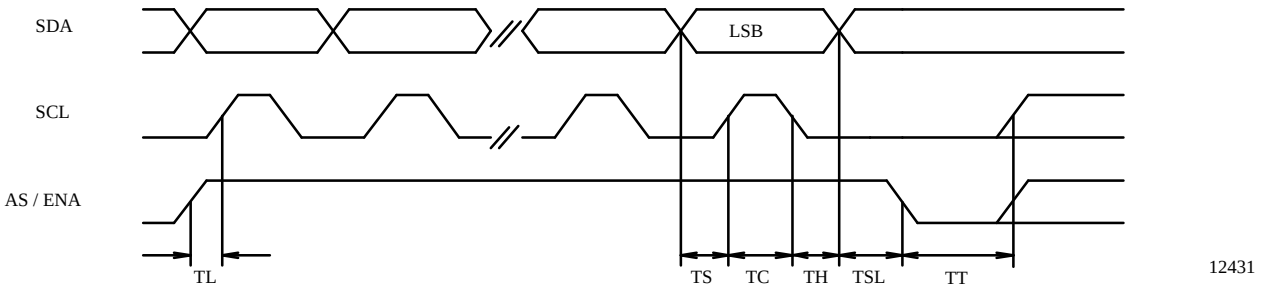


Figure 4.

Parameter	Symbol	Conditions	Min.	Max.	Unit
Setup time	TS		2		µs
Enable hold time	TSL		2		µs
Clock width	TC		2		µs
Enable setup time	TL		10		µs
Enable between two transmissions	TT		10		µs
Data hold time	TH		2		µs

Input/ Output Interface Circuits

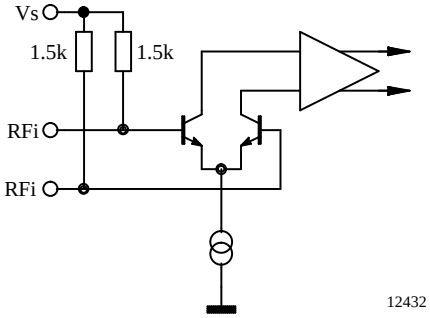


Figure 5. RF Input

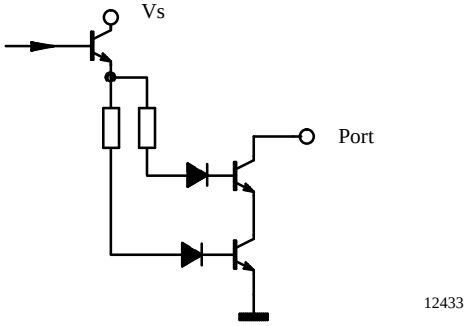


Figure 6. Ports

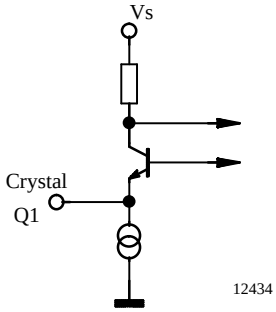


Figure 7. Reference oscillator

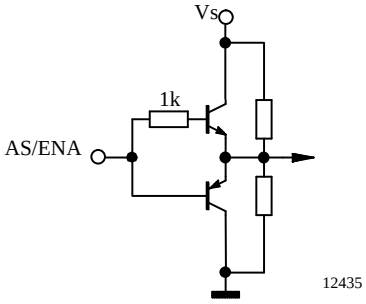


Figure 8. Address select/Enable input

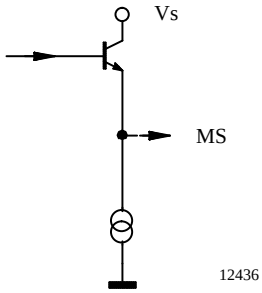


Figure 9. Mixer switch output

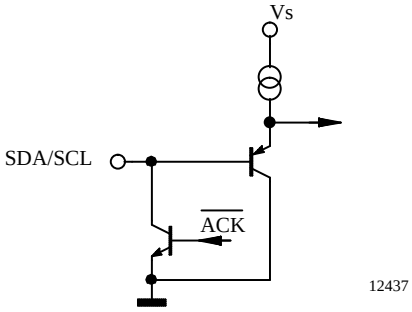


Figure 10. SCL and SDA input

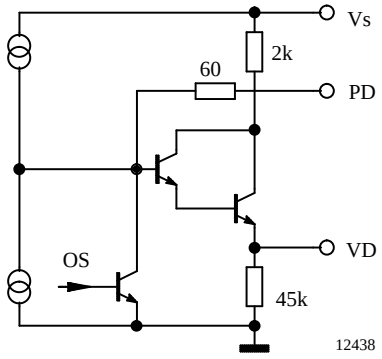


Figure 11. Loop amplifier

Typical Prescaler Input Sensitivity

V_i (mV_{rms} on 50 Ω)

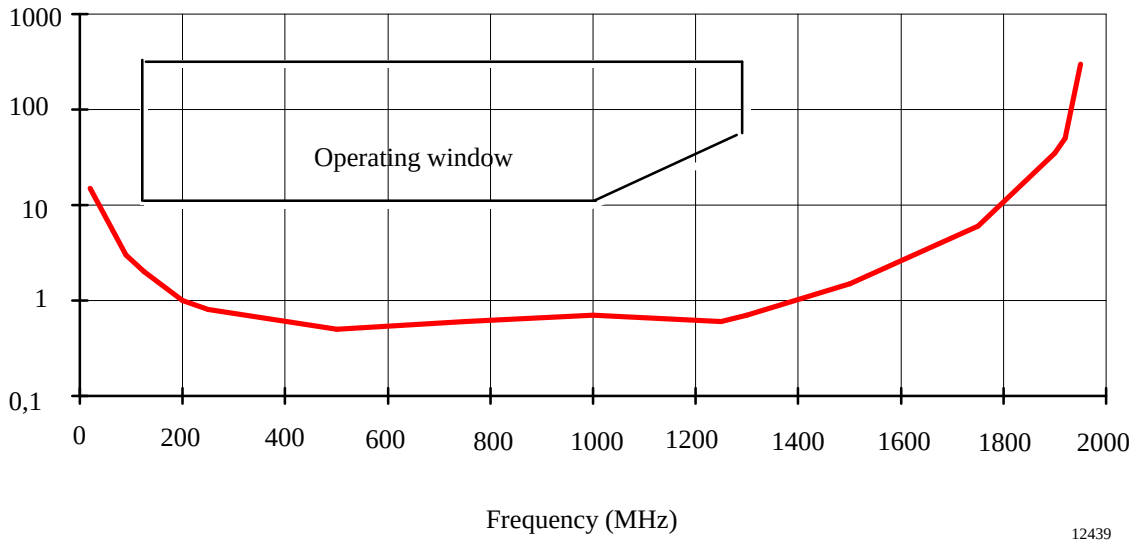


Figure 12.

Typical Input Impedance

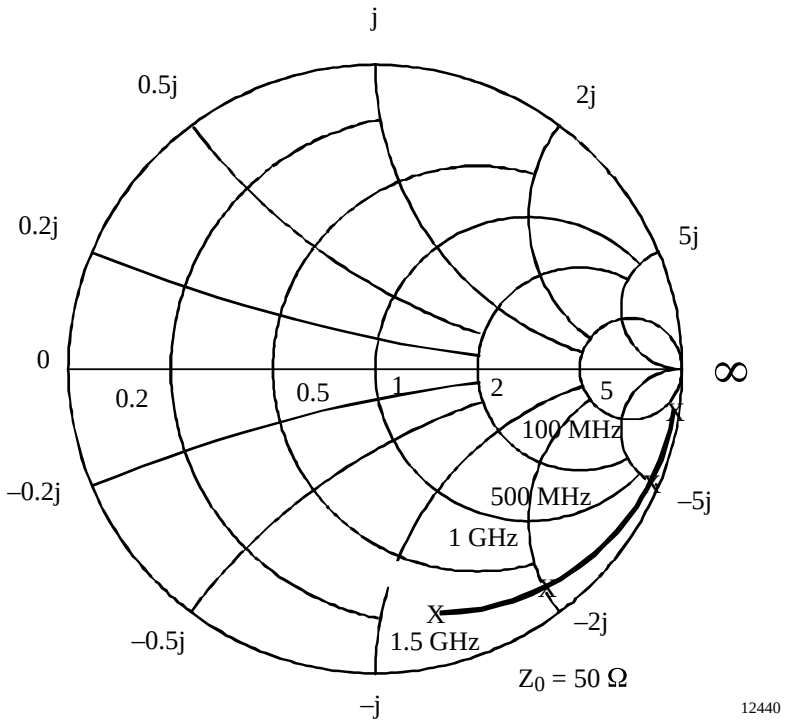


Figure 13.

Application Circuit

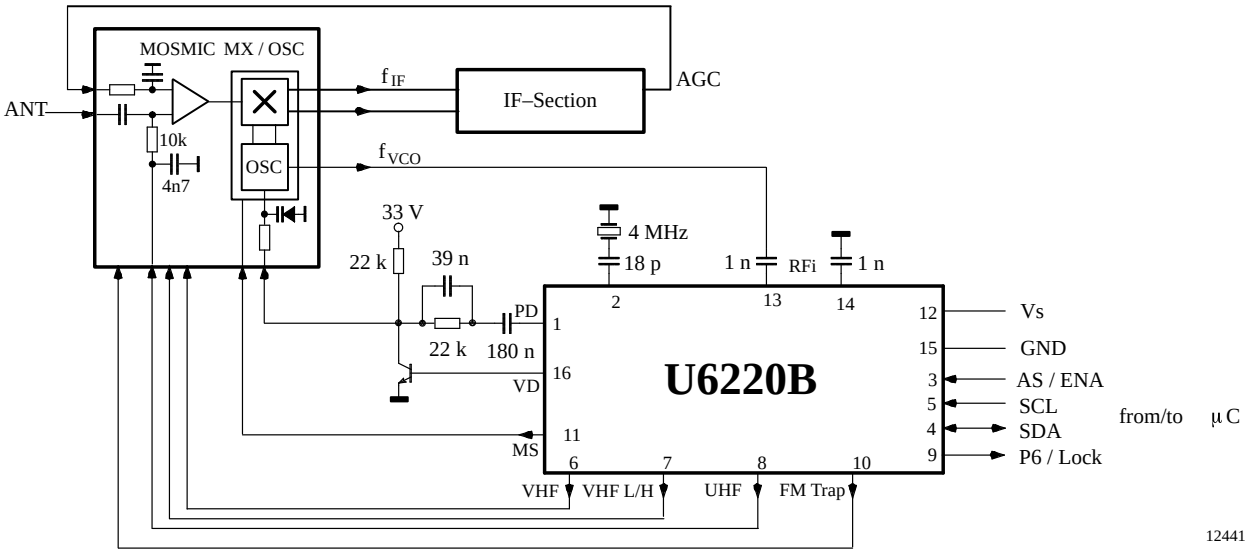
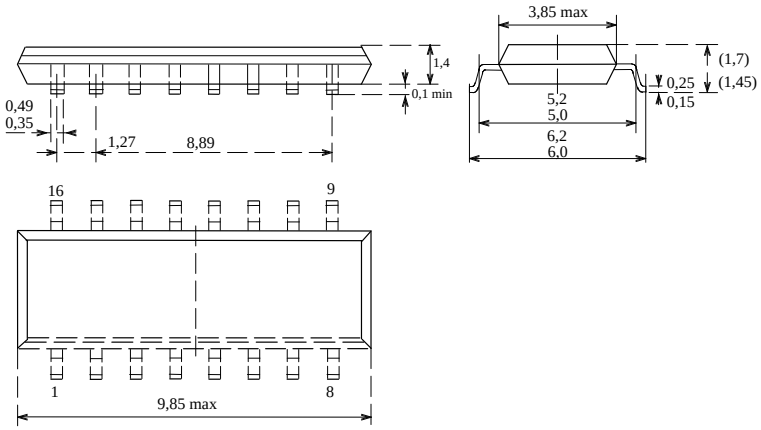


Figure 14.

Package Dimensions

Small outline plastic package, 16 pin-SO16
Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC TELEFUNKEN microelectronic GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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