Test report

Absolute maximum ratings

Parameters	Symbol	Value	Unit	Test no.
Output drain voltage Pin 5, 6, 7, 8	V_{OD}	20	V	84, 85, 86, 87
Analogue supply voltage Pin 16 (with 220 Ω seriell resistance one minute)	V_A V_A	8 to 16 24	V V	24

Electrical characteristics

V_{DD} = 5 V, T_{amb} = 25°C, unless otherwise specified

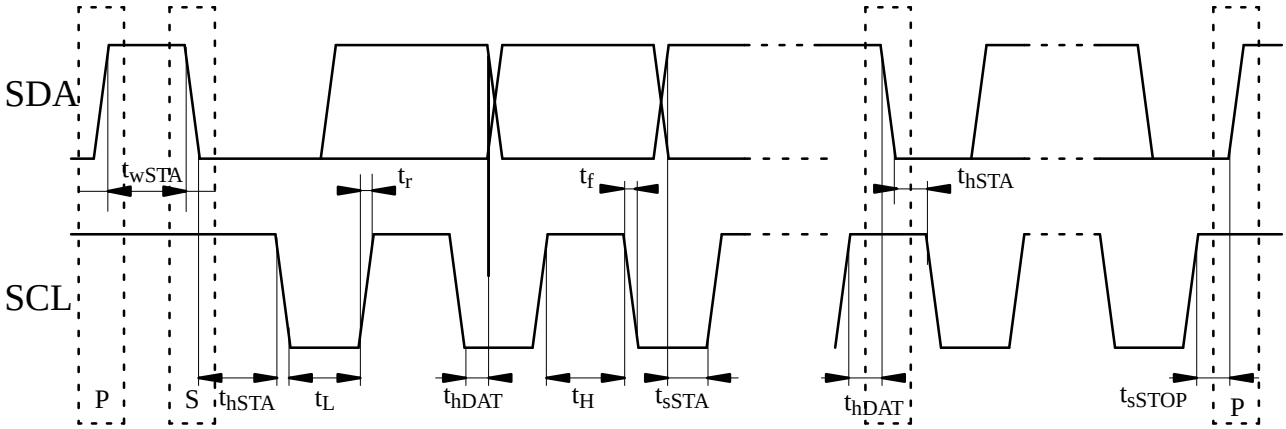
Parameters	Test conditions / Pin	Symbol	Min.	Typ.	Max.	Unit	Test no.
Supply voltage	Pin 1	V_{DD}	4.5	5.0	5.5	V	–
Quiescent supply current	Pin 1	I_{DD}		6.0	11.6	mA	27
FM input sensitivity, FMOSC Pin 9							
f_i = 70 to 120 MHz	R_G = 50 Ω	V_{SFM}	25			mV	168, 169, 170, 171
f_i = 120 to 130 MHz	R_G = 50 Ω	V_{SFM}	50			mV	177
AM input sensitivity,AMOSC Pin 11							
f_i = 0.5 to 35 MHz	R_G = 50 Ω	V_{SAM}	25			mV	150, 151, 152, 153, 154, 155
Oscillator input sensitivity, OSCIN Pin 18							
f_i = 0.1 to 15 MHz	R_G = 50 Ω	V_{SOSC}	100			mV	Digital test: ok or not ok
Switching output SWO 1, SWO 2, SWO 3, SWO 4 (open drain) Pins 5, 6, 7 and 8							
Output voltage LOW LOW Output leakage current HIGH	 I_L = 1 mA I_L = 0.1 mA V5, V6, V7, V8 = 20 V	 V_{SWOL} V_{SWOL} I_{OHL}		 200 20 	 400 100 100	 mV mV nA	 48,49,50,51 52,53,54 84,85,86,87
Phase detector PDFM Pin 13							
Output current 1 Output current 2 Leakage current		$\pm I_{PDFM}$ $\pm I_{PDFM}$	400 100	500 125	600 150 20	µA µA nA	56, 57 58, 59 92
Phase detector PDAM Pin 14							
Output current 1 Output current 2 Leakage current		$\pm I_{PDAM}$ $\pm I_{PDAM}$	75 20	100 25	125 30 20	µA µA nA	88, 89 90, 91 60
Analogue output PDFMO, PDAMO Pins 12 and 15							
Saturation voltage	I = 15 mA	V_{sat}		270	400	mV	46, 83

Electrical characteristics

V_{DD} = 5 V, T_{amb} = 25°C, unless otherwise specified

Parameters	Test conditions / Pin	Symbol	Min.	Typ.	Max.	Unit	Test No.
I^2C bus SCL, SDA, AS							
Input voltage HIGH LOW	Pin 2, 3, 4	V_{iBUS}	 3.0 0		 V_{DD} 1.5	 V V	Digital test: ok or not ok
Output voltage Acknowledge LOW	Pin 3 I_{SDA} = 3 mA	V_O			0.4	V	
Clock frequency	Pin 2	f_{SCL}			100	kHz	
Rise time SDA, SCL	Pin 2, 3	t_r			1	µs	
Fall time SDA, SCL	Pin 2, 3	t_f			300	ns	
Period of SCL HIGH LOW	Pin 2 HIGH LOW	 t_H t_L	 4.0 4.7		 	 µs µs	
Setup time							
Start condition Data Stop condition Time the bus must be free before a new transmission can be started		t_{sSTA} t_{sDAT} t_{sSTOP} t_{wSTA}	4.7 250 4.7 4.7			µs ns µs µs	Digital test: ok or not ok
Hold time							
Start condition DATA		t_{hSTA} t_{hDAT}	4.0 0			µs µs	Digital test: ok or not ok

Bus timing



P = Stop, S = Start

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