DATA SHEET

TEA1114A

Low voltage telephone transmission circuit with dialler interface and regulated strong supply

Product specification
Supersedes data of 1998 Jun 12
File under Integrated Circuits, IC03

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Philips Semiconductors

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Low voltage telephone transmission circuit with dialler interface and regulated strong supply

TEA1114A

FEATURES

- Low DC line voltage; operates down to 1.45 V (excluding voltage drop over external polarity guard)
- Line voltage regulator with adjustable DC voltage
- 3.3 V regulated strong supply point for peripheral circuits compatible with:
  - Speech mode
  - Ringer mode
  - Trickle mode.
- Transmit stage with:
  - Microphone amplifier with symmetrical high impedance inputs
  - DTMF amplifier with confidence tone on receive output.
- Receive stage with:
  - Receive amplifier with asymmetrical output
  - Earpiece amplifier with adjustable gain (and gain boost facility) for all types of earpieces.
- $\overline{\text{MUTE}}$ input for pulse or DTMF dialling
- AGC line loss compensation for microphone and receive amplifiers.

APPLICATIONS

- Line powered telephone sets with LCD module
- Cordless telephones
- Fax machines
- Answering machines.

GENERAL DESCRIPTION

The TEA1114A is a bipolar integrated circuit that performs all speech and line interface functions required in fully electronic telephone sets. It performs electronic switching between speech and dialling. The IC operates at a line voltage down to 1.45 V DC (with reduced performance) to facilitate the use of telephone sets connected in parallel.

When the line current is high enough, a fixed amount of current is derived from the LN pin in order to create a strong supply point at pin V_{DD}. The voltage at pin V_{DD} is regulated to 3.3 V to supply peripherals such as dialler, LCD module and microcontroller.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1114A	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
TEA1114AT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

QUICK REFERENCE DATA

I_{line} = 15 mA; V_{EE} = 0 V; R_{SLPE} = 20 Ω; AGC pin connected to V_{EE}; Z_{line} = 600 Ω; f = 1 kHz; measured according to test circuits given in Figs 14, 15 and 16; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{line}	line current operating range	normal operation	11	–	140	mA
		with reduced performance	1	–	11	mA
V_{LN}	DC line voltage		4.05	4.35	4.65	V
I_{CC}	internal current consumption	V_{CC} = 3.7 V	–	1.25	1.5	mA
V_{CC}	supply voltage for internal circuitry (unregulated)	I_P = 0 mA	–	3.6	–	V
V_{DD}	regulated supply voltage for peripherals					
	speech mode	I_{DD} = −3 mA	3.0	3.3	3.6	V
	ringer mode	I_{DD} = 75 mA	3.0	3.3	3.6	V
I_{DD}	available supply current for peripherals		–	–	−3	mA
$G_{v(TX)}$	typical voltage gain for microphone amplifier	V_{MIC} = 4 mV (RMS)	43.2	44.2	45.2	dB
$G_{v(RX)}$	typical voltage gain for receiving amplifier	V_{IR} = 4 mV (RMS)	32.4	33.4	34.4	dB
$\Delta G_{v(QR)}$	gain setting range for earpiece amplifier	R_{E1} = 100 kΩ	−14	–	+12	dB
$\Delta G_{v(trx)}$	gain control range for microphone and receive amplifiers with respect to I_{line} = 15 mA	I_{line} = 85 mA	–	6.0	–	dB
$\Delta G_{v(trx)(m)}$	gain reduction for microphone and receive amplifiers	$\overline{MUTE}$ = LOW	–	80	–	dB

BLOCK DIAGRAM

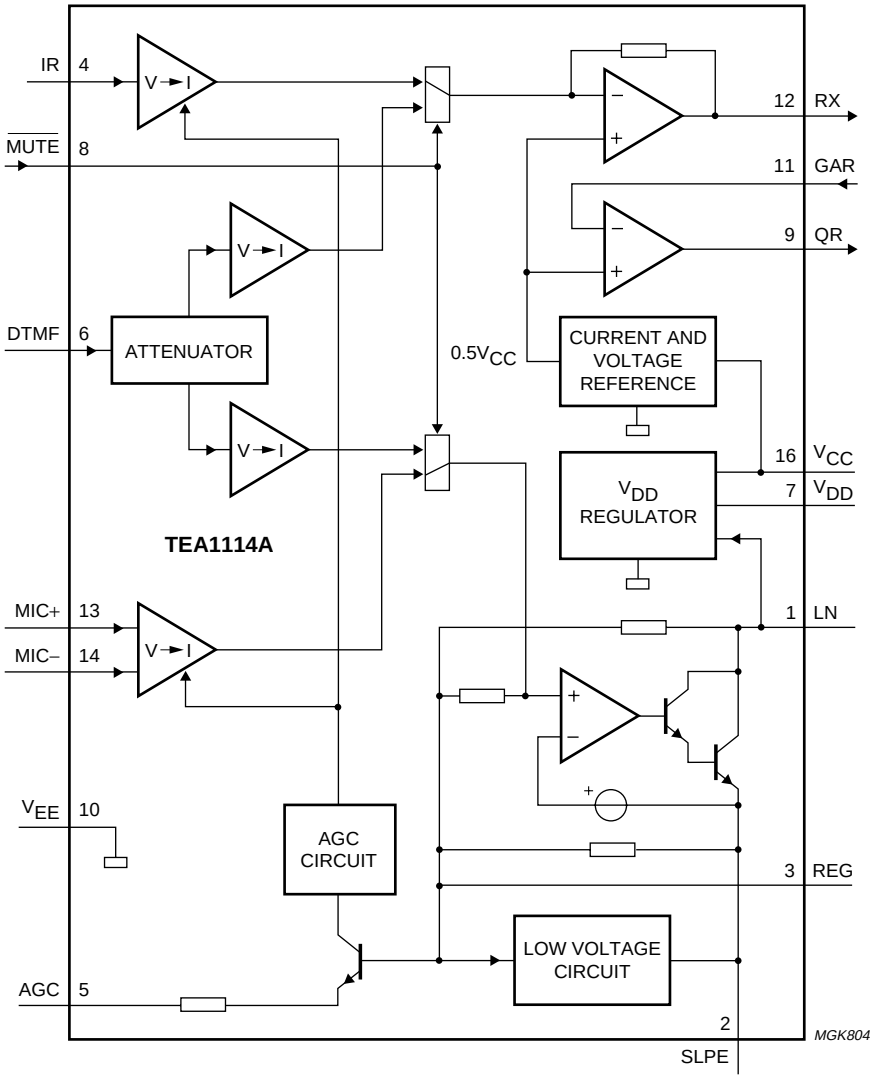


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LN	1	positive line terminal
SLPE	2	slope (DC resistance) adjustment
REG	3	line voltage regulator decoupling
IR	4	receive amplifier input
AGC	5	automatic gain control/ line loss compensation
DTMF	6	dual-tone multi-frequency input
V_{DD}	7	regulated supply for peripherals
$\overline{MUTE}$	8	mute input to select speech or dialling mode (active LOW)
QR	9	earpiece amplifier output
V_{EE}	10	negative line terminal
GAR	11	earpiece amplifier inverting input
RX	12	receive amplifier output
MIC+	13	non-inverting microphone amplifier input
MIC–	14	inverting microphone amplifier input
n.c.	15	not connected
V_{CC}	16	supply voltage for internal circuit

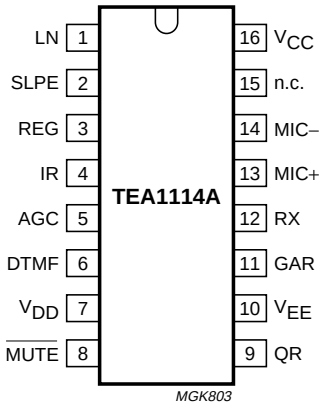


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

All data given in this chapter are typical values, except when otherwise specified.

Supply (pins LN, SLPE, REG, V_{CC} and V_{DD})

The supply for the TEA1114A and its peripherals is obtained from the telephone line (see Fig.3).

THE LINE INTERFACE (PINS LN, SLPE AND REG)

The IC generates a stabilized reference voltage (V_{ref}) between pins LN and SLPE. V_{ref} is temperature compensated and can be adjusted by means of an external resistor (R_{VA}). V_{ref} equals 4.15 V and can be increased by connecting R_{VA} between pins REG and SLPE or decreased by connecting R_{VA} between pins REG and LN. The voltage at pin REG is used by the internal regulator to generate V_{ref} and is decoupled by C_{REG}, which is connected to V_{EE}.
This capacitor, converted into an equivalent inductance (see Section “Set impedance”) realizes the set impedance conversion from its DC value (R_{SLPE}) to its AC value (R_{CC} in the audio-frequency range). The voltage at pin SLPE is proportional to the line current.

The voltage at pin LN is:

$$V_{LN} = V_{ref} + R_{SLPE} \times I_{SLPE}$$

$$I_{SLPE} = I_{line} - I_{CC} - I_P - I_{SUP}$$

where:

I_{line} = line current

I_{CC} = current consumption of the IC

I_P = supply current for external circuits

I_{SUP} = current consumed between LN and V_{EE} by the V_{DD} regulator.

The preferred value for R_{SLPE} is 20 Ω. Changing R_{SLPE} will affect more than the DC characteristics; it also influences the microphone and DTMF gains, the gain control characteristics, the sidetone level and the maximum output swing on the line.

The DC line current flowing into the set is determined by the exchange supply voltage (V_{EXCH}), the feeding bridge resistance (R_{EXCH}), the DC resistance of the telephone line (R_{line}) and the reference voltage (V_{ref}). With line currents below 9 mA, the internal reference voltage (generating V_{ref}) is automatically adjusted to a lower value. This means that more sets can operate in parallel with DC line voltages (excluding the polarity guard) down to an absolute minimum voltage of 1.45 V. At currents below 9 mA, the circuit has limited sending and receiving levels. This is called the low voltage area.

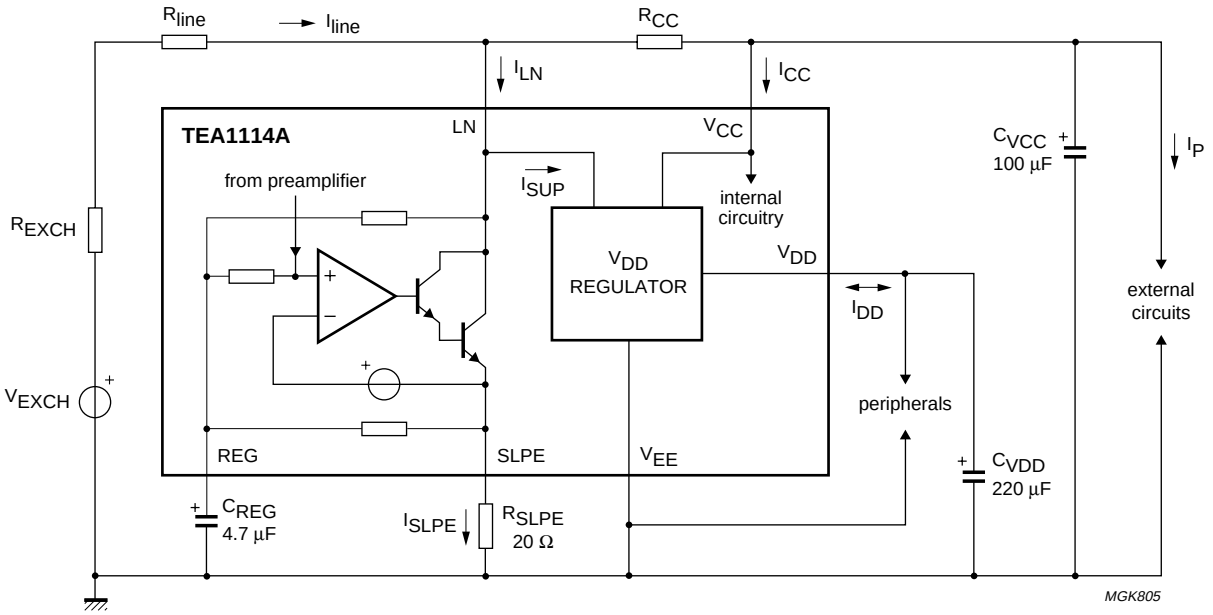


Fig.3 Supply configuration.

THE INTERNAL SUPPLY POINT (PIN V_{CC})

The internal circuitry of the TEA1114A is supplied from pin V_{CC}. This voltage supply is derived from the line voltage by means of a resistor (R_{CC}) and must be decoupled by a capacitor C_{VCC}. It may also be used to supply some external circuits. The V_{CC} voltage depends on the current consumed by the IC and the peripheral circuits as: $V_{CC0} = V_{LN} - R_{CC} \times I_{CC}$

$$V_{CC} = V_{CC0} - R_{CC} \times (I_P + I_{rec})$$

(see also Figs 4 and 5). I_{rec} is the current consumed by the output stage of the earpiece amplifier.

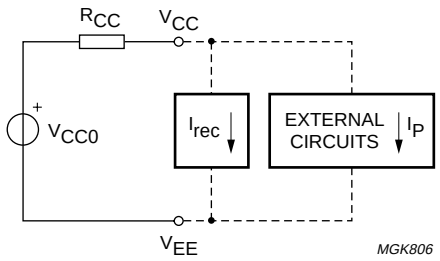
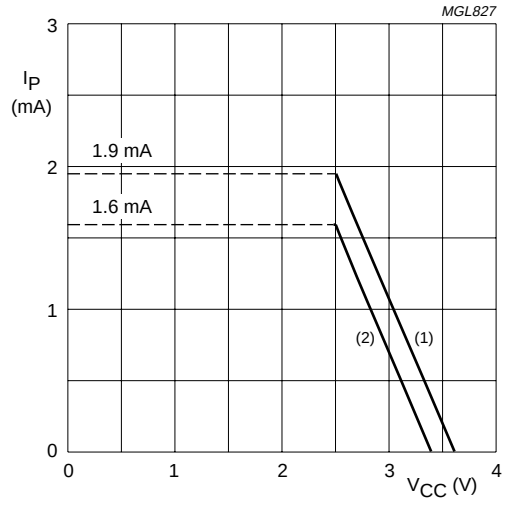


Fig.4 V_{CC} used as supply voltage for external circuits.



$V_{CC} \geq 2.5$ V; $V_{LN} = 4.35$ V at $I_{line} = 15$ mA; $R_{CC} = 619\ \Omega$; $R_{SLPE} = 20\ \Omega$.

Curve (1) is valid when the receiving amplifier is driven: $V_{QR(rms)} = 150$ mV; $R_{L1} = 150\ \Omega$.

Curve (2) is valid when the receiving amplifier is not driven.

Fig.5 Typical current I_P available from V_{CC} for peripheral circuitry.

THE REGULATED SUPPLY POINT (PIN V_{DD})

The V_{DD} regulator delivers a stabilized voltage for the peripherals in transmission mode (nominal V_{LN}) as well as in ringer mode ($V_{LN} = 0$ V). The regulator (see Fig.6) consists of a sense input circuit, a current switch and a V_{DD} output stabilizer. The regulator operates as a current source at the LN input in transmission mode; it takes a constant current of 4.3 mA (at nominal conditions) from pin LN. The current switch reduces the distortion on the line at large signal swings. Output V_{DD} follows the DC voltage at pin LN (with typically 0.35 V difference) up to $V_{DD} = 3.3$ V. The input current of the regulator is constant while the output (source) current is determined by the consumption of the peripherals. The difference between input and output current is shunted by the internal V_{DD} stabilizer.

In ringer mode, the stabilizer operates as a shunt stabilizer to keep V_{DD} at 3.3 V. In this mode, the input voltage $V_{LN} = 0$ V while the input current into pin V_{DD} is delivered by the ringing signal. V_{DD} has to be decoupled by a capacitor C_{VDD}.

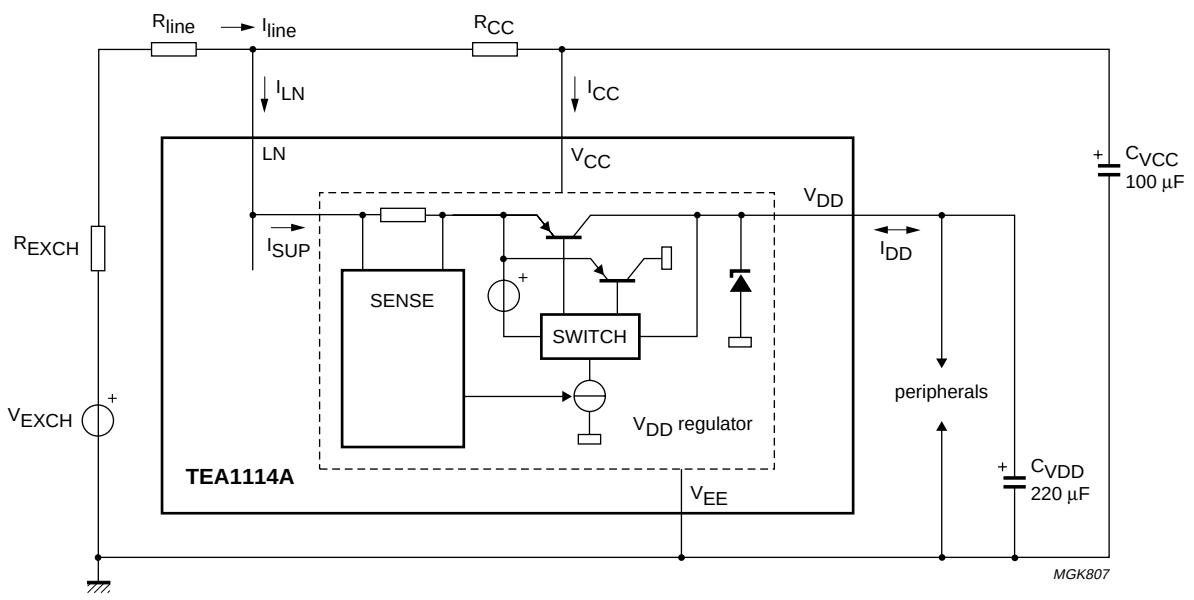
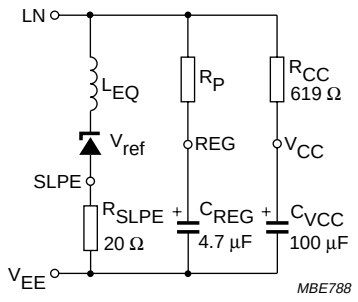


Fig.6 V_{DD} regulator configuration.

Set impedance

In the audio frequency range, the dynamic impedance is mainly determined by the R_{CC} resistor. The equivalent impedance of the circuit is illustrated in Fig.7.



$L_{EQ} = C_{REG} \times R_{SLPE} \times R_P$.
R_P = internal resistance.
R_P = 17.5 kΩ.

Fig.7 Equivalent impedance between LN and V_{EE}.

Transmit stage (pins MIC+, MIC− and DTMF)

MICROPHONE AMPLIFIER (PINS MIC+ AND MIC–)

The TEA1114A has symmetrical microphone inputs. The input impedance between pins MIC+ and MIC– is 64 kΩ (2 × 32 kΩ). The voltage gain from pins MIC+/MIC– to pin LN is set at 44.2 dB (typically).

Automatic gain control is provided on this amplifier for line loss compensation.

DTMF AMPLIFIER (PIN DTMF)

When the DTMF amplifier is enabled, dialling tones may be sent on line. These tones are also sent to the receive output RX at a low level (confidence tone).

The TEA1114A has an asymmetrical DTMF input. The input impedance between DTMF and V_{EE} is 20 kΩ. The voltage gain from pin DTMF to pin LN is set at 26 dB.

Automatic gain control has no effect on the DTMF amplifier.

Receiving stage (pins IR, RX, GAR and QR)

The receive part consists of a receive amplifier and an earpiece amplifier.

THE RECEIVE AMPLIFIER (PINS IR AND RX)

The receive amplifier transfers the receive signal from input IR to output RX. The input impedance of the receive amplifier, between pins IR and V_{EE}, is 20 kΩ. The voltage gain from pin IR to RX is set at 33.4 dB. RX output is intended to drive high ohmic (real) loads. Automatic gain control is provided on the receive amplifier.

THE EARPIECE AMPLIFIER (PINS GAR AND QR)

The earpiece amplifier is an operational amplifier having its output (QR) and inverting input (GAR) available. It can be used in conjunction with two resistors to get some extra gain or attenuation.

In an usual configuration (see Fig.8), output RX drives the earpiece amplifier by means of R_{E1} connected between RX and GAR. Feedback resistor R_{E2} of the earpiece amplifier is connected between QR and GAR. Output QR drives the earpiece.

The gain of the earpiece amplifier (from RX to QR) can be set between +12 and –14 dB by means of resistor R_{E2}.

The preferred value of R_{E1} is 100 kΩ.

The earpiece amplifier offers a gain boost facility relative to the initial gain. Resistor R_{E2} has to be replaced by the network of R_{E21}, R_{E22} and R_{E23} as shown in Fig.8.

The initial gain is defined by: $-\frac{R_{E21} + R_{E22}}{R_{E1}}$

which corresponds to $R_{E23} = \infty$. The gain boost is realized by a defined value of R_{E23} and is:

$$-\frac{R_{E21} + R_{E22}}{R_{E1}} \times \left(1 + \frac{R_{E21} \;//\; R_{E22}}{R_{E23}}\right)$$

Two external capacitors C_{GAR} (connected between GAR and QR) and C_{GARS} (connected between GAR and V_{EE}) ensure stability. The C_{GAR} capacitor provides a first-order low-pass filter. The cut-off frequency corresponds to the time constant $C_{GAR} \times R_{E2}$.
The relationship $C_{GARS} = 10 \times C_{GAR}$ must be fulfilled to ensure stability.

The output voltages of both amplifiers are specified for continuous wave drive. The maximum output swing depends on the DC line voltage V_{LN}, the R_{CC} resistor, the I_{CC} current consumption of the circuit, the I_P current consumption of the peripheral circuits and the load impedance.

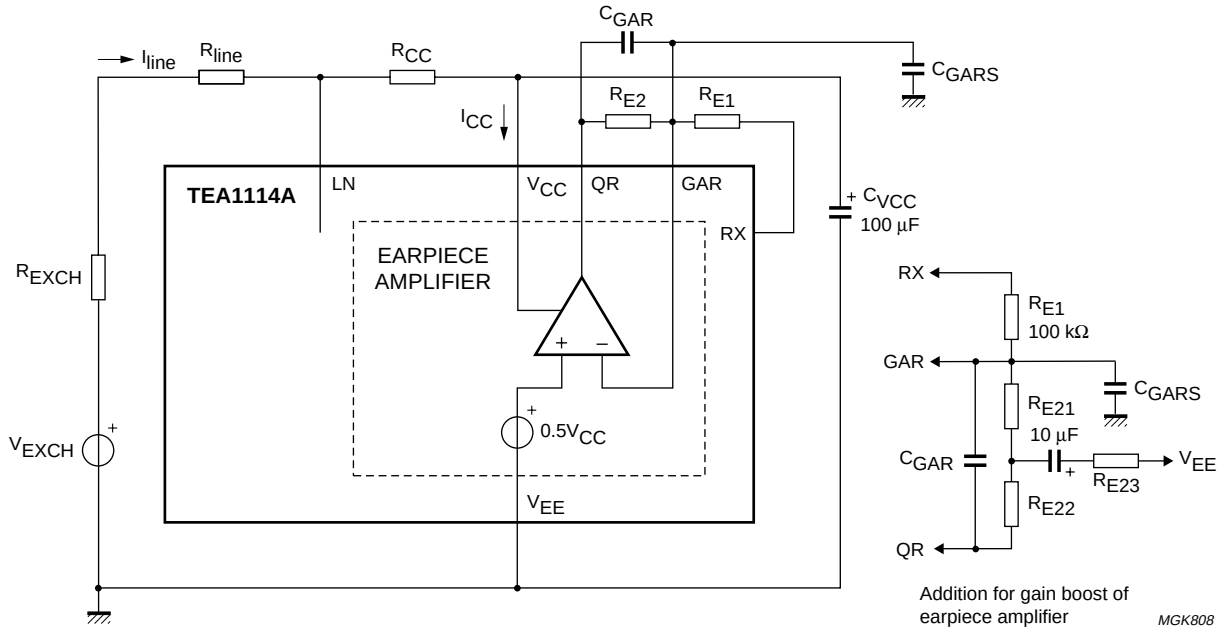


Fig.8 Earpiece amplifier configuration.

Automatic gain control (pin AGC)

The TEA1114A performs automatic line loss compensation. The automatic gain control varies the gain of the microphone amplifier and the gain of the receive amplifier in accordance with the DC line current.

The control range is 6.0 dB (which corresponds approximately to a line length of 5 km for a 0.5 mm diameter twisted-pair copper cable with a DC resistance of 176 Ω/km and an average attenuation of 1.2 dB/km).

The IC can be used with different configurations of feeding bridge (supply voltage and bridge resistance) by connecting an external resistor R_{AGC} between pins AGC and V_{EE}. This resistor enables the I_{start} and I_{stop} line currents to be increased (the ratio between I_{start} and I_{stop} is not affected by the resistor). The AGC function is disabled when pin AGC is left open-circuit.

Mute function (pin $\overline{\text{MUTE}}$)

The mute function performs the switching between the speech mode and the dialling mode.

When $\overline{\text{MUTE}}$ is LOW, the DTMF input is enabled and the microphone and receive amplifier inputs are disabled. In this mode, the DTMF tones are sent to the receive output at a low level (confidence tone).

When $\overline{\text{MUTE}}$ is HIGH, the microphone and receiving amplifiers inputs are enabled while the DTMF input is disabled. The $\overline{\text{MUTE}}$ input is provided with an internal pull-up current source to V_{CC}.

Sidetone suppression

The TEA1114A anti-sidetone network comprising R_{CC} // Z_{line}, R_{ast1}, R_{ast2}, R_{ast3}, R_{SLPE} and Z_{bal} (see Fig.9) suppresses the transmitted signal in the earpiece. Maximum compensation is obtained when the following conditions are fulfilled:

$$R_{SLPE} \times R_{ast1} = R_{CC} \times (R_{ast2} + R_{ast3})$$

$$k = \frac{R_{ast2} \times (R_{ast3} + R_{SLPE})}{R_{ast1} \times R_{SLPE}}$$

$$Z_{bal} = k \times Z_{line}$$

The scale factor k is chosen to meet the compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}.

In practice, Z_{line} varies considerably with the line type and the line length. Therefore, the value of Z_{bal} should be for an average line length which gives satisfactory sidetone suppression with short and long lines. The suppression also depends on the accuracy of the match between Z_{bal} and the impedance of the average line.

The anti-sidetone network for the TEA1114A attenuates the receiving signal from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio frequency range.

A Wheatstone bridge configuration (see Fig.10) may also be used.

More information on the balancing of an anti-sidetone bridge can be obtained in our publication *"Semiconductors for Wired Telecom Systems; Application Handbook, IC03b"*. For ordering information please contact the Philips Semiconductors sales office.

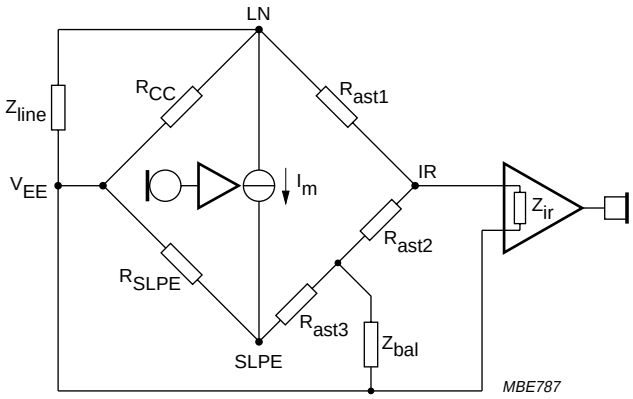


Fig.9 Equivalent circuit of TEA1114A anti-sidetone bridge.

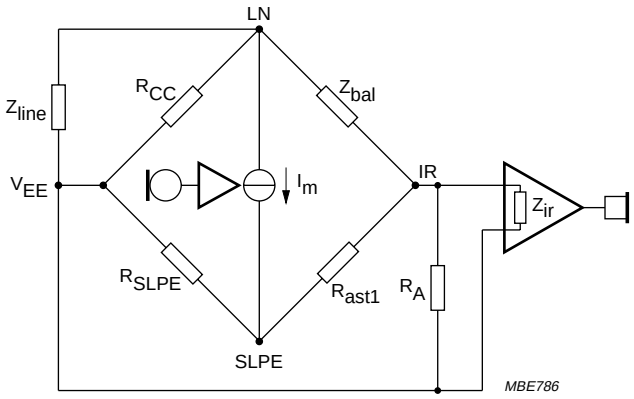


Fig.10 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

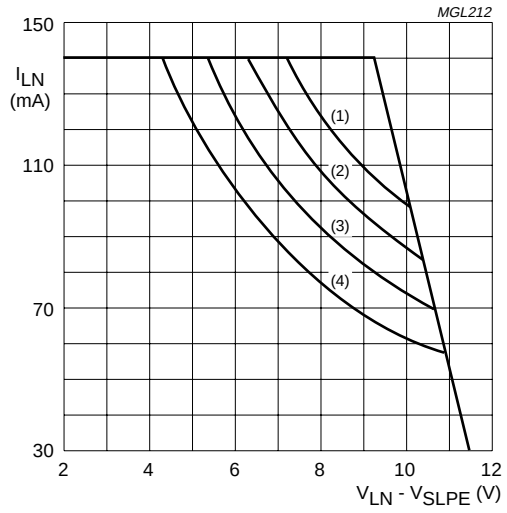
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive continuous line voltage		V_{EE} − 0.4	12	V
	repetitive line voltage during switch-on or line interruption		V_{EE} − 0.4	13.2	V
I_{DD}	maximum input current at pin V_{DD}		–	75	mA
$V_{n(max)}$	maximum voltage on all pins except pin V_{DD}		V_{EE} − 0.4	V_{CC} + 0.4	V
I_{line}	line current	R_{SLPE} = 20 Ω; see Figs 11 and 12	–	140	mA
P_{tot}	total power dissipation	T_{amb} = 75 °C; see Figs 11 and 12			
	TEA1114A		–	625	mW
	TEA1114AT		–	416	mW
T_{stg}	storage temperature		−40	+125	°C
T_{amb}	ambient temperature		−25	+75	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; note 1		
	TEA1114A		70	K/W
	TEA1114AT		115	K/W

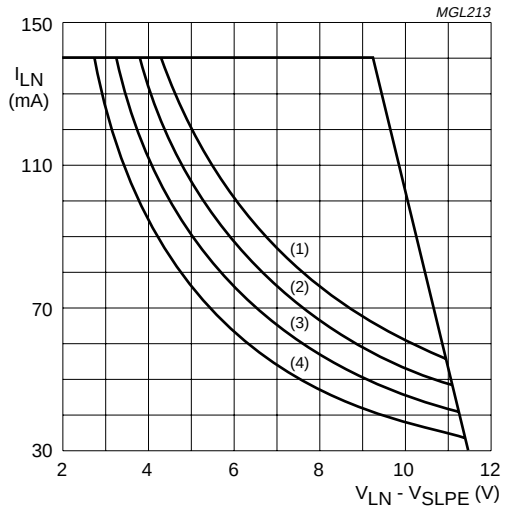
Note

1. Mounted on epoxy board 40.1 × 19.1 × 1.5 mm.



(1) T_{amb} = 45 °C; P_{tot} = 1.000 W.
(2) T_{amb} = 55 °C; P_{tot} = 0.875 W.
(3) T_{amb} = 65 °C; P_{tot} = 0.750 W.
(4) T_{amb} = 75 °C; P_{tot} = 0.625 W.

Fig.11 DIP16 safe operating area (TEA1114A).



(1) T_{amb} = 45 °C; P_{tot} = 0.666 W.
(2) T_{amb} = 55 °C; P_{tot} = 0.583 W.
(3) T_{amb} = 65 °C; P_{tot} = 0.500 W.
(4) T_{amb} = 75 °C; P_{tot} = 0.416 W.

Fig.12 SO16 safe operating area (TEA1114AT).

CHARACTERISTICS

I_{line} = 15 mA; V_{EE} = 0 V; R_{SLPE} = 20 Ω; pin AGC connected to V_{EE}; Z_{line} = 600 Ω; f = 1 kHz; measured according to test circuits given in Figs 14, 15 and 16; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pins V_{LN}, V_{CC}, SLPE, REG and V_{DD})						
THE LINE INTERFACE (PINS LN, SLPE AND REG)						
V_{ref}	stabilized reference voltage between pins LN and SLPE		3.9	4.15	4.4	V
V_{LN}	DC line voltage	I_{line} = 1 mA	–	1.45	–	V
		I_{line} = 4 mA	–	2	–	V
		I_{line} = 15 mA	4.05	4.35	4.65	V
		I_{line} = 140 mA	–	7.1	7.55	V
$V_{LN(Rext)}$	DC line voltage with an external resistor R_{VA}	R_{VA} = 44.2 kΩ (between pins LN and REG)	–	3.6	–	V
$\Delta V_{LN(T)}$	DC line voltage variation with temperature referred to 25 °C	T_{amb} = –25 to +75 °C	–	±40	–	mV
THE INTERNAL SUPPLY POINT (PIN V_{CC})						
I_{CC}	internal current consumption	V_{CC} = 3.6 V	–	1.25	1.5	mA
V_{CC}	supply voltage for internal circuitry	I_P = 0 mA	–	3.6	–	V
THE REGULATED SUPPLY POINT (PIN V_{DD})						
I_{SUP}	input current of the V_{DD} regulator (current from pin LN not flowing through pin SLPE)	I_{line} = 1 mA	–	0	–	mA
		I_{line} = 4 mA	–	2.15	–	mA
		I_{line} ≥ 11 mA	–	4.3	–	mA
V_{DD}	regulated supply voltage in:					
	speech mode	I_{DD} = –3 mA; V_{LN} > 3.6 + 0.25 V (typ.); I_{line} ≥ 11 mA	3.0	3.3	3.6	V
	speech mode at reduced performance	I_{line} = 4 mA	–	V_{LN} – 0.35	–	V
	ringer mode	I_{line} = 0 mA; I_{DD} = 75 mA	3.0	3.3	3.6	V
I_{DD}	regulated supply current available in:					
	speech mode	I_{line} ≥ 11 mA	–	–	–3	mA
	speech mode at reduced performance	I_{line} = 4 mA	–	–0.5	–	mA
	trickle mode	I_{line} = 0 mA; V_{CC} discharging; V_{DD} = 1.2 V	–	–	100	nA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transmit stage (pins MIC+, MIC− and DTMF)						
MICROPHONE AMPLIFIER (PINS MIC+ AND MIC−)						
$\|Z_i\|$	input impedance					
	differential between pins MIC+ and MIC−		–	64	–	kΩ
	single-ended between pins MIC+/MIC− and V_{EE}		–	32	–	kΩ
$G_{v(TX)}$	voltage gain from pins MIC+/MIC− to pin LN	V_{MIC} = 4 mV (RMS)	43.2	44.2	45.2	dB
$\Delta G_{v(TX)(f)}$	voltage gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{v(TX)(T)}$	voltage gain variation with temperature referred to 25 °C	T_{amb} = −25 to +75 °C	–	±0.3	–	dB
CMRR	common mode rejection ratio		–	80	–	dB
$V_{LN(max)(rms)}$	maximum sending signal (RMS value)	I_{line} = 15 mA; THD = 2%	1.8	2.15	–	V
		I_{line} = 4 mA; THD = 10%	–	0.35	–	V
$V_{no(LN)}$	noise output voltage at pin LN	psophometrically weighted (P53 curve); pins MIC+/ MIC− shorted through 200 Ω	–	−78	–	dBmp
DTMF AMPLIFIER (PIN DTMF)						
$\|Z_i\|$	input impedance		–	20	–	kΩ
$G_{v(DTMF)}$	voltage gain from pin DTMF to pin LN	V_{DTMF} = 20 mV (RMS); $\overline{MUTE}$ = LOW	25	26	27	dB
$\Delta G_{v(DTMF)(f)}$	voltage gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{v(DTMF)(T)}$	voltage gain variation with temperature referred to 25 °C	T_{amb} = −25 to +75 °C	–	±0.4	–	dB
$G_{v(ct)}$	voltage gain from pin DTMF to pin RX (confidence tone)	V_{DTMF} = 20 mV (RMS); R_{L2} = 10 kΩ; $\overline{MUTE}$ = LOW	–	−9.2	–	dB
Receiving stage (pins IR, RX, GAR and QR)						
THE RECEIVE AMPLIFIER (PINS IR AND RX)						
$\|Z_i\|$	input impedance		–	20	–	kΩ
$G_{v(RX)}$	voltage gain from pin IR to pin RX	V_{IR} = 4 mV (RMS)	32.4	33.4	34.4	dB
$\Delta G_{v(RX)(f)}$	voltage gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{v(RX)(T)}$	voltage gain variation with temperature referred to 25 °C	T_{amb} = −25 to +75 °C	–	±0.3	–	dB
$V_{RX(max)(rms)}$	maximum receiving signal on pin RX (RMS value)	I_P = 0 mA; sine wave drive; R_{L2} = 10 kΩ; THD = 2%	0.4	–	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert I_{RX(max)} \rvert$	maximum source and sink current on pin RX (peak value)	I_P = 0 mA; sine wave drive	50	–	–	µA
$V_{no(RX)(rms)}$	noise output voltage at pin RX (RMS value)	pin IR open-circuit; R_{L2} = 10 kΩ; psophometrically weighted (P53 curve)	–	–86	–	dBVp
THE EARPIECE AMPLIFIER (PINS GAR AND QR)						
$G_{v(QR)}$	voltage gain from pin RX to pin QR	V_{IR} = 4 mV (RMS); $R_{E1} = R_{E2}$ = 100 kΩ	–	0	–	dB
$\Delta G_{v(QR)}$	voltage gain setting	R_{E1} = 100 kΩ	–14	–	+12	dB
$V_{QR(max)(rms)}$	maximum receiving signal on pin QR (RMS value)	I_P = 0 mA; sine wave drive; R_{L1} = 150 Ω; THD = 2%	0.3	0.38	–	V
		I_P = 0 mA; sine wave drive; R_{L1} = 450 Ω; THD = 2%	0.46	0.56	–	V
$V_{no(QR)(rms)}$	noise output voltage at pin QR (RMS value)	IR open-circuit; R_{L1} = 150 Ω; $R_{E1} = R_{E2}$ = 100 kΩ psophometrically weighted (P53 curve)	–	–86	–	dBVp
		R_{E1} = 100 kΩ; R_{E2} = 25 kΩ	–	–98	–	dBVp
Automatic gain control (pin AGC)						
$\Delta G_{v(trx)}$	voltage gain control range for microphone and receive amplifiers with respect to I_{line} = 20 mA	I_{line} = 85 mA	–	6.0	–	dB
I_{start}	highest line current for maximum gain		–	23	–	mA
I_{stop}	lowest line current for minimum gain		–	59	–	mA
Mute function (pin $\overline{\text{MUTE}}$)						
V_{IL}	LOW-level input voltage		V_{EE} – 0.4	–	V_{EE} + 0.3	V
V_{IH}	HIGH-level input voltage		V_{EE} + 1.5	–	V_{CC} + 0.4	V
I_{MUTE}	input current		–	2	10	µA
$\Delta G_{v(trx)(m)}$	voltage gain reduction for:					
	microphone amplifier	$\overline{\text{MUTE}}$ = LOW	–	80	–	dB
	receive amplifier	$\overline{\text{MUTE}}$ = LOW	–	80	–	dB
	earpiece amplifier	$\overline{\text{MUTE}}$ = LOW	–	80	–	dB
	DTMF amplifier	$\overline{\text{MUTE}}$ = HIGH	–	80	–	dB

TEST AND APPLICATION INFORMATION

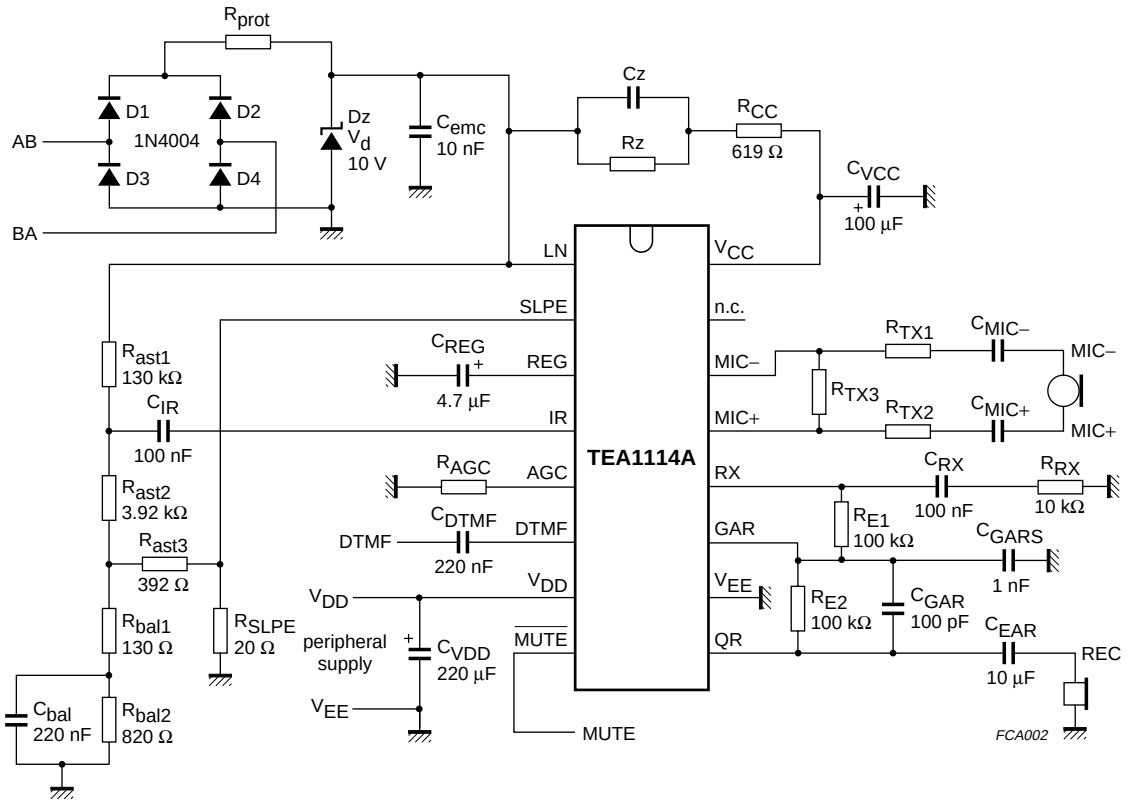
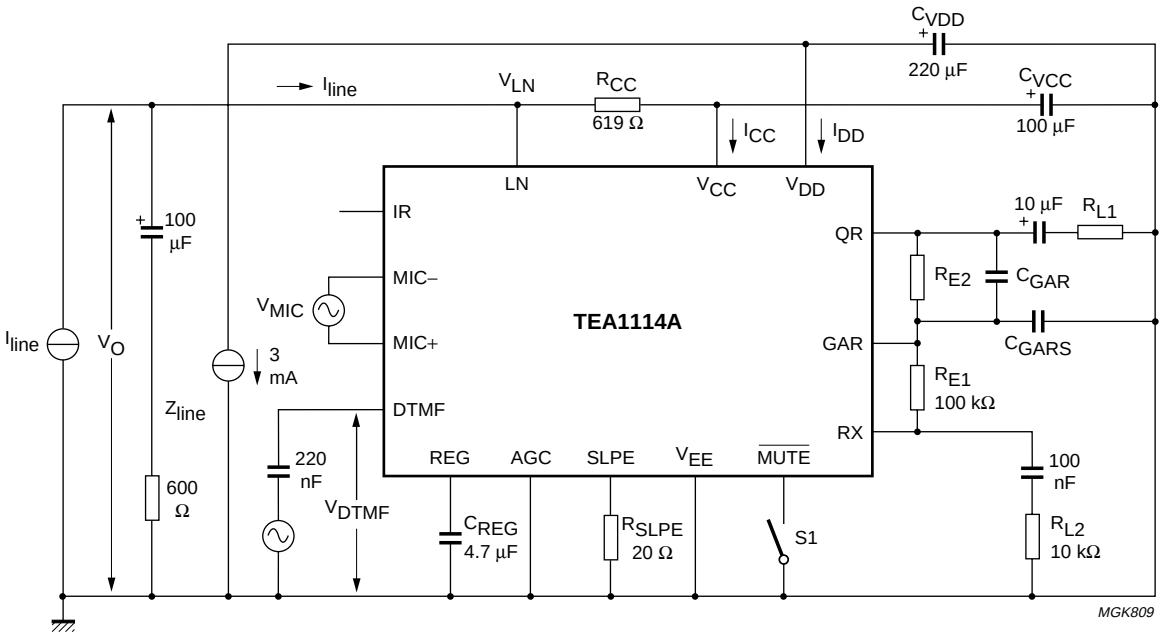


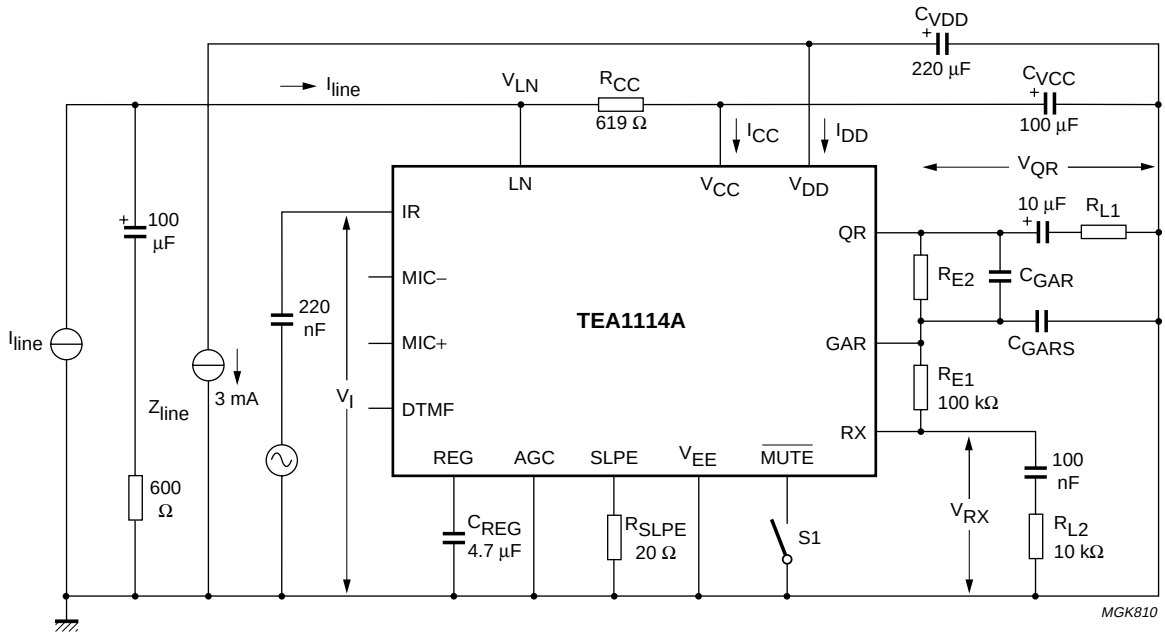
Fig.13 Basic application of the TEA1114A IC.



Voltage gain defined as $G_v = 20 \log \left|\frac{V_O}{V_I}\right|$; $V_I = V_{MIC}$ or V_{DTMF}.

Microphone gain: S1 = open.
DTMF gain and confidence tone: S1 = closed.
Inputs not being tested should be open-circuit.

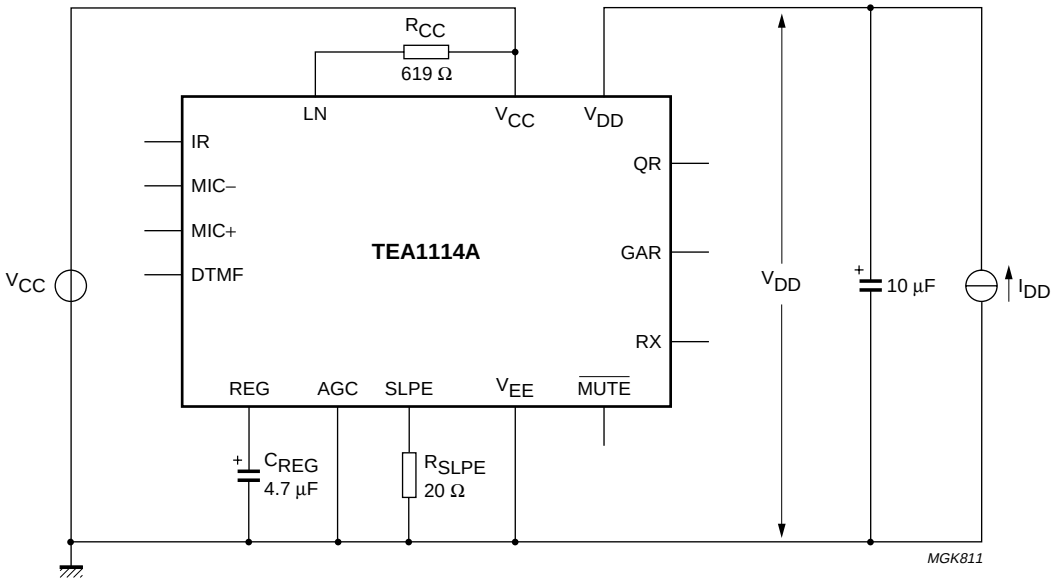
Fig.14 Test figure for defining transmit gains.



Receive and earpiece gains: S1 = open.
Inputs not being tested should be open-circuit.

Voltage gain defined as $G_v = 20 \log \left|\frac{V_O}{V_I}\right|$; $V_O = V_{QR}$ or V_{RX}.

Fig.15 Test figure for defining receive gains.

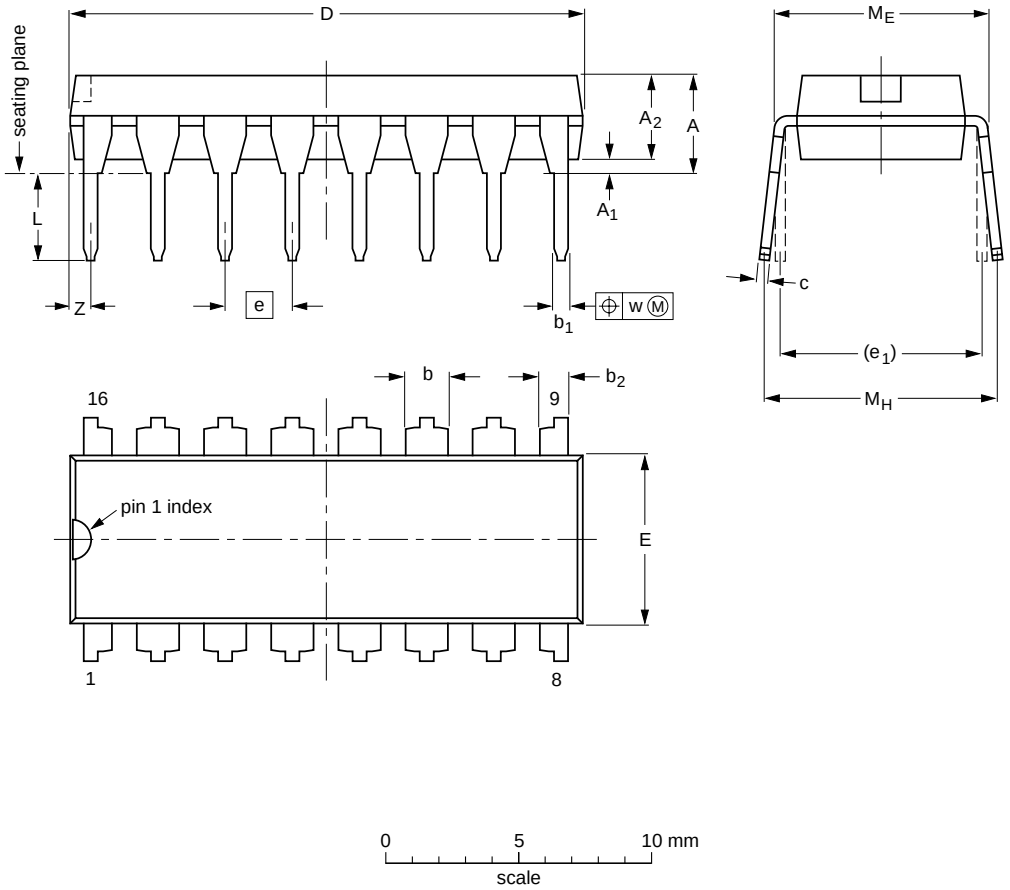


Inputs not being tested should be open-circuit.

Fig.16 Test figure for defining regulated supply (V_{DD}) performance in ringer and trickle mode.

PACKAGE OUTLINES

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

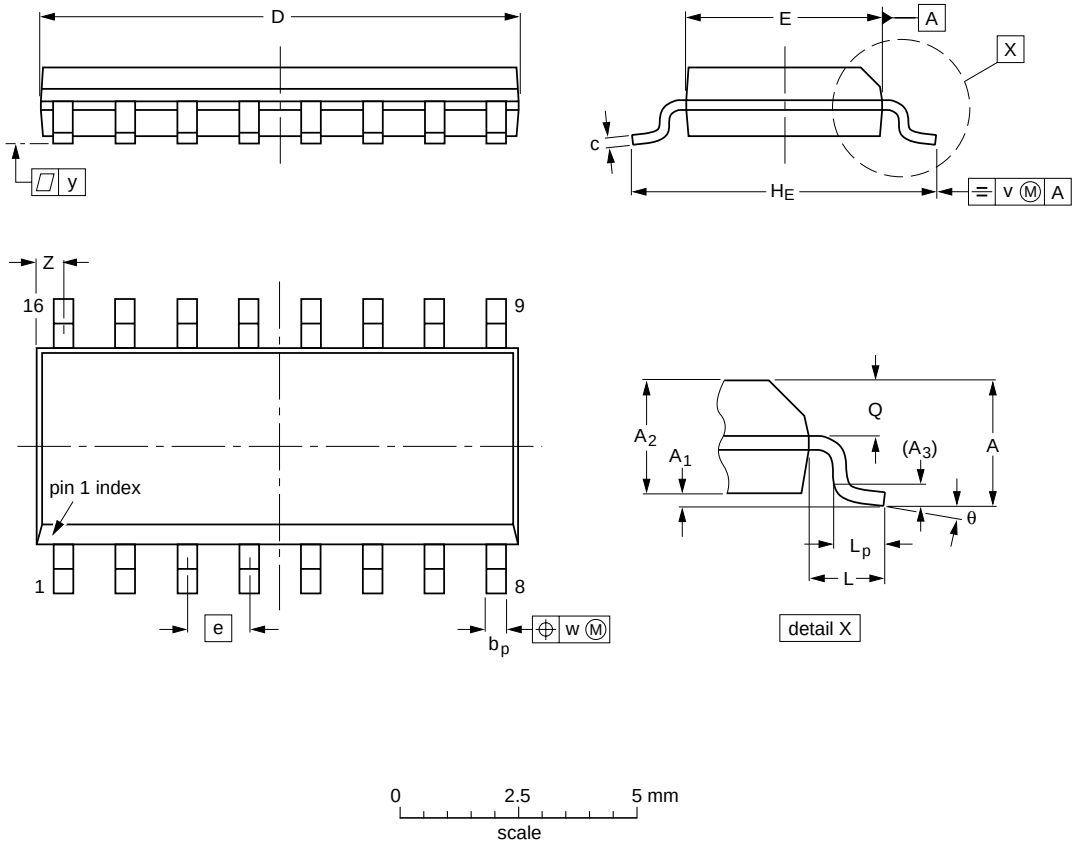
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~95-01-23~~ 97-05-22

SOLDERING

Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Through-hole mount packages

SOLDERING BY DIPPING OR BY SOLDER WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

MANUAL SOLDERING

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Surface mount packages

REFLOW SOLDERING

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

WAVE SOLDERING

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

MANUAL SOLDERING

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of IC packages for wave, reflow and dipping soldering methods

MOUNTING	PACKAGE	SOLDERING METHOD		
		WAVE	REFLOW(1)	DIPPING
Through-hole mount	DBS, DIP, HDIP, SDIP, SIL	suitable(2)	–	suitable
Surface mount	BGA, SQFP	not suitable	suitable	–
	HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(3)	suitable	–
	PLCC(4), SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended(4)(5)	suitable	–
	SSOP, TSSOP, VSO	not recommended(6)	suitable	–

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
3. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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