DATA SHEET

TDA9873H
Multistandard dual carrier stereo sound decoder

Product specification
File under Integrated Circuits, IC02

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Philips
Semiconductors

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Multistandard dual carrier stereo sound decoder TDA9873H

FEATURES

- Low power consumption
- Alignment-free multistandard FM sound demodulation
- No external intercarrier sound band-pass filters required
- Auto mute switchable via I²C-bus
- Multistandard A2 stereo sound decoder
- No adjustment for reduced channel separation requirement
- De-emphasis time constant related to standard
- Very reliable digital identification of sound transmission mode via I²C-bus, alignment-free
- No external filter for pilot input required
- I²C-bus transceiver with MAD (Module ADdress)
- I²C-bus control for all functions
- Stabilizer circuit for ripple rejection and constant output level
- Additional mono output
- Pin aligned with TDA9874AH
- ESD protection on all pins.

GENERAL DESCRIPTION

The TDA9873H is an economic multistandard dual FM demodulator and analog carrier stereo decoder with I²C-bus control.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9873H	QFP44	plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 × 14 × 2.2 mm	SOT205-1

QUICK REFERENCE DATA

V_{CC} = 5 V; T_{amb} = 25 °C; B/G standard (f_{SC1} = 5.5 MHz, f_{SC2} = 5.742 MHz, SC_1/SC_2 = 7 dB, Δf_{AF} = 27 kHz, f_{mod} = 1 kHz, L = R, stereo mode); input level for first SC $V_{i(FM)(rms)}$ = 50 mV; f_{ref} = 4.000 MHz; measured in test circuit of Figs 7 and 8; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		4.5	5	6.6	V
I_{CC}	supply current		40	60	75	mA
$V_{o(rms)}$	AF output level (RMS value)	54% modulation; note 1	400	500	600	mV
$V_{o(cl)(rms)}$	clipping level of the output signal level (RMS value)	THD < 1.5%	1400	–	–	mV
$f_{i(FM)}$	FM-PLL operating frequencies (switchable)	1st sound carrier				
		M standard	–	4.5	–	MHz
		B/G standard	–	5.5	–	MHz
		I standard	–	6.0	–	MHz
		D/K standard	–	6.5	–	MHz
		2nd sound carrier				
		M standard	–	4.72	–	MHz
		B/G standard	–	5.74	–	MHz
		D/K (1) standard	–	6.26	–	MHz
		D/K (2) standard	–	6.74	–	MHz
		D/K (3) standard	–	5.74	–	MHz
S/N_W	weighted signal-to-noise ratio (complete signal path)	CCIR 468-4 weighted; quasi peak; dual mode; B/G standard; note 1	52	56	–	dB
$t_{ident(on)}$	total identification time on for identification mode change	normal mode; note 2	0.35	–	2	s
		fast mode; note 2	0.1	–	0.5	s
$V_{i(FM)(rms)}$	FM-PLL input sensitivity for pull-in (RMS value)	1st carrier	–	–	6	mV
		2nd carrier	–	–	1	mV
$\alpha_{cs(AF)(stereo)}$	AF channel separation (stereo mode; complete signal path)	B/G standard; note 3				
		without alignment	25	30	–	dB
		I^2C-bus alignment	40	45	–	dB
$\alpha_{ct(AF)(dual)}$	AF crosstalk attenuation (dual mode; complete signal path)		65	70	–	dB

Notes

1. Condition for B/G, I and D/K standard: V_{CC} = 5 V and Δf = 27 kHz (m = 54%).
   Condition for M standard: V_{CC} = 5 V and Δf = 13.5 kHz; 6 dB gain added internally, to compensate smaller deviation.
2. The maximum total system identification time on for a channel change is equal to maximum value of $t_{ident(on)}$ plus $t_{I2C\ read\text{-}out}$ (*see also "The I^2C-bus and how to use it"* (order number 9398 393 40011)). The maximum total system identification time off for a channel change is equal to maximum value of $t_{ident(off)}$ plus $t_{I2C\ read\text{-}out}$. The fast mode is proposed mainly during search tuning, program or channel select. If the channel is selected, the identification response should be switched to normal mode for improved reliability. However due to the transition from fast to normal mode, the identification bits are not valid for one integrator period. Therefore the transmitter mode detected during the fast mode has to be stored before changing to normal mode. The storage has to be kept for two seconds (maximum value of $t_{ident(on)}$ in the normal mode) from the moment of transition. The identification can now operate in the normal mode until the next tuning action.
3. R modulated, L monitored.

BLOCK DIAGRAM

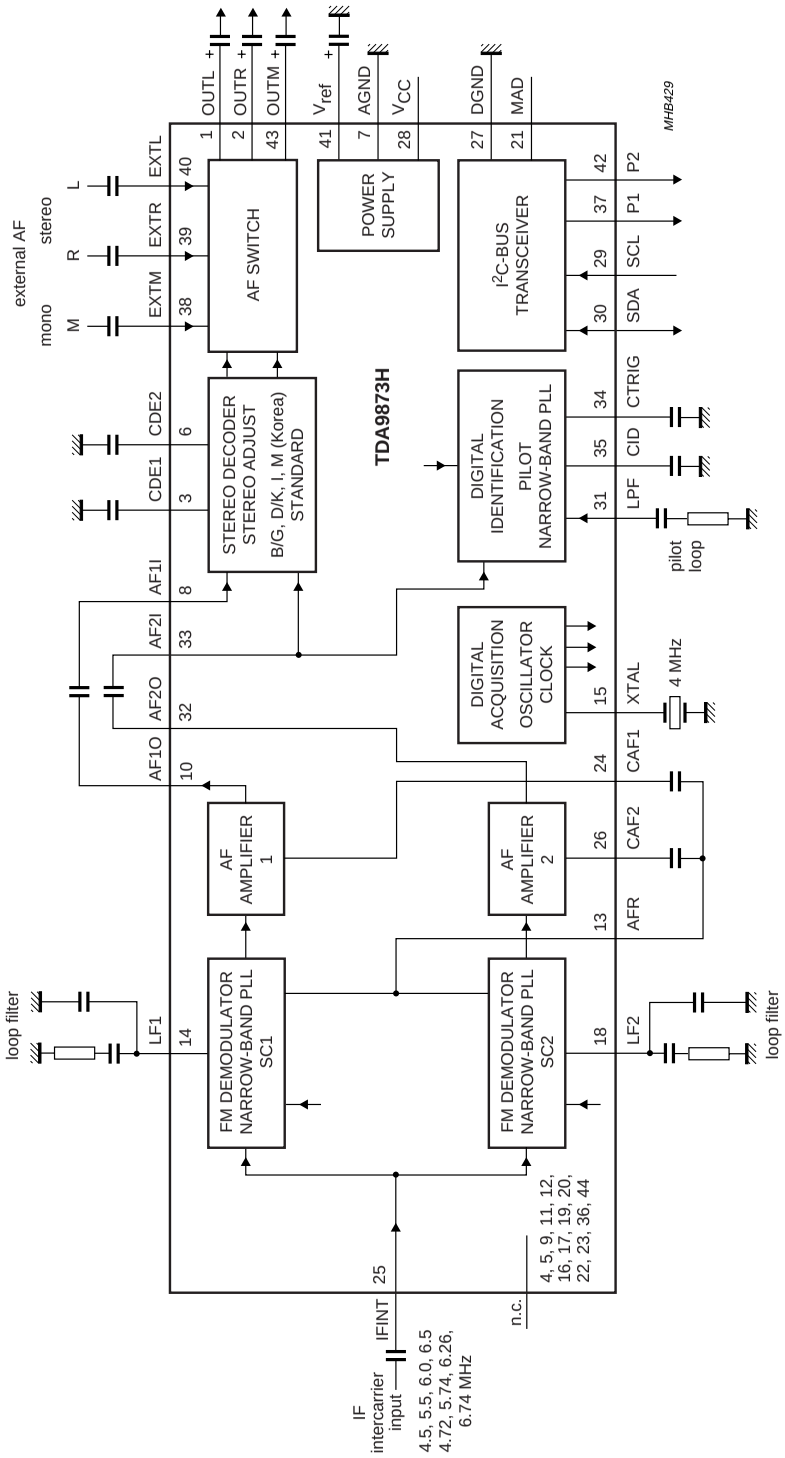


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OUTL	1	left audio output
OUTR	2	right audio output
CDE1	3	de-emphasis 1 capacitor
n.c.	4	not connected
n.c.	5	not connected
CDE2	6	de-emphasis 2 capacitor
AGND	7	analog ground
AF1I	8	audio 1 input
n.c.	9	not connected
AF1O	10	audio 1 output
n.c.	11	not connected
n.c.	12	not connected
AFR	13	AF1/2 signal return
LF1	14	loop filter 1
XTAL	15	4 MHz reference input
n.c.	16	not connected
n.c.	17	not connected
LF2	18	loop filter 2
n.c.	19	not connected
n.c.	20	not connected
MAD	21	programmable address bit (module address)
n.c.	22	not connected

SYMBOL	PIN	DESCRIPTION
n.c.	23	not connected
CAF1	24	audio 1 (AF1) capacitor
IFINT	25	IF intercarrier input
CAF2	26	audio 2 (AF2) capacitor
DGND	27	digital ground
V_{CC}	28	supply voltage (+5 V)
SCL	29	serial clock input (I^2C-bus)
SDA	30	serial data input/output (I^2C-bus)
LPF	31	pilot loop filter
AF20	32	audio 2 output
AF2I	33	audio 2 input
CTRIG	34	trigger capacitor
CID	35	identification capacitor
n.c.	36	not connected
P1	37	output port 1
EXTM	38	external audio input mono
EXTR	39	external audio input right
EXTL	40	external audio input left
V_{ref}	41	reference voltage ($\frac{1}{2}V_{CC}$)
P2	42	output port 2
OUTM	43	mono output
n.c.	44	not connected

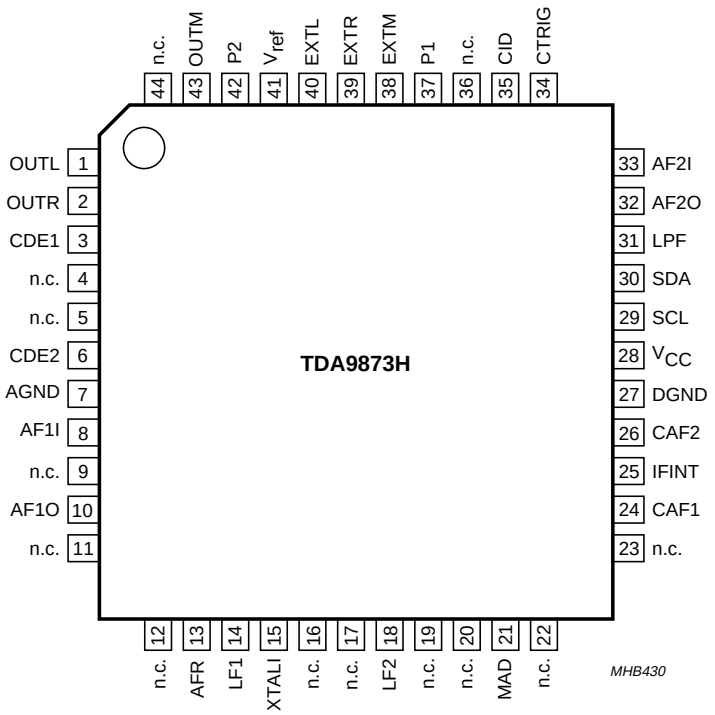


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

FM demodulators

The FM demodulators are Narrow-Band PLLs (NBPLLs) with external loop filters, to provide the required selectivity. To achieve good selectivity, linear Phase Detectors (PDs) and constant input levels are required. The intercarrier signal from the input terminal is fed via high-pass filters and gain controlled amplifiers to the phase detectors. A carrier cancellation circuit placed before the amplifier for the second PLL is used to reduce the first sound carrier. The PD output signals control the integrated relaxation oscillators via the loop filters. The frequency range is approximately 4 to 7 MHz. As a result of locking, the oscillator frequency tracks with the modulation of the input signal and the oscillator control voltages are superimposed by the AF voltages. Using this method, the FM-PLLs operate as FM demodulators. The AF voltages are present at the loop filters and fed via buffers with 0 dB gain to the audio amplifiers. The supported standards and their characteristics are given in Table 1.

Digital acquisition help

A narrow-band PLL requires a measure to lock to the wanted input signal. Each relaxation oscillator of the three integrated PLLs (1st and 2nd sound carriers and pilot carrier) has a wide frequency range. To guarantee correct locking of the PLL with respect to the catching range, the digital acquisition help provides individual control until the VCO frequency is within the standard and PLL dependent lock-in window, related to the standard dependent carriers. It ensures that the oscillator frequency of the FM-PLL is within ±225 kHz of the sound carrier to be demodulated. The pilot carrier frequency window is ±150 Hz.

The working principal of the digital acquisition help is as follows: The VCOs are connected, one at a time, to a down-counter. The counter start value is standard dependent and predefined for each of the three PLLs. After a given counting time the stop value of the down-counter is probed.

If the stop value is lower (higher) than the expected value range, the VCO frequency is higher (lower) than the lock-in window. A negative (positive) control current is injected into the loop filter for a short time, thereby decreasing (increasing) the VCO frequency by a proportional value.

If the stop value meets the expected value range, the VCO frequency is within the defined lock-in window and no control current is injected into the loop filter.

In an endless circle the VCO of the next PLL will be connected to the down-counter and the described procedure starts again.

The whole tracing as well as the counting time itself is derived from the external frequency reference. The cycle time is 256 μs.

Auto mute

If a sound carrier is missed, acquisition pulses are generated when the NBPLL frequency leaves the window edges. To avoid noise at the audio output, an I^{2}C-bus switchable mute-enable stage is built in. If auto mute is enabled via the I^{2}C-bus, the circuit mutes immediately after the first acquisition pulse. If a sound carrier occurs (no further acquisition pulses), the mute stage automatically returns to active mode after 40 ms.

If the 1st sound carrier is not present, the 2nd audio channel will also be muted.

Audio preamplifier

The AF preamplifiers are operational amplifiers with internal feedback, high gain and high common mode rejection. The AF voltages from the PLL demodulators (small output signals) are amplified by approximately 34 dB. Using a DC operating point control circuit, the AF amplifiers are decoupled from the PLL DC voltage. The amplified AF signals are available at the output terminals and fed via external decoupling capacitors to the stereo decoder input terminals.

Stereo decoder

The input circuit incorporates a soft-mute stage which is controlled by the FM-PLL acquisition circuit. The auto mute function can be disabled via the I^{2}C-bus.

The AF output voltage is 500 mV (RMS) for 54% modulation, clipping therefore may occur at high over-modulation. If more headroom is required the input signal can be attenuated by 6 dB via the I^{2}C-bus.

A stereo adjustment (see Fig.6) is incorporated to correct the FM demodulator output voltage spread, see Table 19. If no I^{2}C-bus adjustment is required (potentiometer adjustment or no adjustment) the default value should be 0 dB for B/G, M and D/K (2) standard. For the standards D/K (1) and D/K (3) the 2nd sound carrier frequency is below the1st sound carrier which results in a lower AF output level for the 2nd sound carrier. In this state, a gain of +0.1 dB for D/K (1) and +0.2 dB for D/K (3) is preferred.

In the following dematrix, the modes stereo, mono and dual are processed for the different standards. The 6 dB level difference between B/G and M standard is automatically compensated in the dematrix, therefore no further level adaption is needed.

De-emphasis is performed by two RC low-pass filter networks with internal resistors and external capacitors. The time constant is automatically switched to 50 μs or 75 μs according to the chosen standard.

Due to some frequency response peaking of the FM demodulation, compensation is necessary. This is done by having a slightly larger time constant for the de-emphasis.

All other settings such as AF switch, stereo channel adjustment values or default corrections have to be controlled via the I²C-bus depending on the identification or user definition.

AF switch

The circuit incorporates a single stereo and mono AF output. Using rail-to-rail operational amplifiers, the clipping level is set to 1.4 V (RMS) for V_{CC} = 5 V.

As well as the internal stereo decoder output signal, one external stereo and one mono input can be switched to the AF outputs. Both the mono and stereo outputs can be switched independent of the internal or external sources, see Tables 15 and 25. Fig.6 shows the switch configurations.

A nominal gain of 0 dB for the signals from the external inputs to the outputs is built-in.

Stereo/dual sound identification

The pilot signal is fed to the input of a NBPLL. The PLL circuit generates the synchronized pilot carrier. This carrier is used for the synchronous AM-demodulation to get the low-pass filtered identification signal.

A Schmitt trigger circuit performs pulse shaping of the identification signal when the signal level is higher than the Schmitt trigger threshold. For smaller signal levels there is no AC output signal, thus protecting against mis-identification caused by spurious signal components.

The identification stages consist of two digital PLL circuits and digital integrators to generate the stereo or dual sound identification bits, which can be read out via the I²C-bus.

A 4 MHz crystal oscillator provides the reference clock frequency. The corresponding detection bandwidth is larger than ±50 Hz for the pilot carrier signal, so that f_{pilot} variations from the transmitter can be tracked in the event of missing synchronization with the horizontal frequency f_H. However, the detection bandwidth for the identification signal is limited to approximately ±1 Hz for high identification reliability.

I²C-bus transceiver

The TDA9873H is microcontroller controlled via a 2-wire I²C-bus.

Two wires, serial data (SDA) and serial clock (SCL) carry information between the devices connected to the bus.

The TDA9873H has an I²C-bus slave transceiver with auto-increment.

To avoid conflicts in applications with other ICs providing similar or complementary functions, two slave addresses are available, selected on the pin MAD. A slave address is sent from the master to the slave receiver.

In the TV sound processor family several devices are available. To identify the TDA9873H device, the master sends a slave address with R/$\overline{W}$ bit = 0. The slave then generates an acknowledge and the master sends the data subaddress 254 to the slave, followed by an acknowledge from the slave to the master. The master then sends the slave address with R/$\overline{W}$ bit = 1. The slave then transmits the device identification code 80H to the master, followed by an acknowledge NOT and a STOP condition generated by the master.

Control ports

Two digital open-collector output ports P1 and P2 provide external switching functions in the receiver front-end or IF demodulators. The ports are controlled by the I²C-bus (see Tables 22 and 23) and are freely programmable.

Power supply

The different supply voltages and currents required for the analog and digital circuits are derived from two internal band gap reference circuits. One of the band gap circuits internally generates a voltage of approximately 2.4 V, independent of the supply voltage and temperature. A voltage regulator circuit, connected to this voltage, produces a constant voltage of 3.55 V which is used as an internal reference voltage. The AF reference voltage V_{ref} is $\frac{1}{2}V_{CC}$. Good ripple rejection is achieved with the external capacitor C_{ref} = 100 µF (16 V) in combination with an internal resistor at pin 6. No additional DC load for $\frac{1}{2}V_{CC}$ is allowed.

Analog ground (AGND, pin 7) and digital ground (DGND, pin 27) should be connected directly to the IC.

Power-on reset

When a power-on reset is activated by switching on the supply voltage or because of a supply voltage breakdown, the 117/274 Hz DPLL, 117/274 Hz integrator and the registers will be reset. Both AF channels (main and mono) are muted. The ports are in position HIGH. Gain stereo adjustment is 0 dB. Auto mute is active. For detailed information see Table 12.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage (pin 28)	maximum chip temperature of 125 °C; note 1	0	6.8	V
V_i	input voltage at:				
	pins 1 to 28 and 31 to 44		0	V_{CC}	V
	pins 29 to 30		−0.3	V_{CC}	V
T_{stg}	storage temperature		−25	+150	°C
T_{amb}	operating ambient temperature		−20	+70	°C
V_{es}	electrostatic handling	note 2	−150	+150	V
		note 3	−2500	+2500	V

Notes

1. I_{CC} = 60 mA; T_{amb} = 70 °C; $R_{th(j-a)}$ = 70 K/W.
2. Machine model class B: C = 200 pF; L = 0.75 µH; R = 0 Ω.
3. Human body model class B: C = 100 pF; R = 1.5 kΩ.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	70	K/W

CHARACTERISTICS

V_{CC} = 5 V; T_{amb} = 25 °C; B/G standard (f_{SC1} = 5.5 MHz, f_{SC2} = 5.742 MHz, SC_1/SC_2 = 7 dB, Δf_{AF} = 27 kHz, f_{mod} = 1 kHz, L = R, stereo mode); input level for first SC $V_{i(FM)(rms)}$ = 50 mV; f_{ref} = 4.000 MHz; measured in test circuit of Figs 7 and 8; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin 28)						
V_{CC}	supply voltage		4.5	5	6.6	V
I_{CC}	supply current		40	60	75	mA
FM-PLL demodulator (pin 25); notes 1 to 5						
$V_{i(FM)(rms)}$	FM-PLL input sensitivity for pull-in (RMS value)	1st sound carrier	–	–	6	mV
		2nd sound carrier	–	–	1	mV
	FM-PLL input level for gain controlled operation (RMS value)	1st sound carrier; note 2	6	–	150	mV
		2nd sound carrier; note 2	1	–	100	mV
$V_{i(vid)(p-p)}$	allowable interference video level (peak-to-peak value)	see Fig.5				
		$V_{i(FM1)(rms)}$ = 6 mV	–	–	160	mV
		$V_{i(FM1)(rms)}$ = 150 mV	–	–	2	V
R_i	input resistance		4	5	6	kΩ
$f_{i(FM)}$	FM-PLL operating frequencies (switchable)	1st sound carrier				
		M standard	–	4.5	–	MHz
		B/G standard	–	5.5	–	MHz
		I standard	–	6.0	–	MHz
		D/K standard	–	6.5	–	MHz
		2nd sound carrier				
		M standard	–	4.72	–	MHz
		B/G standard	–	5.74	–	MHz
		D/K (1) standard	–	6.26	–	MHz
		D/K (2) standard	–	6.74	–	MHz
		D/K (3) standard	–	5.74	–	MHz
Δf_{FM}	frequency windows of digital acquisition help	narrow; note 3	–	±225	–	kHz
		wide; note 3	–	±450	–	kHz
Δf_{AF}	frequency deviation	THD < 1.5%; normal gain	–	–	±62	kHz
		THD < 1.5%; reduced gain	–	–	±124	kHz
	frequency deviation for safe identification	V_{CC} = 5 V; stereo: 1 kHz L, 400 Hz R	–	–	±125	kHz
α_{AM}	AM suppression	AM: f_{mod} = 1 kHz; m = 0.3 referenced to 27 kHz FM deviation	40	46	–	dB
$K_{O(FM)}$	VCO steepness $\Delta f_{FM}/\Delta V_{LF1,2}$	note 5	–	3.3	–	MHz/V
$K_{D(FM)}$	phase detector steepness $\Delta I_{LF1,2}/\Delta\varphi(V_{FM})$	note 5	–	4	–	μA/rad
V_{CAF}	DC voltage at CAF1 and CAF2	dependent on intercarrier frequency f_{FM}	1.5	–	3.3	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$B_{AF(-3dB)}$	−3 dB audio frequency bandwidth	measured at AF1O and AF2O; see Figs 7 and 8				
		upper limit dependent on loop filter; note 5	65	80	–	kHz
		lower limit dependent on C_{AF}; C_{AF} = 470 nF; note 4	–	–	20	Hz
$V_{o(FM)(rms)}$	output level (RMS value)	measured at AF1O and AF2O	–	250	–	mV
Audio processing (pins 1, 2, 8 and 33)						
$V_{o(rms)}$	AF output level (RMS value)	f_{mod} = 300 Hz; 54% modulation; switchable by I²C-bus; note 6				
		normal gain	400	500	600	mV
		reduced gain	200	250	300	mV
$V_{o(cl)(rms)}$	AF output clipping level (RMS value)	V_{CC} = 5 V; THD = 1.5%	1400	–	–	mV
R_L	allowable load resistor	AC coupled	10	–	–	kΩ
C_L	allowable load capacitor		–	–	1.5	nF
$R_{L(DC)}$	allowable DC load resistor		100	–	–	kΩ
R_o	output resistance		70	150	300	Ω
THD	total harmonic distortion	$V_{o(rms)}$ = 0.5 V; f_{AF} = 1 kHz	–	0.2	0.5	%
$\alpha_{cs(AF)(stereo)}$	AF channel separation (stereo mode; complete signal path)	without alignment; note 7				
		B/G or M (Korea) standard	25	30	–	dB
		D/K standard	23	27	–	dB
		potentiometer alignment; B/G, M and D/K standard; notes 7 and 8	35	40	–	dB
		I²C-bus alignment; notes 7 and 9				
		B/G and D/K standard	40	45	–	dB
		M standard	35	40	–	dB
$\alpha_{ct(AF)(dual)}$	AF crosstalk attenuation (dual mode; complete signal path)	A = 1 kHz; B = 400 Hz; Δf = ±50 kHz				
		complete signal path	65	70	–	dB
		stereo decoder only	70	75	–	dB
$\alpha_{mute(AF)}$	mute attenuation of AF signal		75	80	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
S/N_W	weighted signal-to-noise ratio (complete signal path)	CCIR 468-4 weighted; quasi peak; dual mode; note 6				
		50 µs de-emphasis; B/G, I and D/K standard	52	56	–	dB
		75 µs de-emphasis; M standard	48	52	–	dB
	signal-to-noise ratio at external AF with stereo decoder only	CCIR 468-4 weighted; quasi peak; $V_{o(rms)}$ = 500 mV	70	75	–	dB
$t_{DEP(B/G)}$	de-emphasis time constant for B/G, D/K and I standard	note 10; see Fig.3	–	50	–	µs
$t_{DEP(M)}$	de-emphasis time constant for M standard	note 10; see Fig.3	–	75	–	µs
f_{ro}	roll-off frequency	470 nF at AF1I and AF2I; without de-emphasis				
		low frequency (–3 dB)	–	–	20	Hz
		high frequency (–0.5 dB)	20	–	–	kHz
PSRR	power supply ripple rejection at OUTL and OUTR (overall performance)	f_{ripple} = 70 Hz; $V_{ripple(p-p)}$ = 100 mV; dual mode; see Fig.4	20	26	–	dB
$R_{i(AF1)}$	AF1I input resistance		32	40	48	kΩ
$R_{i(AF2)}$	AF2I input resistance		32	40	48	kΩ
External additional inputs (pins 38 to 40)						
$V_{i(nom)(rms)}$	nominal input signal voltage (RMS value)		–	0.5	–	V
$V_{i(cl)(rms)}$	clipping voltage level (RMS value)	THD ≤ 1.5%; V_{CC} = 5 V	1.4	–	–	V
G_v	AF signal voltage gain	$G = V_o/V_i$	–1	0	+1	dB
R_i	input resistance		40	50	60	kΩ
f_{ro}	roll-off frequency	low frequency (–3 dB)	–	–	20	Hz
		high frequency (–0.5 dB)	20	–	–	kHz
$\alpha_{ct(ext)}$	AF crosstalk attenuation (external input)	EXTL = 1 kHz; EXTR = 400 Hz	70	75	–	dB
Mono output OUTM (pin 43)						
R_o	output resistance		70	200	350	Ω
R_L	load resistor	AC coupled	10	–	–	kΩ
$R_{L(DC)}$	allowable DC load resistor		100	–	–	kΩ
C_L	load capacitor		–	–	1.5	nF
α_{mute}	mute attenuation		60	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pilot processing (pin 31)						
f_{pilot}	pilot operating frequency ($3.5f_H$)	f_{H1} = 15625 Hz	–	54688	–	Hz
		f_{H2} = 15734 Hz	–	55070	–	Hz
$K_{O(pilot)}$	VCO steepness $\Delta f_{pilot}/\Delta V_{LPF}$	note 11	–	26	–	kHz/V
$K_{D(pilot)}$	phase detector steepness $\Delta I_{LPF}/\Delta\varphi$(pilot)	Δf_{pilot} window ±150 Hz; note 11	–	2	–	μA/rad
$\Delta f_{SC2(pilot)}$	second sound carrier pilot frequency deviation	unmodulated pilot	1.5	2.5	3.5	kHz
$m_{AM(pilot)}$	pilot AM modulation depth		25	50	75	%
Identification (pins 34 and 35)						
$f_{LP(CID)}$	low-pass frequency response at pin CID	–3 dB point	450	600	750	Hz
f_{stereo}	identification operating frequencies	stereo; B/G and D/K standard; $\frac{1}{133}f_{H1}$	–	117.48	–	Hz
$f_{stereo(h)}$		stereo; M standard; $\frac{1}{105}f_{H2}$	–	149.85	–	Hz
f_{dual}		dual; B/G and D/K standard; $\frac{1}{57}f_{H1}$	–	274.12	–	Hz
$f_{dual(h)}$		dual; M standard; $\frac{1}{57}f_{H2}$	–	276.04	–	Hz
$t_{ident(on)}$	total identification time on for identification mode change	normal mode; note 12	0.35	–	2	s
		fast mode; note 12	0.1	–	0.5	s
$t_{ident(off)}$	total identification time off for identification mode change	normal mode; note 12	0.6	–	1.6	s
		fast mode; note 12	0.15	–	0.4	s
Δf_{ident}	identification window width	normal mode; note 13	–	2	–	Hz
		fast mode; note 13	–	8	–	Hz
C/N_{pilot}	pilot sideband carrier-to-noise ratio for start of identification		–	33	–	dBc/Hz
f_{det}	pull-in frequency range of identification PLL (referred to f_{stereo} = 117.48 Hz and f_{dual} = 274.12 Hz)	normal mode lower side	–0.63	–	–0.63	Hz
		normal mode upper side	0.63	–	0.63	Hz
		fast mode lower side	–2.05	–	–2.05	Hz
		fast mode upper side	2.05	–	2.05	Hz
Reference input (operation as crystal oscillator; pin 15)						
$f_{sr(xtal)}$	series resonant frequency of crystal	fundamental mode; C_L = 20 to 30 pF during crystal production	–	4.0	–	MHz
$\Delta f_{w(max)}$	allowed maximum spread of oscillator working frequency	over operating temperature range including ageing and influence of drive circuit; note 3	–	–	$\pm 200 \times 10^{-6}$	–
Δf_R	cutting frequency tolerance		–	–	$\pm 50 \times 10^{-6}$	–
Δf_d	frequency drift		–	–	$\pm 50 \times 10^{-6}$	–
$R_{s(eq)}$	equivalent crystal series resistance		–	60	200	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{s(um)}$	crystal series resistance of unwanted mode		$2 \times R_{s(eq)}$	–	–	Ω
Reference input (operation as input terminal; pin 15)						
f_ω	working frequency		–	4	–	MHz
V_I	DC input voltage		2.3	2.6	2.9	V
R_i	input resistance		2.5	3.0	3.5	kΩ
Δf_{ref}	tolerance of reference frequency	notes 3 and 14	–	–	$\pm 300 \times 10^{-6}$	–
$V_{ref(rms)}$	amplitude of reference signal source (RMS value)	operation as input terminal	80	–	400	mV
$V_{o(ref)}$	output resistance of reference source		–	–	4.7	kΩ
C_K	decoupling capacitance to external reference source	operation as input terminal	22	100	–	pF
I²C-bus transceiver (pins 29 and 30); note 15						
f_{clk}	clock frequency		0	–	100	kHz
V_{IH}	HIGH-level input voltage		3	–	V_{CC}	V
V_{IL}	LOW-level input voltage		–0.3	–	+1.5	V
I_{IH}	HIGH-level input current		–10	–	+10	µA
I_{IL}	LOW-level input current		–10	–	+10	µA
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	–	–	0.4	V
$I_{o(sink)}$	output sink current	V_{CC} = 0 V	–	–	10	µA
$I_{o(source)}$	output source current	V_{CC} = 0 V	–	–	10	µA
Port outputs P1 and P2 (open-collector outputs; pins 37 and 42)						
V_{OL}	LOW-level output voltage	I_o = 1 mA (sink)	–	–	0.3	V
$I_{o(p)}$	port output sink current	port low	–	–	1	mA
Power-on reset						
$V_{CC(sr)}$	supply voltage for start of reset	decreasing supply voltage	2.5	3	3.5	V
$V_{CC(er)}$	supply voltage for end of reset	increasing supply voltage; I²C-bus transmission enabled	–	–	4.5	V

Notes

1. Input level for IF intercarrier from an external generator with 50 Ω source impedance, f_{mod} = 400 Hz, 27 kHz deviation of audio references: level for SC_1 50 mV (RMS), SC_1/SC_2 = 7 dB. S/N and THD measurements are taken at 50 µs de-emphasis.
2. For higher input voltages a series resistor connected to pin 25 is recommended.
3. The tolerance of the reference frequency determines the accuracy of the FM-demodulator centre frequencies, maximum FM deviation, pilot window width and pilot window mid-frequency error.
4. The lower limit of audio bandwidth depends on the value of the capacitors at pins 24 and 26. A value of C_{AF} = 470 nF leads to $f_{AF(-3dB)} < 20$ Hz and a value of C_{AF} = 220 nF leads to $f_{AF(-3dB)} < 40$ Hz.

5. Approximate calculation of the FM-PLL loop filter can be done using the following formula:

$$B_{L\,(-3dB)} = \frac{1}{2\pi}\sqrt{\frac{K_O \times K_D}{C_P}}\left(1.55 - \frac{1}{4R^2 \times K_O \times K_D \times C_P}\right)$$

with K_O = VCO steepness $\left(\frac{rad}{V}\right)$ or $\left(2\pi\frac{Hz}{V}\right)$

K_D = phase detector steepness $\left(\frac{\mu A}{rad}\right)$

R = loop resistor
C_S = series capacitor
C_P = parallel capacitor
$B_{L(-3dB)}$ = loop bandwidth for −3 dB.
Example: $B_{L(-3dB)}$ = 80 kHz: C_S = 3.3 nF; C_P = 680 pF; R = 5.6 kΩ.

6. S/N decreases by 4 dB if no 2nd sound carrier is present; auto mute enabled.
Condition for B/G, I and D/K standard: V_{CC} = 5 V and Δf = 27 kHz (m = 54%).
Condition for M standard: V_{CC} = 5 V and Δf = 13.5 kHz; 6 dB gain added internally, to compensate smaller deviation.
7. R modulated, L monitored. The I²C-bus stereo adjustment has to be set to a default value. For B/G, D/K (2) and M standard the default is 0 dB, for D/K (1) standard 0.1 dB and for D/K (3) standard 0.2 dB.
8. Using potentiometer adjustment, the AF output voltage is reduced by 1.3 dB because of the series resistor (see Fig.8).
9. Separate alignment for each standard necessary. Minimum value for D/K (3) standard is 37 dB.
10. Because the loop transfer function is not flat, the de-emphasis is superimposed by an amplitude response correction that compensates for an influence from the FM demodulators.
11. Approximate calculation of the pilot PLL loop filter can be done using the following formula:

$$f_n = \frac{1}{2\pi}\sqrt{\frac{K_O \times K_D}{C}}$$

$$\vartheta = \frac{R}{2}\sqrt{C \times K_O \times K_D}$$

$B_{L(-3dB)} \approx 1.89 f_n$
The formulae are only valid under the condition: $0.5 \leq \vartheta \leq 0.8$
with K_O = VCO steepness $\left(\frac{rad}{V}\right)$ or $\left(2\pi\frac{Hz}{V}\right)$

K_D = phase detector steepness $\left(\frac{\mu A}{rad}\right)$

R = loop resistor
C = loop capacitor
f_n = natural frequency of PLL
$B_{L(-3dB)}$ = loop bandwidth for −3 dB
ϑ = damping factor.
Example: $B_{L(-3dB)}$ = 544 Hz: C = 100 nF; R = 7.5 kΩ; ϑ = 0.67; f_n = 288 Hz.

12. The maximum total system identification time on for a channel change is equal to the maximum value of $t_{ident(on)}$ plus $t_{I2C\ read\text{-}out}$. The maximum total system identification time off for a channel change is equal to the maximum value of $t_{ident(off)}$ plus $t_{I2C\ read\text{-}out}$. The fast mode is mainly for use during search tuning, program or channel select. If the channel is selected, the identification response should be switched to normal mode for improved reliability. However due to the transition from fast to normal mode, the identification bits are not valid for one integrator period. Therefore the transmitter mode detected during the fast mode must be stored before changing to the normal mode. The storage must be kept for two seconds (maximum value of $t_{ident(on)}$ in the normal mode) from the moment of transition. The identification can now operate in the normal mode until the next tuning action.
13. Identification window is defined as total pull-in frequency range (lower plus upper side) of identification PLL (steady detection) plus window increase due to integrator (fluctuating detection).
14. Window width dependent on f_{ω}.
15. The AC characteristics are in accordance with the I^2C-bus specification. The maximum clock frequency is 100 kHz. Information about the I^2C-bus can be found in the brochure *"The I^2C-bus and how to use it"* (order number 9398 393 40011).

Table 1 TV standard settings

STANDARD	f_{SC1} (MHz)	f_{SC2} (MHz)	PILOT FREQUENCY f_{pilot} (kHz)	STEREO IDENTIFICATION FREQUENCY f_{stereo} (Hz)	DUAL IDENTIFICATION FREQUENCY f_{dual} (Hz)	DE-EMPHASIS t_{DEP} (μs)
M	4.5	4.724	55.0699	149.85	276.04	75
B/G	5.5	5.742	54.6875	117.48	274.12	50
I	6	–	–	–	–	50
D/K (1)	6.5	6.268	54.6875	117.48	274.12	50
D/K (2)	6.5	6.742	54.6875	117.48	274.12	50
D/K (3)	6.5	5.742	54.6875	117.48	274.12	50

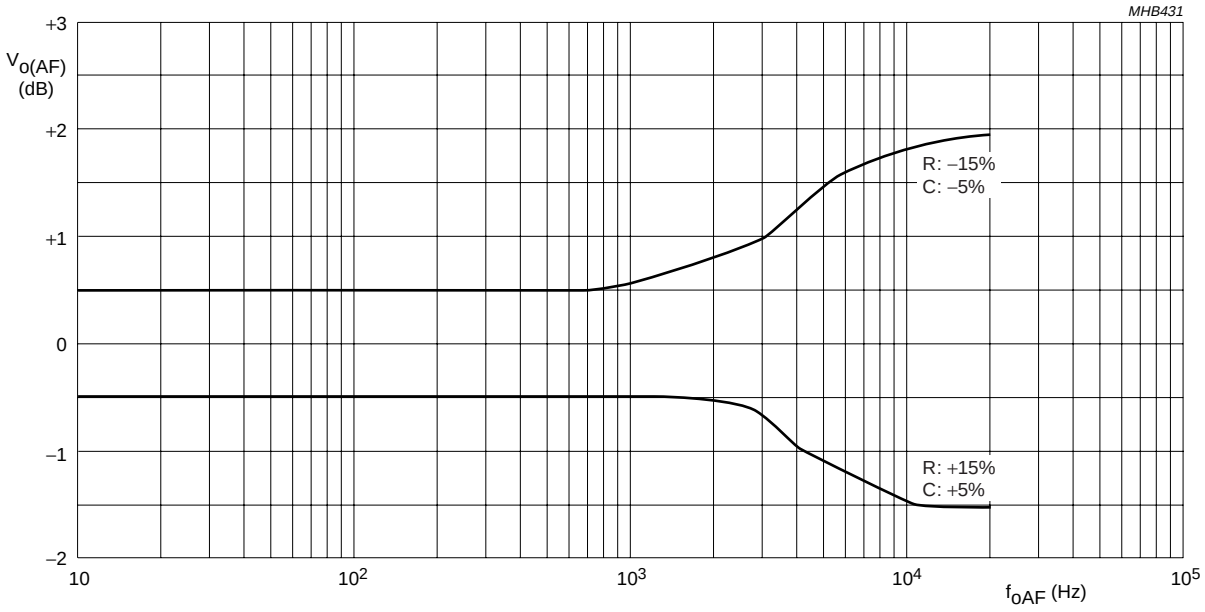
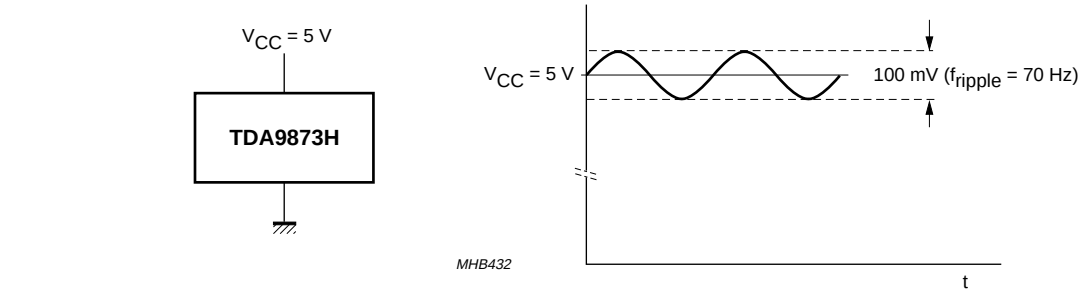
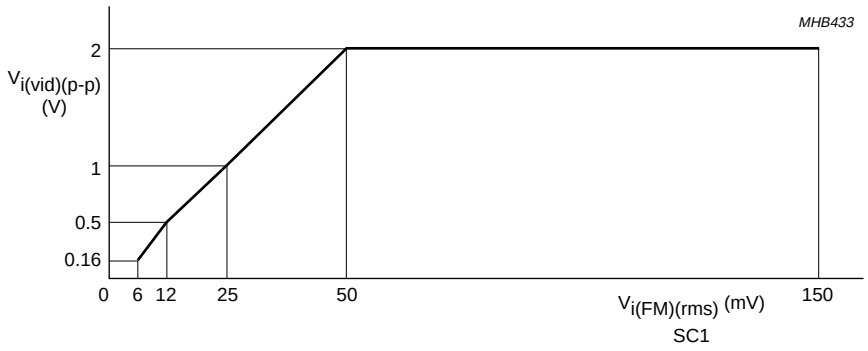


Fig.3 Tolerance scheme of AF frequency response; de-emphasis with C_{DE1}, C_{DE2} = 10 nF (±5%).



$$PSRR = 20\log\frac{V_{ripple}\text{ at OUTR}}{V_{ripple}\text{ at }V_{CC}}$$

Fig.4 Ripple rejection condition.



$\frac{SC1}{SC2}$ = 7 dB

video: colour-bar

Fig.5 Allowable interference video level.

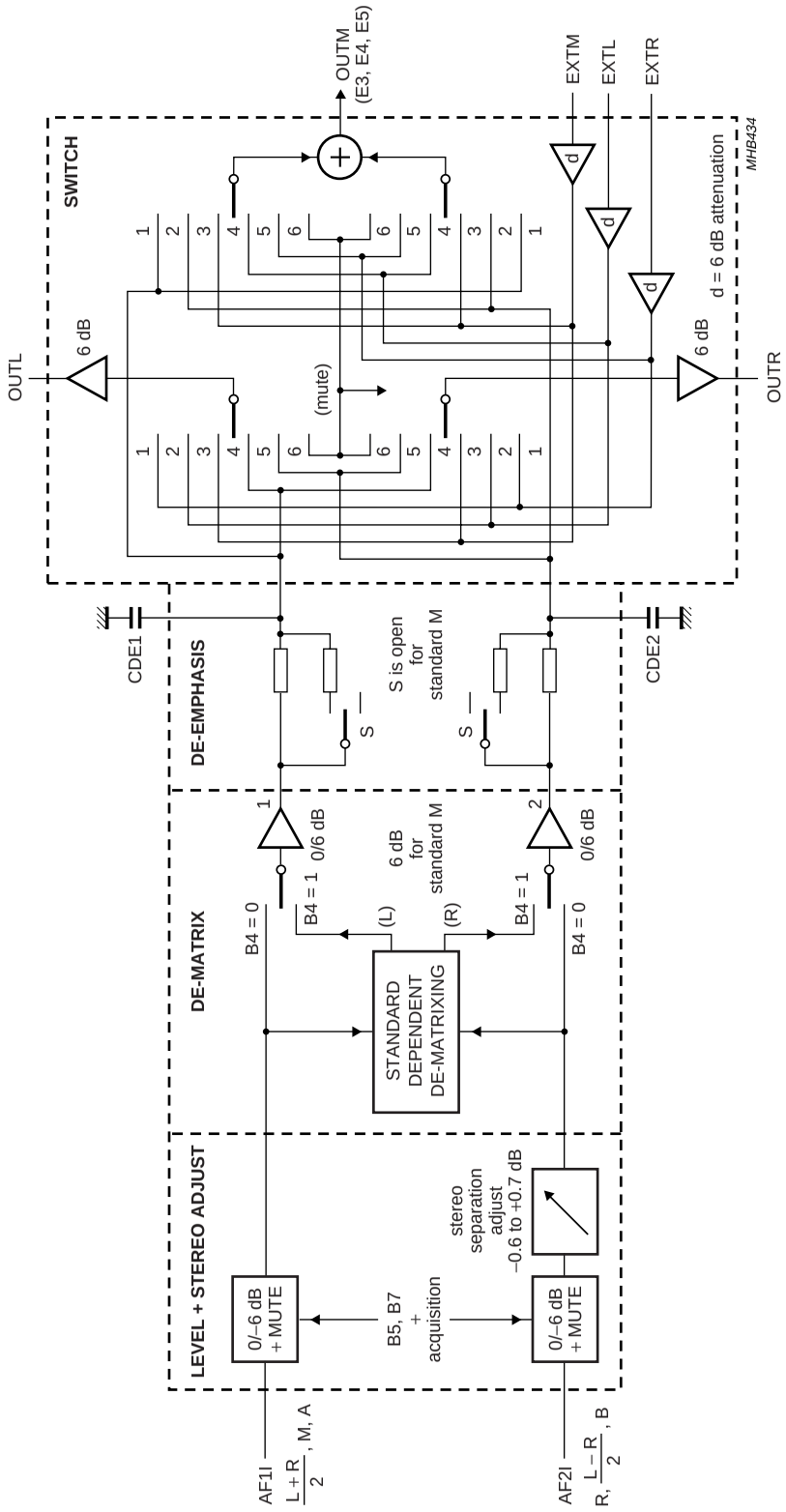


Fig.6 Audio part.

Example: For stereo mode (B4 = 1), OUTL is switched to position 4 and OUTR switched to position 5. For mono mode (B4 = 0), OUTL and OUTR are both switched to position 4.
This means: For mono/stereo switching, not only B4 but also the switch (stereo and mono output) must be set (see Tables 15 and 25).
Stereo output: internal/external source: B0, B1; output switching: B2, B3.

I²C-BUS PROTOCOL

I²C-bus format to read (device identification code)

S	SLAVE ADDRESS	R/$\overline{W}$ = 0	A	SUBADDRESS	A	S	SLAVE ADDRESS	R/$\overline{W}$ = 1	A	DATA	AN	P

Note

1. This data word H80 (device identification code) is read from the subaddress 254 which is set in the last write transfer.

Table 2 Explanation of I²C-bus format to read (device identification code)

NAME	DESCRIPTION
S	START condition; generated by the master
SLAVE ADDRESS	101 101 1; pin MAD not connected (standard)
	101 101 0; pin MAD connected to ground (pin programmable)
R/$\overline{W}$	logic 0 (write); generated by the master
	logic 1 (read); generated by the master
A	acknowledge; generated by the slave
SUBADDRESS	111 111 10 (254)
DATA	slave transmits the device identification code 80H
AN	acknowledge not; generated by the master
P	STOP condition; generated by the master

I²C-bus format to read (slave transmits data)

S	SLAVE ADDRESS	R/$\overline{W}$ = 1	A	DATA	AN	P

Table 3 Explanation of I²C-bus format to read (slave transmits data)

NAME	DESCRIPTION
S	START condition; generated by the master
SLAVE ADDRESS	101 101 1; pin MAD not connected (standard)
	101 101 0; pin MAD connected to ground (pin programmable)
R/$\overline{W}$	logic 1 (read); generated by the master
A	acknowledge; generated by the slave
DATA	slave transmits an 8-bit data word
AN	acknowledge not; generated by the master
P	STOP condition; generated by the master

Table 4 Definition of the transmitted byte after read condition

MSB							LSB
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	0	0	Y	Y	DS	ST	PONR

Table 5 Bit functions Table 4

BITS	FUNCTION
PONR	power-on reset; PONR = 1, power-on reset detected
ST	stereo sound; ST = 1, stereo sound identified
DS	dual sound; DS = 1, dual sound identified
Y	indefinite

Table 6 Interpretation of identification bits

ST	DS	FUNCTION
0	0	mono
0	1	dual sound
1	0	stereo sound
1	1	incorrect identification

Table 7 Power-on reset

PONR	FUNCTION
0	after successful reading of the status register
1	after power-on reset or after supply breakdown

If the master generates an acknowledge not and a STOP condition when it has received the data word READ, the master terminates the bus transfer. On the other hand, if the master generates an acknowledge then the slave started a second transfer with the READ byte and so on until the master generates an acknowledge not and STOP condition.

I²C-bus format to write (slave receives data)

S	SLAVE ADDRESS	R/$\overline{W}$ = 0	A	SUBADDRESS	A	DATA	A	P

Table 8 Explanation of I²C-bus format to write (slave receives data)

NAME	DESCRIPTION
S	START condition
SLAVE ADDRESS	101 101 1; pin MAD not connected (standard)
	101 101 0; pin MAD connected to ground (pin programmable)
R/$\overline{W}$	logic 0 (write)
A	acknowledge; generated by slave
SUBADDRESS	see Table 9
DATA	note 1; see Table 10
P	STOP condition

Note

1. If more than 1 byte of DATA is transmitted, auto-increment is performed, starting from the transmitted subaddress and auto-increment of the subaddress is performed in accordance with the order of Table 9.

Table 9 Subaddress definition (second byte after slave address)

FUNCTION	MSB							LSB
	D7	D6	D5	D4	D3	D2	D1	D0[1]
Switching	0	0	0	0	0	0	0	0
Adjust/standard	0	0	0	0	0	0	0	1
Port	0	0	0	0	0	0	1	0

Note

1. Significant subaddress bit.

Table 10 Data definition (third byte after slave address)

FUNCTION	MSB							LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Switching data	B7	B6	B5	B4	B3	B2	B1	B0
Adjust/standard data	C7	C6	C5	C4	C3	C2	C1	C0
Port data	0	0	E5	E4	E3	E2	E1	E0

Table 11 Bit functions in Table 10

BITS	FUNCTION
B0 and B1	signal source select; see Table 13
B2 and B3	output signal select; see Table 15
B4	stereo setting bit; see Table 15
B5	output level switching; see Table 16
B6	mute bit; see Table 17
B7	auto mute enable; see Table 18
C0 to C3	stereo adjust; see Table 19
C4 to C6	standard switching; see Table 20
C7	identification response time; see Table 21
E0	port 1; see Table 22
E1	port 2; see Table 23
E2	test mode; see Table 24 (not for customer)
E3 to E5	mono output setting; see Table 25

Table 12 Data setting of third byte after power-on reset; see note 1

FUNCTION	MSB							LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Switching data	1	1	X	X	X	X	X	X
Adjust/standard data	0	0	0	0	0	1	1	0
Port data	0	0	1	1	1	0	1	1

Note

1. X = don’t care.

Table 13 Source switching; see Table 10

SIGNAL SOURCE	B1	B0
Internal	0	0
External stereo	1	0
External mono	1	1

Table 14 Stereo decoder outputs (CDE1, CDE2); see Table 10

TRANSMISSION MODE	OUTPUTS	B4
Stereo	stereo	1
Stereo	mono	0
Mono	mono	0
Dual	dual	0

Table 15 Mode and output switching; data byte to select AF inputs and AF outputs

TRANSMISSION MODE	SELECTED MODE	OUTL	OUTR	B4	B3	B2
Mono	M	M	M	0	0	1
Stereo	forced mono	M	M	0	0	1
Stereo	ST	L	R	1	0	0
		R	L	1	1	1
Dual	AB	A	B	0	0	0
	AA	A	A	0	0	1
	BB	B	B	0	1	0
	BA	B	A	0	1	1
External mono	EXTM	EXTM	EXTM	0	0	0
External stereo	EXTL, EXTR	EXTL	EXTR	0	0	0
	EXTL, EXTL	EXTL	EXTL	0	0	1
	EXTR, EXTR	EXTR	EXTR	0	1	0
	EXTR, EXTL	EXTR	EXTL	0	1	1

Table 16 Output level switching; see Table 10

OUTPUT LEVEL	B5
Normal gain	1
Reduced gain	0

Table 17 Mute switching of AF outputs; see Table 10

OUTL, OUTR	B6
Not muted	0
Muted	1

Table 18 Auto mute activating; see Table 10

AUTO MUTE	B7
Disabled	0
Active	1

Table 19 Stereo adjustment, gain adjust in R channel; see Table 10

GAIN STEREO ADJUSTMENT (dB)	DATA			
	C3	C2	C1	C0
–0.6	0	0	0	0
–0.5	0	0	0	1
–0.4	0	0	1	0
–0.3	0	0	1	1
–0.2	0	1	0	0
–0.1	0	1	0	1
0.0	0	1	1	0
+0.1	0	1	1	1
+0.2	1	0	0	0
+0.3	1	0	0	1
+0.4	1	0	1	0
+0.5	1	0	1	1
+0.6	1	1	0	0
+0.7	1	1	0	1

Table 20 Standard switching; see Table 10

STANDARD	C6	C5	C4
B/G	0	0	0
M	0	0	1
D/K (1)	0	1	0
D/K (2)	0	1	1
D/K (3)	1	0	0
I	1	0	1

Table 21 Identification response time; see Table 10

FUNCTION	DATA
RESPONSE TIME	C7
Normal	0
Fast	1

Table 22 Port 1 output; see Table 10

PORT 1	E0
LOW	0
HIGH	1

Table 23 Port 2 output; see Table 10

PORT 2	E1
LOW	0
HIGH	1

Table 24 Test mode; note 1; see Table 10

TEST MODE	E2
Off	0
On	1

Note

1. Not for customer; for Philips Semiconductors only.

Table 25 Mono output; see Table 10

TRANSMISSION MODE	STEREO DECODER	OUTM	E5	E4	E3	B4
Mono	mono	mono	0	0	0	0
Stereo	forced mono	mono	0	0	0	0
Dual	dual	dual A	0	0	0	0
Dual	dual	dual B	0	0	1	0
Stereo	stereo	mono	0	1	0	1
–	–	EXT M	0	1	1	–
–	–	EXT L	1	0	0	–
–	–	EXT R	1	0	1	–
–	–	EXT L/R; $\frac{1}{2}$(L + R)	1	1	0	–
–	–	mute	1	1	1	–

APPLICATION INFORMATION

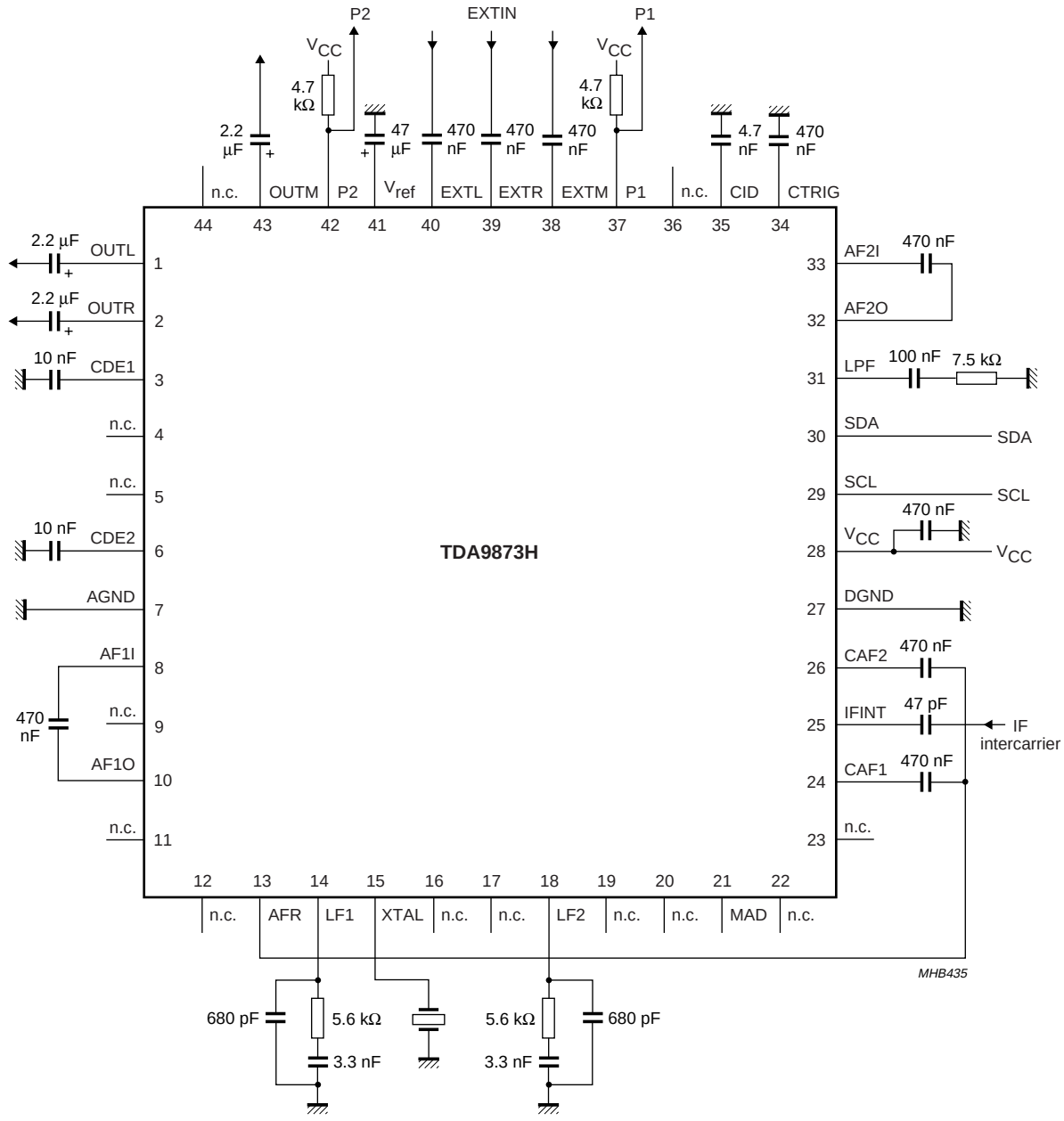


Fig.7 Application circuit without potentiometer alignment.

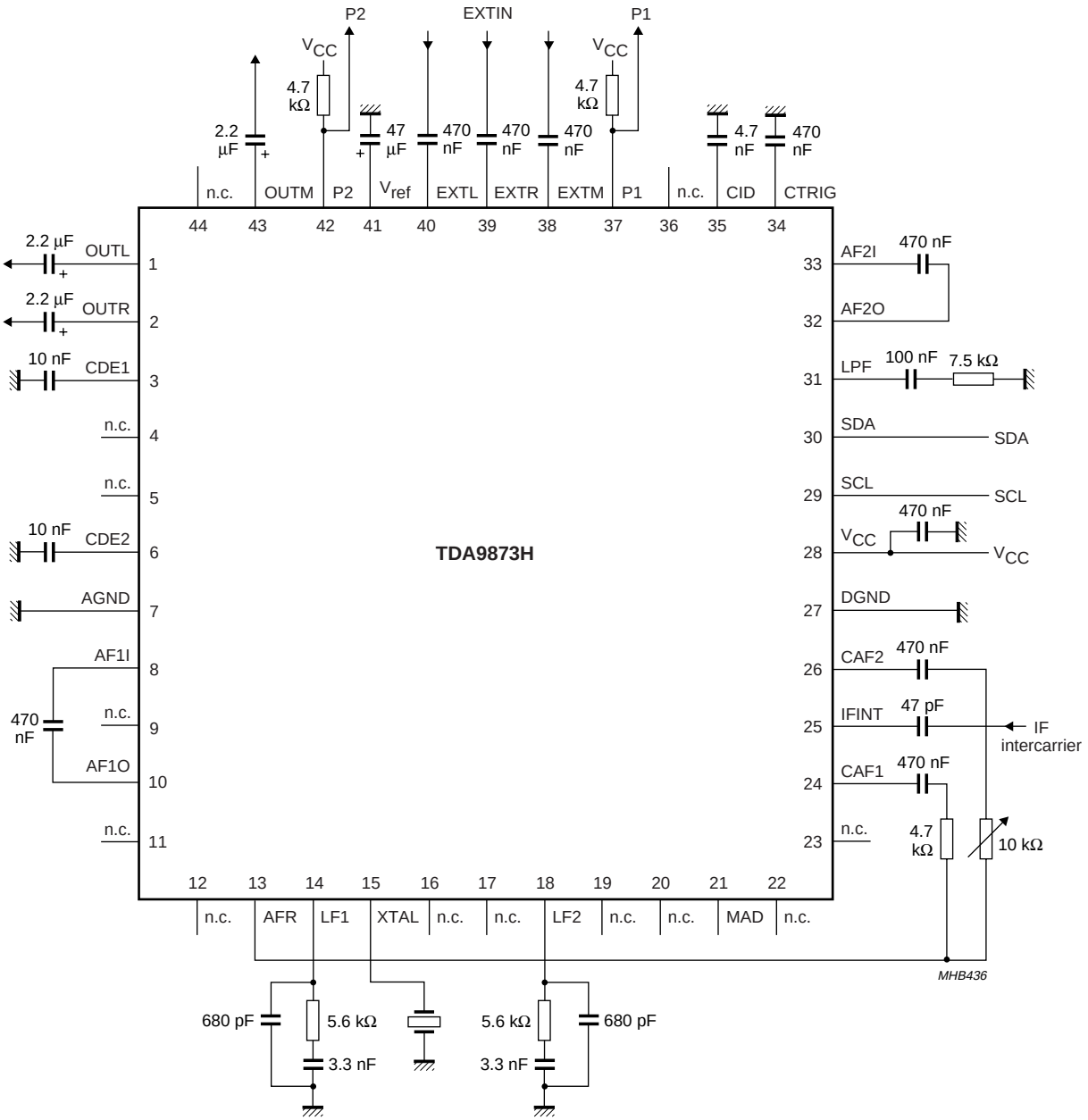


Fig.8 Application circuit with potentiometer alignment.

INTERNAL PIN CONFIGURATIONS

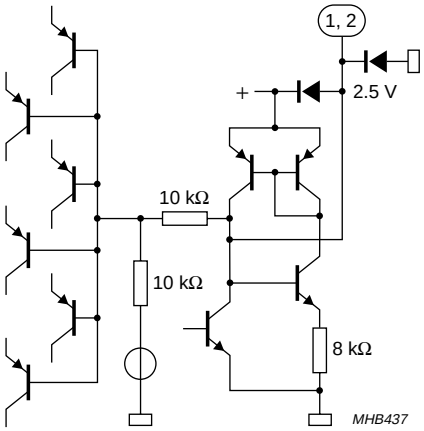


Fig.9 Pin 1; OUTL and pin 2; OUTR.

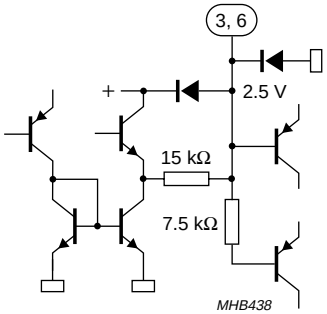


Fig.10 Pin 3; CDE1 and pin 6; CDE2.

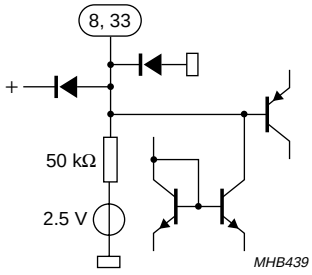


Fig.11 Pin 8; AF1I and pin 33; AF2I.

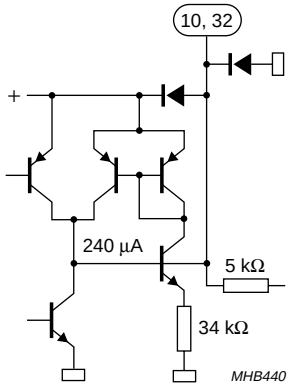


Fig.12 Pin 10; AF1O and pin 32; AF2O.

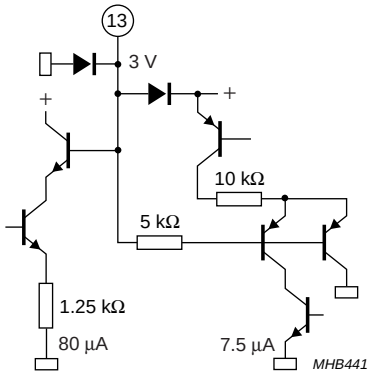


Fig.13 Pin 13; AFR.

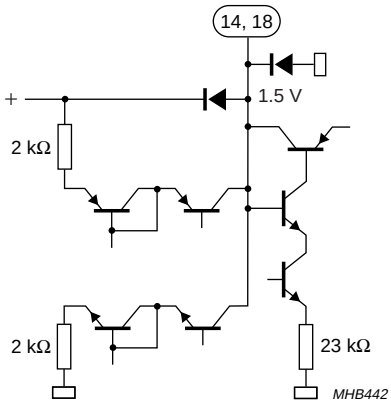


Fig.14 Pin 14; LF1 and pin 18; LF2.

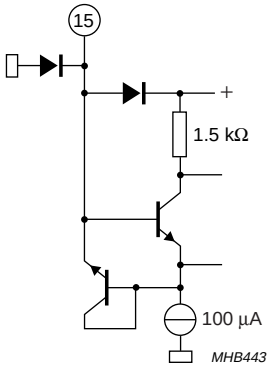


Fig.15 Pin 15; XTAL.

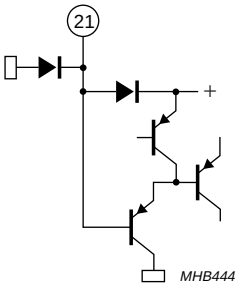


Fig.16 Pin 21; MAD.

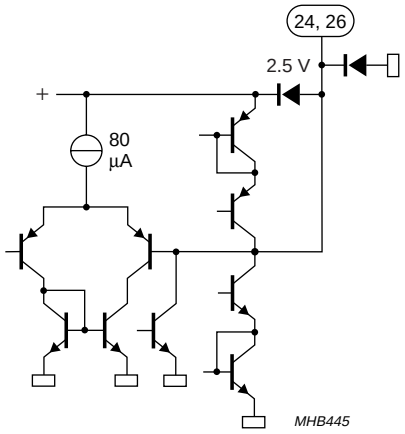


Fig.17 Pin 24; CAF1 and pin 26; CAF2.

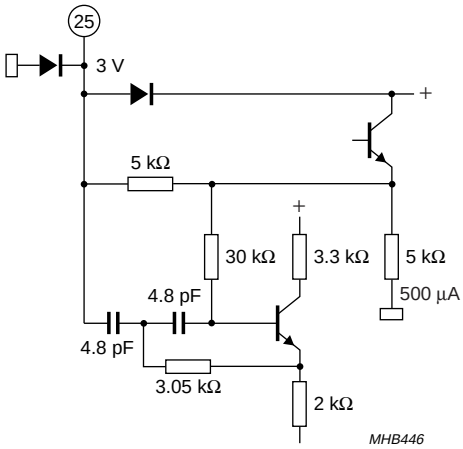


Fig.18 Pin 25; IFINT.

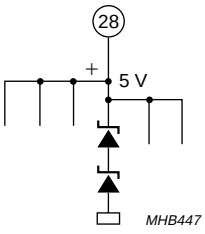


Fig.19 Pin 28; V_{CC}.

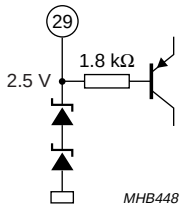


Fig.20 Pin 29; SCL.

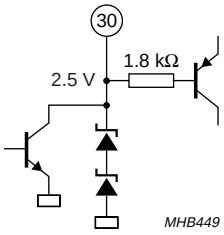


Fig.21 Pin 30; SDA.

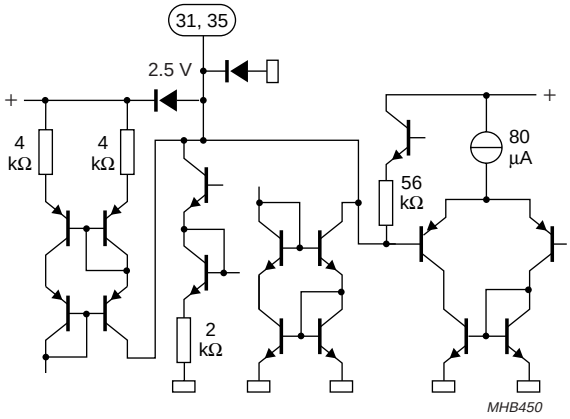


Fig.22 Pin 31; LPF and pin 35; CID.

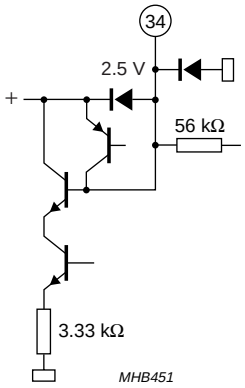


Fig.23 Pin 34; CTRIG.

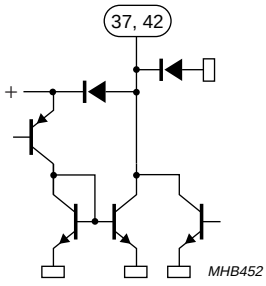


Fig.24 Pin 37; P1 and pin 42; P2.

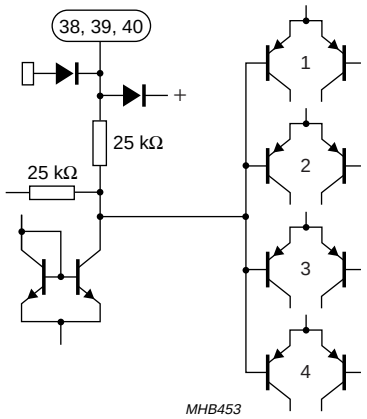


Fig.25 Pin 38; EXTM; pin 39; EXTR and pin 40; EXTL.

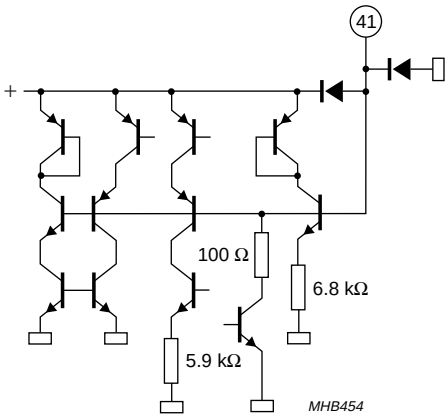


Fig.26 Pin 41; V_{ref}.

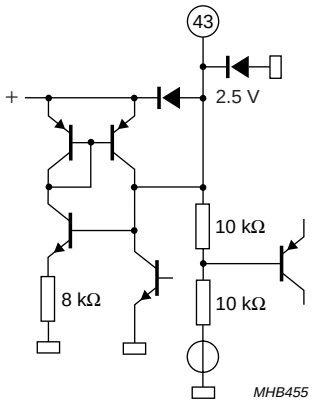
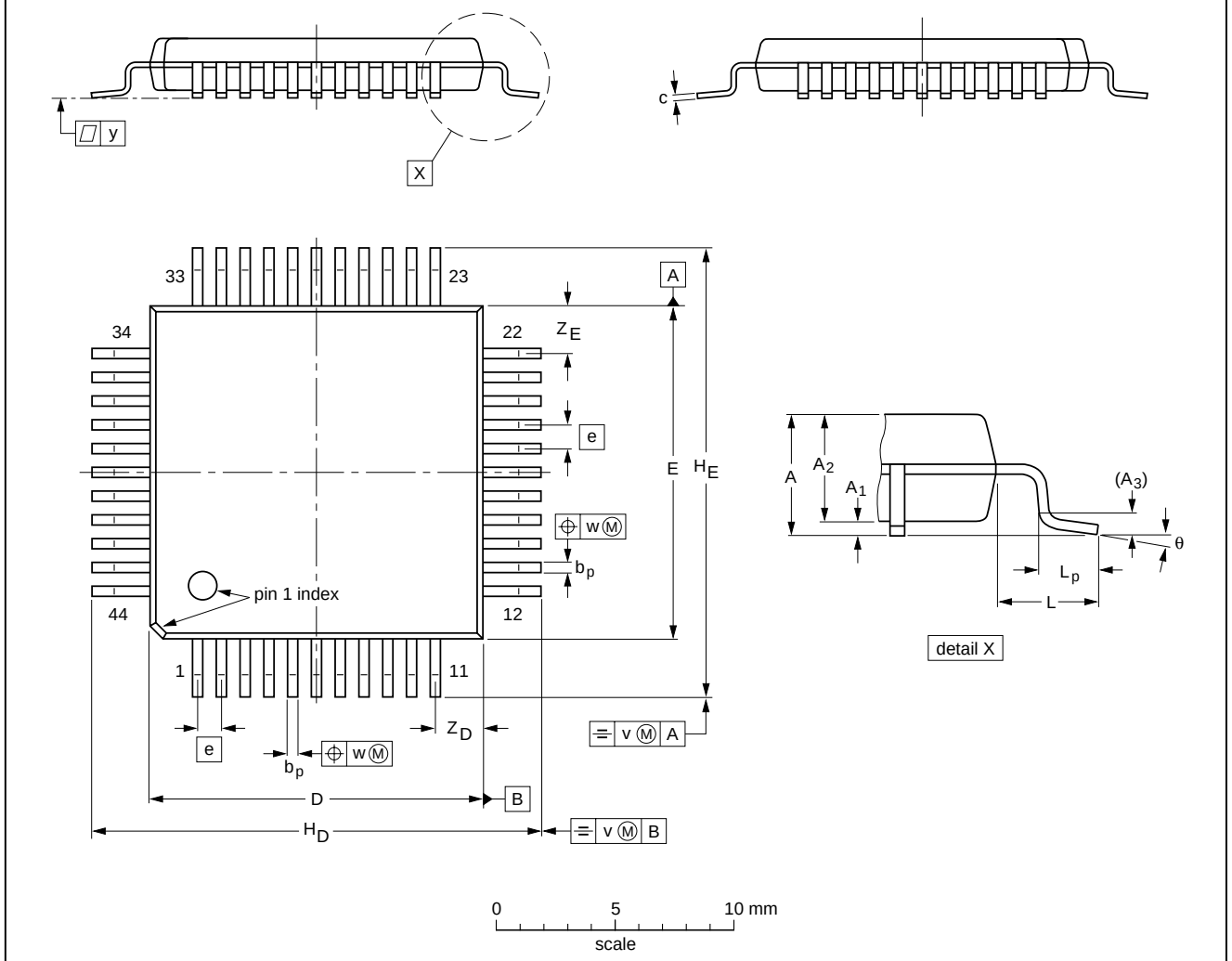


Fig.27 Pin 43; OUTM.

PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 x 14 x 2.2 mm **SOT205-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.60	0.25 0.05	2.3 2.1	0.25	0.50 0.35	0.25 0.14	14.1 13.9	14.1 13.9	1	19.2 18.2	19.2 18.2	2.35	2.0 1.2	0.3	0.15	0.1	2.4 1.8	2.4 1.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT205-1	133E01A					~~95-02-04~~ 97-08-01

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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