DATA SHEET

TDA933xH series
I²C-bus controlled TV display processors

Preliminary specification
File under Integrated Circuits, IC02

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I²C-bus controlled TV display processors TDA933xH series

FEATURES

Available in all ICs:

- Can be used in both single scan (50 or 60 Hz) and double scan (100 or 120 Hz) applications
- A Y, U and V inputs and a linear RGB input with fast blanking
- A separate OSD/text input with a fast blanking or blending option
- Black stretching of non-standard luminance signals
- Switchable matrix for the colour difference signals
- RGB control circuit with Continuous Cathode Calibration (CCC) and white point adjustment
- Blue stretch circuit which offsets colours near white towards blue
- Internal clock generation for the deflection processing which is synchronized by means of a 12 MHz ceramic resonator oscillator
- Horizontal synchronization with two control loops and alignment-free horizontal oscillator
- Soft start and soft stop of the horizontal drive pulses
- Low-power start-up option for the horizontal drive circuit
- Vertical count-down circuit
- Vertical driver optimized for DC-coupled vertical output stages
- Vertical and horizontal geometry processing
- Horizontal and vertical zoom possibility and vertical scroll function for 16 : 9 applications
- I²C-bus control of various functions
- Low dissipation.

GENERAL DESCRIPTION

The TDA933xH series are display processors for 'High-end' television receivers which contain the following functions:

- RGB control processor with a Y, U and V inputs, a linear RGB input for SCART or VGA signals with fast blanking, a linear RGB input for OSD and text signals with a fast blanking or blending option and an RGB output stage with black current stabilization which is realized with the continuous cathode calibration (2-point black current measurement) system.
- Programmable deflection processor with internal clock generation which generates the drive signals for the horizontal, east-west and vertical deflection. The circuit has various features which are attractive for the application of 16 : 9 picture tubes.
- The circuit can be used in both single scan (50 or 60 Hz) and double scan (100 or 120 Hz) applications.

In addition to these functions the TDA9331H and TDA9332H have a multi-sync function for the horizontal PLL, with a frequency range from 30 to 50 kHz ($2f_H$ mode) or 15 to 25 kHz ($1f_H$ mode), so that the IC can also be used to display signals with different line frequencies.

The supply voltage of the ICs is 8 V. They are contained in a 44-pin QFP package.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9330H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2
TDA9331H			
TDA9332H			

SURVEY OF IC TYPES

IC VERSION	VGA MODE	DAC OUTPUT
TDA9330H	no	I²C-bus controlled
TDA9331H	yes	proportional to VGA frequency
TDA9332H	yes	I²C-bus controlled

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Supply					
V_P	supply voltage	–	8.0	–	V
I_P	supply current (pins 17 and 39)	–	50	–	mA
Input voltages					
$V_{i(Y)(b\text{-}w)}$	luminance input signal (black-to-white value)	–	1.0/0.315	–	V
$V_{i(U)(p\text{-}p)}$	U input signal (peak-to-peak value)	–	1.33	–	V
$V_{i(V)(p\text{-}p)}$	V input signal (peak-to-peak value)	–	1.05	–	V
$V_{i(RGB)(b\text{-}w)}$	RGB input signal (black-to-white value)	–	0.7	–	V
$V_{i(Hsync)}$	horizontal sync input (H_D)	–	TTL	–	V
$V_{i(Vsync)}$	vertical sync input (V_D)	–	TTL	–	V
$V_{i(IIC)}$	I²C-bus inputs (SDA and SCL)	–	CMOS 5 V	–	V
Output signals					
$V_{o(RGB)(b\text{-}w)}$	RGB output signal amplitude (black-to-white value)	–	2.0	–	V
$I_{o(hor)}$	horizontal output current	–	–	10	mA
$I_{o(ver)(p\text{-}p)}$	vertical output current (peak-to-peak value)	–	1	–	mA
$I_{o(EW)}$	E-W drive output current	–	–	1.2	mA

BLOCK DIAGRAM

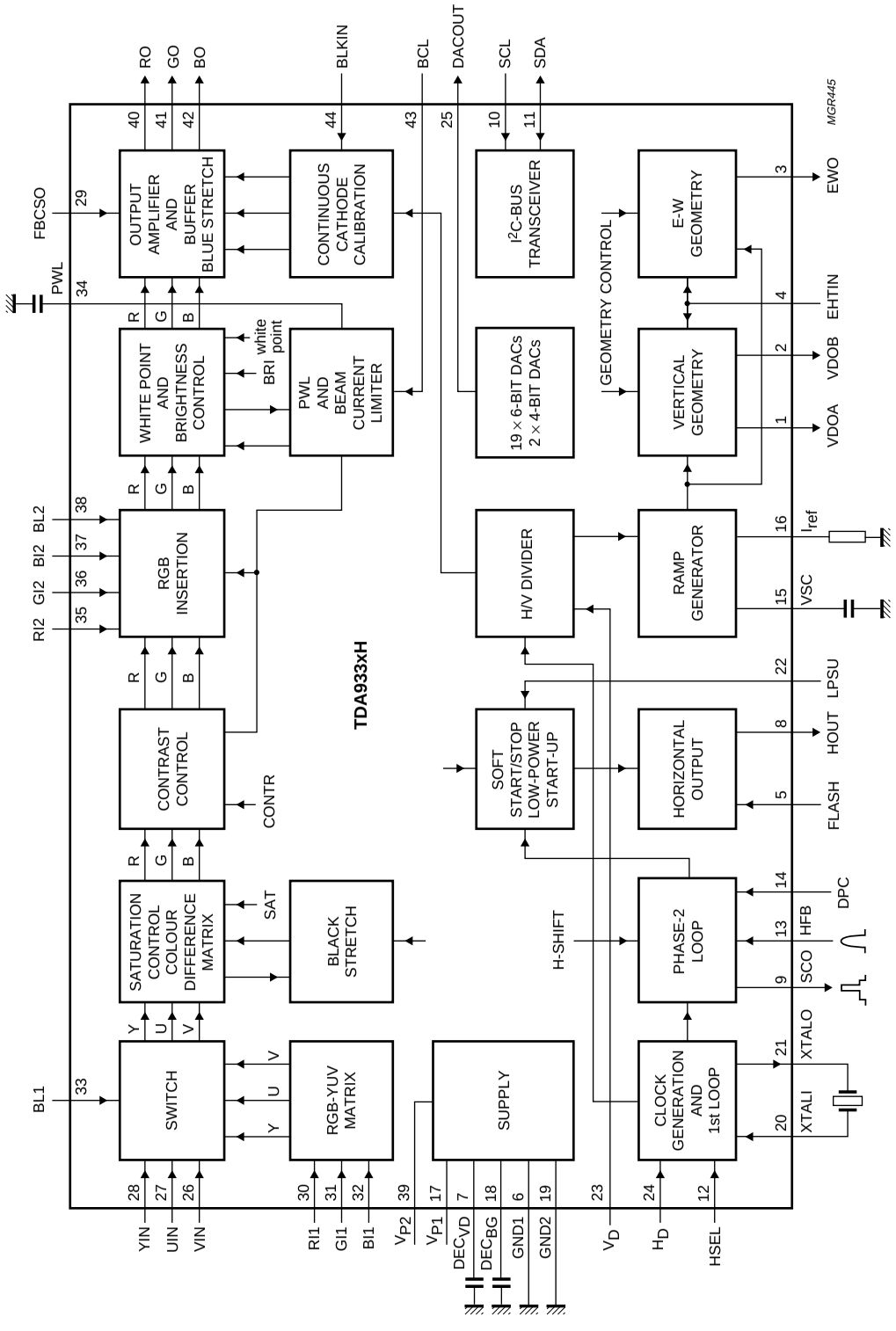


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
VDOA	1	vertical drive output A
VDOB	2	vertical drive output B
EWO	3	E-W output
EHTIN	4	EHT compensation input
FLASH	5	flash detection input
GND1	6	ground 1
DEC_{VD}	7	digital supply decoupling
HOUT	8	horizontal output
SCO	9	sandcastle pulse output
SCL	10	serial clock input
SDA	11	serial data input/output
HSEL	12	selection of horizontal frequency
HFB	13	horizontal flyback pulse input
DPC	14	dynamic phase compensation
VSC	15	vertical sawtooth capacitor
I_{ref}	16	reference current input
V_{P1}	17	positive supply 1 (+8 V)
DEC_{BG}	18	band gap decoupling
GND2	19	ground 2
XTALI	20	crystal input
XTALO	21	crystal output
LPSU	22	low-power start-up supply
V_D	23	vertical sync input
H_D	24	horizontal sync input
DACOUT	25	DAC output
VIN	26	V-signal input
UIN	27	U-signal input
YIN	28	luminance input
FBCSO	29	fixed beam current switch-off input
RI1	30	red 1 input for insertion
GI1	31	green 1 input for insertion
BI1	32	blue 1 input for insertion
BL1	33	fast blanking input for RGB-1
PWL	34	peak white limiting decoupling
RI2	35	red 2 input for insertion
GI2	36	green 2 input for insertion
BI2	37	blue 2 input for insertion
BL2	38	fast blanking/blending input for RGB-2
V_{P2}	39	positive supply 2 (+8 V)
RO	40	red output

SYMBOL	PIN	DESCRIPTION
GO	41	green output
BO	42	blue output
BCL	43	beam current limiting input
BLKIN	44	black current input

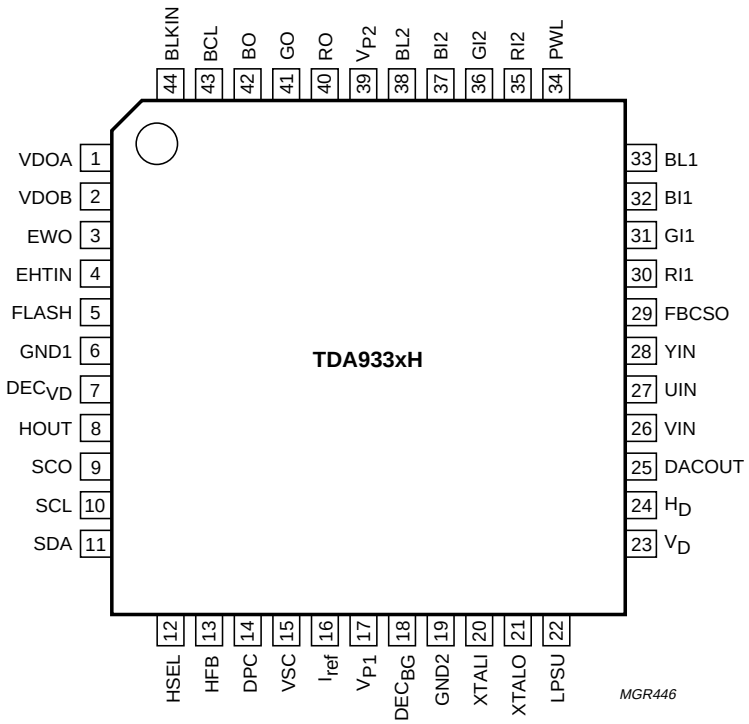


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

RGB control circuit

INPUT SIGNALS

The RGB control circuit of the TDA933xH contains 3 sets of input signals:

- YUV input signals which are supplied by the input processor or the feature box. By means of the GAI bit the luminance input signal sensitivity can be switched between 0.45 V (p-p) and 1.0 V (b-w). The nominal input signals for U and V are 1.33 V (p-p) and 1.05 V (p-p) respectively. These input signals are controlled on contrast, saturation and brightness.
- The first RGB input is intended for external (SCART in $1f_H$ and VGA in $2f_H$ applications) signals and which have an amplitude of 0.7 V (p-p) typical. This input is also controlled on contrast, saturation and brightness.
- The second RGB input is intended for OSD and teletext signals. The required input signals have an amplitude of 0.7 V (p-p). The switching between the internal signal and the OSD signal can be realized via a blending function or via fast blanking. This input is only controlled on brightness.

Switching between the various sources can be realized via the I²C-bus and by fast insertion switches. The fast insertion switches can be enabled via the I²C-bus.

The circuit contains switchable matrix circuits for the colour difference signals so that the colour reproduction can be adapted for PAL/SECAM and NTSC. For NTSC 2 different matrices can be chosen.

OUTPUT AMPLIFIER

The output signal has an amplitude of approximately 2 V (b-w) at nominal input signals and nominal settings of the controls. The required ‘white point setting’ of the picture tube can be realized by means of 3 separate gain settings for the RGB channels.

To obtain an accurate biasing of the picture tube a continuous cathode calibration circuit has been developed. This function is realized by means of a 2-point black level stabilization circuit.

By inserting 2 test levels for each gun and comparing the resulting cathode currents with 2 different reference currents the influence of the picture tube parameters such as the spread in cut-off voltage can be eliminated.

This 2-point stabilization is based on the principle that the ratio between the cathode currents is coupled to the ratio between the drive voltages according to: $\frac{I_{k1}}{I_{k2}} = \left(\frac{V_{dr1}}{V_{dr1}}\right)^{\gamma}$

The feedback loop makes the ratio between the cathode currents I_{k1} and I_{k2} equal to the ratio between the reference currents (which are internally fixed) by changing the (black) level and the amplitude of the RGB output signals via 2 converging loops. The system operates in such a way that the black level of the drive signal is controlled to the cut-off point of the gun so that a very good grey scale tracking is obtained. The accuracy of the adjustment of the black level is only dependent on the ratio of internal currents and these can be made very accurately in integrated circuits. An additional advantage of the 2-point measurement is that the control system makes the absolute value of I_{k1} and I_{k2} identical to the internal reference currents. Because this adjustment is obtained by adapting the gain of the RGB control stage this control stabilizes the gain of the complete channel (RGB output stage and cathode characteristic). As a result variations in the gain figures during life will be compensated for by this 2-point loop.

An important property of the 2-point stabilization is that the offset as well as the gain of the RGB path is adjusted by the feedback loop. Hence the maximum drive voltage for the cathode is fixed by the relationship between the test pulses, the reference current and the relative gain setting of the 3 channels. Consequently, the drive level of the CRT cannot be adjusted by adapting the gain of the RGB output stage. Because different picture tubes may require different drive levels the typical ‘cathode drive level’ amplitude can be adjusted by means of an I²C-bus setting. Depending on the selected cathode drive level the typical gain of the RGB output stages can be fixed taking into account the drive capability of the RGB outputs (pins 40 to 42). More details about the design will be given in the application report (see also Chapter “Characteristics”; note 10).

The measurement of the high and the low current of the 2-point stabilization circuit is performed in 2 consecutive fields. The leakage current is measured in each field. The maximum allowable leakage current is 100 μA.

When the TV receiver is switched on the black current stabilization circuit is directly activated and the RGB outputs are blanked. The blanking is switched off as soon as the loop has stabilized (e.g. the first time that the BCF bit changes from logic 1 to logic 0, see also Chapter “Characteristics”; note 13). This ensures that the switch-on time is reduced to a minimum and is only dependent on the warm-up time of the picture tube.

The black current stabilization system checks the output level of the 3 channels and indicates whether the black level of the lowest RGB output of the IC is in a certain window (WBC bit) or below or above this window (HBC bit). This indication can be read from the I²C-bus and can be used for automatic adjustment of the V_{g2} voltage during the production of the TV receiver.

When a failure occurs in the black current loop (e.g. due to an open-circuit) the BCF status bit is set. This information can be used to blank the picture tube to avoid damage to the screen.

The control circuit contains a beam current limiting circuit and a peak white limiting circuit. The peak white level is adjustable via the I²C-bus. To prevent the peak white limiting circuit reacting on the high frequency content of the video signal a low-pass filter is inserted in front of the peak detector. The capacitor of the low-pass filter is connected externally so that the set maker can adapt the time constant to his wishes. The circuit also contains a soft clipper which prevents the high frequency peaks in the output signal becoming too high. The difference between the peak white limiting level and the soft clipping level is adjustable via the I²C-bus in a few steps.

The vertical blanking is adapted to the vertical frequency of the incoming signal (50 or 100 Hz or, 60 or 120 Hz). When the flyback time of the vertical output stage is greater than the 60 Hz blanking time the blanking can be increased to the same value as that of the 50 Hz blanking. This can be set by means of the LBM bit.

It is possible to insert a blue background when no video is available. This feature can be activated via the EBB bit.

Synchronization and deflection processing

Horizontal synchronization and drive circuit

The horizontal drive signal is obtained from an internal VCO which runs at a frequency of 13.75 MHz. This oscillator is stabilized to this frequency by means of a resonator oscillator which needs an external ceramic resonator (frequency of 12 MHz) as a reference.

It is also possible to supply an external reference signal to the IC (in that event the external resonator should be removed).

The internal VCO is synchronized to the incoming horizontal H_D pulse (applied from the feature box or the input processor) by means of a PLL with an internal time constant. The choice of frequency of the horizontal drive signal ($1f_H$ or $2f_H$) is realized by means of a switching pin which must be connected to ground or left open-circuit.

Because of safety reasons the switching between $1f_H$ and $2f_H$ is possible only when the IC is in the standby mode.

For the TDA9331H and TDA9332H it is also possible to set the horizontal PLL in a ‘multi-sync’ mode. In that condition the circuit detects the frequency of the incoming sync pulses and adjusts the centre frequency of the VCO accordingly. The frequency range in this mode is 30 to 50 kHz at the output.

The horizontal drive signal is generated by a second control loop which compares the phase of the reference signal, applied from the internal VCO, with the flyback pulse. The time constant of this loop is set internally. The IC has a dynamic horizontal phase correction input which can be used to compensate phase shifts which are caused by beam current variations. Additional settings of the horizontal deflection, which are realized via the second loop, are the horizontal shift and a parallelogram correction. The adjustments are realized via the I²C-bus. When no horizontal flyback pulse is detected during three consecutive line periods the NHF status bit is set (output status byte 01-D3; see Table 3).

The horizontal drive signal is switched on and off via the so called soft-start/soft-stop procedure. This function is realized by means of a variation of the t_{on} of the horizontal drive pulse. For EHT generators without a bleeder the IC can be set in a ‘fixed beam current mode’ via the FBC bit. In that event the picture tube capacitance is discharged with a current of approximately 1 mA. The magnitude of the discharge current is controlled via the black current feedback loop. If necessary the discharge current can be enlarged with the help of an external current division circuit. With the fixed beam current option activated it is still possible to have a black screen during switch-off. This can be realized by placing the vertical deflection in an overscan position. This mode is activated via the OSO bit.

An additional function of the IC is the ‘low-power start-up’ feature. This mode is activated when a supply voltage of 5 V is supplied to the start-up pin.

The required current for this function is 3 mA (typ.). In this condition the horizontal drive signal has the nominal t_{off} and the t_{on} grows gradually from zero to approximately 30% of the nominal value. This results in a line frequency of approximately 50 kHz ($2f_H$) or 25 kHz ($1f_H$).

The output signal remains unchanged until the main supply voltage is switched on and the I²C-bus data has been received. The horizontal drive will then gradually change to the nominal frequency and duty cycle via the soft-start procedure. The IC can only be switched on and to standby mode when both standby bits (STB0 and STB1) are changed. The circuit will not react when only one bit changes its polarity.

The IC has a general purpose bus controlled DAC output with a resolution of 6 bits and with an output voltage range between 0.2 to 4 V. In the TDA9331H the DC voltage on this output is proportional to the horizontal line frequency (only in VGA mode). This voltage can be used to control the supply voltage of the horizontal deflection stage, to maintain constant picture width for higher line frequencies.

VERTICAL DEFLECTION AND GEOMETRY CONTROL

The drive signals for the vertical and E-W deflection circuits are generated by a vertical divider which derives its clock signal from the line oscillator. The divider is synchronized by the incoming V_D pulse, generated by the input processor or the feature box. The vertical ramp generator requires an external resistor and capacitor; the tolerances for these components must be small. In the normal mode the vertical deflection is operating in constant slope and adapts its amplitude depending on the frequency of the incoming signal (50 or 60 Hz or, 100 or 120 Hz). When the TDA933xH is switched to the VGA mode the amplitude of the vertical scan is stabilized and independent of the incoming vertical frequency. In this mode the E-W drive amplitude is proportional to the horizontal frequency so that the correction on the screen is not affected.

The vertical drive is realized by a differential output current. The outputs must be DC-coupled to the vertical output stage (e.g. TDA8354). The vertical geometry can be adjusted via the I²C-bus. Controls are possible for the following parameters:

- Vertical amplitude
- S-correction
- Vertical slope
- Vertical shift (only for compensation of offsets in output stage or picture tube)
- Vertical zoom
- Vertical scroll (shifting of the picture in vertical direction when the vertical scan is expanded)
- Vertical wait, an adjustable delay for the start of the vertical scan.

Regarding the vertical wait the following conditions are valid:

- In the $1f_H$ TV mode the start of the vertical scan is fixed and cannot be adjusted with the vertical wait
- In the $2f_H$ TV mode the start of the vertical scan depends on the value of the Vertical Scan Reference (VSR) bus bit. If VSR = 0 the start of the vertical scan is related to the falling edge of the incoming V_D pulse. If VSR = 1 it is related to the rising edge. In both cases the start of the scan can be adjusted with the vertical wait setting.
- In the multi-sync mode (TDA9331H and TDA9332H both in $1f_H$ mode and $2f_H$ mode) the start of the vertical scan is related to the rising edge of the incoming V_D pulse and can be adjusted with the vertical wait setting.

The minimum value for the vertical wait setting is 8 line periods. If the setting is lower than 8 the wait period will remain at 8 line periods.

The East-West (E-W) drive circuit has a single-ended output. The E-W geometry can be adjusted on the following parameters:

- Horizontal width with increased range because of the ‘zoom’ feature
- E-W parabola/width
- E-W corner parabola
- E-W trapezium.

The IC has an EHT compensation input which controls both the vertical and the E-W output signal. The relative control effect on both functions can be adjusted via the I²C-bus (sensitivity of vertical correction is fixed; E-W correction variable).

To avoid damage to the picture tube in the event of missing or malfunctioning vertical deflection, a vertical guard function is available at the sandcastle pin (pin SCO). The vertical guard pulse from the vertical output stage (TDA835x) should be connected to the sandcastle pin which acts as a current sense input. If the guard pulse is missing or lasts too long the NDF bit is set in the status register and the RGB outputs are blanked. If the guard function is disabled via the EVG bit only the NDF status bit is set.

The IC also has inputs for flash and overvoltage protection. More details about these functions are given in Chapter “Characteristics”; note 40.

I²C-BUS SPECIFICATION

The slave address of the IC is given in Table 1. The circuit operates up to clock frequencies of 400 kHz.

Table 1 Slave address (8C)

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	1	1	0	1/0

Valid subaddresses: 00 to 1A, subaddress FE is reserved for test purposes. Auto-increment mode available for subaddresses.

Table 2 Input control bits

FUNCTION	SUBADDRESS (HEX)	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
RGB processing-1	00	MAT	EBB	SBL	RBL	BLS	BKS	IE1	IE2
RGB processing-2	01	MUS	FBC	OBL	AKB	CL3	CL2	CL1	CL0
Wide horizontal blanking	02	HBL	0	GAI	STB0	HB3	HB2	HB1	HB0
Horizontal deflection	03	0	VSR	FAST	STB1	POC	PRD	VGA	ESS
Vertical deflection	04	0	VFF	LBM	DIP	OSO	SVF	EVG	DL
Brightness	05	0	0	A5	A4	A3	A2	A1	A0
Saturation	06	0	0	A5	A4	A3	A2	A1	A0
Contrast	07	0	0	A5	A4	A3	A2	A1	A0
White point R	08	0	0	A5	A4	A3	A2	A1	A0
White point G	09	0	0	A5	A4	A3	A2	A1	A0
White point B	0A	0	0	A5	A4	A3	A2	A1	A0
Peak white limiting	0B	0	0	SC1	SC0	A3	A2	A1	A0
Horizontal shift	0C	0	0	A5	A4	A3	A2	A1	A0
Horizontal parallelogram	0D	0	0	A5	A4	A3	A2	A1	A0
E-W width	0E	0	0	A5	A4	A3	A2	A1	A0
E-W parabola/width	0F	0	0	A5	A4	A3	A2	A1	A0
E-W corner/parabola	10	0	0	A5	A4	A3	A2	A1	A0
E-W trapezium	11	0	0	A5	A4	A3	A2	A1	A0
E-W EHT compensation sensitivity	12	0	0	A5	A4	A3	A2	A1	A0
Vertical slope	13	0	0	A5	A4	A3	A2	A1	A0
Vertical amplitude	14	0	0	A5	A4	A3	A2	A1	A0
S-correction	15	0	0	A5	A4	A3	A2	A1	A0
Vertical shift	16	0	0	A5	A4	A3	A2	A1	A0
Vertical zoom	17	0	0	A5	A4	A3	A2	A1	A0
Vertical scroll	18	0	0	A5	A4	A3	A2	A1	A0
Vertical wait	19	0	0	0	A4	A3	A2	A1	A0
DAC output[1]	1A	0	0	A5	A4	A3	A2	A1	A0

Note

1. See Chapter “Characteristics”; note 44.

Table 3 Output status bits

FUNCTION	SUBADDRESS (HEX)	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Output status bytes	00	POR	FSI	SL	XPR	NDF	IN1	IN2	WBC
	01	ID3	ID2	ID1	ID0	NHF	BCF	FLS	NRF
	02	X	X	X	X	X	X	X	HBC

Input control bits

Table 4 PAL SECAM/NTSC matrix

MAT	MATRIX POSITION
0	PAL matrix
1	NTSC matrix

Table 5 NTSC matrix

MUS	MATRIX POSITION
0	Japanese matrix
1	USA matrix

Table 6 Enable ‘blue-back’

EBB	MODE
0	blue back switched off
1	blue back switched on

Table 7 Service blanking

SBL	SERVICE BLANKING MODE
0	off
1	on

Table 8 RGB blanking

RBL	RGB BLANKING
0	not active
1	active

Table 9 Blue stretch

BLS	BLUE STRETCH MODE
0	off
1	on

Table 10 Black stretch

BKS	BLACK STRETCH MODE
0	off
1	on

Table 11 Enable fast blanking RGB-1

IE1	FAST BLANKING
0	not active
1	active

Table 12 Enable fast blanking RGB-2

IE2	FAST BLANKING
0	not active
1	active

Table 13 Fixed beam current switch-off

FBC	MODE
0	switch-off with blanked RGB outputs
1	switch-off with fixed beam current

Table 14 Blending function on OSD; note 1

OBL	MODE
0	OSD via fast blanking
1	OSD via blending function

Note

1. When the OBL bit is set to logic 1 the blending function is always activated, independent of the setting of the IE2 bit.

Table 15 Black current stabilization

AKB	MODE
0	active
1	not active

Table 16 Cathode drive level (15 steps; 3 V/step)

CL3	CL2	CL1	CL0	SETTING CATHODE DRIVE AMPLITUDE(1)
0	0	0	0	50 V (b-w)
1	0	0	0	74 V (b-w)
1	1	1	1	95 V (b-w)

Note

1. The given values are valid for the following conditions:
   a) Nominal CVBS input signal.
   b) Settings for contrast and white point nominal.
   c) Black and blue stretch switched off.
   d) Gain of output stage such that no clipping occurs.
   e) Beam current limiting not active.
   f) The tolerance on these values is approximately ±3 V.

Table 17 RGB blanking mode

HBL	MODE
0	normal blanking (horizontal flyback)
1	wide blanking

Table 18 Gain of luminance channel

GAI	MODE
0	normal gain [V_{28} = 1 V (b-w)]
1	high gain [V_{28} = 0.45 V (p-p)]

Table 19 Standby

STB0	STB1	CONDITION
0	0	horizontal drive off
0	1	no action
1	0	no action
1	1	horizontal drive on

Table 20 Timing wide blanking (15 steps; $1f_H$ mode 0.29 µs/step; $2f_H$ mode 0.145 µs/step)

HB3	HB2	HB1	HB0	TIMING OF BLANKING	
				$1f_H$ MODE	$2f_H$ MODE
0	0	0	0	–2.03 µs	–1.015 µs
0	1	1	1	0 µs	0 µs
1	1	1	–	2.03 µs	1.015 µs

Table 21 Vertical scan reference in $2f_H$ TV mode

VSR	VERTICAL SCAN REFERENCE
0	falling edge of V_D pulse
1	rising edge of V_D pulse

Table 22 Time constant of first control loop

FAST	TIME CONSTANT
0	normal, see specification
1	increased with 30%

Table 23 Synchronization mode

POC	MODE
0	synchronization active
1	synchronization not active

Table 24 Overvoltage input mode

PRD	OVERVOLTAGE MODE
0	detection mode
1	protection mode

Table 25 Multi-sync mode

VGA	MODE
0	horizontal frequency fixed by internal reference
1	multi-sync function switched on

Table 26 Extended soft start mode

ESS	EXTENDED SOFT START MODE
0	not active
1	active

Table 27 Long blanking mode

LBM	BLANKING MODE
0	adapted to standard (50 or 60 Hz)
1	fixed in accordance with 50 Hz standard

Table 28 Vertical free running frequency in TV mode

VFF	FREQUENCY
0	50 Hz (SVF = 0) or 100 Hz (SVF = 1)
1	60 Hz (SVF = 0) or 120 Hz (SVF = 1)

Table 29 De-interlace phase

DIP	PHASE
0	delay of 1st field (start of synchronized V_D pulse coincides with H-flyback) with 0.5 H
1	delay of 2nd field with 0.5 H

Table 30 Switch-off in vertical overscan

OSO	MODE
0	switch-off undefined
1	switch-off in vertical overscan

Table 31 Select vertical frequency

SVF	MODE
0	vertical frequency is 50 or 60 Hz
1	vertical frequency is 100 or 120 Hz

Table 32 Enable vertical guard (RGB blanking)

EVG	VERTICAL GUARD MODE
0	not active
1	active

Table 33 Interlace

DL	STATUS
0	interlace
1	de-interlace

Table 34 Soft clipping level

SC1	SC0	VOLTAGE DIFFERENCE BETWEEN SOFT CLIPPING AND PWL
0	0	0% above PWL level
0	1	5% above PWL level
1	0	10% above PWL level
1	1	soft clipping off

Output status bits

Table 35 Power-on reset

POR	MODE
0	normal
1	power-down

Table 36 Field frequency indication

FSI	FREQUENCY
0	50 or 100 Hz
1	60 or 120 Hz

Table 37 Phase 1 (φ_1) lock indication

SL	INDICATION
0	not locked
1	locked

Table 38 X-ray protection

XPR	OVERVOLTAGE
0	no overvoltage detected
1	overvoltage detected

Table 39 Output of vertical guard

NDF	VERTICAL OUTPUT STAGE
0	OK
1	failure

Table 40 Indication of RGB-1 insertion

IN1	RGB INSERTION
0	no
1	yes

Table 41 Indication of RGB-2 insertion

IN2	RGB INSERTION
0	no
1	yes

Table 42 Indication of output black level input/output V_{g2} alignment window

WBC	CONDITION(1)
0	black current stabilization outside window
1	black current stabilization inside window

Note

1. See Chapter “Characteristics”; note 14.

Table 43 IC identification

ID3	ID2	ID1	ID0	IC VERSION
0	0	0	0	TDA9330H
0	0	0	1	TDA9332H
0	0	1	1	TDA9331H

Table 44 Condition of horizontal flyback

NHF	CONDITION
0	flyback pulse present
1	flyback pulse not present

Table 45 Indication of failure in black current circuit

BCF	CONDITION
0	normal operation
1	failure in black current stabilization circuit

Table 46 Indication of flash detection

FLS	CONDITION
0	no flash-over detected
1	flash-over detected

Table 47 Locking of reference oscillator to crystal oscillator

NRF	CONDITION
0	reference oscillator is locked
1	reference oscillator is not locked

Table 48 Indication of output black level below or above the middle of V_{g2} alignment window

HBC	CONDITION(1)
0	black current stabilization below window
1	black current stabilization above window

Note

1. See Chapter “Characteristics”; note 14.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		–	9.0	V
T_{stg}	storage temperature		–25	+150	°C
T_{amb}	operating ambient temperature		0	70	°C
T_{sol}	soldering temperature	for 5 s	–	260	°C
T_j	junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	60	K/W

QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611E-part E".*

ESD protection

All pins are protected against ESD by means of internal protection diodes, and meet the following specification:

- Human body model (R = 1.5 kΩ; C = 100 pF): all pins > ±3000 V
- Machine model (R = 0 Ω; C = 200 pF): all pins > ±300 V.

Latch-up performance

At an ambient temperature of 70 °C all pins meet the following specification:

- Positive stress test: $I_{trigger} \geq 100$ mA or $V_{pin} \geq 1.5 \times V_{CC(max)}$
- Negative stress test: $I_{trigger} \leq -100$ mA or $V_{pin} \leq -0.5 \times V_{CC(max)}$.

CHARACTERISTICS

V_P = 8 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
MAIN SUPPLY; PINS 17 AND 39						
V_{P1}	supply voltage		7.2	8.0	8.8	V
V_{POR}	power-on reset voltage level	note 1	5.8	6.1	6.5	V
I_{P1}	supply current	pin 17 plus pin 39	44	50	58	mA
		pin 17	–	22	–	mA
		pin 39	–	28	–	mA
P_{tot}	total power dissipation		–	400	–	mW
LOW-POWER START-UP; PIN 22						
V_{P2}	supply voltage	note 2	4.5	5.0	5.5	V
I_{P2}	supply current		–	3.0	4.5	mA
RGB control circuit						
LUMINANCE INPUT; PIN 28						
$V_{i(Y)(b\text{-}w)}$	luminance input voltage (black-to-white value)	GAI = 0	–	1.0	1.5	V
Z_i	input impedance		10	–	–	MΩ
C_i	input capacitance		–	–	5	pF
$I_{i(Y)(clamp)}$	input current during clamping		–25	0	+25	μA
U/V INPUTS; PINS 27 AND 26						
$V_{i(U)(p\text{-}p)}$	U input signal amplitude (peak-to-peak value)		–	1.33	2.0	V
$V_{i(V)(p\text{-}p)}$	V input signal amplitude (peak-to-peak value)		–	1.05	1.6	V
Z_i	input impedance		10	–	–	MΩ
C_i	input capacitance		–	–	5	pF
$I_{i(UV)(clamp)}$	input current during clamping		–20	0	+25	μA
RGB-1 INPUT (SCART/VGA); PINS 30 TO 32; note 3						
$V_{i(b\text{-}w)}$	input signal amplitude (black-to-white value)		–	0.7	1.0	V
ΔV_o	difference between black level of YUV and RGB-1 signals at the outputs		–	–	10	mV
$I_{i(clamp)}$	input current during clamping		–25	0	+25	μA
Δt_d	delay difference for the three channels	note 4	–	0	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FAST BLANKING INPUT (RGB-1); PIN 33						
$V_{i(BL1)}$	input voltage	no data insertion	0	–	0.45	V
		data insertion	0.9	–	3.0	V
Δt_d	delay difference between insertion to RGB out and RGB in to RGB out	data insertion; note 4	–	10	20	ns
$I_{i(BL1)}$	input current	source current; note 5	–	–0.12	–0.2	mA
SS_{int}	suppression of internal RGB signals	insertion; f_i = 0 to 10 MHz; notes 4 and 6	50	55	–	dB
SS_{ext}	suppression of external RGB signals	no insertion; f_i = 0 to 10 MHz; notes 4 and 6	50	55	–	dB
RGB-2 INPUT (OSD/TEXT); PINS 35 TO 37						
$V_{i(b\text{-}w)}$	input signal amplitude (black-to-white value)		–	0.7	1.0	V
ΔV_o	difference between black level of YUV/RGB-1 and RGB-2 signals at the outputs		–	–	10	mV
$I_{i(clamp)}$	input current during clamping		–40	0	+40	µA
Δt_d	delay difference for the three channels	note 4	–	0	–	ns
BLENDING (FAST BLANKING) INPUT (RGB-2); PIN 38; note 7						
Blending function (OBL = 1)						
$V_{i(BL2)(1)}$	input voltage	no data insertion	0	–	0.05	V
		50% insertion	0.69	0.725	0.76	V
		100% insertion	1.42	1.47	3.0	V
		active blending range	0.31	–	1.14	V
	percentage of data insertion	V_i = 0.31 V	0	1	4	%
		V_i = 0.725 V	45	50	55	%
		V_i = 1.14 V	96	99	100	%
		internal signal = 50%	48	50	52	%
$V_{i(max)}$	slope of blending curve	50% insertion	–	160	–	%/V
Fast blanking function (OBL = 0)						
$V_{i(BL2)(0)}$	input voltage	no data insertion	0	–	0.3	V
		data insertion	0.9	–	3.0	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
General						
Δt_d	delay difference between insertion to RGB out and RGB in to RGB out	data insertion; note 4	–	20	26	ns
$I_{i(BL2)}$	input current	source current; note 5	–	–1	–5	μA
SS_{int}	suppression of internal RGB signals	insertion; f_i = 0 to 10 MHz; notes 4 and 6	50	55	–	dB
SS_{ext}	suppression of external RGB signals	no insertion; f_i = 0 to 10 MHz; notes 4 and 6	50	55	–	dB
COLOUR DIFFERENCE MATRICES; note 3						
PAL/SECAM mode; the colour-difference matrix results in the following signals						
(R – Y)	(B – Y) signal: 2.03/0°			$2.03U_R$		
(B – Y)	(R – Y) signal: 1.14/90°			$1.14\ V_R$		
(B – Y)	(G – Y) signal: 0.70/236°			$-0.39U_R - 0.58V_R$		
NTSC mode; the colour-difference matrix results in the following signals						
MUS-bit = 0						
(B – Y)	(B – Y) signal: 2.03/0°			$2.03U_R$		
(R – Y)	(R – Y) signal: 1.59/95°			$-0.14U_R + 1.58V_R$		
(G – Y)	(G – Y) signal: 0.61/240°			$-0.31U_R - 0.53V_R$		
MUS-bit = 1						
(B – Y)	(B – Y) signal: 2.20/–1°			$2.20U_R - 0.04V_R$		
(R – Y)	(R – Y) signal: 1.53/99°			$-0.24U_R + 1.51V_R$		
(G – Y)	(G – Y) signal: 0.70/223°			$-0.51U_R - 0.48V_R$		
CONTROLS						
Saturation control; note 8						
CR_{sat}	saturation control range	63 steps; see Fig.5	52	–	–	dB
Contrast control; note 8						
CR_{contr}	contrast control range	63 steps; see Fig.6	–	20	–	dB
	tracking between the three channels over a control range of 10 dB		–	–	0.5	dB
Brightness control; note 8						
CR_{bri}	brightness control range	63 steps; see Fig.7	–	±1.0	–	V
BLACK LEVEL STRETCHER; note 9						
$\Delta V_{(bl)(max)}$	maximum black level shift	A-to-A; see Fig.8	15	21	27	IRE
$\Delta V_{(bl)}$	black level shift	at 100% peak white	–1	0	+1	IRE
		at 50% peak white	–1	–	+3	IRE
		at 15% peak white	6	8	10	IRE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RGB AMPLIFIER OUTPUTS: PINS 40 TO 42						
$V_{40-42(b-w)}$	output signal amplitude (black-to-white value)	at nominal luminance input signal, nominal contrast, nominal cathode drive level and white-point adjustment; note 10	–	2.0	–	V
V_o	output voltage range	note 10	1	–	$V_{CC} - 2$	V
Z_o	output impedance	note 11	–	120	150	Ω
I_{sink}	sink current	emitter follower output	–	2	–	mA
$V_{o(RED)(p-p)}$	output signal amplitude for the 'red' channel (peak-to-peak value)	at nominal settings for contrast and saturation control and no luminance signal to the input (R–Y, PAL); note 10	–	2.1	–	V
$V_{bl(nom)}$	nominal black level voltage		–	2.5	–	V
V_{bl}	black level voltage	when black level stabilization is switched off (via AKB bit)	–	2.5	–	V
$t_{W(blank)}$	width of video blanking pulse with HBL bit active	at $1f_H$; note 12	14.4	14.7	15.0	µs
		at $2f_H$; note 12	7.2	7.35	7.5	µs
CR_{bl}	control range of the black current stabilization	notes 13 and 14	–	±1	–	V
V_{blank}	blanking voltage level	difference with black level; note 10	–0.4	–0.5	–0.6	V
$V_{blank(leak)}$	blanking voltage level during leakage measurement		–	–0.1	–	V
$V_{blank(l)}$	blanking voltage level during low measuring pulse		–	0.25	–	V
$V_{blank(h)}$	blanking voltage level during high measuring pulse		–	0.38	–	V
$\Delta V_{(RGB)(mp)}$	adjustment range of the ratio between the amplitudes of the RGB drive voltage and the measuring pulses	note 10	–	±6	–	dB
$V_{bl(WBC)}$	black level at the output at which the WBC bit is set to logic 1	nominal value	2.4	2.5	2.6	V
		window; note 14	–	±100	–	mV
$\Delta bl/\Delta T$	variation of black level with temperature	note 4	–	1.0	–	mV/K

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔV_{bl}	relative variation in black level between the three channels during variations of	note 4				
	supply voltage (±10%)	nominal controls	–	–	20	mV
	saturation (50 dB)	nominal contrast	–	–	20	mV
	contrast (20 dB)	nominal saturation	–	–	20	mV
	brightness (±0.5 V)	nominal controls	–	–	20	mV
	temperature (range 40 °C)		–	–	20	mV
S/N	signal-to-noise ratio of the output signals	notes 4 and 15	60	–	–	dB
B_o	bandwidth of output signals	RGB-1 input; at –3 dB; note 11	14	16	–	MHz
		RGB-2 input; at –3 dB; note 11	16	18	–	MHz
		luminance input; at –3 dB; note 11	13	15	–	MHz
WHITE-POINT ADJUSTMENT						
	I²C-bus setting for nominal gain	HEX code	–	20H	–	
ΔG_{RGB}	adjustment range of RGB drive levels	CL control bits; see Table 16	±2.4	±2.8	±3.2	dB
ΔG_v	gain control range to compensate spreads in picture tube characteristics	white point controls	–	±3	–	dB
2-POINT BLACK CURRENT STABILIZATION; INPUT PIN 44; note 16						
$I_{ref(l)}$	amplitude of low reference current		–	8	–	µA
$I_{ref(h)}$	amplitude of high reference current		–	20	–	µA
I_L	acceptable leakage current		–	±100	–	µA
V_{Iref}	voltage on measurement pin	pin 44; loop closed	3.15	3.3	3.45	V
$I_{scan(max)}$	maximum current during scan	pin 44; loop open-circuit	–	note 16	–	
BEAM CURRENT LIMITING; INPUT PIN 43; note 17						
V_{bias}	internal bias voltage		3.5	3.6	3.7	V
V_{CR}	contrast reduction starting voltage		3.1	3.3	3.5	V
$V_{dif(CR)}$	voltage difference for full contrast reduction		2.0	2.2	2.4	V
V_{bri}	brightness reduction starting voltage		1.6	1.8	2.0	V
$V_{dif(BR)}$	voltage difference for full brightness reduction		–	1	–	V
$I_{ch(int)}$	internal charge current		1.5	2.0	2.5	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{dch(max)}$	maximum discharge current when the PWL is active		3.5	4.0	4.5	mA
PEAK WHITE LIMITER; note 17						
$I_{ch(PWL)}$	charge current PWL filter pin	pin 34; $1f_V$ mode	13	16	19	µA
		pin 34; $2f_V$ mode	26	32	38	µA
$I_{dch(PWL)}$	discharge current PWL filter pin	pin 34; $1f_V$ mode	52	64	76	µA
		pin 34; $2f_V$ mode	100	120	140	µA
$V_{i(Y)(b-w)}$	Y-input signal amplitude at which peak white limiter is activated (black-to-white value)	PWL range (15 steps); at maximum contrast	0.55	–	0.85	V
SOFT CLIPPER; note 18						
$\Delta G_{v(sc)}$	soft clipper gain reduction	maximum contrast; note 18; see Fig.11	–	15	–	dB
	deviation between soft clipper curve and ideal curve	C-to-C; percentage of black-to-white amplitude without clipping; note 4; see Fig.11	–	5	–	%
BLUE STRETCH; note 19						
ΔG_{RG}	decrease of small signal gain for red and green		–	17	–	%
FIXED BEAM CURRENT SWITCH-OFF; notes 20, 21 AND 22						
V_{FBCSO}	detection level		1	1.5	2	V
$V_{i(FBCSO)(max)}$	maximum input voltage		–	–	5.5	V
I_{dch}	discharge current when the fixed beam current function is activated	sink current pin 44; note 23	0.85	1.0	1.15	mA
t_{dch}	discharge time of picture tube		36	37	38	ms
Horizontal synchronization and deflection						
H_D INPUT SIGNAL; PIN 24						
V_{IL}	LOW-level of input voltage	note 24	–	–	0.8	V
V_{IH}	HIGH-level of input voltage	note 24	2.0	–	–	V
$I_{i(HD)}$	input current		–10	–	+10	µA
$t_{r(HD)}$	rise time		–	–	100	ns
$t_{f(HD)}$	fall time		–	–	100	ns
$t_{W(HD)}$	pulse width		1	–	–	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
INTERNAL REFERENCE SIGNAL; CRYSTAL OR RESONATOR CONNECTED TO PINS 20 AND 21; note 25						
f_{xtal}	resonator frequency		–	12	–	MHz
$R_{s(xtal)}$	resonator series resistance	C_L = 60 pF	–	–	30	Ω
$V_{i(stab)(p-p)}$	stabilized input signal (peak-to-peak value)		0.5	0.8	1.0	V
$g_{m(max)}$	maximum transconductance		4	5	–	mA/V
Z_i	input impedance		50	–	–	kΩ
C_i	input capacitance		–	–	10	pF
C_o	output capacitance		–	–	5	pF
EXTERNAL REFERENCE SIGNAL; INPUT PIN 20						
f_{XTALI}	input signal frequency		–	12	–	MHz
$V_{i(XTALI)(p-p)}$	input signal amplitude (peak-to-peak value)		2	–	5	V
FIRST CONTROL LOOP; note 26						
$f_{o(nom)}$	nominal output frequency	$1f_H$ mode; not locked	–	16.05	–	kHz
		$2f_H$ mode; not locked	–	32.1	–	kHz
Δf_{nom}	deviation of nominal frequency	not locked	–1	–	+1	%
$f_{h/cr}$	holding/catching range PLL	$1f_H$ mode; note 27	14.9	–	17.15	kHz
		$2f_H$ mode; note 27	29.8	–	34.3	kHz
Δt_{line}	maximum line time difference per line	$1f_H$ mode	–2	–	+2	µs
		$2f_H$ mode	–1	–	+1	µs
f_{contr}	frequency control range in multi-sync mode	$1f_H$ mode	15	–	25	kHz
		$2f_H$ mode	30	–	50	kHz
Δf_{corr}	maximum speed of frequency correction in multi-sync mode		–	–	100	kHz/s
V_{HSEL}	voltage on frequency select pin	$1f_H$ mode	0	–	1	V
		$2f_H$ mode, pin must be left open-circuit	4	5	5.5	V
SECOND CONTROL LOOP; PIN 14						
$\Delta\varphi_i/\Delta\varphi_o$	control sensitivity (loop gain)	$\Delta t_i/\Delta t_0$	500	–	–	µs/µs
k_{cor}	correction factor k	note 28	–	0.5	–	
t_{contr}	control range from start of horizontal output to mid flyback	$1f_H$ mode; note 29	0	–	23.6	µs
		$2f_H$ mode; note 29	0	–	11.8	µs
t_{shift}	horizontal shift range	$1f_H$ mode; 63 steps	–	±4.5	–	µs
$\Delta\varphi$	control sensitivity for dynamic phase compensation	$1f_H$ mode	–	0.4	–	µs/V
		$2f_H$ mode	–	0.2	–	µs/V
$V_{i(DP)(comp)}$	input voltage range for dynamic phase compensation	pin 14; note 30	1.5	4	6.5	V
Z_i	input impedance	pin 14; note 30		100		kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{par(cor)(max)}$	maximum range of the parallelogram correction	$1f_H$ mode, end of field, flyback width 11 µs; note 31	±0.48	±0.54	±0.60	µs
		$2f_H$ mode; end of field; flyback width 5.5 µs; note 31	±0.24	±0.27	±0.30	µs
$t_{H(shift)}$	horizontal shift range	$2f_H$ mode; 63 steps	–	±2.25	–	µs
HORIZONTAL FLYBACK INPUT; PIN 13						
$V_{sw(HBLNK)}$	switching level for horizontal blanking		0.2	0.3	0.4	V
$V_{sw(p2)}$	switching level for φ-2 loop		3.8	4.0	4.2	V
$V_{i(HFB)(max)}$	maximum input voltage		–	–	V_P	V
Z_i	input impedance		10	–	–	MΩ
HORIZONTAL OUTPUT; PIN 8, OPEN COLLECTOR; note 32						
V_{OL}	LOW-level output voltage	I_o = 10 mA	–	–	0.3	V
$I_{o(max)}$	maximum allowed output current		10	–	–	mA
$V_{o(max)}$	maximum allowed output voltage		–	–	V_P	V
δ	duty factor	V_o = LOW (t_{on})	51.6	51.8	52.0	%
t_{on}	switch-on time of horizontal drive pulse	note 32	152	156	160	ms
t_{off}	switch-off time of horizontal drive pulse	note 32	41	42	43	ms
$t_{on(ss)}$	switch-on time for extended soft start	note 32	1100	1150	1200	ms
Δt	jitter (σ)	$1f_H$ mode; note 33	–	1.4	–	ns
		$2f_H$ mode; note 33	–	1.0	–	ns
SANDCASTLE OUTPUT; PIN 9; note 34						
$V_{SCO(0)}$	zero level		0	0.5	1.0	V
I_{sink}	sink current		0.5	0.7	0.9	mA
$V_{o(SCO)}$	output voltage	during clamp pulse	4.2	4.5	4.8	V
		during blanking	2.3	2.5	2.7	V
I_{source}	source current		0.5	0.7	0.9	mA
$I_{i(grd)}$	guard pulse input current required to stop the blanking after a vertical blanking period	note 35	1.0	–	3.0	mA
$t_{W(1)}$	pulse width at $1f_H$	clamp pulse	3.3	3.5	3.7	µs
		vertical blanking (50 or 60 Hz)	–	22/17	–	lines
$t_{W(2)}$	pulse width at $2f_H$	clamp pulse	1.7	1.8	1.9	µs
		vertical blanking (100 or 120 Hz)	–	Fig.10	–	lines

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d(bk-HD)}$	delay of start of burst key to start of H_D pulse	$1f_H$ mode	5.2	5.4	5.6	µs
		$2f_H$ mode	2.6	2.7	2.8	µs
Vertical synchronization and geometry processing						
V_D INPUT SIGNAL; PIN 23						
V_{IL}	LOW-level of input voltage		–	–	0.8	V
V_{IH}	HIGH-level of input voltage		2.0	–	–	V
$I_{i(VD)}$	input current		–10	–	+10	µA
$t_{r(VD)}$	rise time		–	–	100	ns
$t_{f(VD)}$	fall time		–	–	100	ns
$t_{W(VD)}$	pulse width		1	–	–	line
VERTICAL DIVIDER AND RAMP GENERATOR; PINS 15 AND 16; note 36						
	number of lines per field (VGA mode is valid only for TDA9331H and TDA9332H)	$1f_H$ TV mode	244	–	511.5	lines
		$1f_H$ VGA mode	175	–	450	lines
		$2f_H$; $2f_V$; TV mode	244	–	511.5	lines
		$2f_H$; $1f_V$; TV mode	488	–	1023.5	lines
		$2f_H$ VGA mode	350	–	900	lines
	divider value when not locked (number of lines per field)	$1f_H$ or $2f_H$; $2f_V$; TV mode; VFF = 0	–	312.5	–	lines
		$1f_H$ or $2f_H$; $2f_V$; TV mode; VFF = 1	–	262.5	–	lines
		$2f_H$; $1f_V$; TV mode; VFF = 0	–	625	–	lines
		$2f_H$; $1f_V$; TV mode; VFF = 1	–	525	–	lines
		$1f_H$; VGA mode	–	288	–	lines
		$2f_H$; VGA mode	–	576	–	lines
$V_{saw(p-p)}$	sawtooth amplitude (peak-to-peak value)	VS = $1f_H$; C = 100 nF; R = 39 kΩ	–	3.0	–	V
I_{dch}	discharge current		–	1.2	–	mA
$I_{ch(ext)(R)}$	charge current set by external resistor	R = 39 kΩ; VS = $1f_H$; SVF = 0	–	16	–	µA
		R = 39 kΩ; VS = $1f_H$; SVF = 1	–	32	–	µA
V_{slope}	vertical slope	control range (63 steps)	–20	–	+20	%
ΔI_{ch}	charge current increase	60/50 Hz or 120/100 Hz	18.0	19.0	20.0	%
V_{rampL}	LOW-voltage level of ramp		–	2.3	–	V
VERTICAL DRIVE OUTPUTS; PINS 1 AND 2						
$I_{o(diff)(p-p)}$	differential output current (peak-to-peak value)	VA = $1f_H$	0.88	0.95	1.02	mA
I_{CM}	common mode current		360	400	440	µA
$V_{o(VDO)}$	output voltage range		0	–	4.0	V
	vertical linearity	upper/lower ratio; note 37	0.99	1.01	1.03	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DE-INTERLACE						
	first field delay	DIP = 0; note 38	–	0.5H	–	
E-W WIDTH; note 39						
CR	control range	63 steps	100	–	65	%
$I_{o(eq)}$	equivalent output current	VGA = 0; note 39	0	–	700	μA
$V_{o(EW)}$	E-W output voltage range		1.0	–	8.0	V
$I_{o(EW)}$	E-W output current range		0	–	1200	μA
E-W PARABOLA/WIDTH						
CR	control range	63 steps	0	–	22	%
$I_{o(eq)}$	equivalent output current	E-W = $3f_H$	0	–	440	μA
E-W CORNER/PARABOLA						
CR	control range	63 steps	–43	–	0	%
$I_{o(eq)}$	equivalent output current	PW = $3f_H$; E-W = $3f_H$	–190	–	0	μA
E-W TRAPEZIUM						
CR	control range	63 steps	–5	–	+5	%
$I_{o(eq)}$	equivalent output current		–100	–	+100	μA
E-W EHT TRACKING						
$V_{i(EHTIN)}$	input voltage		1.2	–	2.8	V
m_{scan}	scan modulation range		–7	–	+7	%
φ_{EW}	sensitivity	63 steps	0	–	9	%/V
VERTICAL AMPLITUDE						
CR	control range	63 steps; SC = 00H	80	–	120	%
$I_{o(eq)(diff)(p-p)}$	equivalent differential vertical drive output current (peak-to-peak value)	SC = 00H	760	–	1140	μA
VERTICAL SHIFT						
CR	control range	63 steps	–5	–	+5	%
$I_{o(eq)(diff)(p-p)}$	equivalent differential vertical drive output current (peak-to-peak value)		–50	–	+50	μA
S-CORRECTION						
CR	control range	63 steps	0	–	30	%
VERTICAL EHT TRACKING/OVERVOLTAGE PROTECTION						
V_i	input voltage		1.2	–	2.8	V
m_{scan}	scan modulation range		4.5	5	5.5	%
φ_{vert}	vertical sensitivity		5.7	6.3	6.9	%/V
$I_{o(eq)(EW)}$	EW equivalent output current		+100	–	–100	μA
$V_{ov(det)}$	overvoltage detection level	note 40	3.7	3.9	4.1	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VERTICAL ZOOM MODE (OUTPUT CURRENT VARIATION WITH RESPECT TO NOMINAL SCAN); note 41						
	vertical zoom factor	63 steps	0.75	–	1.38	
	output current limiting and RGB blanking		1.01	1.05	1.08	
VERTICAL SCROLL; note 42						
CR	control range (percentage of nominal picture amplitude)	63 steps	–18	–	+19	%
VERTICAL WAIT; note 43						
$t_{d(scan)}$	delay of start vertical scan	23 steps	8	–	31	lines
FLASH DETECTION INPUT; PIN 5; note 40						
$V_{i(FLASH)}$	input voltage range		0	–	V_P	V
$V_{FLASH(det)}$	voltage detection level		–	2	–	V
$V_{det(hys)}$	detection level hysteresis		–	0.2	–	V
$t_{W(FLASH)}$	pulse width		200	–	–	ns
I²C-bus control inputs/outputs; pins 10 and 11						
V_i	input voltage level		0	–	5.5	V
V_{IL}	LOW-level input voltage		–	–	1.5	V
V_{IH}	HIGH-level input voltage		3.5	–	–	V
I_{IL}	LOW-level input current	V_{IL} = 0 V	–	0	–	μA
I_{IH}	HIGH-level input current	V_{IH} = 5.5 V	–	0	–	μA
V_{OL}	LOW-level output voltage	SDA; I_{OL} = 6 mA	–	–	0.6	V
DAC OUTPUT; PIN 25; note 44						
$V_{o(min)}$	minimum output voltage		0.15	0.3	0.4	V
$V_{o(max)}$	maximum output voltage		3.7	4.0	4.3	
Z_o	output impedance	note 44	0.3	–	10	kΩ

Notes

1. The normal operation of the IC is guaranteed for a supply voltage range between 7.2 and 8.8 V. When the supply voltage drops below the power-on reset level the POR status bit is set and the horizontal output is switched off. When the supply voltage is between 7.2 V and the power-on reset level the horizontal frequency is kept in the specified holding range.
2. For the low power start-up mode a supply voltage of 5 V has to be supplied to pin 22. The current which is required for this function is limited to 3.0 mA (typ.). In this condition the horizontal drive signal has a frequency of approximately 50 kHz ($2f_H$) or 25 kHz ($1f_H$) with nominal t_{off} and with a t_{on} of approximately 30% of the nominal value. The start-up mode is continued as soon as the main supply voltage is switched on and the I²C-bus data has been received. When the main supply is present the 5 V supply on pin 22 can be removed. If low power start-up is not used pin 22 should be connected to ground.
3. The RGB to YUV matrix on the RGB-1 input is the inverse of the YUV to RGB matrix for PAL. For a one-to-one transfer from the RGB-1 input to the RGB output the PAL colour difference matrix should be selected (bus bit MAT = 0).
4. This parameter is not tested during production but is guaranteed by the design and qualified by means of matrix batches which are made in the pilot production period.

5. The inputs for RGB-1 and RGB-2 insertion (pins 33 and 38) both supply a small source current to the pins. If the pins are left open-circuit the input voltage will rise above the insertion switching level.
6. This parameter is measured at nominal settings of the various controls.
7. The switching of the OSD (RGB-2) input has 2 modes, the selection between the 2 modes can be made via the I²C-bus. The blending control curve is given in Fig.4. The blender input is optimized for the blender output of the SAA5800 (ArtistIC) i.e.
   a) Fast switching between the OSD signal and the internal RGB signals.
   b) Blending (fading) function between the OSD signal and the internal RGB signals.
8. The saturation, contrast and brightness control are active on the YUV signals and on the first RGB input signals. Nominal contrast is specified with the DAC in position 20H. Nominal saturation as maximum −10 dB.
   a) The second RGB input (which is intended to be used for OSD and teletext display) can only be controlled on brightness.
9. For video signals with a black level which deviates from the back-porch blanking level the signal is ‘stretched’ to the blanking level. The amount of correction depends on the IRE value of the signal (see Fig.8). The black level is detected by means of an internal capacitor. The black level stretcher can be switched on and off via the BKS bit in the I²C-bus. The values given in the specification are valid only when the luminance input signal has an amplitude of 1 V (b-w).
10. Because of the 2-point black current stabilization circuit both the black level and the amplitude of the RGB output signals depend on the drive characteristic of the picture tube. The system checks whether the returning measuring currents meet the requirement and adapts the output level and gain of the circuit when necessary. Therefore the typical value of the black level and amplitude at the output are just given as an indication for the design of the RGB output stage.
    a) The 2-point black level system adapts the drive voltage for each cathode in such a way that the 2 measuring currents have the right value. This has the consequence that a change in the gain of the output stage will be compensated by a gain change of the RGB control circuit. Because different picture tubes may require different drive voltage amplitudes the ratio between the output signal amplitude and the inserted measuring pulses can be adapted via the I²C-bus. This is indicated in the parameter ‘Adjustment range of RGB drive levels’.
    b) Because of the dependence of the output signal amplitude on the application the soft clipping limiting has been related to the input signal amplitude.
    c) It should be noted that the signal amplitude at the RGB outputs of the TDA933xH depends on the gain of the RGB amplifiers. To get the nominal signal amplitude of 2 V (b-w) at the RGB outputs for a cathode drive level of 74 V (b-w) and the nominal setting of the drive level bits (C_{L3210} = 1000, see Table 16) the gain of the RGB amplifiers should be 37.
11. For $2f_H$ or VGA applications it is advised to use external PNP emitter followers as buffers on the RGB outputs of the TDA933xH, to avoid reduction of the RGB bandwidth by the capacitance of the wiring between the TDA933xH and the RGB power amplifiers on the picture tube panel.
12. When the reproduction of 4 : 3 pictures on a 16 : 9 picture tube is realized by means of a reduction of the horizontal scan amplitude the edges of the picture may be slightly disturbed. This effect can be prevented by adding an additional blanking pulse to the RGB signals. The blanking pulse is derived form the horizontal oscillator and is directly related to the incoming video signal (independent of the flyback pulse). The additional blanking pulse overlaps the normal blanking signal with approximately 1 μs ($1f_H$) or 0.5 μs ($2f_H$) on both sides. This blanking is activated by the HBL bit. The phase of the wide blanking can be controlled by the HB3 to HB0 bits in 15 steps.

13. Start-up behaviour of the CCC loop. After the horizontal output is released via the STB bits the RGB outputs are blanked and the CCC loop is activated. Because the picture tube is cold the measured cathode currents are too small, and gain as well as offset are set at the maximum value so that the CCC loop gets out of range and the BCF status bit is set to logic 1. At the moment the picture tube is warm the loop comes within range and the set signal for the BCF bit is removed. The BCF status bit is set if the voltage of at least one of the cutoff measurement lines at the RGB outputs is lower than 1.5 V or higher than 3.5 V. The RGB outputs are unblanked as soon as the BCF bit changes from logic 1 to logic 0. To avoid a bright picture after switch-on with a warm picture tube, reset of the BCF bit is disabled for a period of 0.5 s after switch-on of the horizontal output. If required the blanking period of the RGB outputs can be made longer by forcing the blanking level at the RGB outputs via RBL = 1. When the BCF status bit changes from logic 1 to logic 0, the RBL bit can be set to logic 0 after a certain waiting period.
14. The V_{g2} voltage of the picture tube can be aligned with the help of status bits WBC and HBC. The WBC bit becomes logic 1 if the lowest of the three RGB output voltages during the cut-off measurement lines is within the alignment window of ±0.1 V around 2.5 V. The HBC bit is logic 0 if the lowest cut-off level is below 2.5 V, and logic 1 if this level is above 2.5 V.
    a) The V_{g2} voltage should be aligned such that the WBC bit becomes logic 1. If the WBC bit is logic 0, the HBC bit indicates in which direction the V_{g2} voltage should be adjusted. If HBC = 0 the DC level at the RGB outputs of the IC is too low, and the V_{g2} voltage should be adjusted lower until WBC becomes logic 1. If HBC = 1 the DC level is too high, and the V_{g2} voltage should be adjusted higher until WBC becomes logic 1.
    b) It should be noted that the WBC bit is only meant for factory alignment of the V_{g2} voltage. If the value of the WBC bit depends on the video content this is no problem. Correct operation of the black current loop is guaranteed as long as status bit BCF = 0, meaning that the DC level of the measurement lines at the RGB outputs of the IC is between 1.5 and 3.5 V.
15. Signal-to-noise ratio (S/N) is specified as a peak-to-peak signal with respect to RMS noise (bandwidth 10 MHz).
16. This is a current input. When the black current feedback loop is closed (only during measurement lines or during fixed beam current switch off), the voltage at this pin is clamped at 3.3 V. When the loop is open-circuit the input is not clamped and the maximum sink current is approximately 100 μA. The voltage on the pin must not exceed the supply voltage.
17. The control circuit contains a Peak White Limiting (PWL) circuit and a soft clipper. The detection level of the PWL is adjustable via the I²C-bus and has a control range between 0.55 and 0.85 V (b-w). This amplitude is related to the Y input signal (typical amplitude 1 V (b-w) at maximum contrast setting. The output signal of the PWL detector is filtered by means of an external capacitor so that the high frequency components of the video signal will not activate the limiting action. Because the capacitor is externally available the set maker can adapt the filter time-constant to his wishes. The contrast reduction of the PWL is obtained by discharging the capacitor of the beam current limiting input.
    a) In addition to the PWL circuit the IC contains a soft clipper function which limits the high frequency signals when they exceed the peak white limiting level. The difference between the peak white limiting level and the soft clipping level is adjustable via the I²C-bus and can be varied between 0 and 10% in 3 steps (soft clipping level equal or higher than the PWL level). It is also possible to switch-off the soft clipping function.
18. The soft clipper gain reduction is measured by applying a sawtooth signal with rising slope and 1 V (b-w) at the luminance input. To prevent the beam current limiter from operating a DC voltage of 3.5 V must be applied to pin 43. The contrast is set at the maximum value, the PWL (peak white limiting) level at the minimum value, and the soft clipping level is set at 0% above the PWL level (SC_{10} = 00). The tangents of the sawtooth waveform at one of the RGB outputs is now determined at the beginning and end of the sawtooth. The soft clipper gain reduction is defined as the ratio of the slopes of the tangents for black and white, see Fig.11.
19. When the blue stretch function is activated (via the I²C-bus bit BLS) the gain of the red and green channel is reduced for input signals which exceed a value of 80% of the nominal amplitude. This has the result that the white point is shifted to a higher colour temperature.

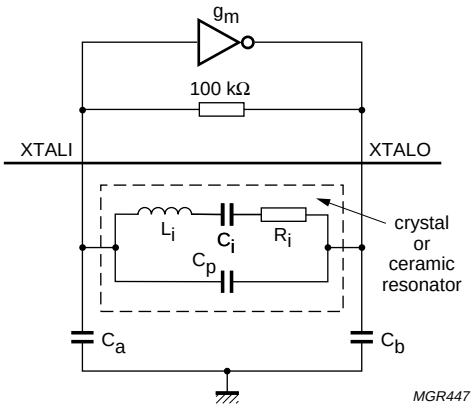
20. Switch-off behaviour of TDA933xH. For applications with an EHT generator without bleeder resistor the picture tube capacitance can be discharged with a fixed beam current at switch off of the set. The magnitude of the discharge current is controlled via the black current loop. The fixed beam current mode can be activated with the FBC bit. With the fixed beam current option activated it is still possible to have a black screen during switch-off. This is realized by placing the vertical deflection in the overscan position. This mode is activated by the OSO bit. There are two possible situations for switch-off (see notes 21 and 22).
21. The set is switched to standby via the I²C-bus. In this situation the procedure is as follows;
    a) Vertical scan is completed.
    b) Vertical flyback is completed.
    c) Slow stop of the horizontal output is started, by gradually reducing the 'on time' at the horizontal output from nominal to zero.
    d) At the same moment the fixed beam current is forced via the black current loop (if FBC = 1).
    e) If OSO = 1 the vertical deflection stays in overscan position, if OSO = 0 the vertical deflection keeps running.
    f) The slow stop time is approximately 42 ms, the fixed beam current is flowing for 37 ms (88% of slow stop time).
22. The set is switched off via the mains power switch. When the mains supply is switched off the supply voltage of the line deflection circuit of the TV set will decrease. A detection circuit must be made that monitors this supply voltage. When the supply voltage suddenly decreases the FBCSO (fixed beam current switch-off) pin of the TDA933xH must be pulled HIGH. In this situation the procedure is as follows:
    a) Vertical scan is completed.
    b) Vertical flyback is completed.
    c) The fixed beam current is forced via the black current loop (if FBC = 1). The horizontal output keeps running. As the supply voltage for the line transformer decreases, the EHT voltage will also decrease.
    d) If OSO = 1 the vertical deflection stays in overscan position, if OSO = 0 the vertical deflection keeps running.
    e) When the supply voltage of the TDA933xH drops below the POR (power-on reset) level, horizontal output and fixed beam current are stopped.
23. The discharge current for the picture tube can be enlarged with an external current division circuit on the black current input (pin 44). The current division should only be active for high cathode currents, so that the operation of the black current stabilization loop is not affected.
24. A stable switching of the H_D input has been realized by using a Schmitt trigger input.
25. The simplified circuit diagram of the oscillator is given in Fig.3. To ensure that the oscillator will start-up the ceramic resonator must fulfil the following condition: $C_L^2 \times R_i \leq 1.1 \times 10^{-19}$
    a) Example: When the resonator is loaded with 60 pF (this is a typical value for a 12 MHz resonator) the series resistance of the resonator must be smaller than 30 Ω.
    b) A suitable ceramic resonator for use with the TDA933xH is the Murata CST12.0MT, which has the load capacitances C_a and C_b built-in. For higher accuracy it is also possible to use a quartz crystal, that is even less critical with respect to start-up because of its lower load capacitance.
26. The HSEL pin must be connected to ground in a $1f_H$ application. It must be left open-circuit for a $2f_H$ application. The TDA9331H and TDA9332H can be switched in a multi-sync mode in which the horizontal frequency can vary between 15 and 25 kHz ($1f_H$ mode) or 30 and 50 kHz ($2f_H$ mode).
27. The indicated frequency range is valid only when a stable reference frequency (e.g. obtained with an accurate crystal) is available. The tolerance of the reference resonator has to be taken into account to obtain the real frequency range.
28. The correction factor k of the phase-2 loop is defined as the amount of correction per line period of a phase error between the horizontal flyback pulse and the internal phase-2 reference pulse. When k = 0.5 the phase error between the flyback pulse and the internal reference is halved each line period.

29. The control range of the second control loop depends on the line frequency. The maximum control range from the rising edge of HOUT to the centre of the flyback pulse is always 37% of one line period, for the centre position of the dynamic phase compensation (4.0 V at pin 14).
30. The dynamic phase compensation input (pin 14) is connected to an internal reference voltage of 4.0 V via a resistor of 100 kΩ. If dynamic phase compensation is not used this pin should be decoupled to ground (pin 19) via a capacitor of 100 nF.
31. The range of the parallelogram correction is proportional to the width of the horizontal flyback pulse.
32. For a safe operation of the horizontal output transistor and to obtain a controlled switch-on time of the EHT the horizontal drive starts up in a soft start mode. The horizontal drive starts with a very short 'on time' of the horizontal output transistor (line locked clock pulse, i.e. 72 ns), the 'off time' of the transistor is identical to the 'off time' in normal operation. The starting frequency during switch-on is therefore approximately twice the normal value. The t_{on} is slowly increased to the nominal value in a time of approximately 150 ms (see Fig.13). When the nominal frequency is reached the PLL is closed in such a way that only very small phase corrections are necessary. This ensures a safe operation of the output stage.
    a) For picture tubes with Dynamic Astigmatic Focusing (DAF) guns it is preferred that the rise of the EHT voltage between 75 and 100% must be even slower than the rise time from 0 to 75%. This can be realized by means of the ESS bit. When the ESS bit is activated the total switch-on time of the horizontal output pulse is approximately 1150 ms.
    b) During switch-off the soft-stop function is active. This is realized by decreasing the t_{on} of the output transistor complementary to the start-up behaviour. The switch-off time is approximately 43 ms. The slow stop procedure is synchronized to the start of the first new vertical field after the reception of the switch-off command. During the soft-stop period the fixed beam current switch-off can be activated (see also note 20). This current is active during the first 37 ms (88%) of the slow stop time.
    c) The horizontal output is gated with the flyback pulse so that the horizontal output transistor cannot be switched on during the flyback pulse. This protection is not active during the switch-on or switch-off period.
33. This parameter is not tested during production and is just given as application information for the designer of the television receiver.
34. The rise and fall times of the blanking pulse and clamping pulse at the sandcastle output (pin 9) depend on the capacitive load. The value of the source current during the rising edge or sink current during the falling edge is 0.7 mA (typ.).
35. The vertical guard pulse from the vertical output stage should fall within the vertical blanking period (see Figs 9 and 10) and should have a width of at least one line period.
36. The switching between the $1f_V$ or the $2f_V$ mode is realized via the SVF bit.
37. The vertical linearity is measured on the differential output current at the vertical drive output (pins 1 and 2) for zero S-correction. The linearity is defined as the ratio of the upper and lower half amplitude at the vertical output. The upper amplitude is measured between lines 27 and 167, the lower amplitude between lines 167 and 307 for a 50 Hz video signal.
38. The field detection mechanism is explained in Fig.14.
    a) The incoming V_D pulse is synchronized with the internal clock signal 2 kHz that is locked to the incoming H_D pulse. If the synchronized V_D pulse of a field coincides with the internally generated horizontal blanking signal HBLNK then this is field 1. If the synchronized V_D pulse does not coincide with the horizontal blanking signal then this is field 2. The 2 kHz and the HBLNK signals are both output signals of the horizontal divider circuit that is part of the line-locked clock generator. A reliable field detection is important for correct interlacing and de-interlacing and for the correct timing of the measurement lines of the black current loop. For the best noise margin the edges of the V_D pulse should be on approximately $\frac{1}{4}$ and $\frac{3}{4}$ of the line, referred to the rising edges of the H_D input signal.
    b) If bus bit VSR = 0 the falling edge of the V_D pulse is used as reference for both field detection and start of vertical scan. If VSR = 1 the rising edge is used.

39. Output range percentages mentioned for E-W control parameters are based on the assumption that the East-West modulator is dimensioned such that 400 μA variation in E-W output current of the IC is equivalent to 20% variation in picture width. In VGA mode the E-W output current is proportional to the applied line frequency.
40. The IC has protection inputs for flash protection and overvoltage protection.
    a) The flash protection input is used to immediately switch-off the horizontal drive output in the event of a picture tube flashover, for protection of the line output transistor. An external flash detection circuit is needed. When the flash input is pulled HIGH the horizontal output is switched off and the FLS status bit is set. When the input turns LOW again the horizontal output is switched on immediately without I²C-bus intervention via the slow start procedure.
    b) The overvoltage (X-ray) protection is combined with the EHT compensation input. When this protection is activated the horizontal drive can be directly switched off (via the slow stop procedure). It is also possible to continue the horizontal drive and only set the XPR status bit in output byte 01 of the I²C-bus. The choice between the 2 modes of operation is made via the PRD bit.
41. The ICs have a zoom adjustment possibility for the horizontal and vertical deflection. For this reason an extra DAC has been added in the vertical amplitude control which controls the vertical scan amplitude between 0.75 and 1.38 of the nominal scan. At an amplitude of 1.05 times the nominal scan the output current is limited and the blanking of the RGB outputs is activated: this is illustrated in Fig.12. In addition to the variation of the vertical amplitude the picture can be vertically shifted on the screen via the ‘scroll’ function.
    a) The nominal scan height must be adjusted at a position of 19H (25 DEC) of the vertical ‘zoom’ DAC and 1FH (31 DEC) for the vertical ‘scroll’ DAC.
42. The vertical scroll function is active only in the expand mode of the vertical zoom, i.e. at a DAC position greater than 10H (16 DEC).
43. With the vertical wait function the start of the vertical scan can be delayed with respect to the incoming vertical sync pulse. The operation is different for the various scan modes. The differences are indicated in Table 49. See also Figs 9 and 10. The minimum value for the vertical wait is 8 line periods. If the setting is lower than 8 the wait period will remain 8 line periods.
44. In the TDA9330H and TDA9332H the DAC output is I²C-bus controlled.
    a) In the TDA9331H the DAC output voltage is proportional to the centre frequency of the line-oscillator. In TV mode the output voltage will always be at the minimum value. In VGA mode the output is at the minimum value for the lowest centre frequency (32 kHz), and at the maximum value for the highest centre frequency (48 kHz).
    b) The output impedance of the DAC output depends on the output voltage. The output consists of an emitter follower with an internal resistor of 50 kΩ to ground.

Table 49 Operation of the vertical wait function

MODE	START OF VERTICAL SCAN
$1f_H$; TV mode	fixed; see Fig.9
$2f_H$; TV mode; VSR = 0	end of V_D plus vertical wait setting
$2f_H$; TV mode; VSR = 1	start of V_D plus vertical wait setting
$1f_H$; multi sync mode	start of V_D plus vertical wait setting
$2f_H$; multi sync mode	start of V_D plus vertical wait setting



$$f_{osc} = \frac{1}{2\pi\sqrt{L_i \times \frac{C_i \times C_L}{C_i + C_L}}}$$

$$C_L = C_p + \frac{C_a \times C_b}{C_a + C_b}$$

Requirement for start-up:

$$C^2{}_L \times R_i \leq 1.1 \times 10^{-19}$$

Fig.3 Simplified diagram crystal oscillator.

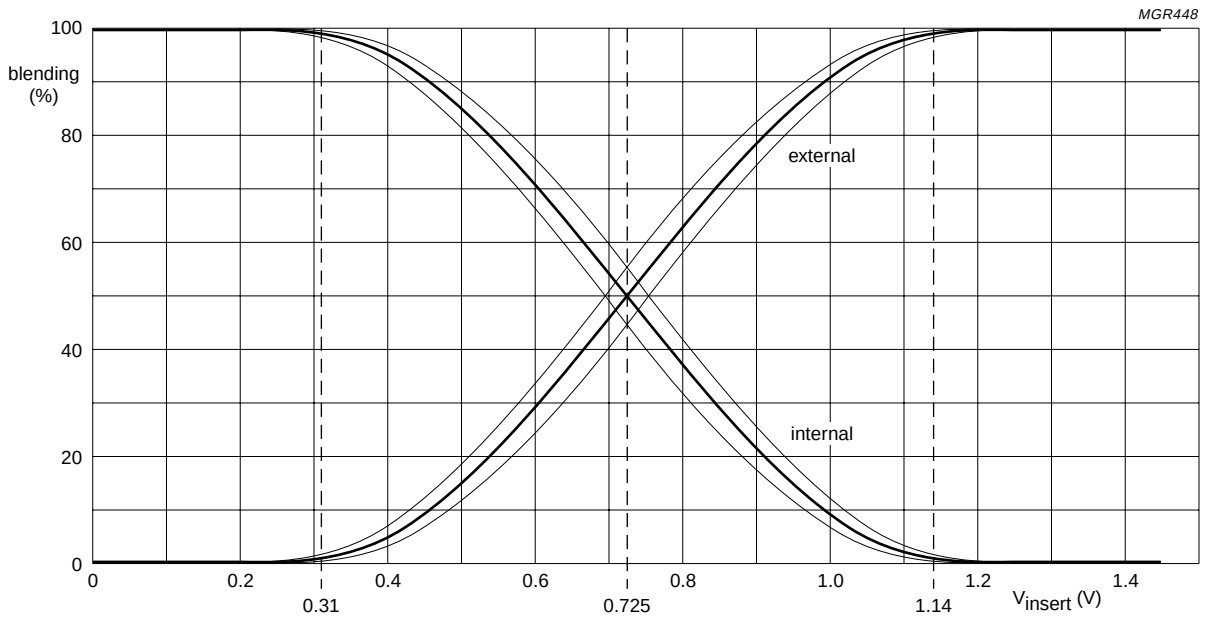


Fig.4 Blending characteristic (typical curve and minimum/maximum limits).

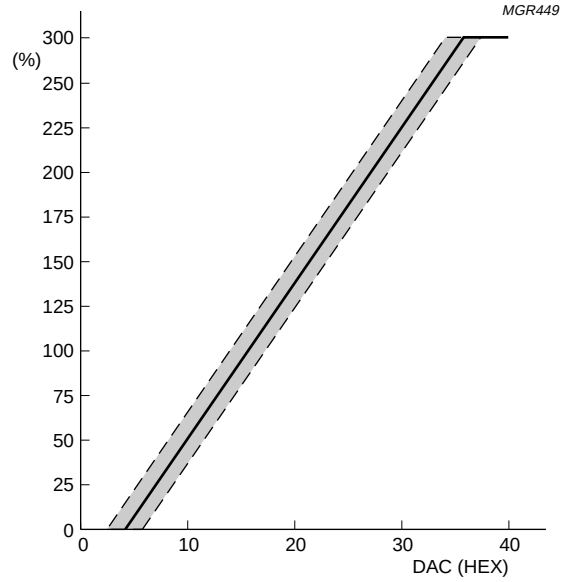


Fig.5 Saturation control curve.

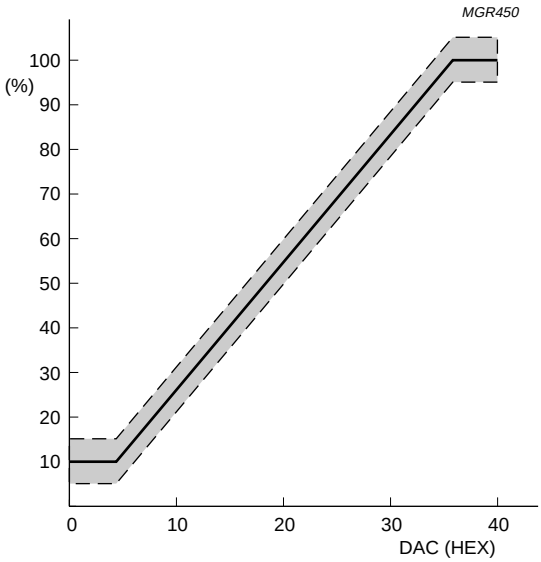
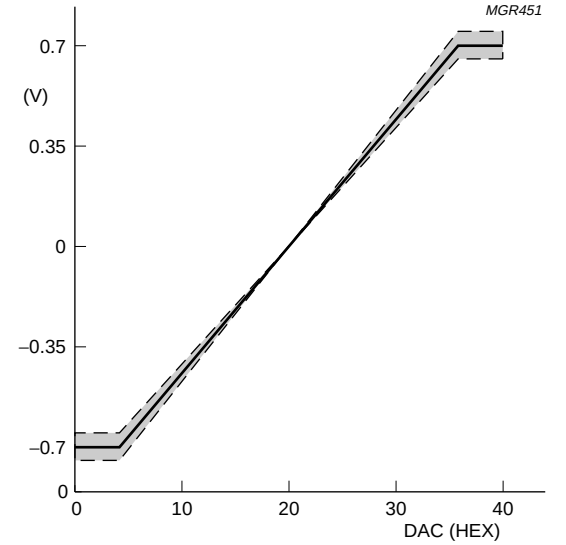


Fig.6 Contrast control curve.



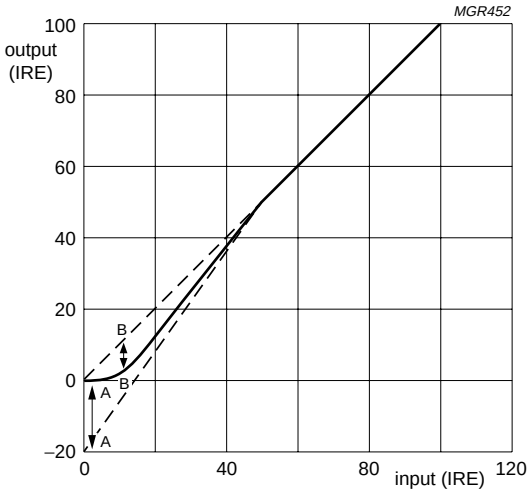
Conditions:

Settings for cathode drive level and white point nominal.

Gain of RGB amplifiers such that the amplitude at the RGB outputs is 2 V (b-w).

Relative to cut-off level.

Fig.7 Brightness control curve.



A-to-A: maximum black level shift.

B-to-B: level shift at 15% of peak white.

Fig.8 I/O relation of black level stretch circuit.

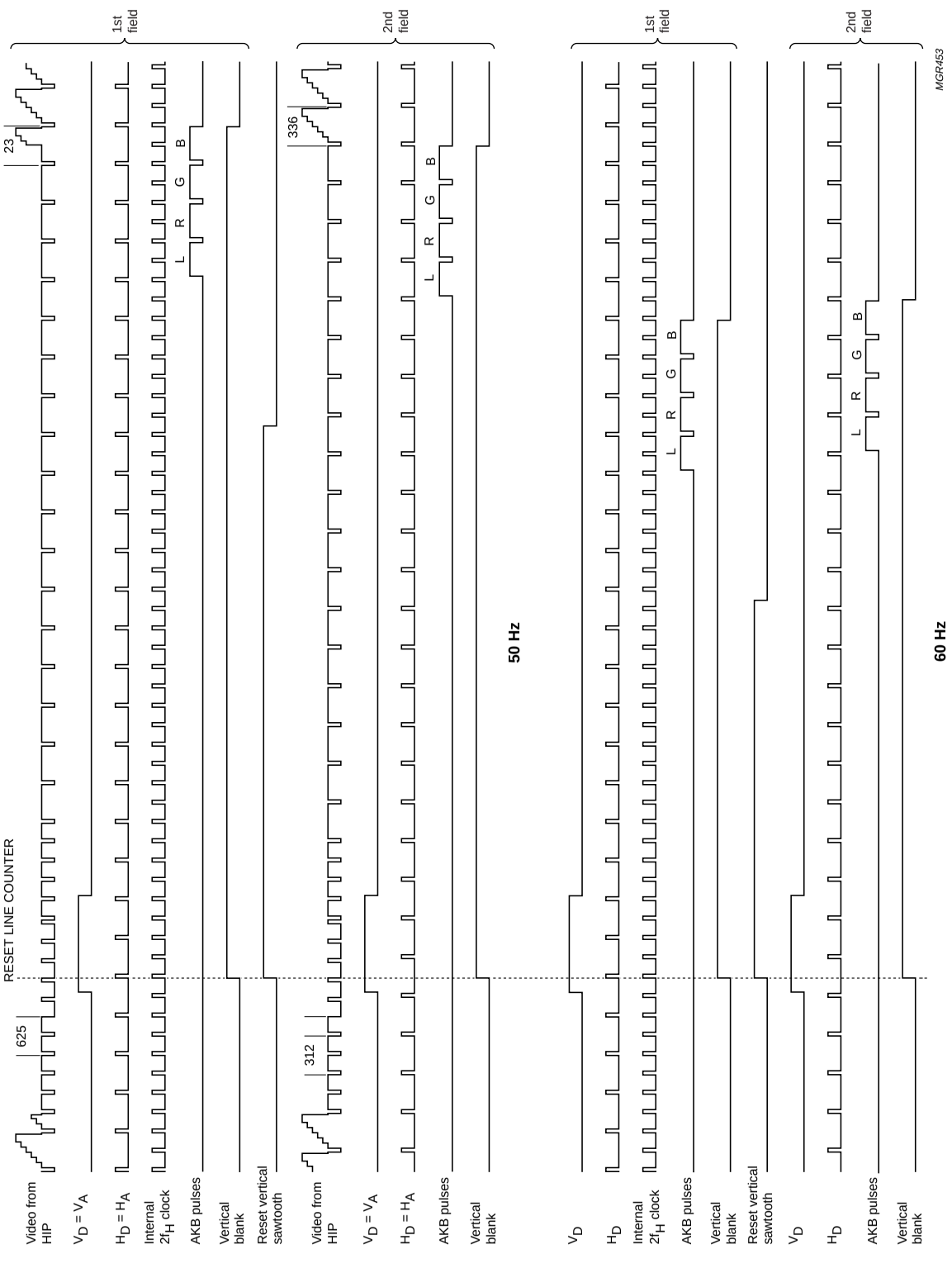


Fig.9 Vertical timing pulses for $1f_H$ TV mode.

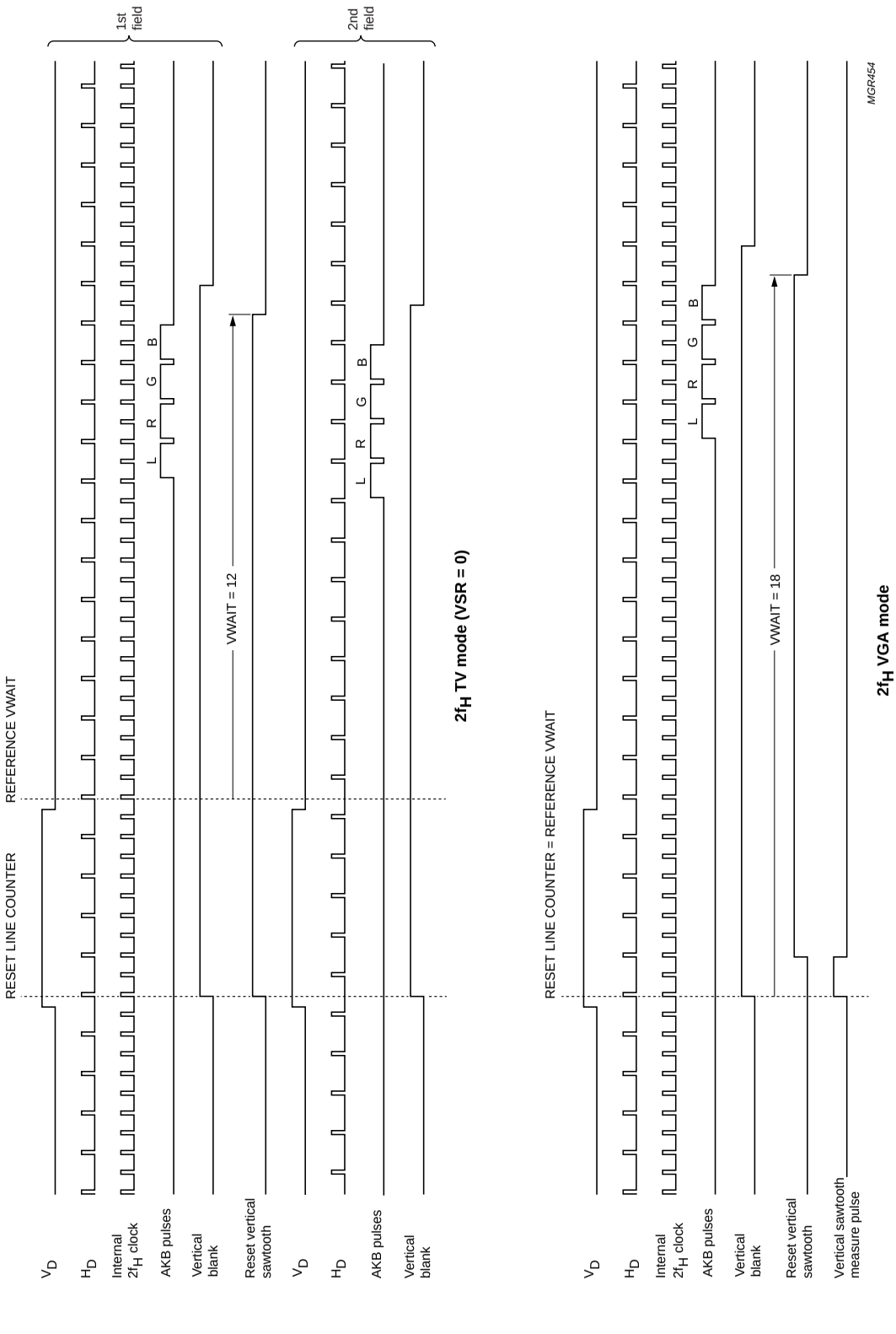
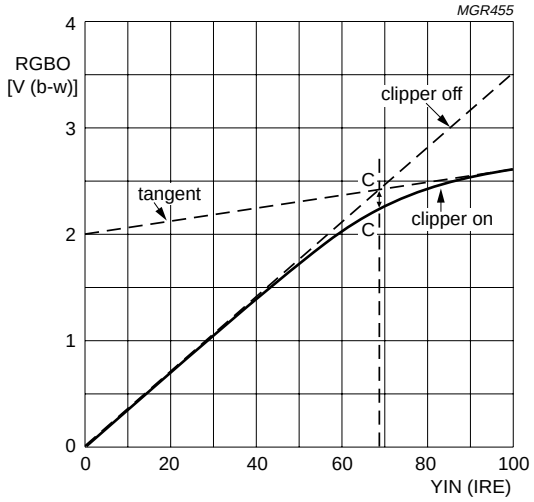


Fig.10 Vertical timing pulses for $2f_H$ TV mode and VGA mode.



C-to-C: maximum deviation between tangents and actual curve.
See also Chapter “Characteristics”; note 18.

Fig.11 Soft clipper characteristic.

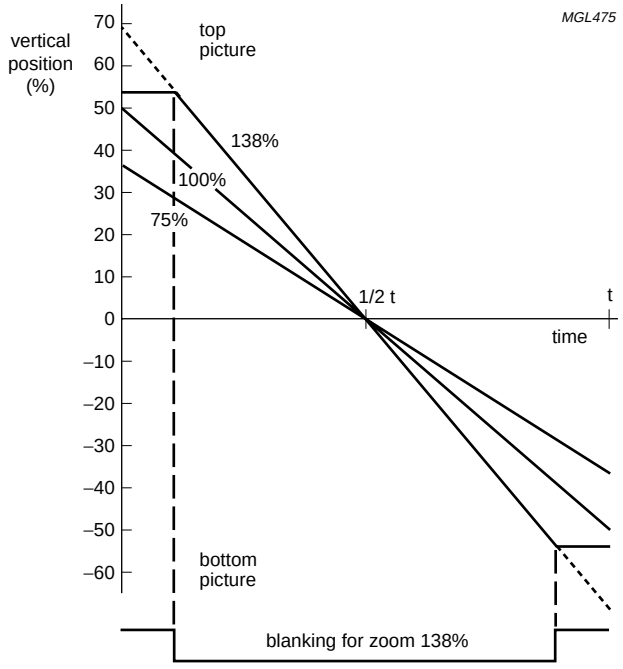


Fig.12 Vertical drive waveform and blanking pulse for different zoom factors.

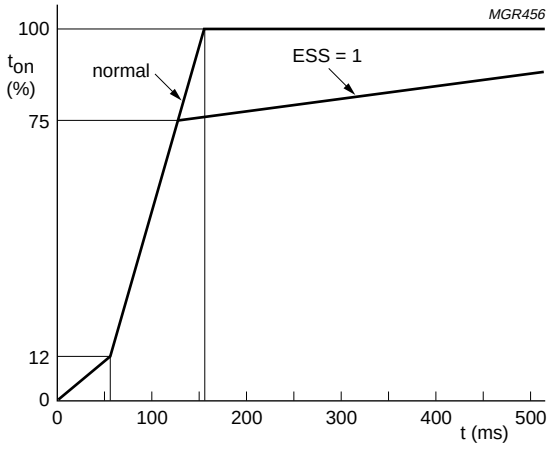
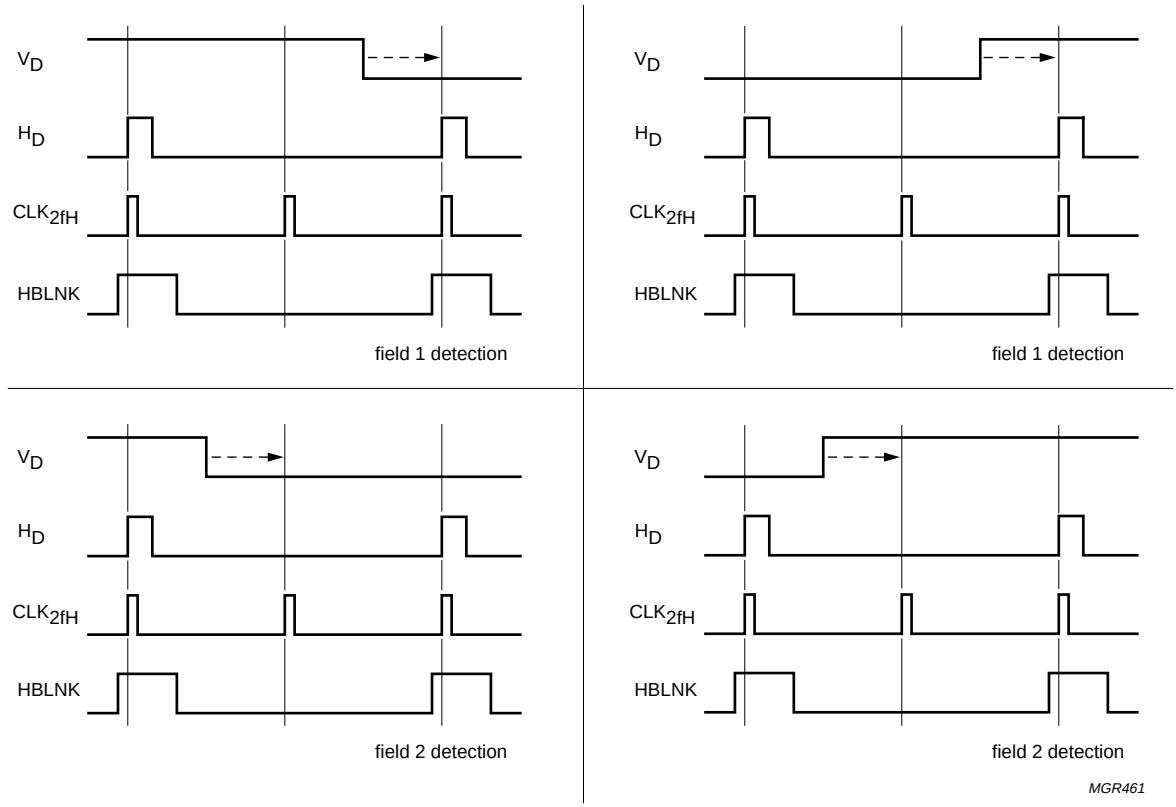


Fig.13 Soft-start behaviour.



a. Falling edge of V_D pulse is reference (VSR = 0). b. Rising edge of V_D pulse is reference (VSR = 1).

See also Chapter “Characteristics”; note 38.

Fig.14 Field detection mechanism.

TEST AND APPLICATION INFORMATION

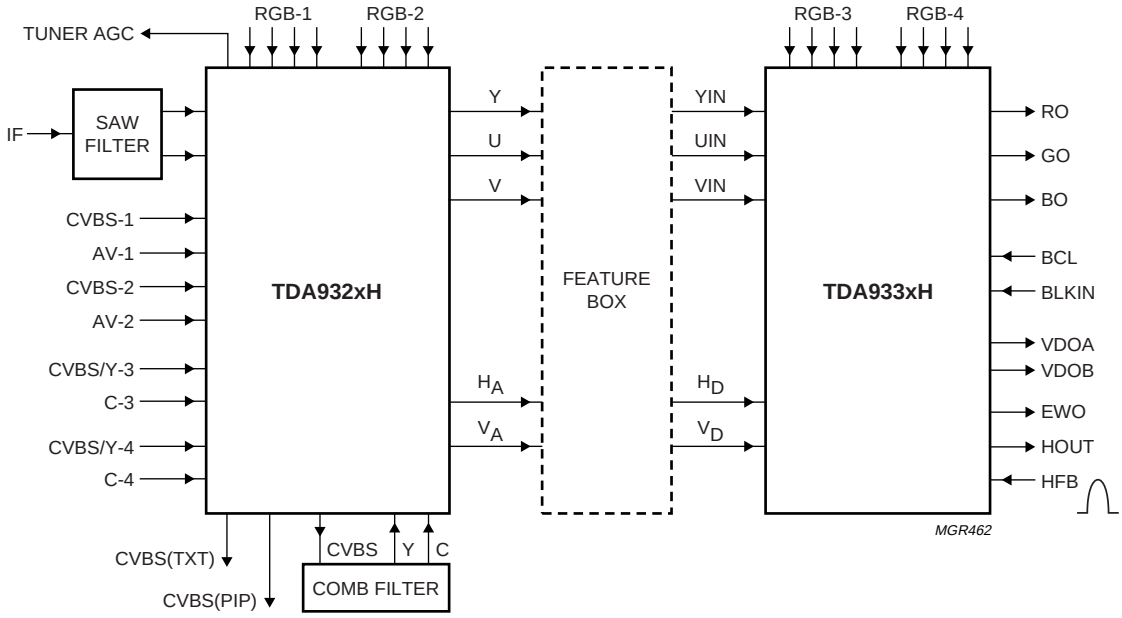
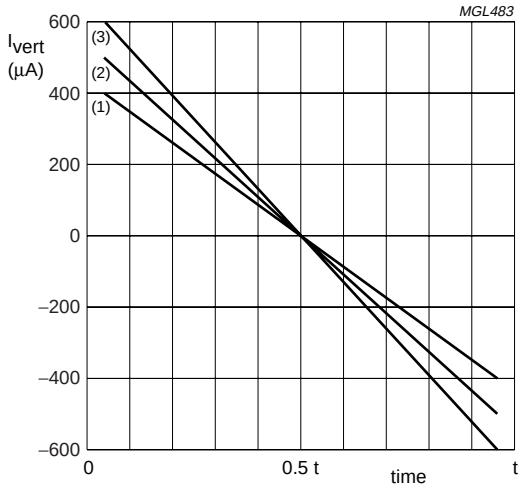
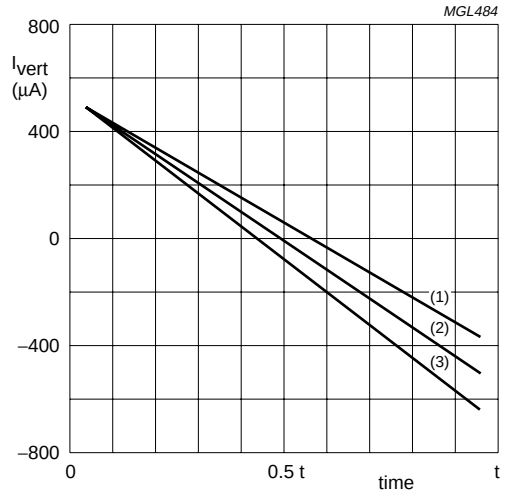


Fig.15 Application diagram.



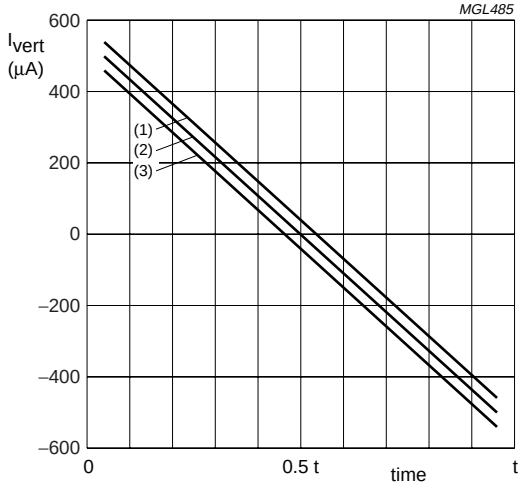
VSH = 31; SC = 0; $I_{VERT} = I_{2(VDOB)} - I_{1(VDOA)}$.
(1) VA = 0.
(2) VA = 31.
(3) VA = 63.

Fig.16 Control range of vertical amplitude.



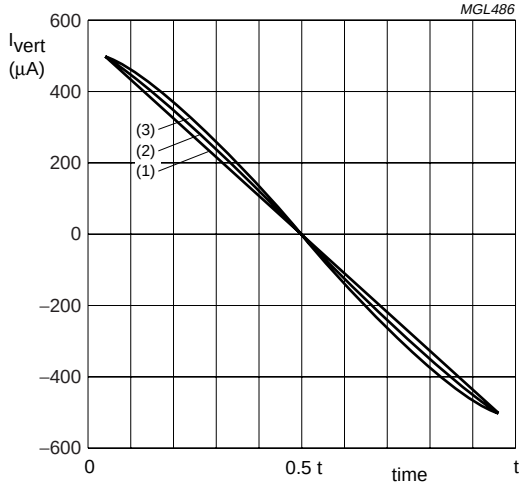
VA = 31; VHS = 31; SC = 0.
(1) VS = 0.
(2) VS = 31.
(3) VS = 63.

Fig.17 Control range of vertical slope.



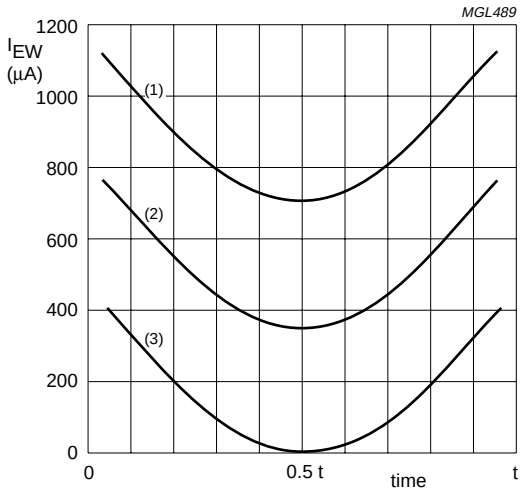
VA = 31; SC = 0.
(1) VSH = 0.
(2) VSH = 31.
(3) VSH = 63.

Fig.18 Control range of vertical shift.



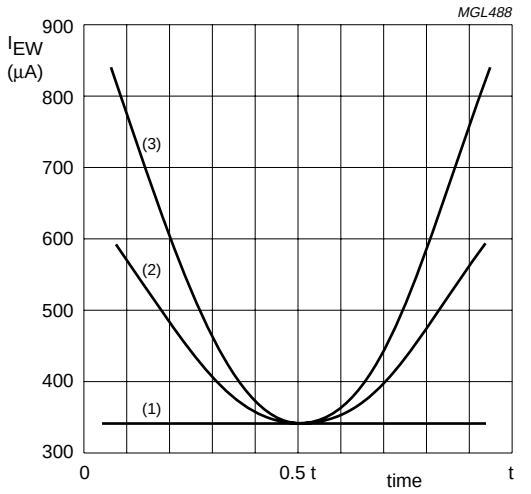
VA = 31; VHS = 31.
(1) SC = 0.
(2) SC = 31.
(3) SC = 63.

Fig.19 Control range of S-correction.



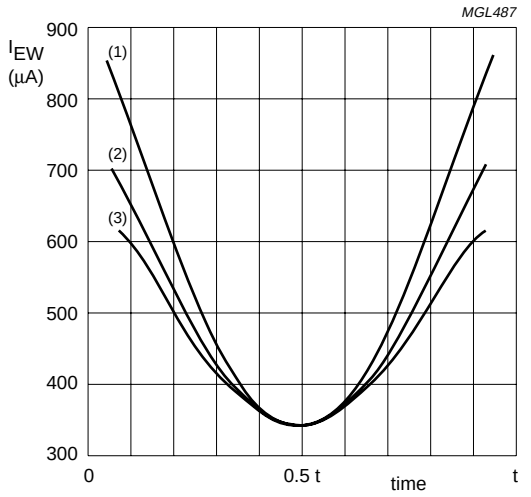
PW = 31; CP = 31.
(1) EW = 0.
(2) EW = 31.
(3) EW = 63.

Fig.20 Control range of E-W width.



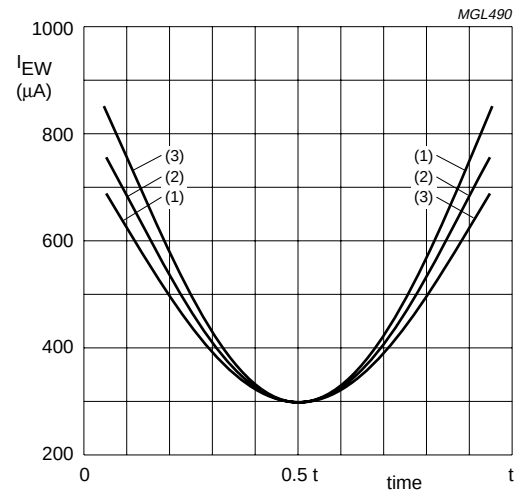
EW = 31; CP = 31.
(1) PW = 0.
(2) PW = 31.
(3) PW = 63.

Fig.21 Control range of E-W parabola/width ratio.



EW = 31; PW = 63.
(1) CP = 0.
(2) CP = 31.
(3) CP = 63.

Fig.22 Control range of E-W corner/parabola ratio.



EW = 31; PW = 31.
(1) TC = 0.
(2) TC = 31.
(3) TC = 63.

Fig.23 Control range of E-W trapezium correction.

Adjustment of geometry control parameters

The deflection processor of the TDA933xH offers 13 control parameters for picture alignment as follows:

For the vertical picture alignment;

- S-correction
- Vertical amplitude
- Vertical slope
- Vertical shift
- Vertical zoom
- Vertical scroll
- Vertical wait.

For the horizontal picture alignment;

- Horizontal shift
- Horizontal parallelogram
- E-W width with extended range because of the zoom function
- E-W parabola width
- E-W corner parabola
- E-W trapezium correction.

It is important to notice that the ICs are designed for use with a DC-coupled vertical deflection stage. This is the reason why a vertical linearity alignment is not necessary (and therefore not available).

For a particular combination of picture tube types, vertical output stage and E-W output stage the required values for the settings of S-correction, E-W parabola/width ratio and E-W corner/parabola ratio have been determined. These parameters can be preset via the I²C-bus and do not need any additional adjustment. The rest of the parameters are preset with the mid-value of their control range (i.e. $1f_H$), or with the values obtained by previous TV set adjustments.

The vertical shift control is intended for compensation of offsets in the external vertical output stage or in the picture tube. It can be shown that without compensation these offsets will result in a certain linearity error, especially with picture tubes that need large S-correction. The total linearity error is in 1st-order approximation proportional to the value of the offset, and to the square of the S-correction that is needed. The necessity to use the vertical shift alignment depends on the expected offsets in the vertical output stage and picture tube, on the required value of the S-correction and on the demands upon vertical linearity.

For adjustment of the vertical shift and vertical slope, independent of each other, a special service blanking mode can be entered by setting the SBL bit HIGH. In this mode the RGB outputs are blanked during the second half of the picture. There are 2 different methods for alignment of the picture in vertical direction. Both methods make use of the service blanking mode.

The first method is recommended for picture tubes that have a marking for the middle of the screen. With the vertical shift control the last line of the visible picture is positioned exactly in the middle of the screen. After this adjustment the vertical shift should not be changed. The top of the picture is placed by adjustment of the vertical amplitude, and the bottom by adjustment of the vertical slope.

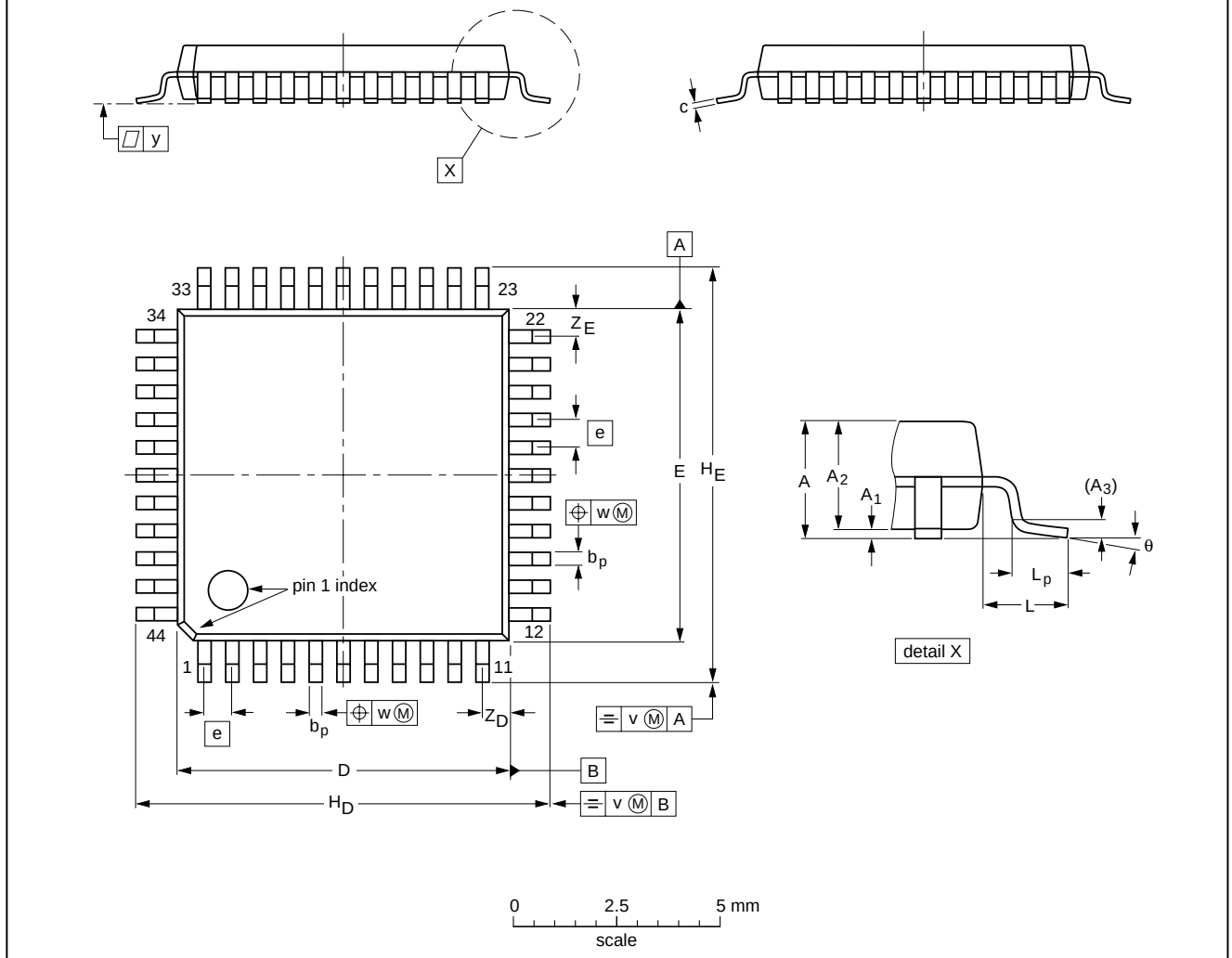
The second method is recommended for picture tubes that have no marking for the middle of the screen. For this method a video signal is required in which the middle of the picture is indicated (e.g. the white line in the circle test pattern). The beginning of the blanking is positioned exactly on the middle of the picture using the vertical slope control. The top and bottom of the picture are then placed symmetrical with respect to the middle of the screen by adjustment of the vertical amplitude and vertical shift. After this adjustment the vertical shift has the correct setting and should not be changed.

If the vertical shift alignment is not required VSH should be set to its mid-value (i.e. VSH = 1FH or 31 DEC). The top of the picture is then placed by adjustment of the vertical amplitude and the bottom of the picture by adjustment of the vertical slope. After the vertical picture alignment the picture is positioned in the horizontal direction by adjustment of the E-W width and the horizontal shift. Finally (if necessary) the left and right-hand sides of the picture are aligned in parallel by adjusting the E-W trapezium control.

To obtain the full range of the vertical zoom function the adjustment of the vertical geometry should be carried out at a nominal setting of the zoom DAC at position 19H (25 DEC) and the vertical scroll DAC at 1FH (31 DEC).

PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm **SOT307-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						~~95-02-04~~ 97-08-01

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

CAUTION
Wave soldering is NOT applicable for all QFP packages with a pitch (e) equal or less than 0.5 mm.

If wave soldering cannot be avoided, for QFP packages with a pitch (e) larger than 0.5 mm, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

NOTES

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