DATA SHEET

TDA8705A
6-bit high-speed dual Analog-to-Digital Converter (ADC)

Product specification
Supersedes data of November 1994
File under Integrated Circuits, IC02

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Philips
Semiconductors

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6-bit high-speed dual Analog-to-Digital Converter (ADC)

TDA8705A

FEATURES

- 2 times 6-bit resolution
- Sampling rate up to 80 MHz
- High signal-to-noise ratio over a large analog input frequency range (5.5 effective bits at 20 MHz full-scale input at f_{clk} = 80 MHz)
- TTL output
- Two separated inputs (AC-coupling)
- TTL compatible digital inputs
- Low-level AC clock input signal allowed
- Internal reference voltage regulator (external reference regulation possible)
- Power dissipation only 250 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required.

APPLICATIONS

High-speed analog-to-digital conversion for:

- DBS (Digital Broadcast Satellite)
- QPSK (Quadrature Phase Shift Keying) demodulation
- Video.

GENERAL DESCRIPTION

The TDA8705A is a 6-bit high-speed dual analog-to-digital converter (ADC) for satellite video and other applications. It converts the two analog input signals into two 6-bit binary-coded digital words at a maximum sampling rate of 80 MHz. All digital inputs and outputs are TTL compatible, although a low-level sine wave clock input signal is allowed.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		20	27	32	mA
I_{CCD}	digital supply current		10	14	18	mA
I_{CCO}	output stages supply current		10	14	18	mA
ILE	DC integral linear error		–	±0.25	±0.5	LSB
DLE	DC differential linearity error		–	±0.25	±0.5	LSB
AILE	AC integral linearity error	note 1	–	±0.5	±1.0	LSB
$f_{clk(max)}$	maximum clock frequency		80	–	–	MHz
P_{tot}	total power dissipation		–	250	–	mW

Note

1. Full-scale sine wave (f_i = 20 MHz; f_{clk} = 80 MHz).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8705AT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

BLOCK DIAGRAM

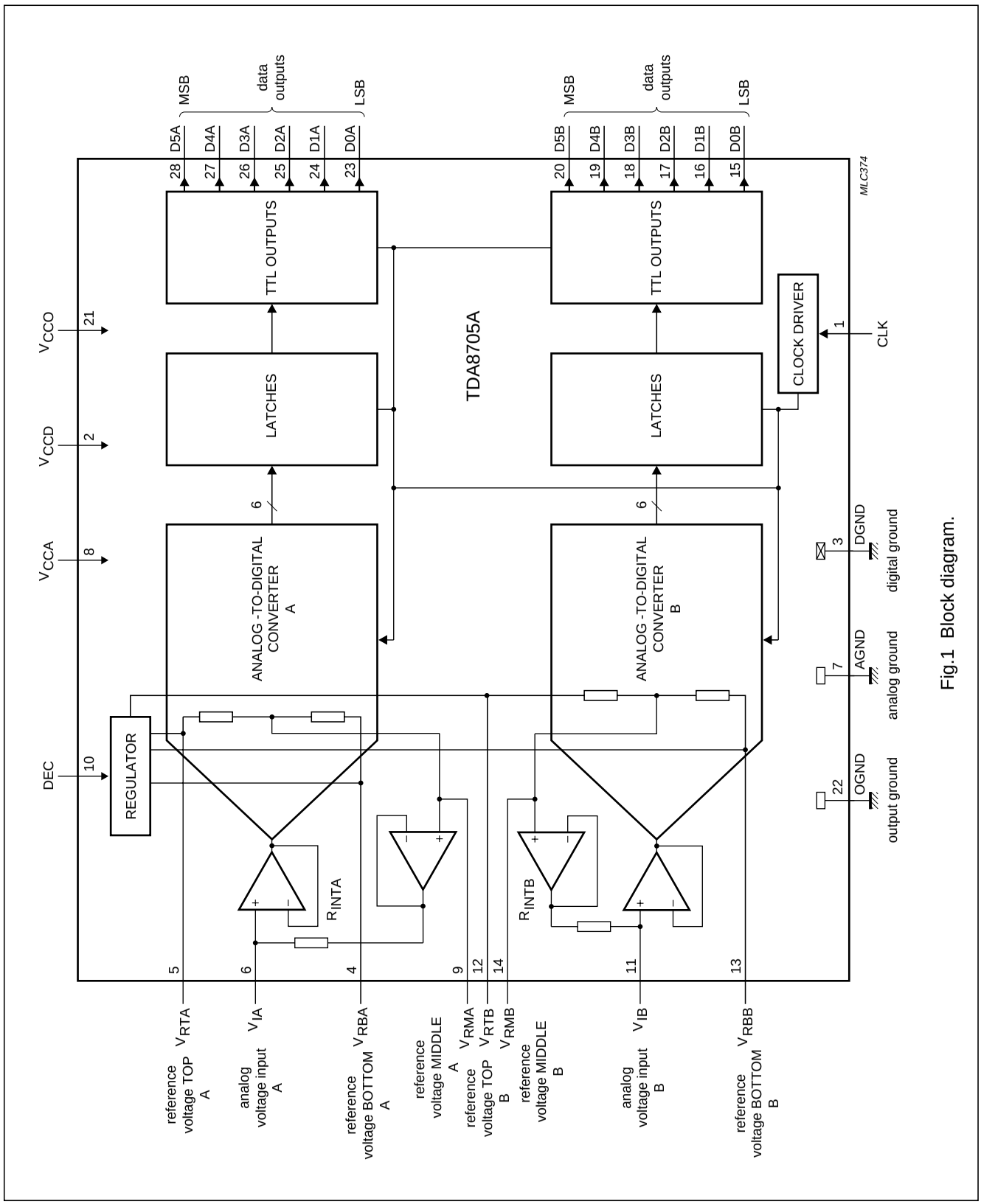


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CLK	1	clock input
V_{CCD}	2	digital supply voltage (+5 V)
DGND	3	digital ground
V_{RBA}	4	reference voltage BOTTOM for ADC A (decoupling)
V_{RTA}	5	reference voltage TOP for ADC A (decoupling)
V_{IA}	6	analog input voltage for ADC A
AGND	7	analog ground
V_{CCA}	8	analog supply voltage (+5 V)
V_{RMA}	9	reference voltage MIDDLE for ADC A (decoupling)
DEC	10	decoupling input
V_{IB}	11	analog input voltage for ADC B
V_{RTB}	12	reference voltage TOP for ADC B (decoupling)
V_{RBB}	13	reference voltage BOTTOM for ADC B (decoupling)
V_{RMB}	14	reference voltage MIDDLE for ADC B (decoupling)
D0B	15	data output; bit 0 (LSB), ADC B
D1B	16	data output; bit 1, ADC B
D2B	17	data output; bit 2, ADC B
D3B	18	data output; bit 3, ADC B
D4B	19	data output; bit 4, ADC B
D5B	20	data output; bit 5 (MSB), ADC B
V_{CCO}	21	supply voltage for output stages (+5 V)
OGND	22	output ground
D0A	23	data output; bit 0 (LSB), ADC A
D1A	24	data output; bit 1, ADC A
D2A	25	data output; bit 2, ADC A
D3A	26	data output; bit 3, ADC A
D4A	27	data output; bit 4, ADC A
D5A	28	data output; bit 5 (MSB), ADC A

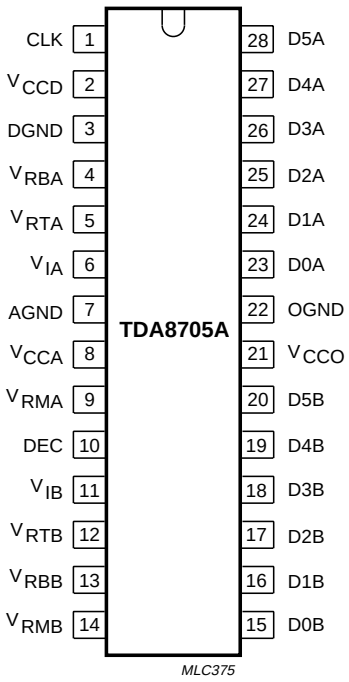


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	note 1	–0.3	+7.0	V
V_{CCD}	digital supply voltage	note 1	–0.3	+7.0	V
V_{CCO}	output stages supply voltage	note 1	–0.3	+7.0	V
ΔV_{CC}	supply voltage differences between V_{CCA} and V_{CCD}		–1.0	+1.0	V
ΔV_{CC}	supply voltage differences between V_{CCO} and V_{CCD}		–1.0	+1.0	V
ΔV_{CC}	supply voltage differences between V_{CCA} and V_{CCO}		–1.0	+1.0	V
V_I	input voltage	referenced to AGND	–0.3	+7.0	V
$V_{clk(p-p)}$	AC input voltage for switching (peak-to-peak value)	referenced to DGND	–	V_{CCD}	V
I_O	output current		–	10	mA
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
T_j	junction temperature		–	+150	°C

Note

1. The supply voltages V_{CCA}, V_{CCO} and V_{CCD} may have any value between –0.3 V and +7 V provided the difference between V_{CCA}, V_{CCO} and V_{CCD} is between –1 V and +1 V.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	70	K/W

CHARACTERISTICS

V_{CCA} = V_8 to V_7 = 4.75 to 5.25 V; V_{CCD} = V_2 to V_3 = 4.75 to 5.25 V; V_{CCO} = V_{21} to V_{22} = 4.75 to 5.25 V; AGND, OGND and DGND shorted together; V_{CCA} to V_{CCD} = –0.25 to +0.25 V; V_{CCO} to V_{CCD} = –0.25 to +0.25 V; V_{CCA} to V_{CCO} = –0.25 to +0.25 V; T_{amb} = 0 to +70 °C; typical values measured at V_{CCA} = V_{CCD} = V_{CCO} = 5 V and T_{amb} = 25 °C; C_L = 15 pF; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		20	27	32	mA
I_{CCD}	digital supply current		10	14	18	mA
I_{CCO}	output stages supply current		10	14	18	mA
Inputs						
CLOCK INPUT CLK; REFERENCED TO DGND; note 1						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{clk} = 0.4 V	–1	–	+1	μA
I_{IH}	HIGH level input current	V_{clk} = 2.7 V	–	–	20	μA
Z_I	input impedance	f_{clk} = 80 MHz	–	2	–	kΩ
C_I	input capacitance	f_{clk} = 80 MHz	–	2	–	pF
V_I ANALOG INPUT VOLTAGE FOR A AND B; REFERENCED TO AGND						
R_I	DC parallel input resistance		20	–	–	kΩ
C_I	parallel input capacitance	f_i = 20 MHz	–	1.5	–	pF
α_{CT}	crosstalk between V_{IA} and V_{IB}	f_i = 20 MHz	40	–	–	dB
Reference voltages for the resistor ladder (A and B); see Table 1						
V_{RB}	reference voltage BOTTOM		1.9	2.0	2.1	V
V_{RT}	reference voltage TOP		2.8	2.9	3.0	V
V_{diff}	differential reference voltage $V_{RT} - V_{RB}$		0.85	0.90	0.95	V
I_{ref}	reference current		–	2	–	mA
R_{LAD}	resistor ladder		–	450	–	Ω
TC_{RLAD}	temperature coefficient of the resistor ladder		–	3280	–	ppm
V_{osB}	offset voltage BOTTOM	note 2	–	200	–	mV
V_{osT}	offset voltage TOP	note 2	–	200	–	mV
$V_{i(p-p)}$	input voltage amplitude (peak-to-peak value)		0.45	0.50	0.55	V
Outputs (A and B)						
DIGITAL OUTPUTS D5 TO D0 (REFERENCED TO DGND)						
V_{OL}	LOW level output voltage	I_O = 1 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = –1 mA	2.4	–	V_{CCD}	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Switching characteristics						
CLOCK INPUT CLK; note 1; see Fig.3						
$f_{clk(max)}$	maximum clock frequency		80	–	–	MHz
t_{CPH}	clock pulse width HIGH		5.5	–	–	ns
t_{CPL}	clock pulse width LOW		5.5	–	–	ns
Analog signal processing						
LINEARITY						
ILE	DC integral linearity error		–	±0.25	±0.5	LSB
DLE	DC differential linearity error		–	±0.25	±0.5	LSB
AILE	AC integral linearity error	note 3	–	±0.5	±1.0	LSB
OFE	offset error between A and B	f_i = 10 MHz; f_{clk} = 40 MHz; note 4	±1	–	±2	LSB
GE	gain error between A and B	f_i = 10 MHz; f_{clk} = 40 MHz; note 4	±1	–	±2	LSB
MID	middle scale output code (A and B)		31	–	32	
BANDWIDTH; f_{clk} = 80 MHz						
B	–0.5 dB analog bandwidth	full-scale sine wave; note 5	–	50	–	MHz
t_{STLH}	analog input settling time LOW-to-HIGH	full-scale square wave; Fig.4; note 6	–	8	–	ns
t_{STHL}	analog input settling time HIGH-to-LOW	full-scale square wave; Fig.4; note 6	–	5	–	ns
HARMONICS; f_{clk} = 40 MHz; see Fig.5						
h_1	fundamental harmonics (full scale)	f_i = 20 MHz	–	–	0	dB
h_{all}	harmonics (full scale); all components	f_i = 20 MHz				
	second harmonics		–	–45	–	dB
	third harmonics		–	–41	–	dB
THD	total harmonic distortion	f_i = 20 MHz	–	–39	–34	dB
SIGNAL-TO-NOISE RATIO; note 7; see Fig.5						
S/N	signal-to-noise ratio (full scale)	without harmonics; f_{clk} = 80 MHz; f_i = 20 MHz	33	36	–	dB
EFFECTIVE BITS; note 7; see Fig.5						
EB	effective bits	f_{clk} = 80 MHz				
		f_i = 10 MHz	–	5.7	–	bits
		f_i = 20 MHz	–	5.5	–	bits
		f_i = 30 MHz	–	5.1	–	bits

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TWO-TONE; note 8						
TTIR	two-tone intermodulation rejection	f_{clk} = 80 MHz	–	48	–	dB
BIT ERROR RATE						
BER	bit error rate	f_{clk} = 80 MHz; f_i = 20 MHz; V_I = ±16 LSB at code 32	–	10^{-12}	–	times/ samples
Timing (f_{clk} = 80 MHz; C_L = 15 pF); note 9; see Fig.3						
t_{ds}	sampling delay time		–	–	2	ns
t_h	output hold time		5	–	–	ns
t_d	output delay time		–	–	11	ns

Notes

1. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 1 ns.
2. Analog input voltages producing code 00 up to and including 3F:
   a) V_{osB} (voltage offset BOTTOM) is the difference between the analog input which produces data equal to 00 and the reference voltage BOTTOM (V_{RB}) at T_{amb} = 25 °C.
   b) V_{osT} (voltage offset TOP) is the difference between V_{RT} (reference voltage TOP) and the analog input which produces data outputs equal to 3F at T_{amb} = 25 °C.
3. Full-scale sine wave (f_i = 20 MHz; f_{clk} = 80 MHz).
4. The Offset Error (OFE) and Gain Error (GE) are determined by taking results from a simultaneous acquisition on both ADCs of a sine wave greater than full-scale. The occurrences of code 0 and 63 are used to calculate the OFE (mid-scale-to-mid-scale) and the GE (amplitude difference) between the two converters A and B.
5. The –0.5 dB analog bandwidth is determined by the 0.5 dB reduction in the reconstructed output, the input being a full-scale sine wave. It is determined with a beat frequency method; no glitches occurrence.
6. The analog input settling time is the minimum time required for the input signal to be stabilized after a sharp full-scale input (square-wave signal) in order to sample the signal and obtain correct output data.
7. Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8K acquisition points per period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to signal-to-noise ratio: S/N = EB × 6.02 + 1.76 dB.
8. Intermodulation measured relative to either tone with analog input frequencies of 20.0 MHz and 20.1 MHz. The two input signals have the same amplitude and the total amplitude of both signals provides full scale to the converter.
9. Output data acquisition: the output data is available after the maximum delay time of t_d.

Table 1 Output coding and input voltage (typical values; referenced to AGND)

STEP	$V_{I(p-p)}$ A or B (V)	BINARY OUTPUT BITS					
		D5	D4	D3	D2	D1	D0
Underflow	<2.2	0	0	0	0	0	0
0	2.2	0	0	0	0	0	0
1	2.208	0	0	0	0	0	1
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
62	2.692	1	1	1	1	1	0
63	2.7	1	1	1	1	1	1
Overflow	>2.7	1	1	1	1	1	1

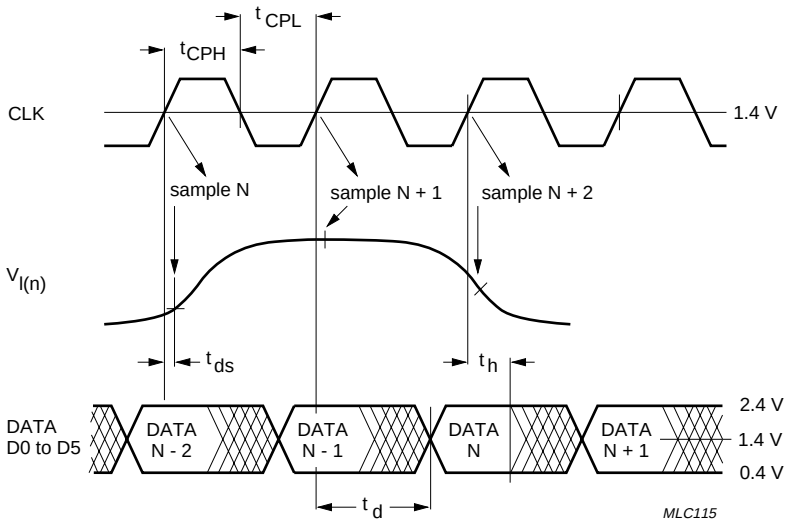


Fig.3 Timing diagram for data output.

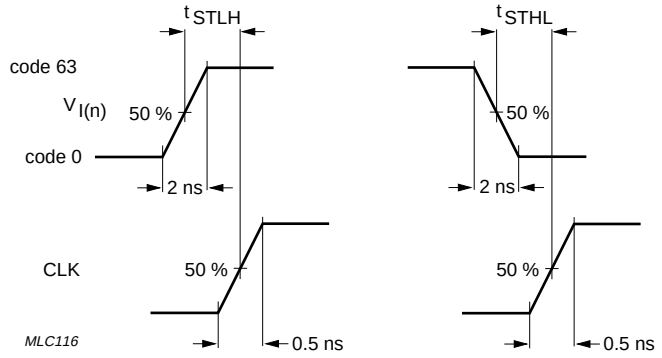
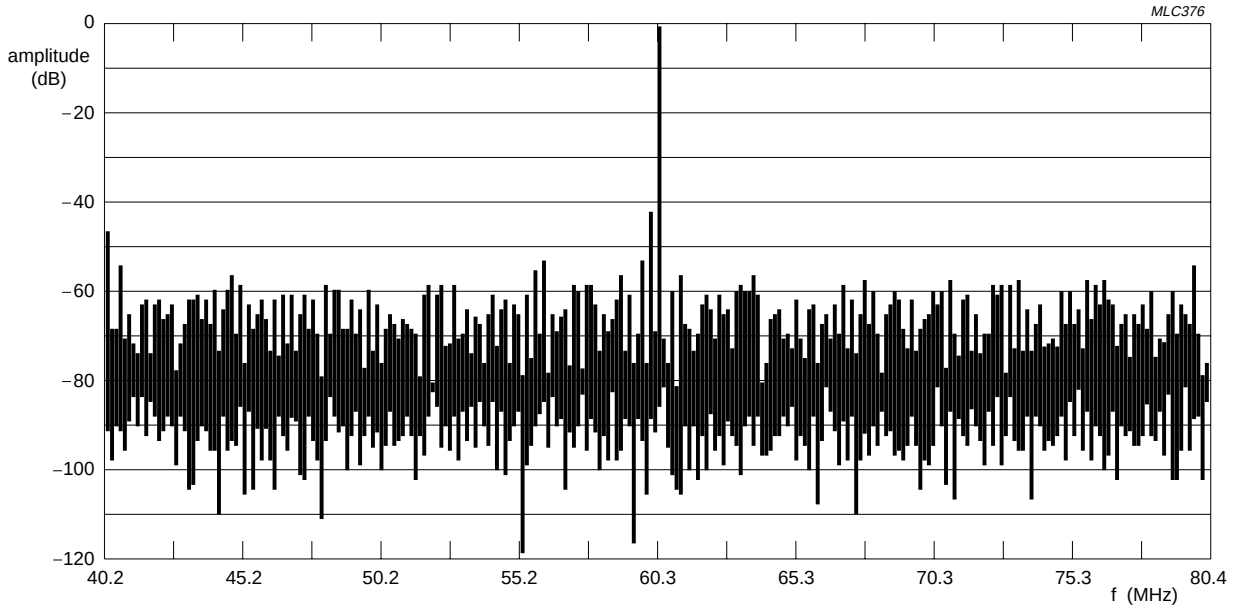


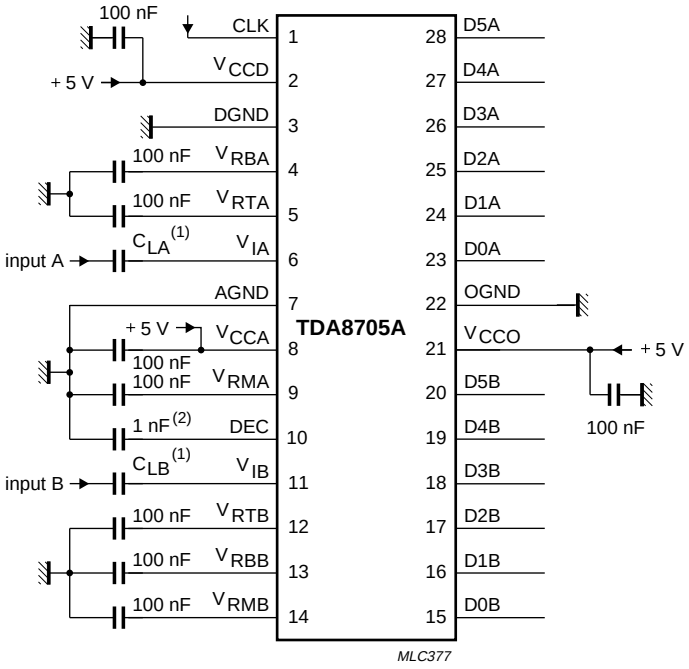
Fig.4 Analog input settling-time diagram.



Effective bits: 5.54; THD = –39.89 dB;
Harmonic levels (dB): 2nd = –46.51; 3rd = –41.21; 4th = –80.65; 5th = –60.16; 6th = –54.51.

Fig.5 Typical Fast Fourier Transform (f_{clk} = 80 MHz; f_i = 20 MHz).

APPLICATION INFORMATION



The analog and digital supplies should be separated and decoupled.

$V_{RT(n)}$, $V_{RM(n)}$ and $V_{RB(n)}$ and DEC inputs are decoupled to AGND.

(1) In the event of AC-coupling, C_{LA} and C_{LB} values are chosen in accordance with the classical low frequencies cut-off formulae

$$f_{CL} = \frac{1}{2 \times \pi \times R_I \times C_L}$$ where input resistance R_I is the value measured under DC conditions.

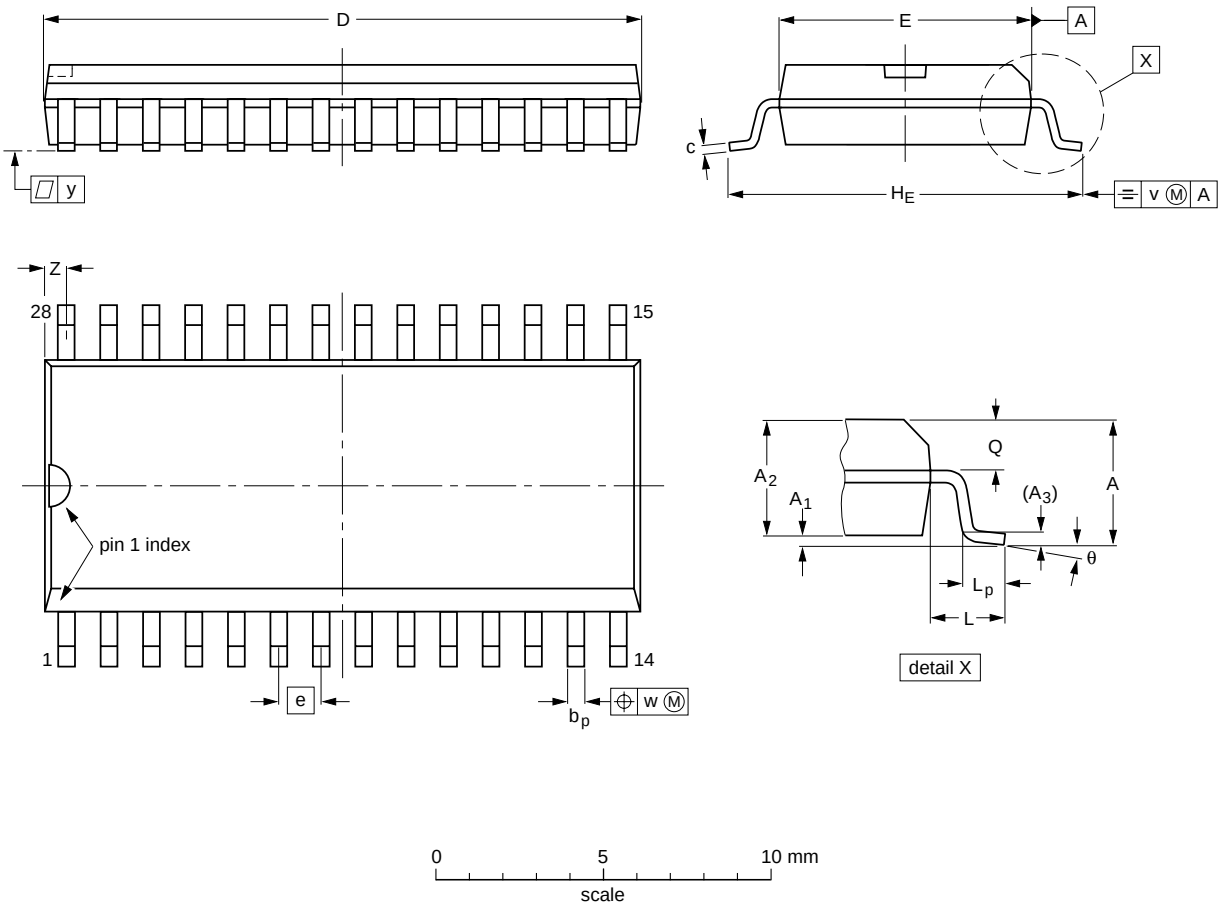
In the event of DC-coupling, C_{LA} and C_{LB} capacitors are omitted. The DC biassing and AC modulation signal directly applied to inputs (pin 6 and 11), must be in the range of $V_{RT(n)} - V_{RB(n)}$.

(2) When pin 10 (DEC) is short-circuited to AGND, an external regulator can be connected to $V_{RT(n)}$ and $V_{RB(n)}$.

Fig.6 Application diagram.

PACKAGE OUTLINE

SO28: plastic small outline package; 28 leads; body width 7.5 mm **SOT136-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~95-01-24~~ 97-05-22

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

NOTES

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