DATA SHEET

TDA8012M

Low power PLL FM demodulator for satellite TV receivers

Product specification

Supersedes data of 1995 Feb 02

File under Integrated Circuits, IC02

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Philips
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Low power PLL FM demodulator for satellite TV receivers

TDA8012M

FEATURES

- High input sensitivity
- Fully balanced two-pin Voltage Controlled Oscillator (VCO)
- Low input impedance (50 Ω)
- Low impedance video baseband output
- Internal voltage stabilizer
- Keyed AFC or peak-to-peak AFC
- Carrier detector
- AGC output
- Suitable for High Definition TV (HDTV).

APPLICATIONS

- Direct Broadcast Satellite (DBS) receivers.

GENERAL DESCRIPTION

The TDA8012M is a sensitive PLL FM demodulator which is used for the second IF in satellite receivers. It provides Automatic Gain Control (AGC) and Automatic Frequency Control (AFC) outputs that can be used to optimize the level and frequency of the input signal. During the searching procedure, the AFC output provides a signal which is used for carrier detection.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		4.5	5.0	5.5	V
I_{CC}	supply current	V_{CC} = 5 V; T_{amb} = 25 °C	50	60	70	mA
V_i	input signal voltage level		53	57	61	dBμV
$V_{o(p-p)}$	video output signal voltage amplitude (peak-to-peak value)	Δf_o = 25 MHz (p-p)	–	1	–	V
f_i	operating input frequency		–	480	–	MHz

ORDERING INFORMATION

TYPE NUMBER	PACKAGES		
	NAME	DESCRIPTION	VERSION
TDA8012M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

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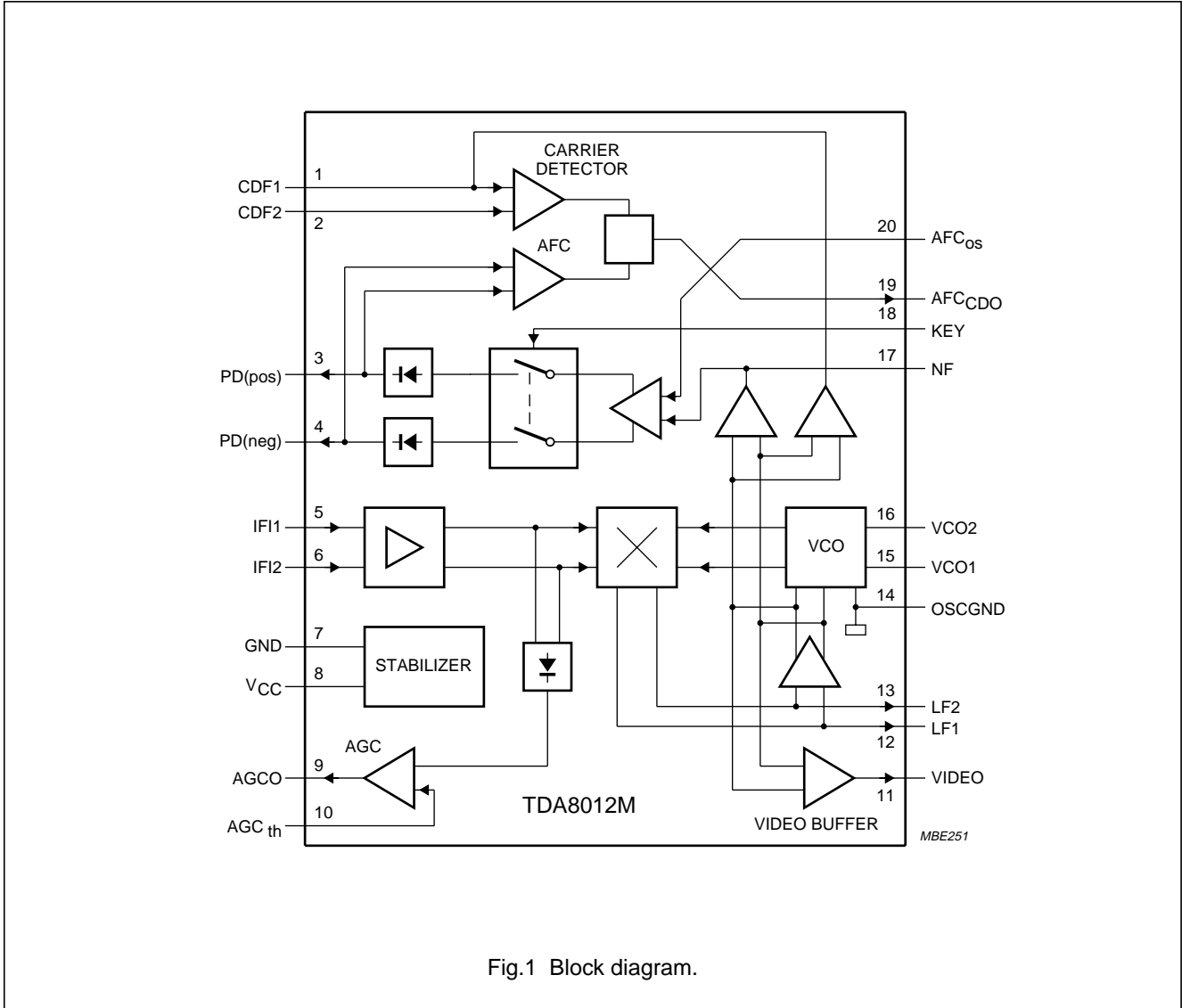
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BLOCK DIAGRAM

Fig.1 Block diagram.

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PINNING

| SYMBOL	PIN	DESCRIPTION
CDF1	1	carrier detector filter 1 input
CDF2	2	carrier detector filter 2 input
PD(pos)	3	positive peak detector output
PD(neg)	4	negative peak detector output
IFI1	5	IF input 1
IFI2	6	IF input 2
GND	7	ground
V_{CC}	8	supply voltage
AGCO	9	AGC output
AGC_{th}	10	AGC threshold voltage input
VIDEO	11	baseband signal output
LF1	12	loop filter 1 input
LF2	13	loop filter 2 input
OSCGND	14	oscillator ground
VCO1	15	oscillator tank circuit 1 input
VCO2	16	oscillator tank circuit 2 input
NF	17	noise filter input
KEY	18	key pulse input
AFC_{CDO}	19	AFC and carrier detector output
AFC_{os}	20	AFC offset input
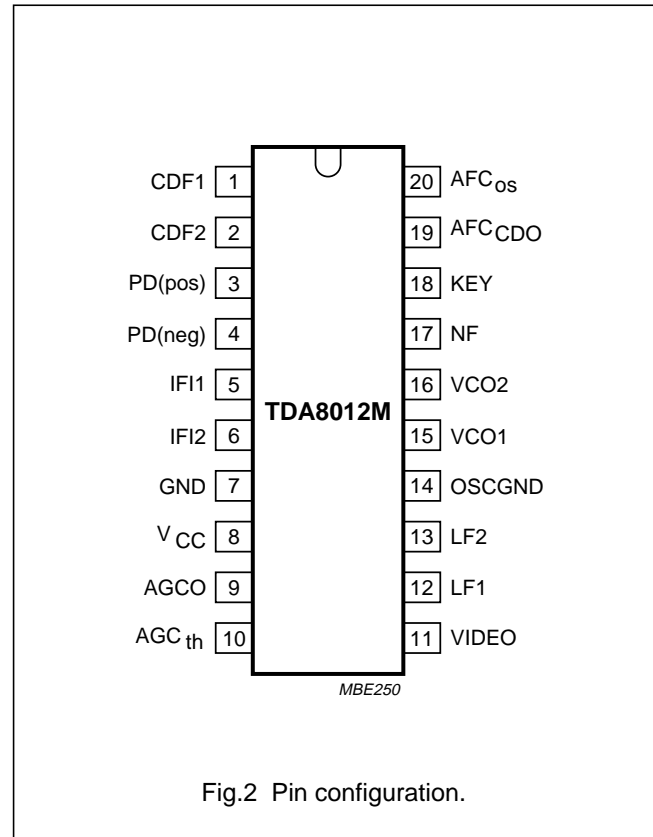
Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8012M is a low power PLL FM demodulator designed for use in satellite TV reception systems.

The demodulator is based on a Phase-Locked Loop (PLL) structure including a fully balanced two-pin VCO. A high gain IF amplifier ensures a high input sensitivity. The video output voltage is supplied via a highly linear video buffer which has a low output impedance. The centre frequency of the VCO and the loop characteristics can be set using external components.

The circuit provides an AGC signal which is used to drive a gain-controlled IF amplifier (TDA8011T or TDA8010M) to ensure a stable PLL demodulation characteristic.

An analog AFC voltage is also made available. This signal can be suitably applied to the input of the ADC port of the PLL frequency synthesizer (TSA5055). The AFC function may be keyed to address D2MAC and MUSE systems.

The TDA8012M includes a Carrier Detector (CD) which is used for channel detection during search procedures.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	−0.3	6.0	V
$V_{i(max)}$	maximum input voltage on all pins	−0.3	V_{CC}	V
$I_{source(max)}$	maximum output source current	–	10	mA
t_{sc}	maximum short-circuit time on all outputs	–	10	s
Z_L	AC load impedance at video output	600	–	Ω
T_{stg}	storage temperature	−55	+150	°C
T_j	junction temperature	–	+150	°C
T_{amb}	operating ambient temperature	−10	+80	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	120	K/W

CHARACTERISTICS

V_{CC} = 5 V; f_i = 480 MHz; V_i = 57 dBμV; T_{amb} = 25 °C; measured in application circuit of Fig.4; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CC}	supply voltage		4.75	5.0	5.25	V
I_{CC}	supply current	note 1	50	60	70	mA
Voltage controlled oscillator						
K_{VCO}	voltage controlled oscillator constant	V_{CC} = 4.75 to 5.25 V; T_{amb} = −10 το +80 °C	22.5	25	27.5	MHz/V
$\delta f_o/\delta T$	voltage controlled oscillator drift	note 2	–	-70×10^{-6}	–	°C⁻¹
Δf_o	voltage controlled oscillator shift	V_{CC} = 4.75 to 5.25 V	–	–	±750	kHz
Frequency demodulator						
V_i	input signal voltage level	note 3	53	57	61	dBμV
Z_i	input impedance	real part; note 4	–	50	–	Ω
		parallel inductive part; note 4	–	130	–	nH
K_{PD}	phase detector constant	V_i = 57 dBμV	–	0.37	–	V/rad
G_v	phase-lock loop gain	drift; note 5	–	2	–	dB
		shift; note 5	–	2	–	dB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$Z_{o(diff)}$	differential output impedance of the phase detector		1.6	2	2.4	kΩ
CR_{PLL}	phase-lock loop capture range	note 6	–	±17	–	MHz
G_{diff}	differential gain	note 7	–	±2	–	%
Φ_{diff}	differential phase	note 7	–	±2	–	deg
IM3	third-order intermodulation distortion	note 8	50	–	–	dB
Video output						
$V_{o(p-p)}$	baseband output signal amplitude (peak-to-peak value)	Δf_o = 25 MHz	0.9	1.0	1.1	V
$V_{O(DC)}$	DC voltage level of video output		2.1	2.35	2.6	V
Z_o	output impedance		–	10	50	Ω
Automatic gain control (note 9)						
AGC_{th}	AGC threshold as a function of the voltage applied to pin 10	I_{AGC} = 0.5 mA; $0.1V_{CC}$	–	–	53	dBμV
		I_{AGC} = 0.5 mA; $0.9V_{CC}$	61	–	–	dBμV
LD	level detector	shift; V_{CC} = 4.75 to 5.25 V	–	1	–	dB
		drift; T_{amb} = −10 to +80 °C	–	1	–	dB
	AGC steepness	I_{AGC} = 0.5 mA; note 10	–	8	–	mA/dB
$V_{sat(AGC)}$	low level AGC output saturation voltage	I_{AGC} = 1 mA	–	200	500	mV
Keying pulse						
t_{key}	input keyed pulse time period		–	64	–	μs
$t_{W(key)}$	keyed pulse width		8	–	–	μs
V_{IL}	LOW level input keyed pulse voltage	key on	–	–	0.8	V
V_{IH}	HIGH level input keyed pulse voltage	key off	2.7	–	–	V
Z_i	input impedance		1	–	–	kΩ
AFC and carrier detector output (note 11)						
$\delta V_{AFC}/\delta f$	AFC steepness		4.9	5.5	6.1	V/MHz
AFC_{shift}	shift of AFC voltage in relation to VCO shift with unmodulated 480 MHz input signal	ΔV_{CC} = ±5%	–	±180	±500	kHz
AFC_{drift}	drift of AFC voltage in relation to the VCO	T_{amb} = 80 °C; note 12	–	−400	–	kHz

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Notes

1. The DC supply current is defined for V_{CC} = 5 V.

2. This typical value of −70 ppm/°C or -70×10^{-6} °C^{-1} can be found in the reference measuring set-up shown in Fig.3. The temperature drift may be adjusted by the temperature coefficient of the external capacitor in the tank circuit.

3. The circuit is designed for an input level of 57 dBμV. The maximum allowable input level is 61 dBμV. However, for levels other than 57 dBμV the optimum loop filter values will be different from those given for the 57 dBμV input level in the reference measuring set-up.

4. The input impedance is reduced to a resistor with a parallel reactance. The values are given at 480 MHz. In order to reduce the radiation from the oscillator to the RF input, it is recommended to use a symmetrical drive.

5. The PLL loop gain shift and drift are given without loop filter shift and drift (non-temperature compensated external components).

6. The capture range or lock-in range is defined as the PLL normal operating range. This value depends strongly on the loop filter characteristics.

7. Measurements with test signals in accordance with CCIR recommendation 473-3. FM modulated signal with DBS parameters:

   a) 625 lines PAL TV system

   b) 25 MHz/V modulator sensitivity

   c) 1 V (p-p) video signal

   d) No SAW filter is used.

8. No SAW filter is used at the input:

   a) 16 MHz/V modulator sensitivity

   b) 4.43 MHz sine wave colour signal [660 mV (p-p)]

   c) 3.25 MHz sine wave luminance signal [700 mV (p-p)]

   d) Two Wegner sound sub-carriers at 7.02 and 7.2 MHz (100 mV)

   e) Intermodulation distance is defined as the distance between the luminance signal and the intermodulation products.

9. The characteristics of the AGC function are measured in the application circuit of Fig.4. The circuit illustrated in Fig.4 has been designed to set the maximum AGC current of 1 mA. The output of the AGC function is capable of handling up to 5 mA. The maximum AGC current can be increased to 5 mA by decreasing the value of the resistor connected between pins 8 and 9.

10. In the application circuit (see Fig.4) the voltage at the AGC output decreases when the IF input level increases above the adjusted AGC threshold.

11. The outputs from the AFC and carrier detector are combined at pin 19 (see Fig.3). During search tuning, when the input frequency is outside the capture range, the combined output (carrier detector function) is at a LOW level (any voltage below $0.6V_{CC}$). When the PLL becomes locked, the voltage at pin 19 rises to a HIGH level ($V_{19} = 0.8V_{CC}$ to V_{CC}). When the input channel is close to the centre frequency, V_{19} falls to the LOW level. As shown in Fig.3, the voltage at pin 19 is now a function of the centre frequency (AFC function). This information may be read by a microcontroller via the ADC of the satellite frequency synthesizer (TSA5055) and the I²C-bus.

12. The drift of the AFC voltage is measured in accordance with the following method:

    a) At room temperature (T_{amb} = 25 °C) the TDA8012M is driven by a 480 MHz unmodulated signal. The voltage at pin 20 must be adjusted to obtain a 1.5 V output at the AFC output (pin 19).

    b) At T_{amb} = 80 °C, due to its temperature drift, the AFC output voltage differs from 1.5 V. The input frequency must, therefore, be adjusted to obtain 1.5 V at the AFC output. The drift of the AFC voltage will then be equal to the difference between the new input frequency and 480 MHz.
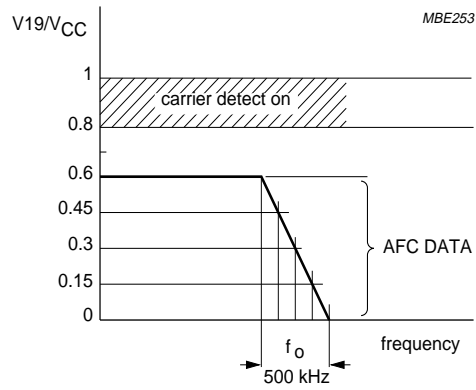
Fig.3 AFC and carrier detector output.
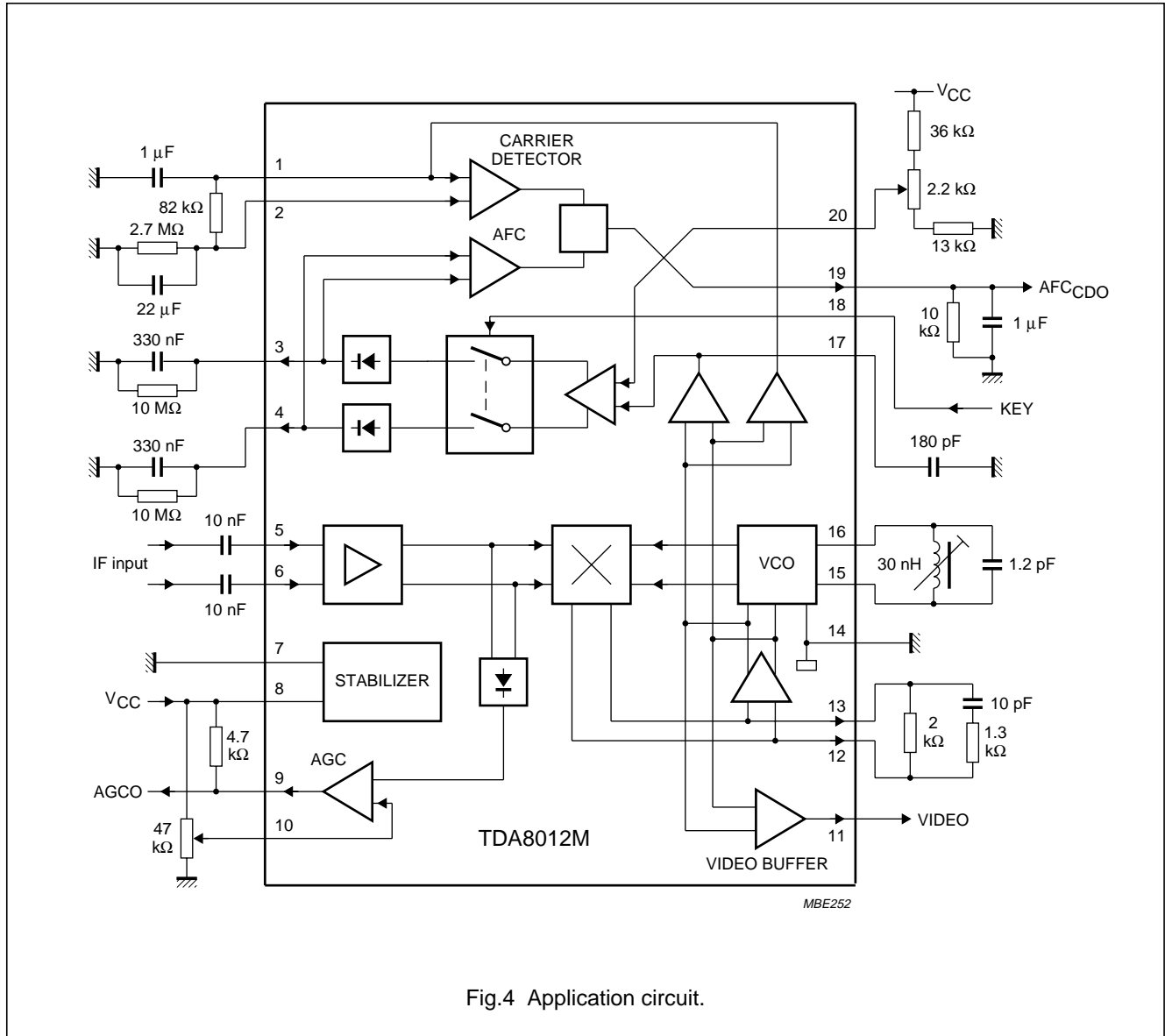
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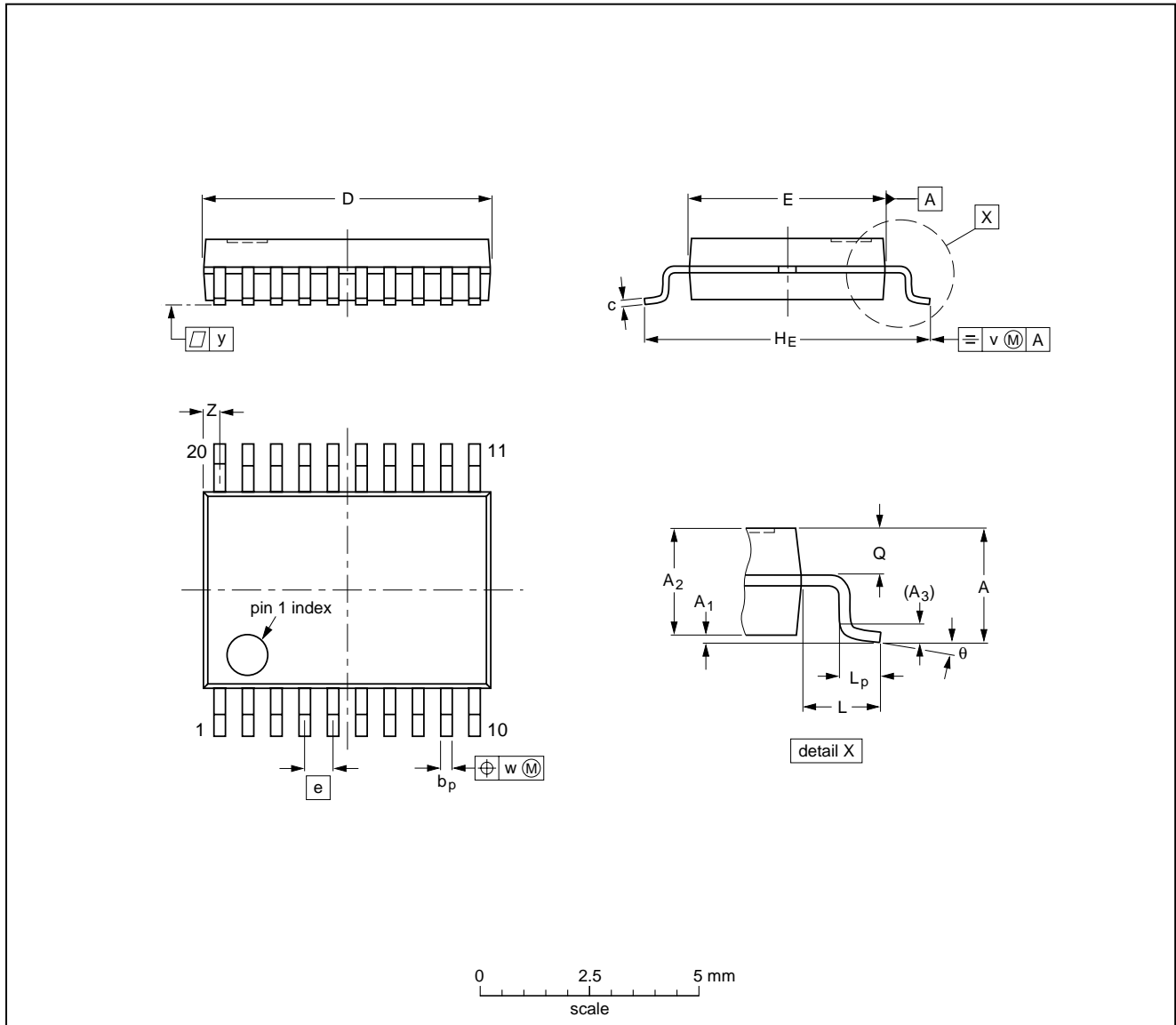

Fig.4 Application circuit.

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PACKAGE OUTLINE

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm

SOT266-1


```
0        2.5        5 mm
|__|__|__|__|__|__|__|
        scale
```

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A₁	A₂	A₃	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT266-1						~~90-04-05~~ 95-02-25

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

NOTES

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NOTES

NOTES

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