DATA SHEET

TDA8004
IC card interface

Product specification
File under Integrated Circuits, IC02

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Philips
Semiconductors

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IC card interface TDA8004

FEATURES

- IC card interface
- 3 or 5 V supply for the IC (GND and V_{DD})
- Step-up converter for V_{CC} generation (separately powered with a 5 V ±10% supply, V_{DDP}, PGND)
- 3 specific protected half duplex bidirectional buffered I/O lines (C4, C7 and C8)
- V_{CC} regulation (5 V ±5% on 2 × 100 nF multilayer ceramic capacitors with ESR, I_{CC} < 65 mA at 4.5 V < V_{DDP} < 6.5 V, current spikes of 40 nAs up to 20 MHz, with controlled rise and fall times, filtered overload detection approximately 90 mA)
- Thermal and short-circuit protections on all card contacts
- Automatic activation and deactivation sequences (initiated by software or by hardware in the event of a short-circuit, card take-off, overheating or supply drop-out)
- Enhanced ESD protection on card side (>6 kV)
- 26 MHz integrated crystal oscillator
- Clock generation for the card up to 20 MHz (divided by 1, 2, 4 or 8 through CLKDIV1 and CLKDIV2 signals) with synchronous frequency changes
- Non-inverted control of RST via pin RSTIN
- ISO 7816, GSM11.11 and EMV (payment systems) compatibility
- Supply supervisor for spikes killing during power-on and power-off
- One multiplexed status signal $\overline{OFF}$.

APPLICATIONS

- IC card readers for banking
- Electronic payment
- Identification
- Pay TV.

GENERAL DESCRIPTION

The TDA8004 is a complete low cost analog interface for asynchronous smart cards. It can be placed between the card and the microcontroller with very few external components to perform all supply protection and control functions.

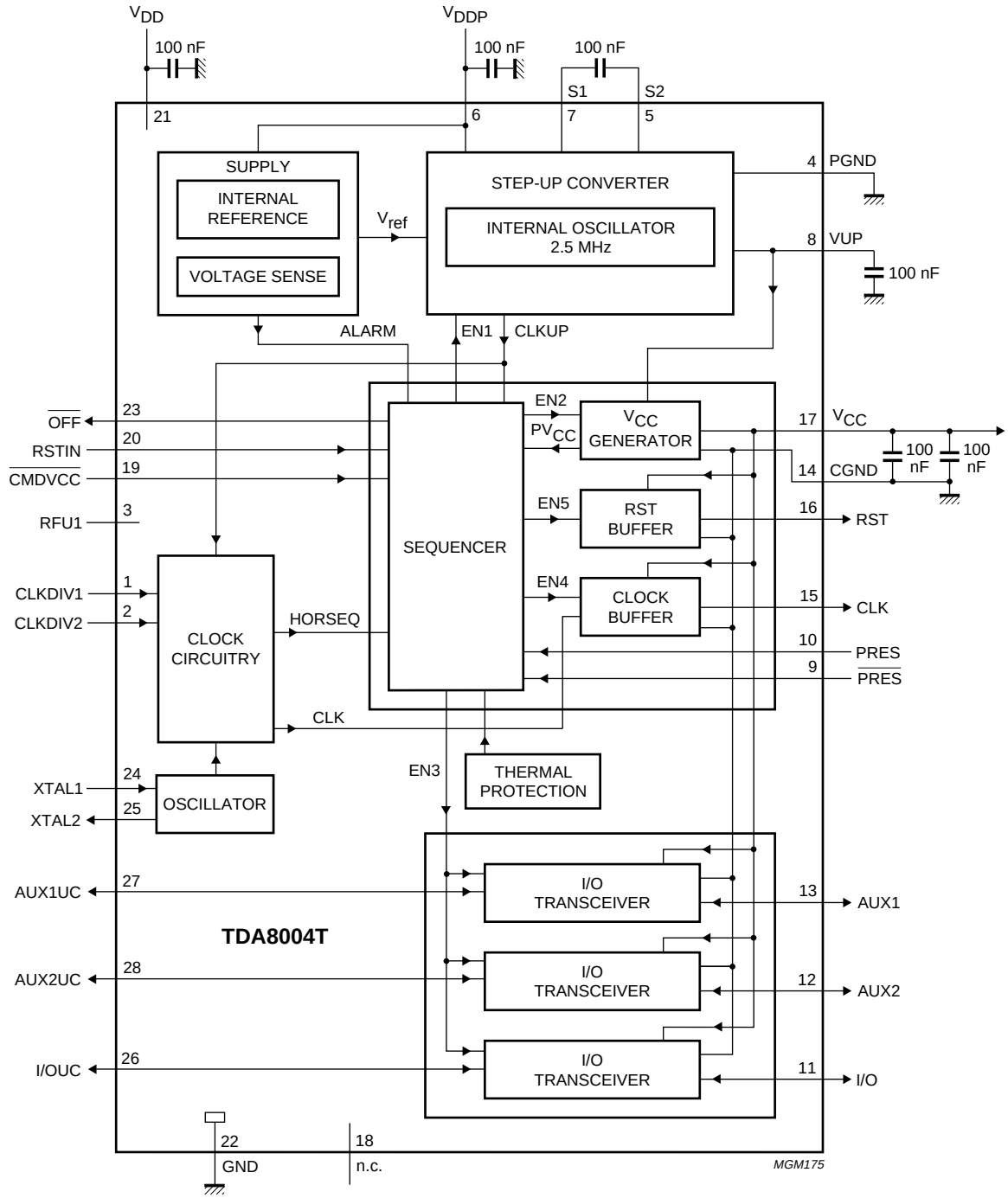
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8004T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		2.7	–	6.5	V
V_{DDP}	step-up supply voltage		4.5	5	6.5	V
I_{DD}	supply current	inactive mode; V_{DD} = 3.3 V; f_{XTAL} = 10 MHz	–	–	1.2	mA
		active mode; V_{DD} = 3.3 V; f_{XTAL} = 10 MHz	–	–	1.5	mA
I_{DDP}	step-up supply current	inactive mode; V_{DDP} = 5 V; f_{XTAL} = 10 MHz	–	–	0.1	mA
		active mode; V_{DDP} = 5 V; f_{XTAL} = 10 MHz	–	–	18	mA
Card supplies						
V_{CC}	card supply voltage	DC load <65 mA	4.75	–	5.25	V
		AC current spikes of 40 nAs	4.75	–	5.25	V
I_{CC}	card supply current	from 0 to 5 V, on 2 × 100 nF	–	–	65	mA
General						
f_{CLK}	card clock frequency		0	–	20	MHz
t_{de}	deactivation cycle duration		60	80	100	µs
P_{tot}	continuous total power dissipation	T_{amb} = –25 to +85 °C	–	–	0.56	W
T_{amb}	operating ambient temperature		–25	–	+85	°C

BLOCK DIAGRAM



All capacitors are mandatory.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
CLKDIV1	1	I	control with CLKDIV2 for choosing CLK frequency
CLKDIV2	2	I	control with CLKDIV1 for choosing CLK frequency
RFU1	3	I	reserved for future use (to be connected to V_{DD} or microcontroller I/O; active HIGH)
PGND	4	supply	power ground for step-up converter
S2	5	I/O	capacitance connection for step-up converter (a 100 nF capacitor must be connected between pins S1 and S2)
V_{DDP}	6	supply	power supply voltage for step-up converter
S1	7	I/O	capacitance connection for step-up converter (a 100 nF capacitor must be connected between pins S1 and S2)
VUP	8	I/O	output of step-up converter (a 100 nF capacitor must be connected to PGND)
$\overline{\text{PRES}}$	9	I	card presence contact input (active LOW)
PRES	10	I	card presence contact input (active HIGH)
I/O	11	I/O	data line to and from card (C7) (internal 10 kΩ pull-up resistor connected to V_{CC})
AUX2	12	I/O	auxiliary line to/from card (C8) (internal 10 kΩ pull-up resistor connected to V_{CC})
AUX1	13	I/O	auxiliary line to/from card (C4) (internal 10 kΩ pull-up resistor connected to V_{CC})
CGND	14	supply	ground for card signals
CLK	15	O	clock to card (C3)
RST	16	O	card reset (C2)
V_{CC}	17	O	supply for card (C1) (decouple with 200 nF capacitor)
n.c.	18	–	not connected
$\overline{\text{CMDVCC}}$	19	I	start activation sequence input from microcontroller (active LOW)
RSTIN	20	I	card reset input from microcontroller (active HIGH)
V_{DD}	21	supply	supply voltage
GND	22	supply	ground
$\overline{\text{OFF}}$	23	O	NMOS interrupt to microcontroller (active LOW) with 20 kΩ pull-up resistor connected to V_{DD}
XTAL1	24	I	crystal connection or input for external clock
XTAL2	25	O	crystal connection
I/OUC	26	I/O	microcontroller data I/O line (internal 10 kΩ pull-up resistor connected to V_{DD})
AUX1UC	27	I/O	auxiliary line to/from microcontroller (internal 10 kΩ pull-up resistor connected to V_{DD})
AUX2UC	28	I/O	auxiliary line to/from microcontroller (internal 10 kΩ pull-up resistor connected to V_{DD})

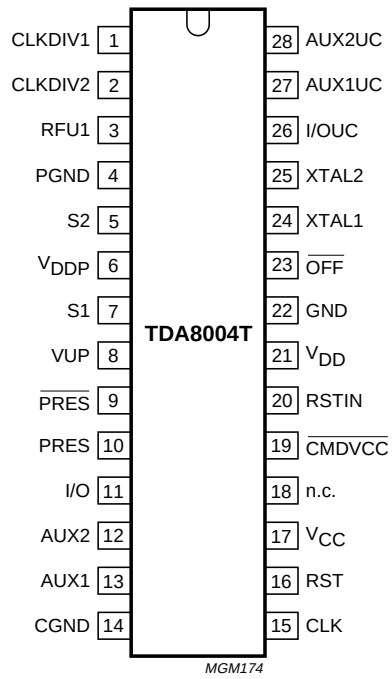


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Power supply

The supply pins for the IC are V_{DD} and GND. V_{DD} should be in the range from 2.7 to 6.5 V. All card contacts remain inactive during powering up or powering down.
The sequencer is not activated until V_{DD} reaches $V_{th2} + V_{hys(th2)}$. When V_{DD} falls below V_{th2}, an automatic deactivation of the contacts is performed.

For generating a 5 V ±5% V_{CC} supply to the card, an integrated voltage doubler is incorporated. This step-up converter should be separately supplied by V_{DDP} and PGND (from 4.5 to 6.5 V).

The supply voltages V_{DD} and V_{DDP} may be applied to the IC in any time sequence.

If a voltage between 7 and 9 V is available within the application, this voltage may be tied to pin VUP, thus blocking the step-up converter. In this case, V_{DDP} must be tied to V_{DD} and the capacitor between pins S1 and S2 may be omitted.

Voltage supervisor

This block surveys the V_{DD} supply. A defined reset pulse of approximately 10 ms (t_W) is used internally for maintaining the IC in the inactive mode during powering up or powering down of V_{DD} (see Fig.3).

As long as V_{DD} is less than $V_{th2} + V_{hys2}$, the IC will remain inactive whatever the levels on the command lines. This also lasts for the duration of t_W after V_{DD} has reached a level higher than $V_{th2} + V_{hys(th2)}$.

The system controller should not try to start an activation during this time.

When V_{DD} falls below V_{th2}, a deactivation sequence of the contacts is performed.

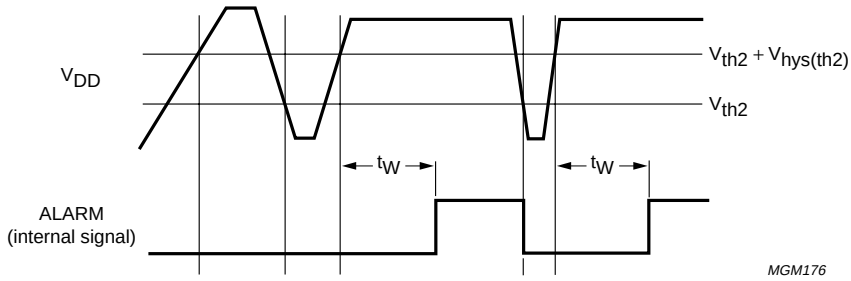


Fig.3 Alarm as a function of V_{DD} (t_W = 10 ms).

Clock circuitry

The clock signal (CLK) to the card is either derived from a clock signal input on pin XTAL1 or from a crystal up to 26 MHz connected between pins XTAL1 and XTAL2.

The frequency may be chosen at f_{XTAL}, $\frac{1}{2}f_{XTAL}$, $\frac{1}{4}f_{XTAL}$ or $\frac{1}{8}f_{XTAL}$ via pins CLKDIV1 and CLKDIV2.

The frequency change is synchronous, which means that during transition, no pulse is shorter than 45% of the smallest period and that the first and last clock pulse around the change has the correct width.

In the case of f_{XTAL}, the duty factors dependant on the signal at XTAL1.

In order to reach a 45 to 55% duty factor on pin CLK the input signal on XTAL1 should have a duty factor of 48 to 52% and transition times of less than 5% of the input signal period.

If a crystal is used with f_{XTAL}, the duty factor on pin CLK may be 45 to 55% depending on the layout and on the crystal characteristics and frequency.

In the other cases, it is guaranteed between 45 and 55% of the period.

The crystal oscillator runs as soon as the IC is powered up. If the crystal oscillator is used, or if the clock pulse on XTAL1 is permanent, then the clock pulse will be applied to the card according to the timing diagram of the activation sequence (see Fig.4).

If the signal applied to XTAL1 is controlled by the system controller, then the clock pulse will be applied to the card when the system controller will send it (after completion of the activation sequence).

Table 1 Clock circuitry definition

CLKDIV1	CLKDIV2	CLK
0	0	$\frac{1}{8}f_{XTAL}$
0	1	$\frac{1}{4}f_{XTAL}$
1	1	$\frac{1}{2}f_{XTAL}$
1	0	f_{XTAL}

I/O circuitry

The three data lines I/O, AUX1 and AUX2 are identical.

The Idle state is realized by both lines (I/O and I/OUC) being pulled HIGH via a 10 kΩ resistor (I/O to V_{CC} and I/OUC to V_{DD}).

I/O is referenced to V_{CC}, and I/OUC to V_{DD}, thus allowing operation with $V_{CC} \neq V_{DD}$.

The first side on which a falling edge occurs becomes the master. An anti-latch circuit disables the detection of falling edges on the other line, which becomes a slave.

After a time delay (approximately 200 ns), the N transistor on the slave side is turned on, thus transmitting the logic 0 present on the master side.

When the master side returns to logic 1, the P transistor on the slave side is turned on during the time delay $t_{d(edge)}$, and then both sides return to their Idle states.

The maximum frequency on these lines is 1 MHz.

Logic circuitry

INACTIVE STATE

After power-on reset, the circuit enters the inactive state. A minimum number of circuits are active while waiting for the microcontroller to start a session.

- All card contacts are inactive (approximately 200 Ω to GND)
- I/OUC, AUX1UC and AUX2UC are high impedance (10 kΩ pull-up resistor connected to V_{DD})
- Voltage generators are stopped
- XTAL oscillator is running
- Voltage supervisor is active.

Activation sequence

After power-on and, after the internal pulse width delay, the system controller may check the presence of the card with the signal $\overline{OFF}$ ($\overline{OFF}$ = HIGH while $\overline{CMDVCC}$ is HIGH means that the card is present; $\overline{OFF}$ = LOW while $\overline{CMDVCC}$ is HIGH means that no card is present).

If the card is in the reader, the system controller may start a card session by pulling $\overline{CMDVCC}$ LOW.

The following sequence then occurs (see Fig.4):

- $\overline{CMDVCC}$ is pulled LOW (t_0)
- The voltage doubler is started ($t_1 \sim t_0$)
- V_{CC} rises from 0 to 5 V with a controlled slope ($t_2 = t_1 + \frac{1}{2}3T$) (I/O, AUX1 and AUX2 follow V_{CC} with a slight delay
- I/O, AUX1 and AUX2 are enabled ($t_3 = t_1 + 4T$)
- CLK is applied to the C3 contact (t_4)
- RST is enabled ($t_5 = t_1 + 7T$).

The clock may be applied to the card in the following way:

Set RSTIN HIGH before setting $\overline{CMDVCC}$ LOW, and reset it LOW between t_3 and t_5; CLK will start at this moment. RST will remain LOW until t_5, where RST is enabled to be the copy of RSTIN. After t_5, RSTIN has no further action on CLK. This is to allow a precise count of CLK pulses before toggling RST.

If this feature is not needed, then $\overline{CMDVCC}$ may be set LOW with RSTIN LOW. In this case, CLK will start at t_3, and after t_5, RSTIN may be set HIGH in order to get the Answer To Request (ATR) from the card.

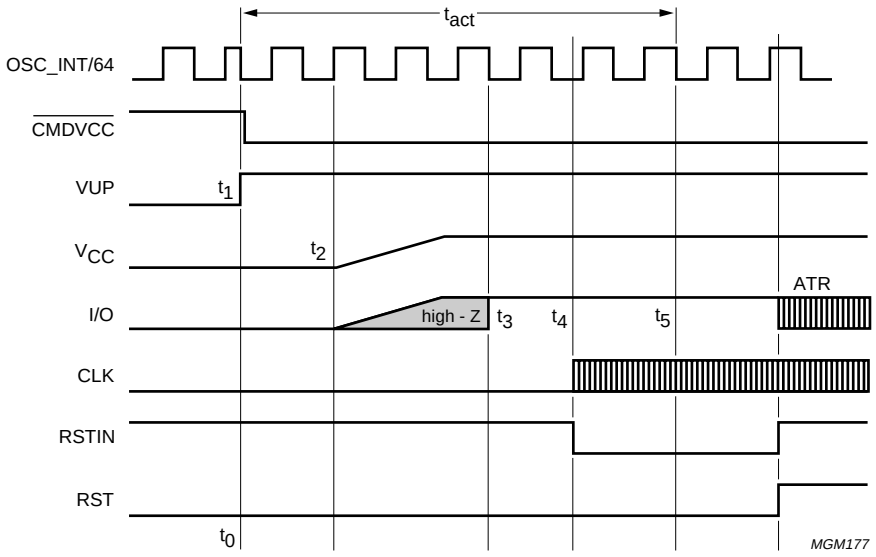


Fig.4 Activation sequence.

Active state

When the activation sequence is completed, the TDA8004 will be in the active state. Data is exchanged between the card and the microcontroller via the I/O lines.
The TDA8004 is designed for cards without V_{PP} (this is the voltage required to program or ensure the internal non-voltage memory).

Deactivation sequence

When a session is completed, the microcontroller sets the $\overline{\text{CMDVCC}}$ line to the HIGH state. The circuit then executes an automatic deactivation sequence by counting the sequencer back and ends in the inactive state (see Fig.5):

- RST goes LOW $\rightarrow$ ($t_{11} = t_{10}$)
- CLK is stopped $\rightarrow$ ($t_{12} = t_{11} + \frac{1}{2}T$)
- I/O, AUX1 and AUX2 are output into high-impedance state $\rightarrow$ ($t_{13} = t_{11} + T$) (10 kΩ pull-up resistor connected to V_{CC})
- V_{CC} falls to zero $\rightarrow$ ($t_{14} = t_{11} + \frac{1}{2}3T$)
- VUP falls to zero $\rightarrow$ ($t_{15} = t_{11} + 5T$) and all card contacts become low-impedance to GND (I/OUC, AUX1UC and AUX2UC remain pulled up to V_{DD} via a 10 kΩ resistor).

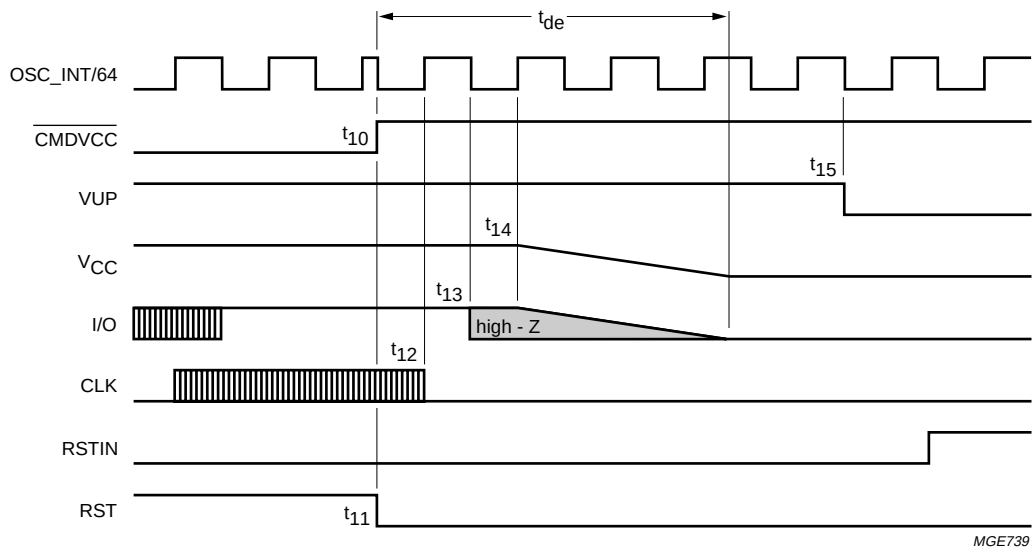


Fig.5 Deactivation sequence.

Fault detection

The following fault conditions are monitored by the circuit:

- Short-circuit or high current on V_{CC}
- Removing card during transaction
- V_{DD} dropping
- Overheating.

There are two different cases:

1. $\overline{\text{CMDVCC}}$ HIGH: (outside a card session) then, $\overline{\text{OFF}}$ is LOW if the card is not in the reader, and HIGH if the card is in the reader. A supply voltage drop is detected by the supply supervisor, generate an internal power-on reset pulse, but don't act upon $\overline{\text{OFF}}$. The card is not powered-up, so no short-circuit or overheating is detected.
2. $\overline{\text{CMDVCC}}$ LOW: (within a card session) then, $\overline{\text{OFF}}$ falls LOW if the card is extracted, or if a short-circuit has occurred on V_{CC}, or if the temperature on the IC has become too high. As soon as the fault is detected, an emergency deactivation is automatically performed (see Fig.6). When the system controller sets $\overline{\text{CMDVCC}}$ back to HIGH, it may sense $\overline{\text{OFF}}$ again in order to distinguish between a hardware problem or a card extraction. If a supply voltage drop is detected whilst the card is activated, then an emergency deactivation will be performed, but $\overline{\text{OFF}}$ remains HIGH.

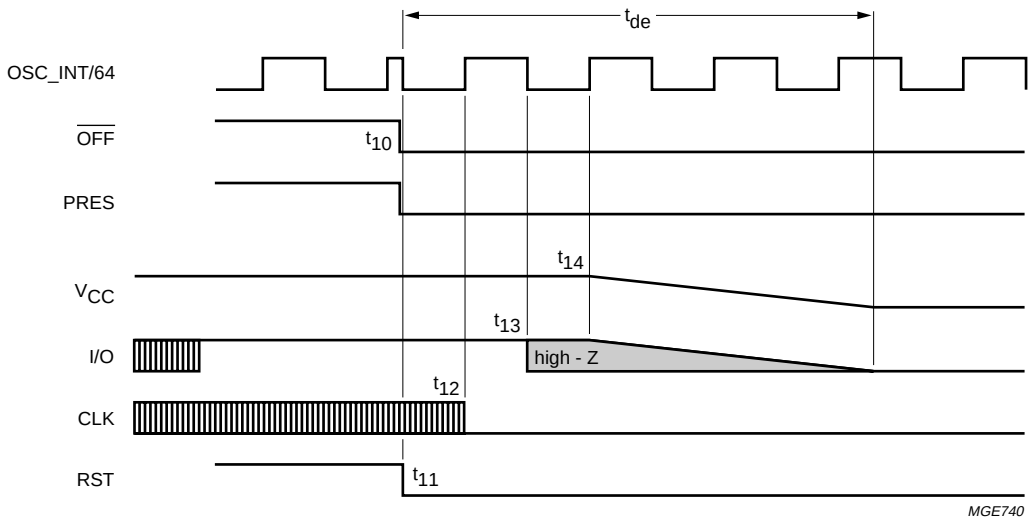


Fig.6 Emergency deactivation sequence.

V_{CC} regulator

V_{CC} buffer is able to deliver up to 65 mA continuously.

It has an internal overload detection at approximately 90 mA.

This detection is internally filtered, allowing spurious current pulses up to 200 mA to be drawn by the card without causing a deactivation.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); notes 1 and 2.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}, V_{DDP}	supply voltage		–0.3	+7	V
V_{n1}	voltage on pins: XTAL1, XTAL2, RSTIN, AUX2UC, AUX1UC, I/OUC, CLKDIV1, CLKDIV2, $\overline{CMDVCC}$ and $\overline{OFF}$		–0.3	+7	V
V_{n2}	voltage on card contact pins PRES and $\overline{PRES}$		–0.3	+7	V
V_{n3}	voltage on pin VUP		–	+9	V
T_{stg}	IC storage temperature		–55	+125	°C
P_{tot}	continuous total power dissipation	T_{amb} = –25 to +85 °C	–	0.56	W
$T_{j(max)}$	maximum junction temperature		–	+150	°C
V_{es1}	electrostatic voltage on pins: I/O, RST, V_{CC}, AUX1, CLK, AUX2, PRES and $\overline{PRES}$		–6	+6	kV
V_{es2}	electrostatic voltage on all other pins		–2	+2	kV

Notes

1. All card contacts are protected against any short with any other card contact.
2. Stress beyond these levels may cause permanent damage to the device. This is a stress rating only and functional operation of the device under this condition is not implied.

HANDLING

Every pin withstands the ESD test according to MIL-STD-883C class 3 for card contacts, class 2 for the remaining. Method 3015 (HBM; 1500 Ω; 100 pF) 3 pulses positive and 3 pulse negative on each pin referenced to ground.

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	70	K/W

CHARACTERISTICS

V_{DD} = 3.3 V; V_{DDP} = 5 V; T_{amb} = 25 °C; all parameters remain within limits but are only statistically tested for the temperature range; f_{XTAL} = 10 MHz; unless otherwise specified; all currents flowing into the IC are positive.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Temperature						
T_{amb}	operating ambient temperature		–25	–	+85	°C
Supplies						
V_{DD}	supply voltage		2.7	–	6.5	V
V_{DDP}	supply voltage for the voltage doubler		4.5	5	6.5	V
$V_{o(VUP)}$	output voltage on pin VUP from step-up converter		–	5.5	–	V
$V_{i(VUP)}$	input voltage to be applied on VUP in order to block the step-up converter		7	–	9	V
I_{DD}	supply current	inactive mode	–	–	1.2	mA
		active mode; CLK = XTAL; C_L = 30 pF	–	–	1.5	mA
I_P	supply current for the step-up converter	inactive mode	–	–	0.1	mA
		active mode; CLK = XTAL; C_L = 30 pF	–	–	18	mA
V_{th2}	threshold voltage on V_{DD} (falling)		2.2	–	2.4	V
$V_{hys(th2)}$	hysteresis on V_{th2}		50	–	150	mV
t_W	width of the internal ALARM pulse		6	–	20	ms
Card supply voltage (V_{CC}) (a ceramic multilayer capacitance with low ESR of 2 × 100 nF should be used in order to meet these specifications)						
V_{CC}	output voltage	inactive mode; no load	–	–	0.1	V
		inactive mode; I_{CC} = 1 mA	–	–	0.4	V
		active mode; I_{CC} < 65 mA DC	4.75	–	5.25	V
		active mode; single current pulse of 100 mA; 2 µs	4.75	–	5.25	V
		active mode; current pulses of 40 nAs with I_{CC} < 200 mA; t < 400 ns; f < 20 MHz	4.75	–	5.25	V
I_{CC}	output current	from 0 to 5 V; C = 100 nF	–	–	65	mA
		V_{CC} short-circuit to ground	–	–	120	mA
SR	slew rate	up and down	0.11	0.17	0.22	V/µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal connections (XTAL1 and XTAL2)						
C_{ext}	external capacitors on XTAL1 and XTAL2	depending on specification of crystal or resonator used	–	–	15	pF
$f_{i(XTAL)}$	crystal input frequency		2	–	26	MHz
$V_{IH(XTAL)}$	HIGH-level input voltage on XTAL1		$0.8V_{DD}$	–	V_{DD} + 0.2	V
$V_{IL(XTAL)}$	LOW-level input voltage on XTAL1		–0.3	–	$0.2V_{DD}$	V
Data lines (I/O, I/OUC, AUX1, AUX2, AUX1UC and AUX2UC) (I/O, AUX1 and AUX2 have internal 10 kΩ pull-up resistors at V_{CC}; I/OUC, AUX1UC and AUX2UC have internal 10 kΩ pull-up resistors at V_{DD})						
$V_{OH(I/O)}$	HIGH-level output voltage on pin I/O	I_{OH} = –60 µA	V_{CC} – 0.9	–	V_{CC} + 0.1	V
		I_{OH} = –100 µA	3.5	–	–	V
I_{edge}	current from I/O when active pull-up active	$V_{OH} = V_{CC}$ – 0.5 V	–1	–	–	mA
V_{OL}	LOW-level output voltage on pins I/O, AUX1 and AUX2	$I_{I/O}$ = 1 mA	–	–	300	mV
V_{OH}	HIGH-level output voltage on pins I/OUC, AUX1UC and AUX2UC	I_{OH} = –20 µA	$0.75V_{DD}$	–	V_{DD} + 0.2	V
V_{OL}	LOW-level output voltage on pins I/OUC, AUX1UC and AUX2UC	$I_{I/OUC}$ = 1 mA	–	–	300	mV
V_{IH}	HIGH-level input voltage on pins I/O, AUX1 and AUX2		1.8	–	V_{CC} + 0.3	V
V_{IL}	LOW-level input voltage on pins I/O, AUX1 and AUX2		–0.3	–	+0.8	V
I_{LIH}	input leakage current HIGH on pins I/O, AUX1 and AUX2	$V_{IH} = V_{CC}$	–	–	10	µA
I_{IL}	LOW-level input current on pins I/O, AUX1 and AUX2	V_{IL} = 0 V	–	–	600	µA
V_{IH}	HIGH-level input voltage on pins I/OUC, AUX1UC and AUX2UC		$0.7V_{DD}$	–	V_{DD} + 0.3	V
V_{IL}	LOW-level input voltage on pins I/OUC, AUX1UC and AUX2UC		0	–	$0.3V_{DD}$	V
$\lvert I_{LIH} \rvert$	input leakage current HIGH on pins I/OUC, AUX1UC and AUX2UC	$V_{IH} = V_{DD}$	–	–	10	µA
I_{IL}	LOW-level input on pins I/OUC, AUX1UC and AUX2UC	V_{IL} = 0 V	–	–	600	µA
$V_{inactive}$	voltage on pins I/O, AUX1 and AUX2 outside a session	no load	–	–	0.1	V
		$I_{I/O}$ = 1 mA	–	–	0.3	V
$R_{pu(int)}$	internal pull-up resistance between pins I/OUC, AUX1UC, AUX2UC and V_{DD}		9	11	13	kΩ
$R_{pu(int)}$	internal pull-up resistance between pins I/O, AUX1, AUX2 and V_{CC}		9	11	13	kΩ
$t_{d(edge)}$	delay between falling edge on pins I/OUC and I/O (or I/O and I/OUC)		–	200	–	ns
t_r	rise time	C_i = 30 pF	–	–	1	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_f	fall time	C_o = 30 pF	–	–	0.1	µs
$f_{I/O(max)}$	maximum frequency on pins I/O, AUX1 and AUX2		–	–	1	MHz
Internal oscillator						
$f_{osc(int)}$	frequency of internal oscillator		2.2	–	3.2	MHz
Reset output to the card (RST)						
$V_{o(inactive)}$	output voltage in inactive mode	no load	0	–	0.1	V
		I_o = 1 mA	0	–	0.3	V
$t_{d(RSTIN-RST)}$	delay between pins RSTIN and RST	RST enabled	–	–	2	µs
V_{OL}	LOW-level output voltage	I_{OL} = 200 µA	0	–	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = –200 µA	4.3	–	V_{CC}	V
		I_{OH} = –50 µA	V_{CC} – 0.5	–	V_{CC}	V
t_r, t_f	rise and fall times	C_o = 30 pF	–	–	0.1	µs
Clock output to the card (CLK)						
$V_{o(inactive)}$	output voltage in inactive mode	no load	0	–	0.1	V
		I_o = 1 mA	0	–	0.3	V
V_{OL}	LOW-level output voltage	I_{OL} = 200 µA	0	–	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = –200 µA	V_{CC} – 0.5	–	V_{CC}	V
		I_{OH} = –50 µA	V_{CC} – 0.5	–	V_{CC}	V
t_r, t_f	rise and fall times	C_L = 30 pF; note 1	–	–	8	ns
δ	duty factor (except for f_{XTAL})	C_L = 30 pF; note 1	45	–	55	%
SR	slew rate (rise and fall)	C_L = 30 pF	0.2	–	–	V/ns
Logic inputs (CLKDIV1 CLKDIV2,PRES, $\overline{\text{PRES}}$, $\overline{\text{CMDVCC}}$, RSTIN and RFU1); note 2						
V_{IL}	LOW-level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	–	V
$\lvert I_{LIL} \rvert$	input leakage current LOW	$0 < V_{IL} < V_{DD}$	–	–	10	µA
$\lvert I_{LIH} \rvert$	input leakage current HIGH	$0 < V_{IH} < V_{DD}$	–	–	10	µA
$\overline{\text{OFF}}$ output ($\overline{\text{OFF}}$ has an internal 20 kΩ pull-up resistor to V_{DD})						
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	–	–	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = –15 µA	$0.75V_{DD}$	–	–	V
Protections						
T_{sd}	shut-down temperature		–	135	–	°C
$I_{CC(sd)}$	shut-down current at V_{CC}		–	–	110	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing						
t_{act}	activation sequence duration		–	180	220	µs
t_{de}	deactivation sequence duration		60	80	100	µs
t_3	start of the window for sending CLK to the card		–	–	130	µs
t_5	end of the window for sending CLK to the card		140	–	–	µs

Notes

1. The transition times and duty factor definitions are shown in Fig.7; $\delta = \frac{t_1}{(t_1 + t_2)}$
2. $\overline{\text{PRES}}$ and $\overline{\text{CMDVCC}}$ are active LOW; RSTIN and PRES are active HIGH; for CLKDIV1 and CLKDIV2 see Table 1; RFU1 must be tied HIGH.

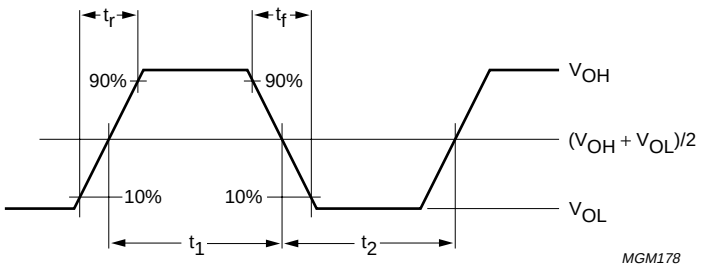


Fig.7 Definition of transition times.

APPLICATION INFORMATION

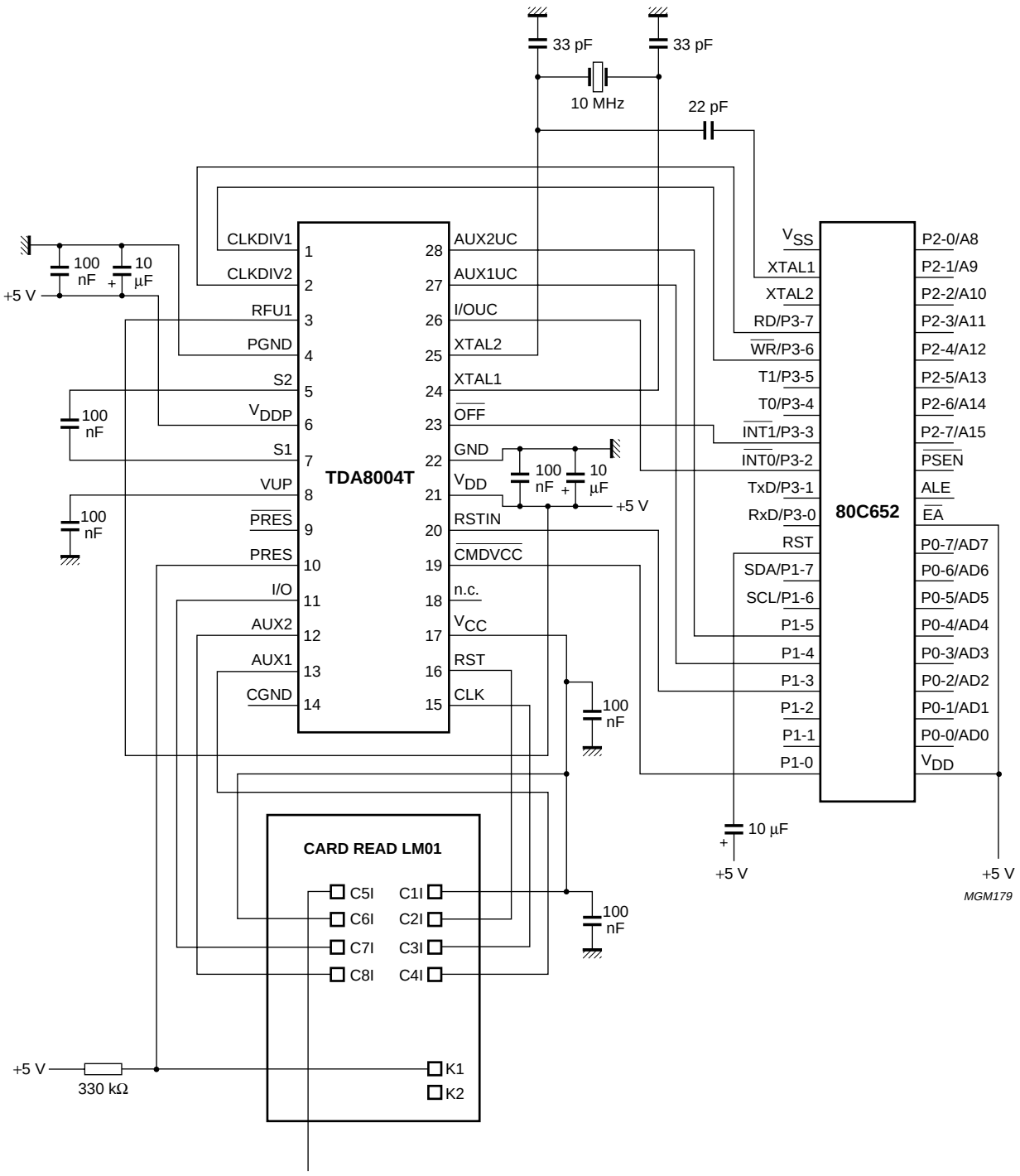
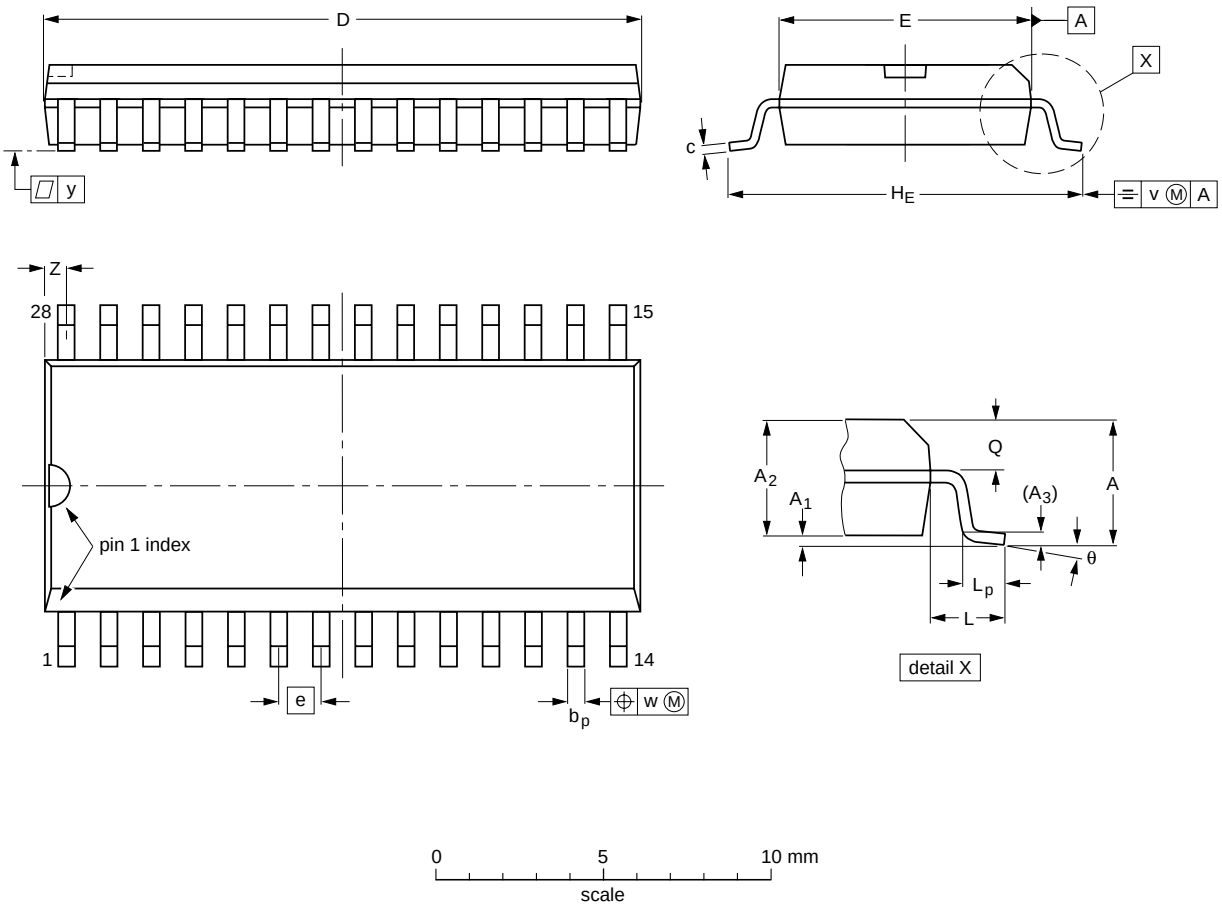


Fig.8 Application diagram.

PACKAGE OUTLINE

SO28: plastic small outline package; 28 leads; body width 7.5 mm **SOT136-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~95-01-24~~ 97-05-22

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
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