INTEGRATED CIRCUITS

DATA SHEET

TDA1563Q

2 × 25 W high efficiency car radio power amplifier

Preliminary specification
File under Integrated Circuits, IC01

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Philips Semiconductors

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FEATURES

- Low dissipation due to switching from Single-Ended (SE) to Bridge-Tied Load (BTL) mode
- Differential inputs with high Common Mode Rejection Ratio (CMRR)
- Mute/standby/operating (mode select pin)
- Zero crossing mute circuit
- Load dump protection circuit
- Short-circuit safe to ground, to supply voltage and across load
- Loudspeaker protection circuit
- Device switches to single-ended operation at excessive junction temperature
- Thermal protection at high junction temperature (170 °C)
- Diagnostic information (clip and protection/prewarning)
- Clipping information is selectable between THD = 2.5% or 10%.

GENERAL DESCRIPTION

The TDA1563Q is a monolithic power amplifier in a 17 lead Single In-Line (SIL) plastic power package. It contains two identical 25 W amplifiers. The dissipation is minimized by switching from SE to BTL mode, only when a higher output voltage swing is needed. The device is primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	DC biased	6.0	14.4	18.0	V
		non operating	–	–	30	V
		load dump	–	–	45	V
I_{ORM}	repetitive peak output current		–	–	4	A
I_q	quiescent supply current	$R_L = \infty$	–	95	150	mA
I_{stb}	standby current		–	1	50	μA
$\|Z_i\|$	input impedance		90	120	150	kΩ
P_o	output power	$R_L = 4\ \Omega$; EIAJ	–	38	–	W
		$R_L = 4\ \Omega$; THD = 10%	23	25	–	W
		$R_L = 4\ \Omega$; THD = 2.5%	18	20	–	W
G_v	closed loop voltage gain	$P_o = 1$ W	25	26	27	dB
CMRR	common mode rejection ratio	f = 1 kHz; $R_s = 0\ \Omega$	–	80	–	dB
SVRR	supply voltage ripple rejection	f = 1 kHz; $R_s = 0\ \Omega$	45	60	–	dB
$\|\Delta V_O\|$	DC output offset voltage		–	–	100	mV
α_{cs}	channel separation	$R_s = 0\ \Omega$; $P_o = 15$ W	40	60	–	dB
$\|\Delta G_v\|$	channel unbalance		–	–	1	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1563Q	DBS17P	plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)	SOT243-1

BLOCK DIAGRAM

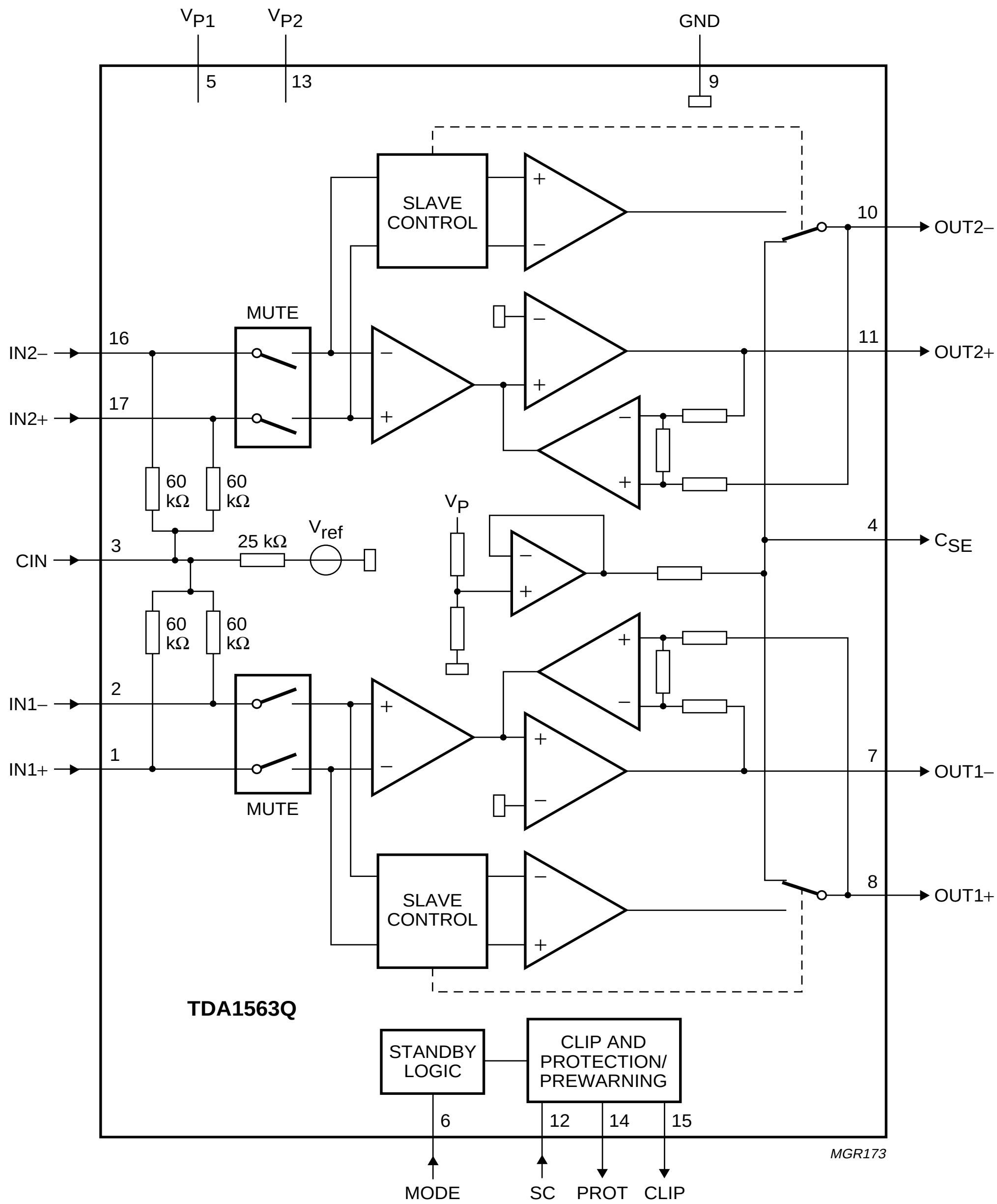


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
IN1+	1	non-inverting input 1
IN1–	2	inverting input 1
CIN	3	common input
C_{SE}	4	electrolytic capacitor for Single-Ended (SE) mode
V_{P1}	5	supply voltage 1
MODE	6	mute/standby/operating
OUT1–	7	inverting output 1
OUT1+	8	non-inverting output 1
GND	9	ground
OUT2–	10	inverting output 2
OUT2+	11	non-inverting output 2
SC	12	selectable clip
V_{P2}	13	supply voltage 2
PROT	14	diagnostic: protection/prewarning
CLIP	15	diagnostic: clip
IN2–	16	inverting input 2
IN2+	17	non-inverting input 2

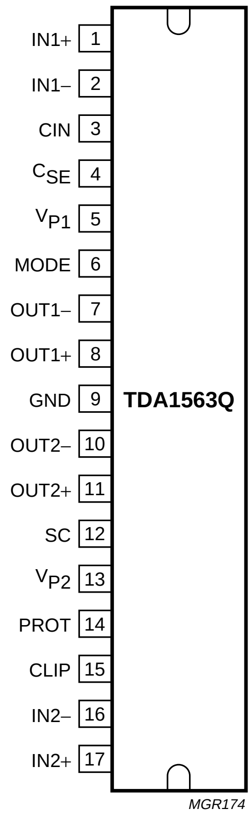


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA1563Q contains two identical amplifiers with differential inputs. At low output power (up to output amplitudes of 3 V (RMS) at V_P = 14.4 V), the device operates as a normal SE amplifier. When a larger output voltage swing is needed, the circuit switches internally to BTL operation.

With a sine wave input signal the dissipation of a conventional BTL amplifier up to 2 W output power is more than twice the dissipation of the TDA1563Q (see Fig.11).

In normal use, when the amplifier is driven with music-like signals, the high (BTL) output power is only needed for a small percentage of time. Under the assumption that a music signal has a normal (Gaussian) amplitude distribution, the dissipation of a conventional BTL amplifier with the same output power is approximately 70% higher (see Fig.12).

The heatsink has to be designed for use with music signals. With such a heatsink, the thermal protection will disable the BTL mode when the junction temperature exceeds 150 °C. In this case the output power is limited to 5 W per amplifier.

The gain of each amplifier is internally fixed at 26 dB. With the MODE pin, the device can be switched to the following modes:

- Standby with low standby current (<50 μA)
- Mute condition, DC adjusted
- On, operation.

The information on pin SC (selectable clip) determines at which distortion figures a clip signal will be generated at the clip output. A logic 0 applied to pin SC will select clip detection at THD = 10%, a logic 1 selects THD = 2.5%. A logic 0 can be realised by connecting this pin to ground. A logic 1 can be realised by connecting it to V_{logic} (see Fig.8) or the pin can also be left open. This pin may not be connected to V_p because it's maximum input voltage is 18 V (V_p > 18 V under load dump conditions).

The device is fully protected against short-circuiting of the output pins to ground and to the supply voltage. It is also protected against short-circuiting the loudspeaker and high junction temperatures. In the event of a permanent short-circuit condition to ground or the supply voltage, the output stage will be switched off resulting in a low dissipation. With permanent short-circuiting of the loudspeaker, the output stage will be repeatedly switched on and off. The duty cycle in the 'on' condition is low enough to prevent excessive dissipation.

To avoid plops during switching from 'mute' to 'on' or from 'on' to 'mute/standby' while an input signal is present, a built-in zero-crossing detector allows only switching at zero input voltage. However, when the supply voltage drops below 6 V (e.g. engine start), the circuit mutes immediately avoiding clicks coming from electronic circuitry preceding the power amplifier.

The voltage on the electrolytic capacitor C_{SE} (pin 4) is kept at 0.5 × V_P by means of a voltage buffer (see Fig.1). The value of this capacitor has an important influence on the output power in SE mode, especially at low signal frequencies. A high value is recommended to minimize dissipation at low frequencies.

The two diagnostic outputs (clip and protection/prewarning) are open collector outputs and require a pull-up resistor.

The clip output will be LOW when the THD of the output signal is higher as the selected clip level (10% or 2.5%).

The protection/prewarning output gives information about:

- Short-circuit protection:
  - When a short-circuit occurs (for at least 50 ms) at the outputs to ground or the supply voltage, the output stages are switched off to prevent excessive dissipation. The outputs will be switched on again approx. 20 ms after removing the short. During this short-circuit condition the protection pin will be LOW.
  - When a short-circuit occurs across the load, the output stages are switched off during approx. 20 ms. After that time a check is performed whether the short is still present. The power dissipation in any short-circuit condition is very low.
- Temperature detection:
  - A prewarning indicates the temperature protection will become active. The prewarning can be used to reduce the input signal and so reducing the power dissipation.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage	operating	–	18	V
		non operating	–	30	V
		load dump; t_r > 2.5 ms	–	45	V
$V_{P(sc)}$	short-circuit safe voltage		–	18	V
V_{rp}	reverse polarity voltage		–	6	V
I_{ORM}	repetitive peak output current		–	4	A
P_{tot}	total power dissipation		–	60	W
T_{stg}	storage temperature		–55	+150	°C
T_{vj}	virtual junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–40	–	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-c)}$	thermal resistance from junction to case	see note 1	1.3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		40	K/W

Note

1. The value of $R_{th(c-h)}$ depends on the application (see Fig.3).

Heatsink design

There are two parameters that determine the size of the heatsink. The first is the rating for the virtual junction temperature and the second is the ambient temperature at which the amplifier must still deliver its full power in the BTL mode.

With a conventional BTL amplifier, the maximum power dissipation with a music-like signal (at each amplifier) will be approximately two times 6.5 W.

At a virtual junction temperature of 150 °C and a maximum ambient temperature of 65 °C, $R_{th(vj-c)}$ = 1.3 K/W and $R_{th(c-h)}$ = 0.2 K/W, the thermal resistance of the heatsink should be: $\frac{150-65}{2 \times 6.5} - 1.3 - 0.2 = 5$ K/W

Compared to a conventional BTL amplifier, the TDA1563Q has a higher efficiency. The thermal resistance of the heatsink should be: $1.7\left(\frac{150-65}{2 \times 6.5}\right) - 1.3 - 0.2 = 9.6$ K/W

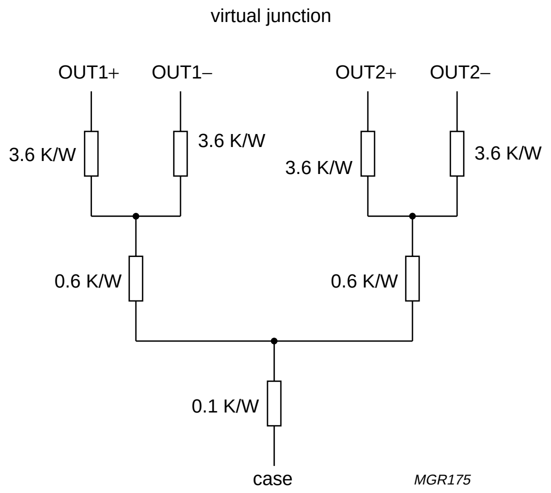


Fig.3 Thermal equivalent resistance network.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measured in Fig.8; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_P	supply voltage	note 1	6.0	14.4	18.0	V
I_q	quiescent supply current	$R_L = \infty$	–	95	150	mA
I_{stb}	standby current		–	1	50	μA
V_C	average electrolytic capacitor voltage at pin 4		–	7.1	–	V
$\|\Delta V_O\|$	DC output offset voltage	on state	–	–	100	mV
		mute state	–	–	100	mV
Mode select switch (see Fig.4)						
V_{ms}	voltage at mode select pin (pin 6)	standby condition	0	–	1	V
		mute condition	2	–	3	V
		on condition	4	5	V_p	V
I_{ms}	switch current through pin 6	V_{ms} = 5 V	–	–	40	μA
Diagnostic						
$V_{PROT/CLIP}$	output voltage at diagnostic pins: protection/prewarning (pin 14) and clip (pin 15)	active at logic 0	–	–	0.5	V
$I_{PROT/CLIP}$	current through pin 14 or 15	active at logic 0	2	–	–	mA
V_{SC}	input voltage at selectable clip pin (pin 12)					
	logic 0, THD = 10%		–	–	0.5	V
	logic 1, THD = 2.5%		1.5	–	18	V
Protection						
T_{pre}	prewarning temperature		–	145	–	°C
T_{dis}	BTL disable temperature	note 2	–	150	–	°C

Notes

1. The circuit is DC biased at V_P = 6 to 18 V and AC operating at V_P = 8 to 18 V.
2. If the junction temperature exceeds 150 °C, the output power is limited to 5 W per channel.

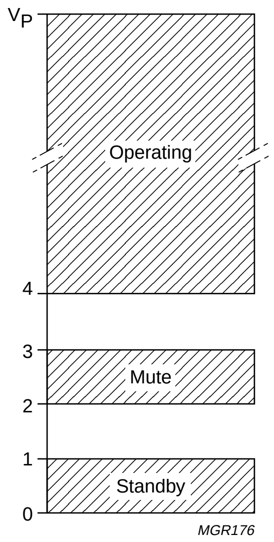


Fig.4 Switching levels of the mode select switch.

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; C_{SE} = 1000 µF; f = 1 kHz; T_{amb} = 25 °C; measured in Fig.8; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power	THD = 0.5%	15	19	–	W
		THD = 10%	23	25	–	W
		EIAJ	–	38	–	W
		V_P = 13.2 V; THD = 0.5%	–	16	–	W
		V_P = 13.2 V; THD = 10%	–	20	–	W
THD	total harmonic distortion	P_o = 1 W; note 1	–	0.1	–	%
P_d	dissipated power		see Figs 11 and 12			W
B_p	power bandwidth	THD = 1%; P_o = –1 dB with respect to 15 W	–	20 to 15000	–	Hz
$f_{ro(l)}$	low frequency roll-off	–1 dB; note 2	–	25	–	Hz
$f_{ro(h)}$	high frequency roll-off	–1 dB	130	–	–	kHz
G_v	closed loop voltage gain	P_o = 1 W	25	26	27	dB
SVRR	supply voltage ripple rejection	R_s = 0 Ω; V_{ripple} = 2 V (p-p)				
		on	45	60	–	dB
		mute	–	90	–	dB
		standby; f = 100 Hz to 10 kHz	80	–	–	dB
CMRR	common mode rejection ratio	R_s = 0 Ω	–	80	–	dB
$\|Z_i\|$	input impedance		90	120	150	kΩ
$\|\Delta Z_i\|$	mismatch in input impedance		–	1	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{SE\text{-}BTL}$	SE to BTL switch voltage level	note 3	–	3	–	V
$\lvert V_{o(mute)} \rvert$	mute mode output voltage (RMS value)	V_i = 1 V (RMS)	–	80	150	μV
$V_{n(o)}$	noise output voltage	on; R_s = 0 Ω; note 4	–	80	150	μV
		on; R_s = 10 kΩ; note 4	–	85	–	μV
		mute; note 5	–	80	150	μV
α_{cs}	channel separation	R_s = 0 Ω; P_o = 15 W	40	60	–	dB
$\lvert \Delta G_v \rvert$	channel unbalance		–	–	1	dB

Notes

1. The distortion is measured with a bandwidth of 10 Hz to 30 kHz.
2. Frequency response externally fixed (input capacitors determine low frequency roll-off).
3. The SE to BTL switch voltage level depends on V_P.
4. Noise output voltage measured with a bandwidth of 20 Hz to 20 kHz.
5. Noise output voltage is independent of R_s.

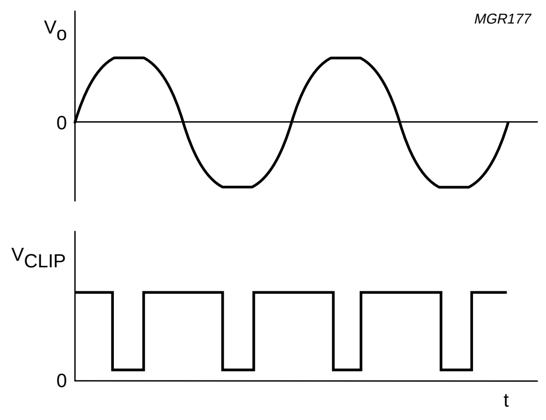


Fig.5 Clip detection waveforms.

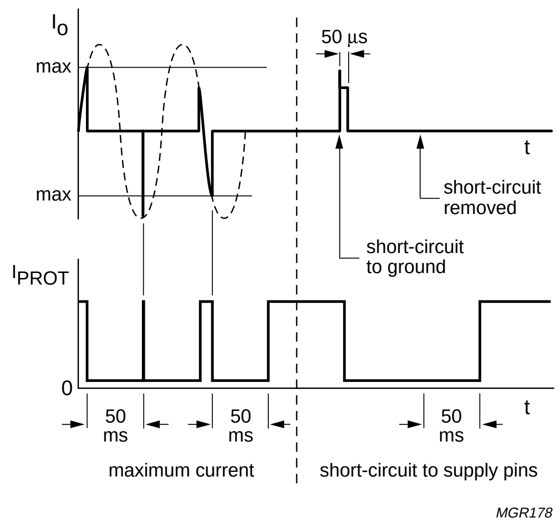


Fig.6 Protection waveforms.

TEST AND APPLICATION INFORMATION

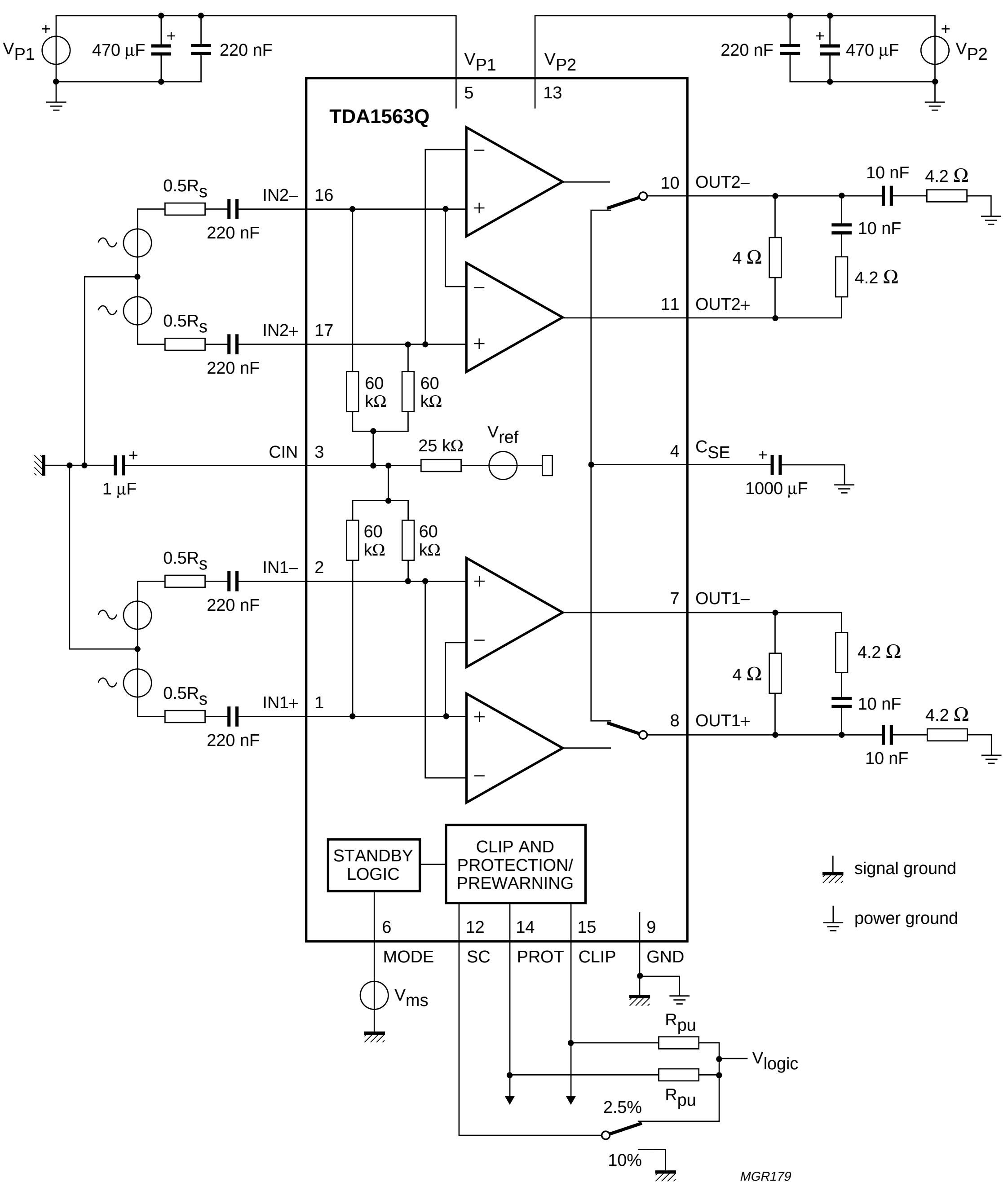
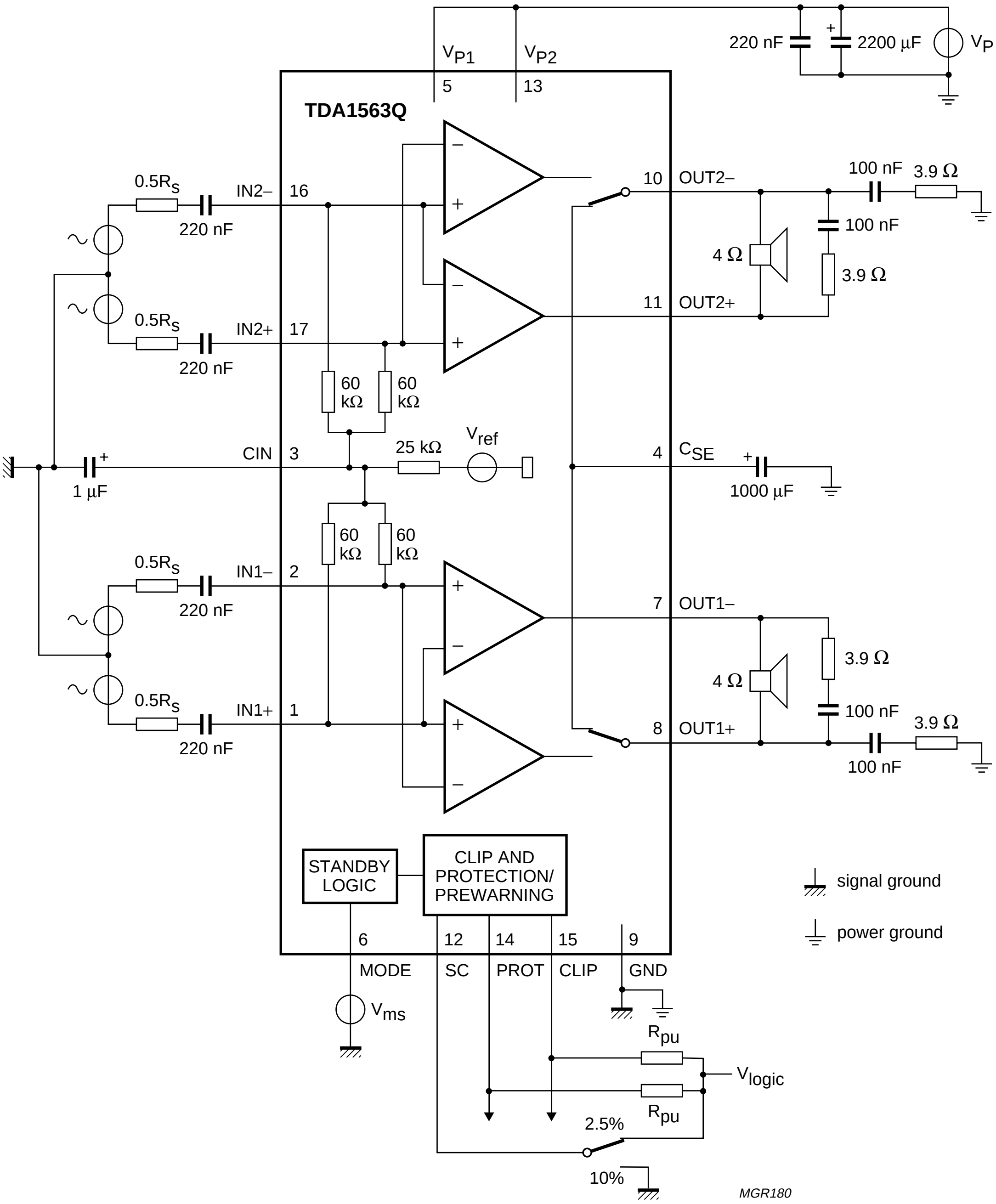
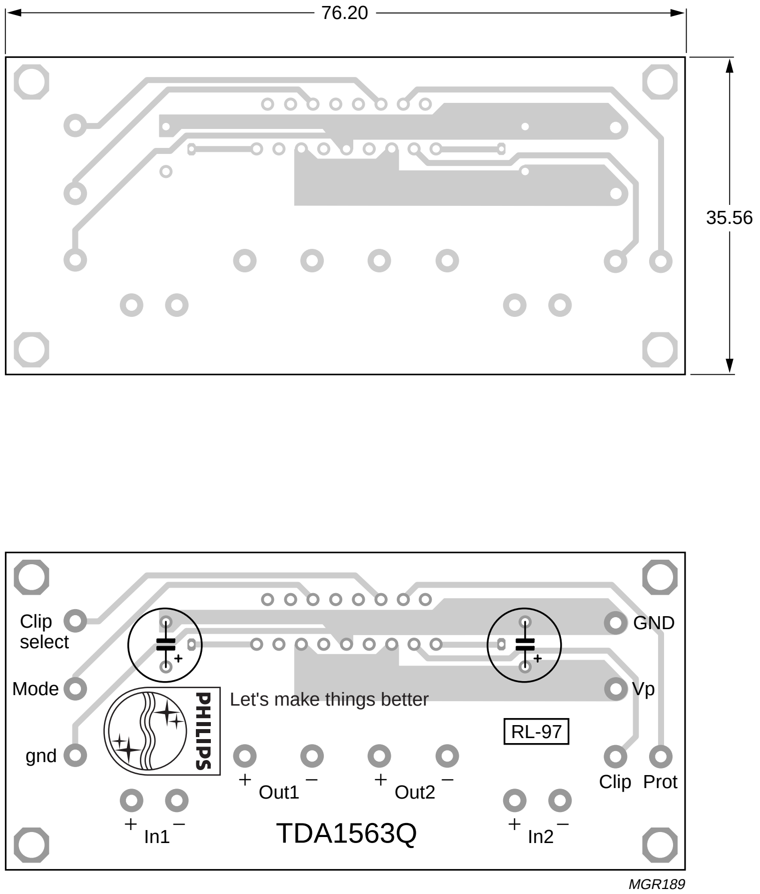


Fig.7 Test diagram.



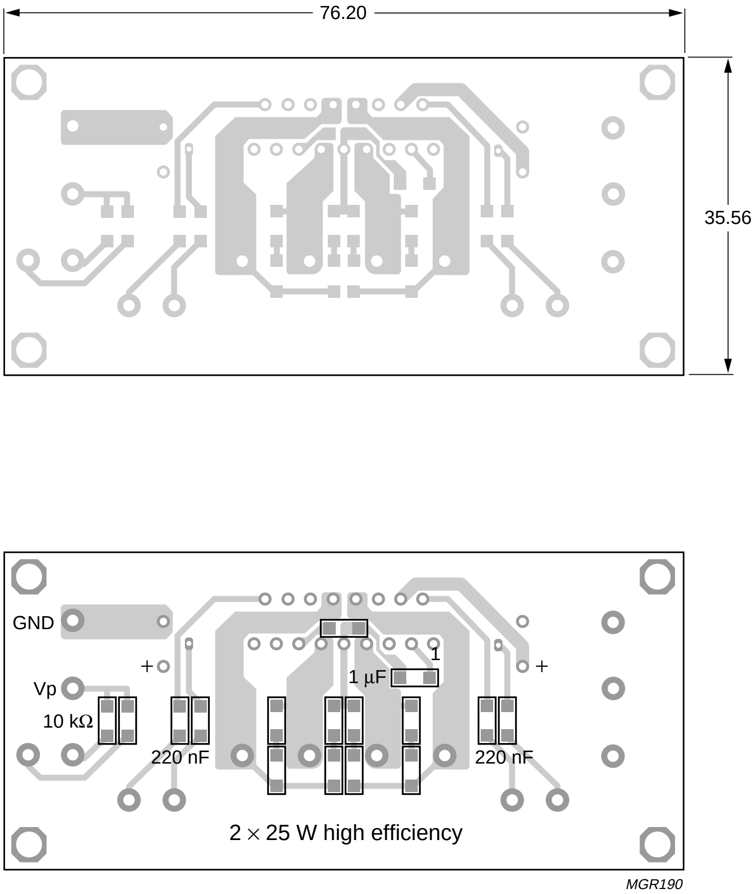
Connect Boucherot filter to pin 8 respectively pin 10 with the shortest possible connection.

Fig.8 Application diagram.



Dimensions in mm.

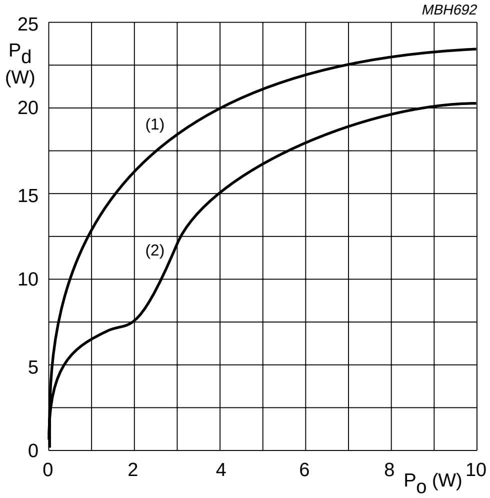
Fig.9 Printed-circuit board layout (component side) for the application of Fig.8.



Dimensions in mm.

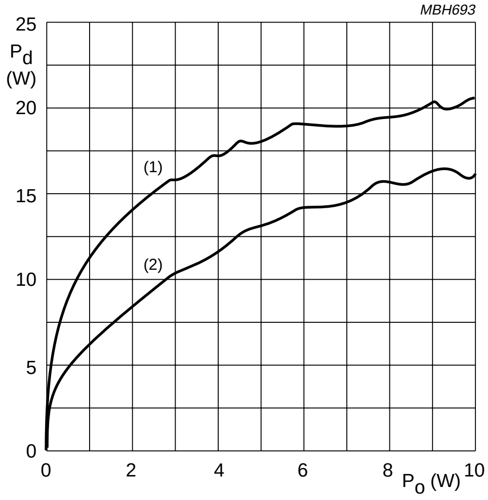
Fig.10 Printed-circuit board layout (soldering side) for the application of Fig.8.

ADDITIONAL APPLICATION INFORMATION



Input signal 1 kHz, sinusoidal; V_P = 14.4 V.
(1) For a conventional BTL amplifier.
(2) For TDA1563Q.

Fig.11 Dissipation; sine wave driven.



(1) For a conventional BTL amplifier.
(2) For TDA1563Q.

Fig.12 Dissipation; pink noise through IEC-268 filter.

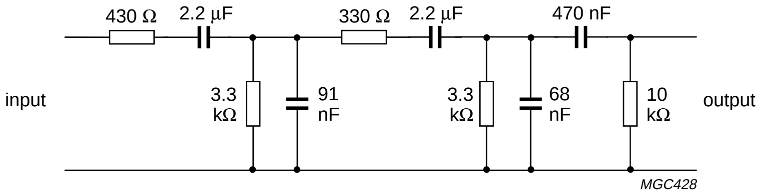


Fig.13 IEC-268 filter.

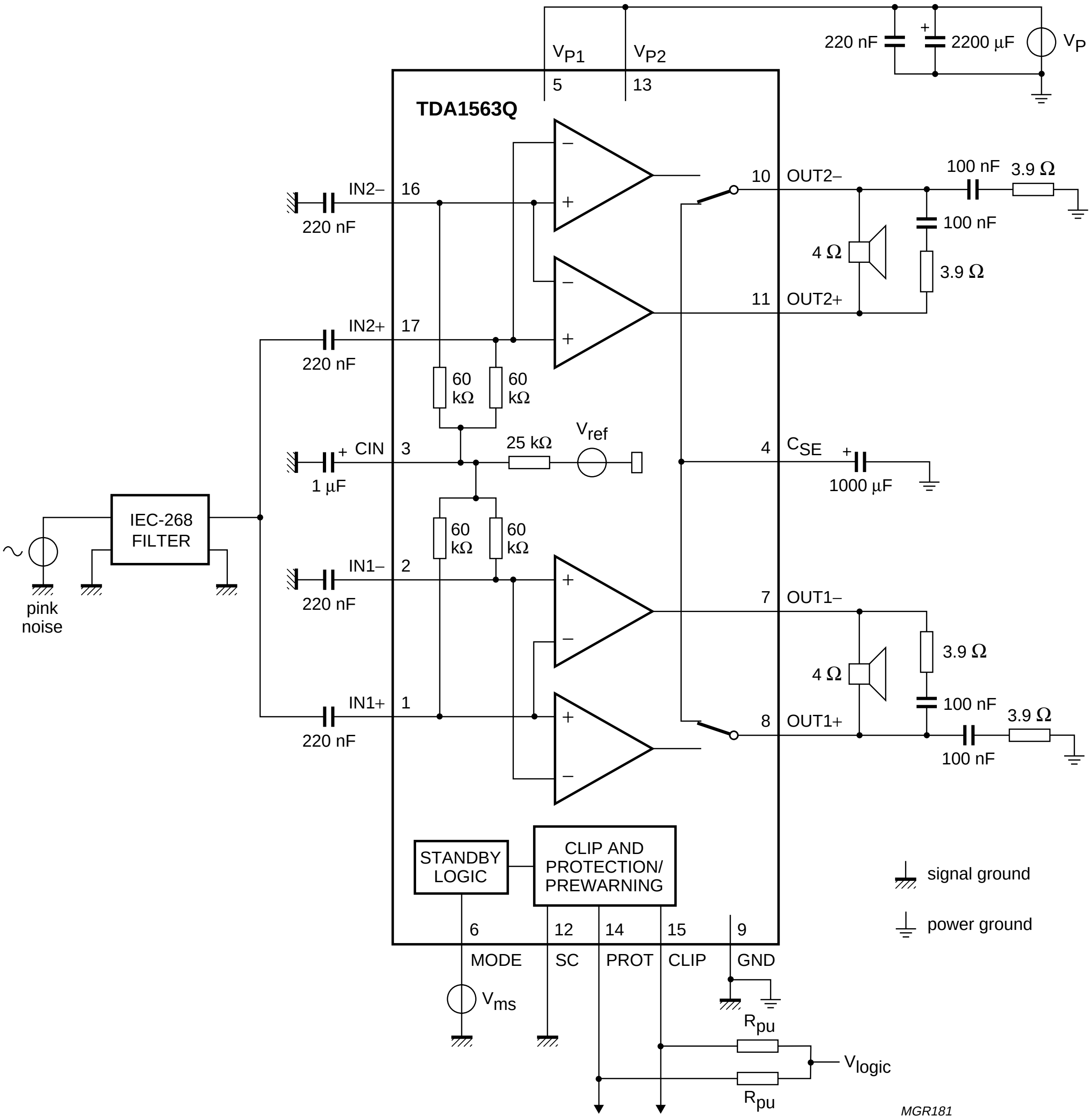
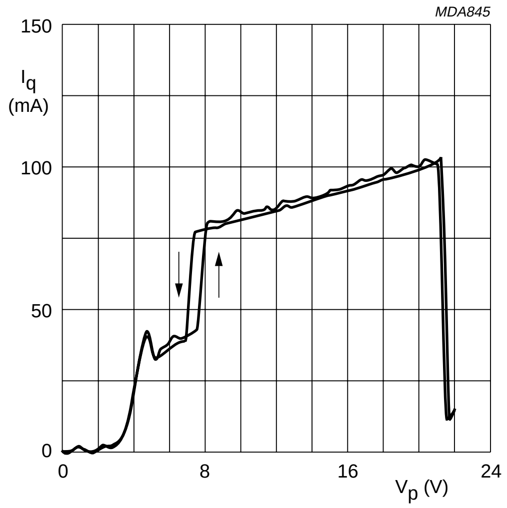
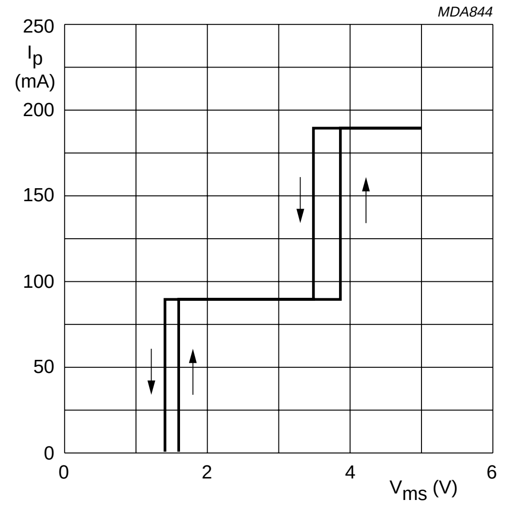


Fig.14 Test and application diagram for dissipation measurements with a music-like signal (pink noise).



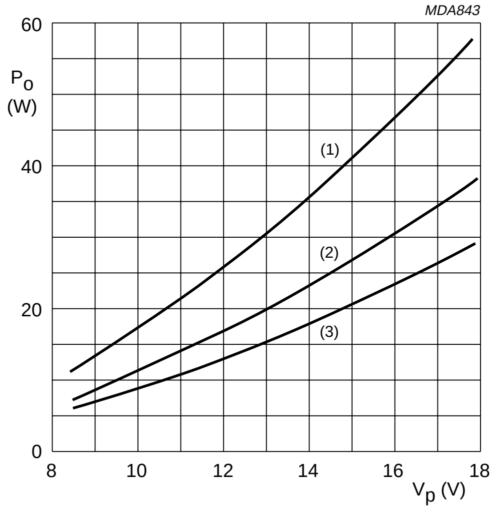
V_{ms} = 5 V; R_l = ∞.

Fig.15 Quiescent current as a function of V_P.



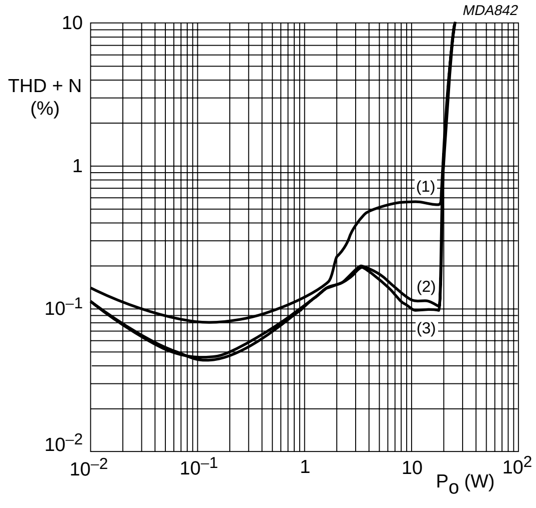
V_P = 14.4 V; V_i = 25 mV.

Fig.16 I_P as a function of V_{ms} (pin 6).



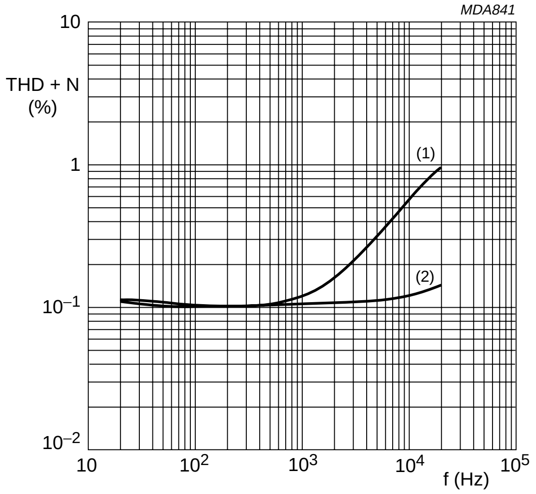
(1) EIAJ, 100 Hz.
(2) THD = 10 %.
(3) THD = 0.5 %.

Fig.17 Output power as a function of V_P.



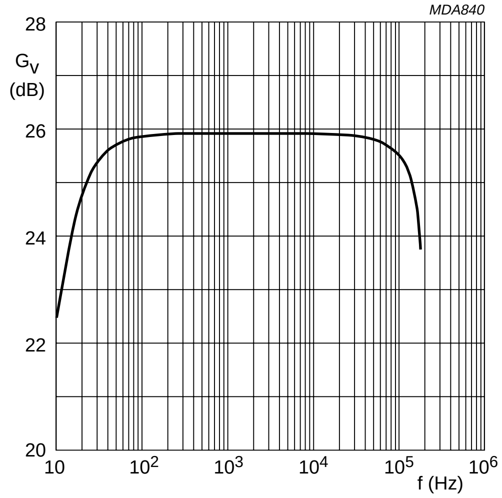
(1) f = 10 kHz.
(2) f = 1 kHz.
(3) f = 100 Hz.

Fig.18 THD + noise as a function of P_o.



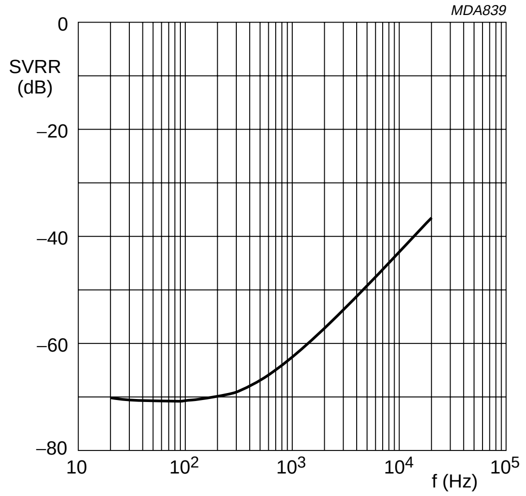
(1) P_o = 10 W.
(2) P_o = 1 W.

Fig.19 THD + noise as a function of frequency.



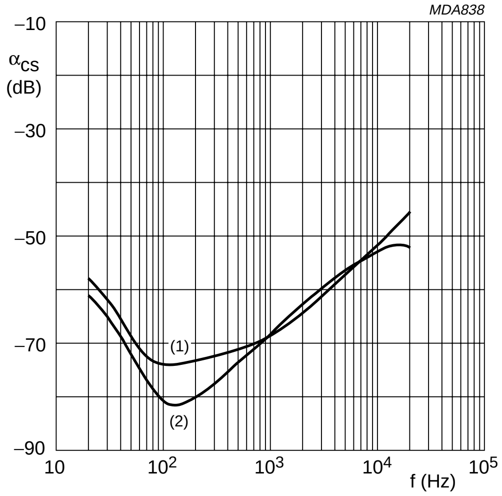
V_i = 10 mV.

Fig.20 Gain as a function of frequency.



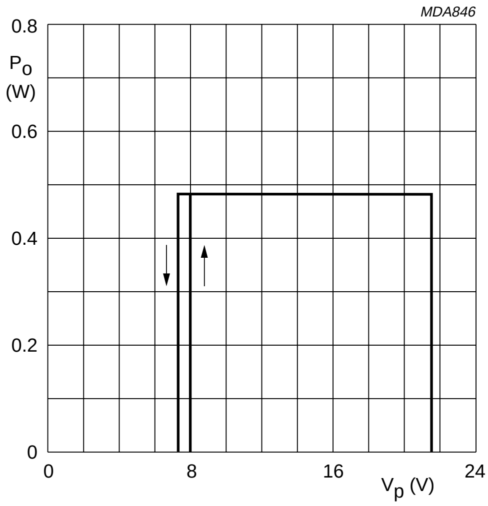
$V_{ripple(p-p)}$ = 2 V.

Fig.21 SVRR as a function of frequency.



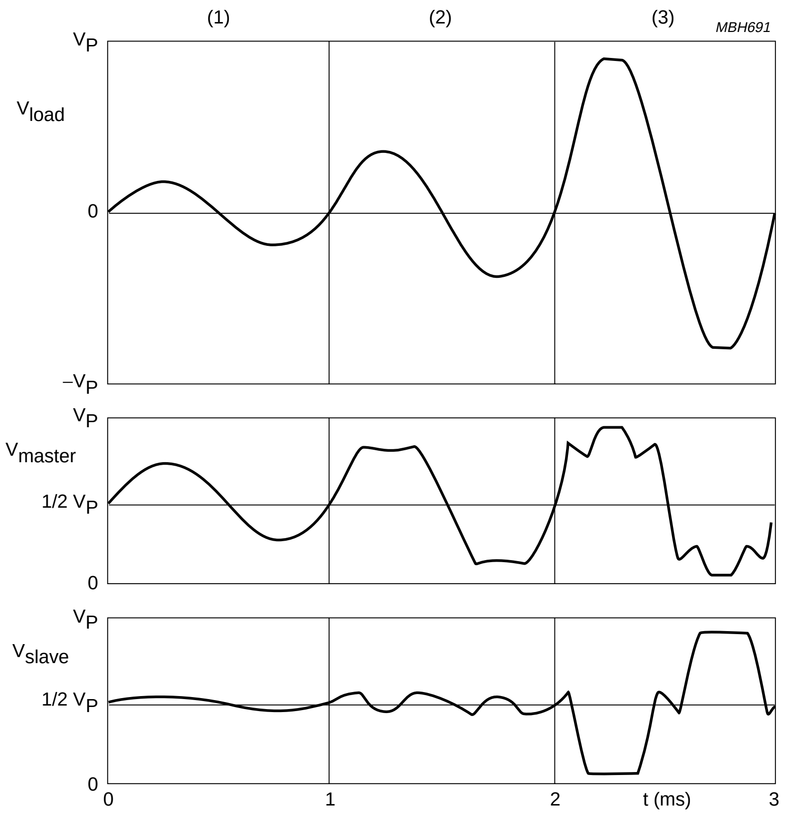
(1) P_o = 10 W.
(2) P_o = 1 W.

Fig.22 Channel separation as a function of frequency.



V_i = 10 mV.

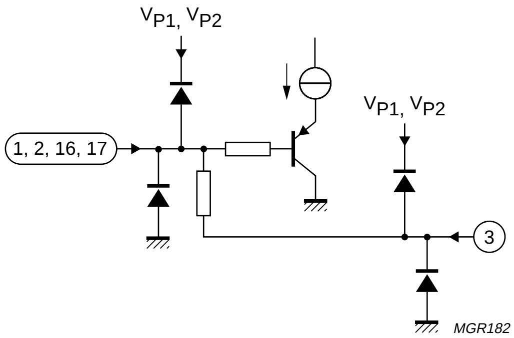
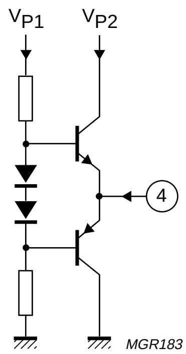
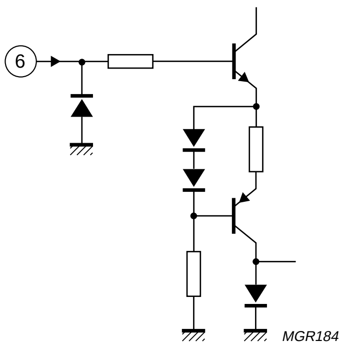
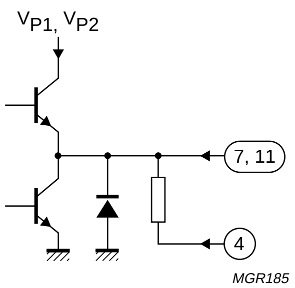
Fig.23 AC operating as a function of V_p.

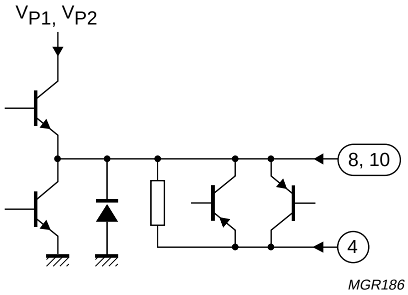
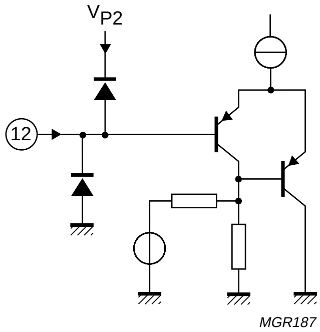
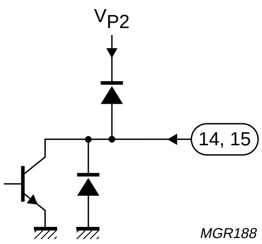


See Fig.7:
$V_{load} = V_7 - V_8$ or $V_{11} - V_{10}$.
$V_{master} = V_7$ or V_{11}.
$V_{slave} = V_8$ or V_{10}.

Fig.24 Output waveforms.

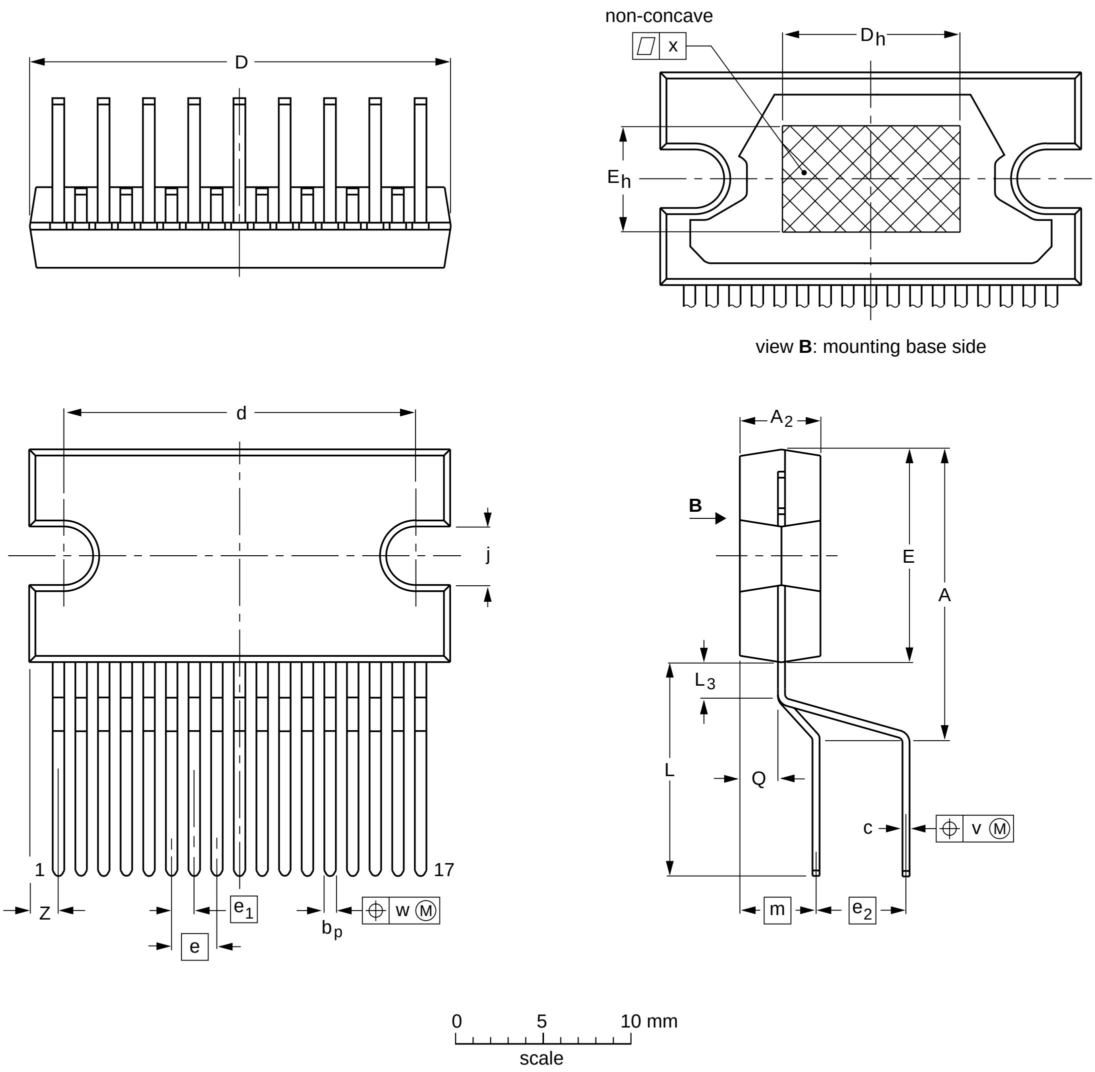
INTERNAL PIN CONFIGURATION

PIN	NAME	EQUIVALENT CIRCUIT
1, 2, 16, 17 and 3	IN1+, IN1–, IN2–, IN2+ and CIN	
4	C_{SE}	
6	MODE	
7, 11	OUT1–, OUT2+	

PIN	NAME	EQUIVALENT CIRCUIT
8, 10	OUT1+, OUT2–	
12	SC	
14, 15	PROT, CLIP	

PACKAGE OUTLINE

DBS17P: plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm) **SOT243-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	j	L	L_3	m	Q	v	w	x	$Z^{(1)}$
mm	17.0 15.5	4.6 4.2	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	1.27	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.4	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT243-1						~~95-03-11~~ 97-12-16

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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