DATA SHEET

DIGITAL dcc COMPACT CASSETTE

TDA1381
DCC write amplifier (WRITE3)

Preliminary specification
File under Integrated Circuits, IC01

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Philips Semiconductors

PHILIPS

DCC write amplifier (WRITE3) TDA1381

FEATURES

- Single 3 V power supply
- Low standby current consumption
- 20 bidirectional current outputs (2 × nine heads)
- Single point main data and auxiliary current setting
- Reduction of power consumption between write pulses
- Soft switching of output currents
- Serial data input
- Timing is compatible with TDA1319T
- Uncommitted operational amplifier available.

GENERAL DESCRIPTION

The TDA1381 has been designed to drive an 18-channel inductive recording head which is suitable for the DCC (Digital Compact Cassette) system. The bidirectional current outputs are controlled by a two-wire serial bus. The amplitude of the write current pulses can be set by either voltage or current control. The circuit can be switched to standby mode to minimize supply current consumption.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		2.7	3.0	4.0	V
I_{DD}	supply current	note 1	–	9	12	mA
$I_{DD(av)}$	average supply current	note 2	–	26.5	–	mA
I_{stb}	total standby current		–	0.1	0.3	mA
$I_{WDAT(max)}$	maximum write current for main data channels 0 to 7	note 3	100	–	–	mA
$I_{WAUX(max)}$	maximum write current for auxiliary channel	note 3	115	–	–	mA
$I_{EAUX(max)}$	maximum erase current for auxiliary channel	note 3	153	–	–	mA
$P_{d(av)}$	average power dissipation	note 2	–	80	–	mW
T_{amb}	operating ambient temperature		–30	–	+85	°C

Notes

1. No head connected; all outputs unloaded; V_{DD} = 3 V.
2. In the auxiliary and data write mode; writing DCC data; I_{WDAT} = 60 mA; V_{DD} = 3 V; f_{clk} = 3.072 MHz. Data channels resistively loaded with 6 Ω, auxiliary channel resistively loaded with 4 Ω between pins 23 and 24, and 37 and 38.
3. Resistors connected in accordance with test circuit of Fig.7.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1381H	TQFP48(1)	plastic thin quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-1

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Handbook"* (order number 9398 510 63011) are followed.

BLOCK DIAGRAM

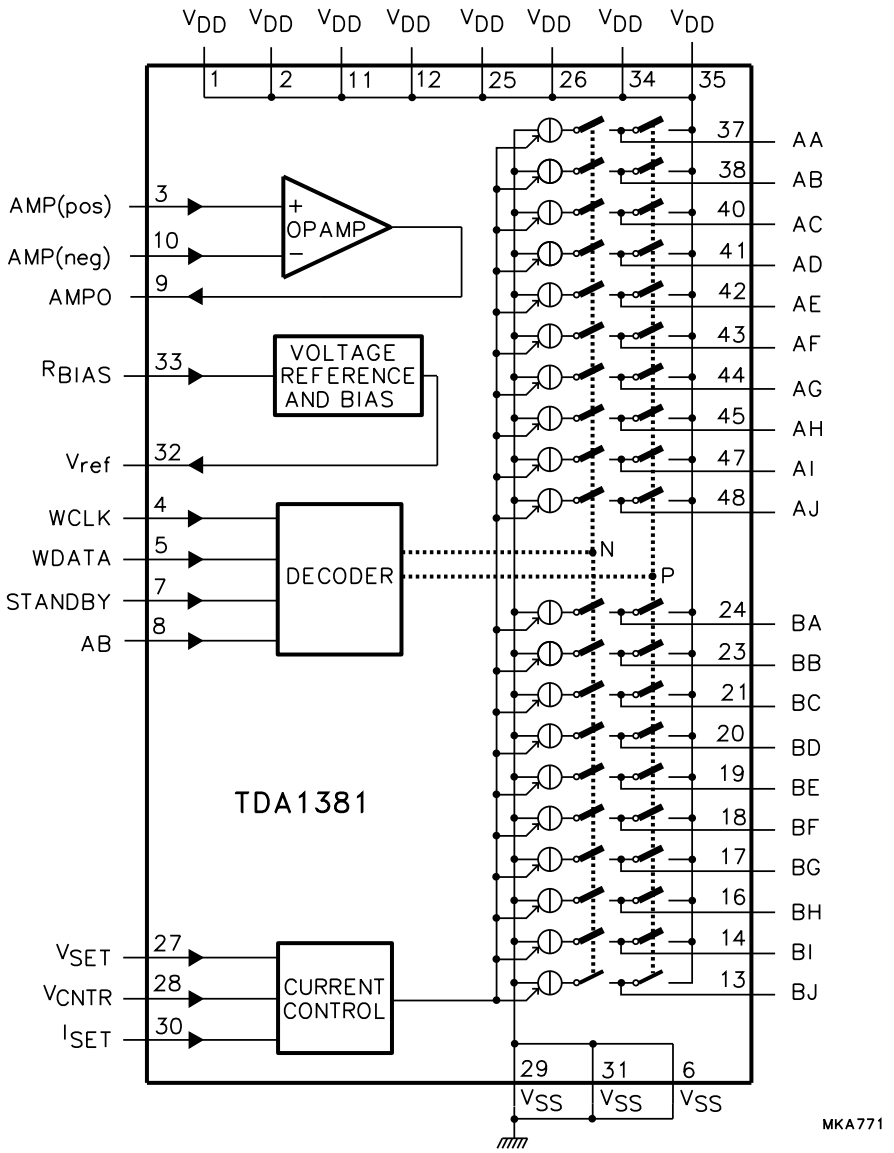


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{DD}	1	supply voltage
V_{DD}	2	supply voltage
AMP(pos)	3	operational amplifier non-inverting input
WCLK	4	write clock input
WDATA	5	write data input
V_{SS}	6	ground
STANDBY	7	standby mode control input
AB	8	tape sector A or B select input
AMPO	9	operational amplifier output
AMP(neg)	10	operational amplifier inverting input
V_{DD}	11	supply voltage
V_{DD}	12	supply voltage
BJ	13	sector B write pulse output J
BI	14	sector B write pulse output I
n.c.	15	not connected
BH	16	sector B write pulse output H
BG	17	sector B write pulse output G
BF	18	sector B write pulse output F
BE	19	sector B write pulse output E
BD	20	sector B write pulse output D
BC	21	sector B write pulse output C
n.c.	22	not connected
BB	23	sector B write pulse output B
BA	24	sector B write pulse output A
V_{DD}	25	supply voltage
V_{DD}	26	supply voltage
V_{SET}	27	control voltage input
V_{CNTR}	28	voltage-to-current conversion setting input
V_{SS}	29	ground
I_{SET}	30	control current input
V_{SS}	31	ground
V_{ref}	32	reference voltage output
R_{BIAS}	33	bias current resistor
V_{DD}	34	supply voltage
V_{DD}	35	supply voltage
n.c.	36	not connected
AA	37	sector A write pulse output A
AB	38	sector A write pulse output B
n.c.	39	not connected
AC	40	sector A write pulse output C

SYMBOL	PIN	DESCRIPTION
AD	41	sector A write pulse output D
AE	42	sector A write pulse output E
AF	43	sector A write pulse output F
AG	44	sector A write pulse output G
AH	45	sector A write pulse output H
n.c.	46	not connected
AI	47	sector A write pulse output I
AJ	48	sector A write pulse output J

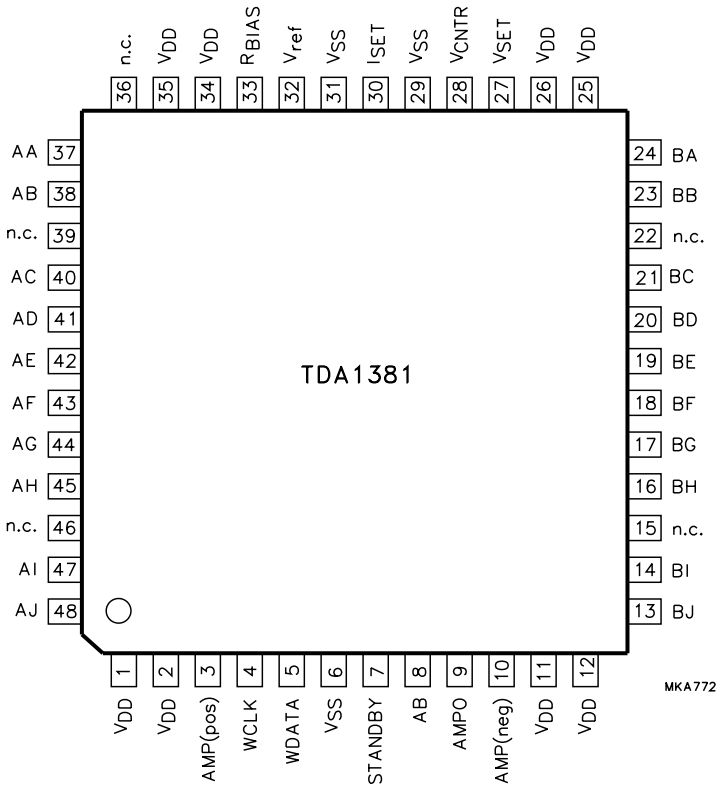


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA1381 is designed to drive the elements of an 18-channel recording head, containing nine elements for tape sector A and nine elements for sector B. A brief functional description of each block (see Fig.1) is given below.

Decoder

The IC is controlled by the 32-bit wide serial data word which is clocked in at WDATA (pin 5). The clock frequency (WCLK, pin 4) is 3.072 MHz with a clock period of 325 ns. The write pulses are made available at the outputs AA to AJ when tape sector A is selected (pin 8 HIGH) or at the outputs BA to BJ when tape sector B is selected (pin 8 LOW). The principle of connection of the recording head to the IC is illustrated in Fig.4.

The timing sequence of the write pulses is shown in Fig.5. The operating mode of the IC can be set by the first 3 bits of WDATA. The signals TCH0 to TCH7 and TCHAUX determine the direction of the write current. When TCH_n is HIGH, the current flows as indicated in Fig.4. When TCH_n is LOW current flows in the opposite direction. The various modes of operation are given in Table 1. The standby mode can also be forced by setting the STANDBY input (pin 7) HIGH.

Current control

The write current at the outputs is regulated by the current control circuit. The principle of this circuit is shown in Fig.3.

The value of the current I_{WDAT} can be set using an external voltage V_{SET}, connected between pin 27 and V_{SS}. In this configuration, pin 28 has to be resistively loaded to another voltage source or V_{SS} (see Fig.7). The current control circuit regulates the voltage between pins 27 and 28 to zero. When a resistor R_{set} is connected between pin 28 and V_{SS}, a current gain factor (G_{if}) can be defined as:

$$G_{if} = \frac{I_{WDAT}}{\left(\frac{V_{SET}}{R_{SET}}\right)}$$

Table 1 Modes of operation.

MODE		WRITE CURRENT		CONTROL BIT(1)		
MAIN DATA CHANNELS	AUXILIARY CHANNEL	MAIN DATA CHANNELS	AUXILIARY CHANNEL(3)	TDAPLB(2) (DATA CHANNEL PLAYBACK)	TAUPLB(2) (AUXILIARY CHANNEL PLAYBACK)	TERAUX (AUXILIARY CHANNEL ERASE)
Read	read	off	off	1	1	X
Write	read	I_{WDAT}	off	0	1	X
Write	write	I_{WDAT}	$AW \times I_{WDAT}$	0	0	0
Write	erase	I_{WDAT}	$AE \times I_{WDAT}$	0	0	1
Read	write	off	$AW \times I_{WDAT}$	1	0	0
Read	erase	off	$AE \times I_{WDAT}$	1	0	1

Notes

1. Where 0 = LOW, 1 = HIGH and X = don't care.
2. When both TDAPLB and TAUPLB are HIGH, the IC is set to the standby mode.
3. A_W and A_E are multiplication factors (see Section “Current control”).

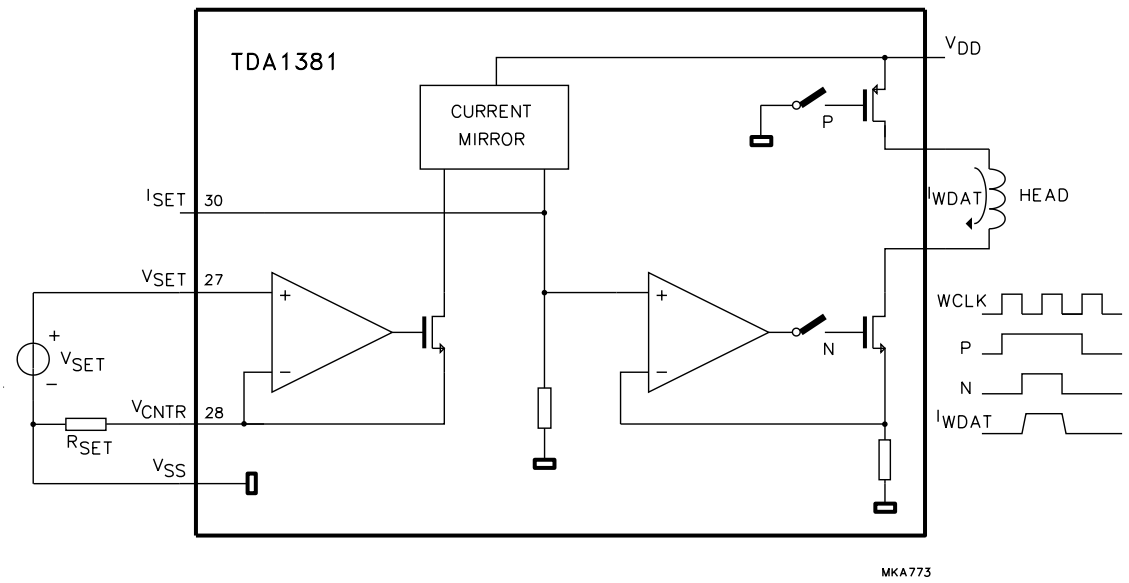


Fig.3 Principle of the write current control circuit.

It is also possible to set the write current by providing a current I_i into I_{SET} (pin 30). In this configuration pin 27 must be connected to V_{SS} and pin 28 must be connected to V_{DD}.

The current gain factor is now defined as: $G_{if} = \frac{I_{WDAT}}{I_i}$

During AUX write (outputs AA, AB or BA, BB active) the output current I_{WDAT} is increased by a factor A_W. During the erase mode of the auxiliary channel (TERAUX = HIGH, see Table 1), the output current I_{WDAT} is increased by a factor A_E.

Outputs

Each channel of the chosen sector is selected in sequence. Depending on the data word, the current is directed forward or reversed through the heads. The outputs that are not selected are kept floating to prevent any incorrect current flow. In HIGH state (one of the switches P is closed) the output is internally connected to V_{DD}. In the LOW state (one of the switches N is closed) the output is connected to a current source.

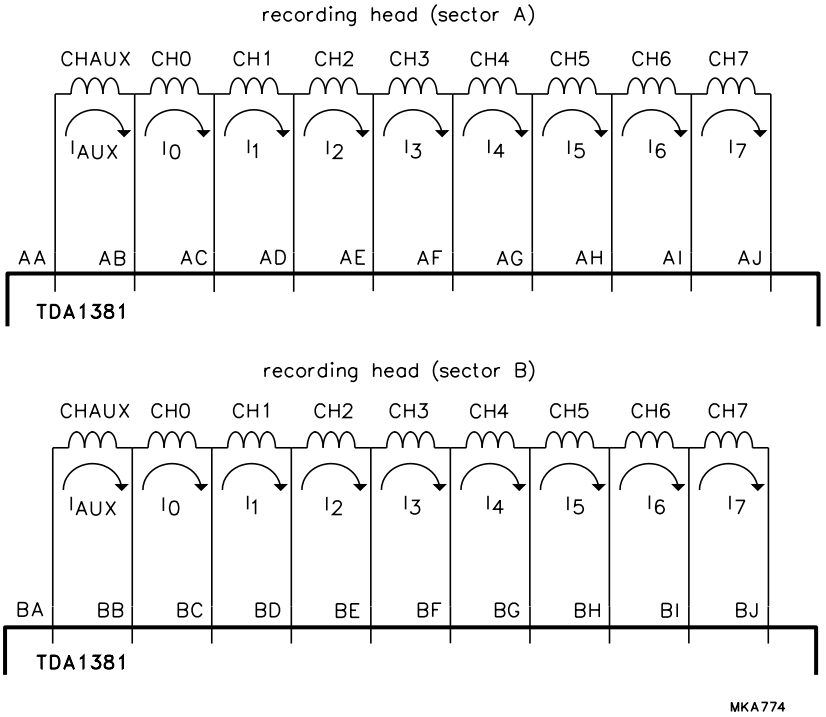


Fig.4 Definition of the output currents.

Voltage reference

A reference voltage is available at pin 32. This voltage is derived from a bandgap reference source, and can be used to derive a control voltage for the current control circuit.

Standby

The circuit is set to the standby mode when TDAPLB = 1 and TAUPLB = 1 (see Table 1), or when a HIGH level is applied to pin 7. After a HIGH-to-LOW transition at pin 7, the IC will remain in the standby mode until TDAPLB = 0 or TAUPLB = 0. When the IC is in the standby mode, the current amplifier is switched off to minimize the power consumption, all write current outputs are floating, and the voltage reference is switched off.

Operational amplifier

An uncommitted operational amplifier is available for use in a tape head temperature compensation circuit with the read IC TDA1380.

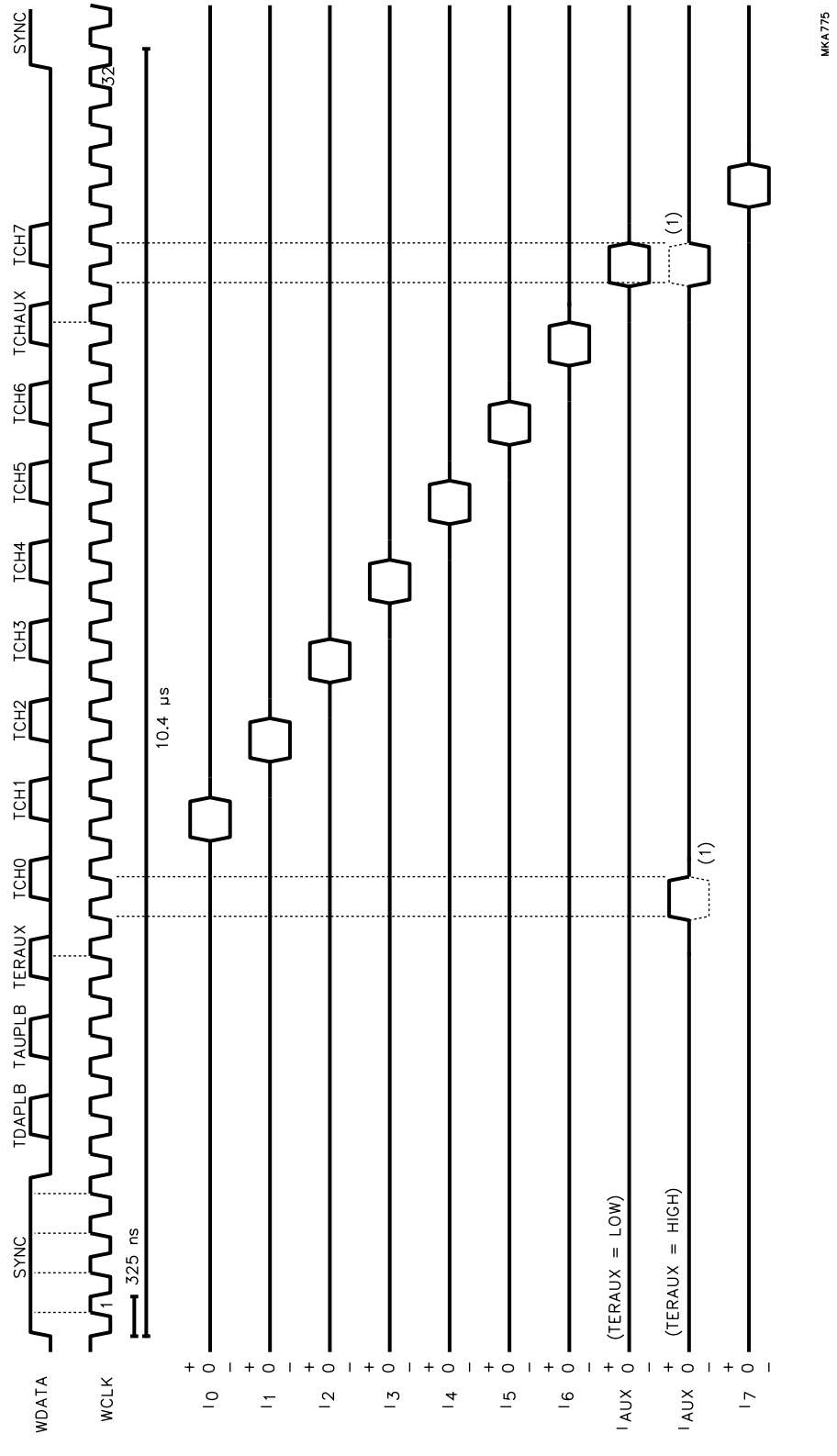


Fig.5 Data format and timing sequence of the write pulses.

(1) Erase pulses are inverted every other cycle of 32 clock pulses.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); all voltages referenced to V_{SS} (pins 6, 29 and 31); all currents are positive into the IC.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–0.3	5.5	V
V_I	input voltage pins 4, 5, 7 and 8		–0.3	5.5	V
V_n	input voltage on other pins	V_{DD} + 0.3 V < 5.5 V	–0.3	V_{DD} + 0.3	V
$I_{IW(max)}$	maximum input current on write pulse outputs (pins 13, 14, 16 to 21, 23, 24, 37, 38, 40 to 45, 47 and 48)		–200	+200	μA
$I_{I(max)}$	maximum input current on supply and ground pins (pins 1, 2, 6, 11, 12, 25, 26, 29, 31, 34 and 35)		–250	+250	μA
$I_{n(max)}$	maximum input current on other pins (pins 3 to 5, 7 to 10, 27, 28, 30, 32 and 33)		–10	+10	μA
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–30	+85	°C
V_{es}	electrostatic handling	note 1	–3000	+3000	V
		note 2	–300	+300	V

Notes

1. Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
2. Machine model: equivalent to discharging a 200 pF capacitor through a 25 Ω series resistor and a 2.5 μH series inductor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	65	K/W

CHARACTERISTICS

V_{DD} = 3 V (pins 1, 2, 11, 12, 25, 26, 34 and 35 tied together externally); T_{amb} = 25 °C; f_{clk} = 3.072 MHz; measured in test circuit of Fig.7; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.7	3.0	4.0	V
I_{DD}	supply current	note 1	–	9	12	mA
I_{stb}	total standby current	standby mode	–	0.1	0.3	mA
$P_{d(av)}$	average power dissipation	note 2	–	120	–	mW
Digital inputs (pins 4, 5, 7 and 8)						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	V_{DD}	5.5	V
V_{IL}	LOW level input voltage		–0.3	0	$0.3V_{DD}$	V
I_{LI}	input leakage current		–10	0	+10	μA
t_{su}	WDATA set-up time	see Fig.6	30	–	–	ns
t_h	WDATA hold time	see Fig.6	30	–	–	ns
Analog inputs/output (pins 27, 28, 30, 32 and 33)						
V_{SET}	input voltage (pin 27)		0.4	–	$V_{DD} - 1.3$	V
V_{CNTR}	input voltage (pin 28)		0.4	–	$V_{DD} - 1.3$	V
V_{ref}	output reference voltage (pin 32)	I_o < 500 μA	1.95	2.05	2.15	V
G_{if}	current gain factor	with voltage input	550	700	850	
		with current input	590	720	850	
Write pulse outputs (pins 13, 14, 16 to 21, 23, 24, 37, 38, 40 to 45, 47 and 48)						
$I_{WDAT(min)}$	minimum output current channels 0 to 7	f_{clk} = 6.15 MHz	–	–	20	mA
$I_{WDAT(max)}$	maximum output current channels 0 to 7	note 3	100	–	–	mA
$I_{AUX(max)}$	maximum output current auxiliary channel	note 3	153	–	–	mA
A_W	relative auxiliary write current increase		1.0	1.2	1.4	dB
A_E	relative auxiliary erase current increase		3.0	3.7	4.4	dB
ΔI_{WDAT}	deviation between main data channels per sector	note 4	–	–	0.5	dB
$\frac{\Delta I_{WDAT}}{\Delta T}$	temperature coefficient of the output currents	note 5	–	200×10^{-6}	–	K^{-1}

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operational amplifier (pins 3, 9 and 10); note 6						
G_o	DC open loop gain		–	45	–	dB
B_G	gain bandwidth		–	1	–	MHz
V_o	output voltage (pin 9)		0.5	–	V_{DD} – 1.3	V
$V_{i(cm)}$	common mode input voltage (pins 3 and 10)		0.85	–	V_{DD}	V

Notes

1. No head connected, all outputs unloaded.
2. Auxiliary and data write mode; I_{WDAT} = 100 mA.
3. Maximum resistive load of auxiliary channel is 6.5 Ω; maximum resistive load of data channels is 10 Ω.
4. $20 \log \frac{I_{WDAT(max)}}{I_{WDAT(min)}}$ for channels 0 to 7, I_{WDAT} = 100 mA.
5. With constant V_{SET} or I_{SET} (see Fig.7).
6. R_L > 100 kΩ; C_L < 100 pF; load connected between pin 9 and V_{SS}.

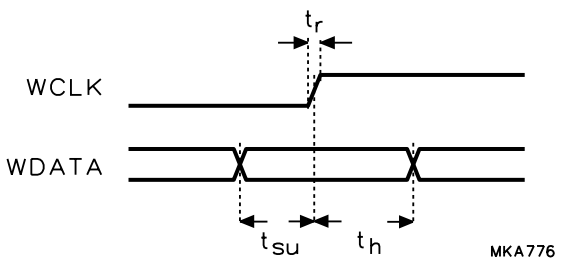


Fig.6 Timing relationship between the edges of WCLK and WDATA.

TEST AND APPLICATION INFORMATION

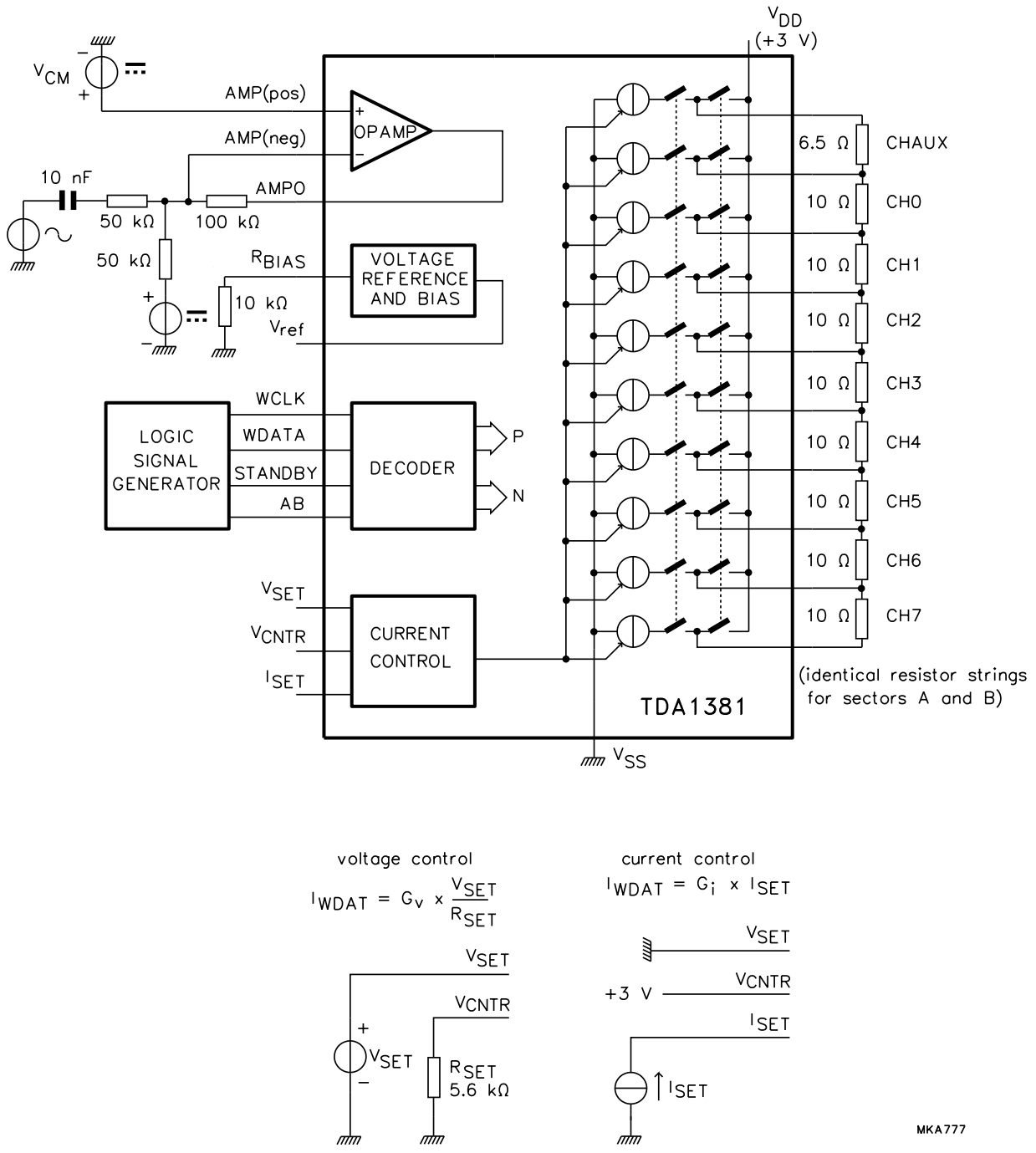


Fig.7 Test circuit.

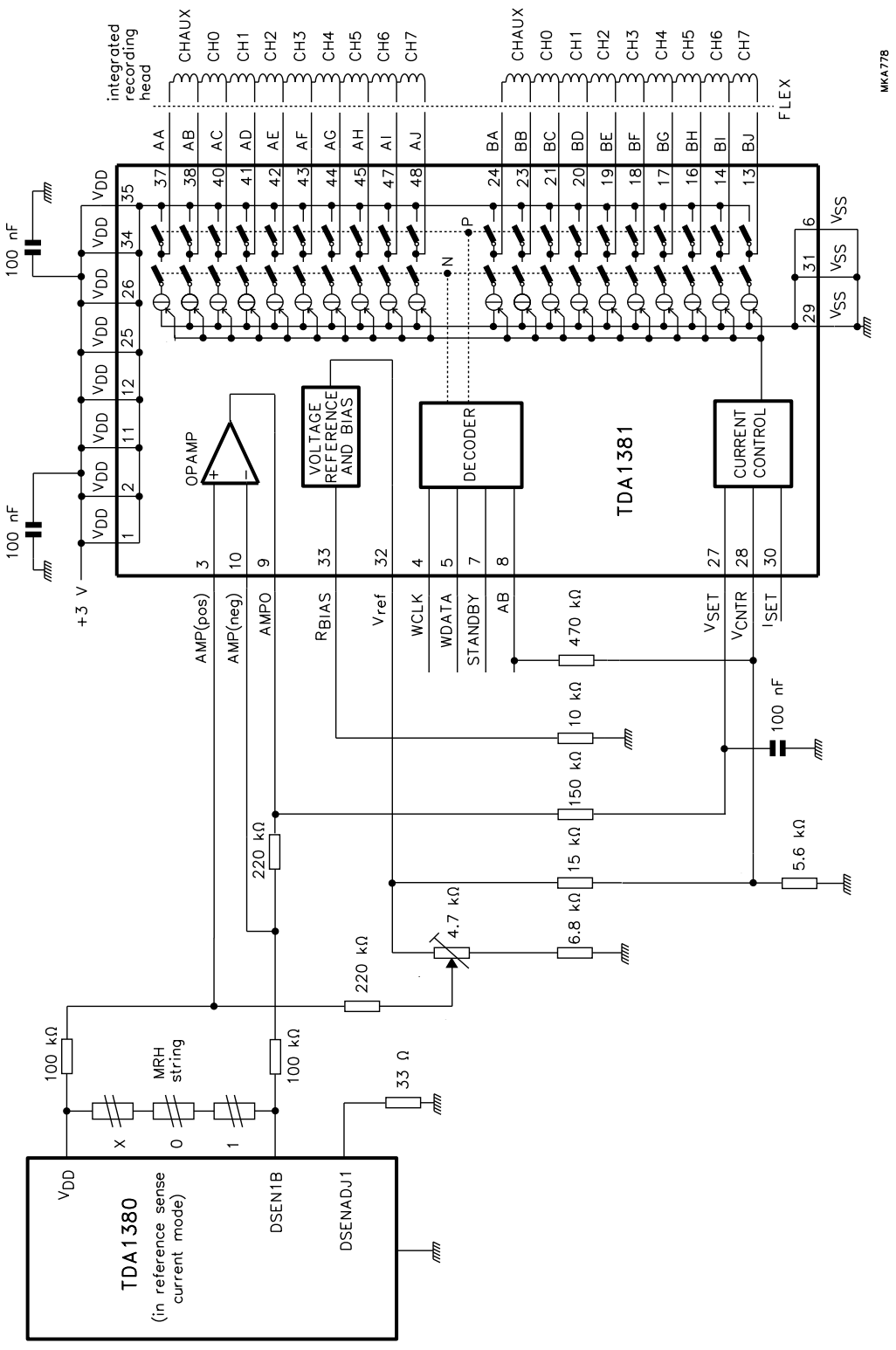
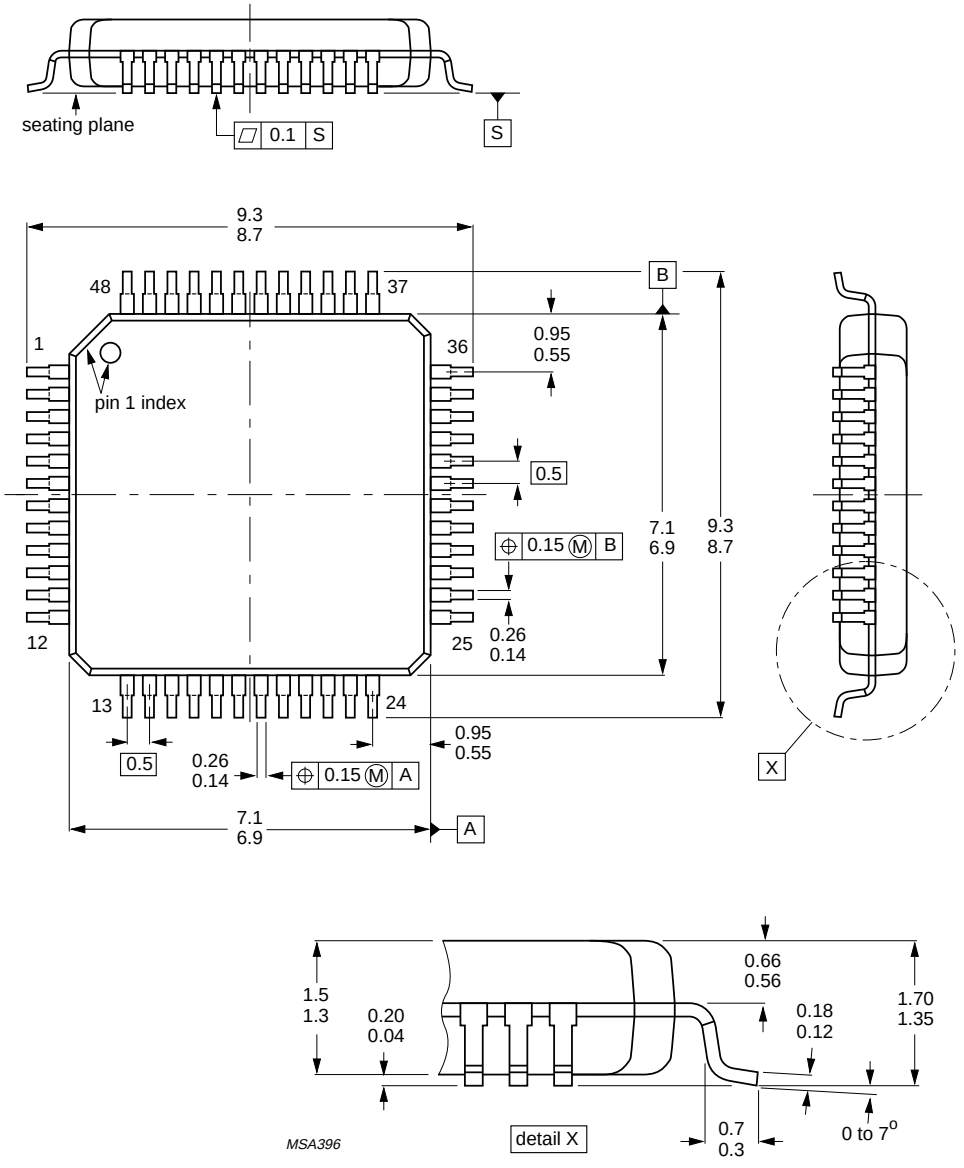


Fig.8 Application diagram.

PACKAGE OUTLINE



Dimensions in mm.

Fig.9 Plastic thin quad flat package; 48 leads; body 7 × 7 × 1.4 mm (TQFP48; SOT313-1).

SOLDERING

Plastic quad flat-packs

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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