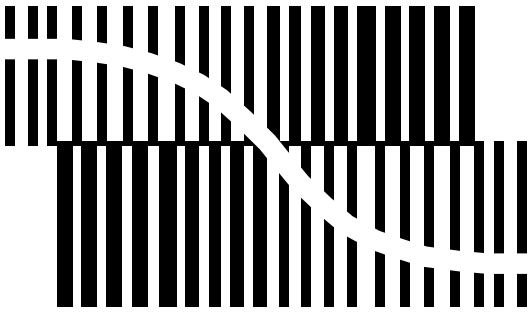
DATA SHEET



TDA1373H
General Digital Input (GDIN)

Product specification
Supersedes data of 1995 Aug 28
File under Integrated Circuits, IC01

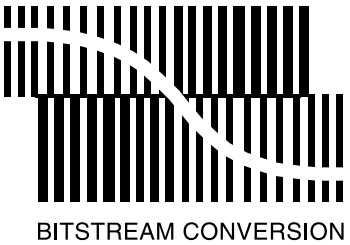
1996 Jul 17

Philips
Semiconductors

PHILIPS

General Digital Input (GDIN) TDA1373H

FEATURES



- Four operating modes:
  - Sample Rate Conversion (SRC) mode
  - AD/DA mode
  - SLAVE-VCO mode
  - SLAVE-VCXO mode
- Full digital sample rate conversion over a wide range of input sample rates
- Fast and automatic detection and locking to the input sample rate with continuous tracking
- Digital Phase-Locked Loop (PLL) with adaptive bandwidth which removes jitter on the digital audio input
- Audio outputs (soft) muted during loop acquisition
- Full linear phase processing based on all-FIR filtering
- Integrated full digital IEC 958 demodulator for digital input signals (AES/EBU or SPDIF format) with intelligent error handling
- Extended input sample frequency range
- IEC 958 Channel Status (CS) and User Channel (UC) outputs
- On-chip CS and/or UC demodulation and buffering (consumer and professional format)
- Dedicated subcode processing for Compact Disc (CD)
- Final output quantization to 16, 18 or 20 bits with optional in-audio-band noise shaping
- Bitstream input and output for coupling with 1-bit analog-to-digital conversion (ADC) and digital-to-analog conversion (DAC)
- I^2S and Japanese serial input formats supported for SRC and DAC functions
- I^2S and Japanese serial output formats supported for SRC and ADC functions
- I^2S and Japanese 4× oversampled serial output available for SRC and ADC functions
- 8-bit digital gain/attenuation control
- Switchable Digital Signal Processor (DSP)-interface (I^2S input and output) for additional audio processing
- Additional clock outputs available at 768, 384, 256 and $128f_{so}$
- 3-line serial microcontroller interface, compatible with the Philips CD I.C. protocol (HCL)
- 5 V power supply
- 0.7 μm double metal Complementary Metal Oxide Semiconductor (CMOS)
- SRC THD + N:
  - −113 dB over the 0 to 20 kHz band (1 kHz, 20 bits input and output) (see Fig.3)
  - −95 dB over the 0 to 20 kHz band (1 kHz, 16 bits input and output)
- Pass band ripple smaller than ±0.004 dB for up-sampling and down-sampling filters
- Stop band suppression:
  - selectable between 70 dB and 50 dB for 64× up-sampling filters
  - 80 dB for 128× down-sampling filters
- Microcontroller operated and stand-alone mode.

APPLICATIONS

- Professional audio equipment for:
  - mixing
  - recording
  - editing
  - broadcasting
- CD-Recordable (CD-R)
- Digital Speaker Systems (DSS)
- Digital Compact Cassette recorders (DCC)
- Digital Audio Tape (DAT) and MD recorders
- Digital amplifiers
- Jitter killers.

GENERAL DESCRIPTION

The TDA1373H is a General Digital Input (GDIN) device for audio signals which is able to perform a high-quality sample rate conversion of digital audio signals (**SRC mode**). The device reads several serial input formats and signals in the IEC 958 digital audio format (also known as AES/EBU or SPDIF signals). For this purpose a full Audio Digital Input Circuit (ADIC) is present in the device.

An internal digital PLL results in extensive jitter removal from incoming digital audio signals without any analog loop electronics. The standard 20 bit output word length can be limited to 16 or 18 bits by means of 'in-audio-band noise shaping'.

The GDIN digital filters can also be reused for Bitstream ADC and DAC conversion (**AD/DA mode**). The internal digital PLL can be reconfigured to operate the GDIN in a slave mode, where the output sample frequency of the device is locked to the incoming sample rate (**SLAVE-VCO** and **SLAVE-VCXO** modes).

The combination of an ADIC function, sample rate conversion and Bitstream ADC and DAC results in a device with a highly versatile functionality and large replacement value in consumer and professional audio sets.

QUICK REFERENCE DATA

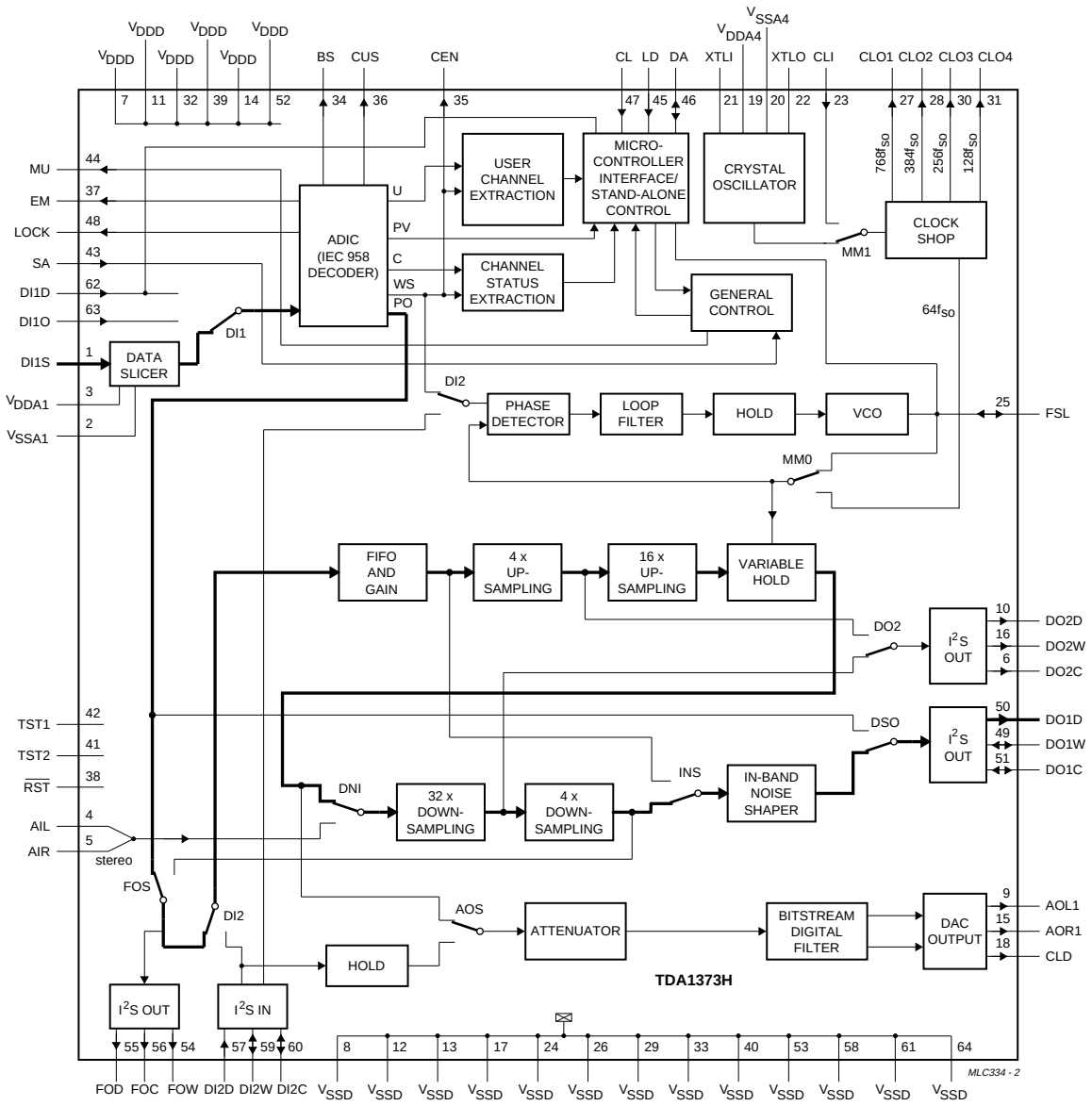
All inputs and outputs CMOS compatible; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	$f_{so} > 44.1$ kHz	4.75	5	5.5	V
		$f_{so} \leq 44.1$ kHz	4.5	5	5.5	V
$I_{DD(tot)}$	total supply current	$f_{so} = 44.1$ kHz	–	155	–	mA
P_{tot}	total power dissipation	$f_{so} = 44.1$ kHz	–	775	–	mW
		$f_{so} = 49$ kHz; $V_{DD} = 5.5$ V	–	1030	–	mW
IEC 958 input DI1S (high-sensitivity IEC input)						
$V_{i(p-p)}$	AC input voltage (peak-to-peak value)		0.2	–	V_{DD}	V
Clock and timing						
$f_{so(max)}$	maximum output sample frequency	$V_{DD} = 4.75$ V	49	55	–	kHz
Temperature						
T_{amb}	operating ambient temperature		0		70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1373H	QFP64	Plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.7 mm; high stand-off height	SOT319-1

BLOCK DIAGRAM



Switches MM1 and MM0 are controlled indirectly via the mode selection. All other switches can be controlled directly by the user.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION	TYPE
DI1S	1	IEC 958 digital audio input 'S' (200 mV peak-to-peak value)	E036A
V_{SSA1}	2	IEC 958 slicer analog ground	E038A
V_{DDA1}	3	IEC 958 slicer analog supply voltage	E037A
AIL	4	Bitstream audio input left	HPP01
AIR	5	Bitstream audio input right	HPP01
DO2C	6	serial digital audio output 2; bit clock output ($192f_{so}$)	OPF40
V_{DDD}	7	digital supply voltage; note 1	–
V_{SSD}	8	digital ground; note 2	–
AOL1	9	Bitstream audio output left	OPF40
DO2D	10	DLO = 0; serial digital audio output 2; data; DLO = 1; Bitstream audio output left inverted ($\overline{AOL1}$); note 3	OPF40
V_{DDD}	11	digital supply voltage; note 1	–
V_{SSD}	12	digital ground; note 2	–
V_{SSD}	13	digital ground; note 2	–
V_{DDD}	14	digital supply voltage; note 1	–
AOR1	15	Bitstream audio output right	OPF40
DO2W	16	DLO = 0; serial digital audio output 2; word select output ($4f_{so}$); DLO = 1; Bitstream audio output right inverted ($\overline{AOR1}$); note 3	OPF40
V_{SSD}	17	digital ground; note 2	–
CLD	18	Bitstream DAC clock (192 or $128f_{so}$)	OPF43
V_{DDA4}	19	oscillator analog supply voltage	E037A
V_{SSA4}	20	oscillator analog ground	E038A
XTLI	21	crystal input $768f_{so}$	OSX01
XTLO	22	crystal output	OSX01
CLI	23	external VCO input (SLAVE-VCO mode only)	HPP01
V_{SSD}	24	digital ground; note 2	–
FSL	25	SA = 0 (microcontroller operated) external VCO output (slave modes only); SA = 1 (stand-alone control) DI11 control line; note 4	HOF21
V_{SSD}	26	digital ground; note 2	–
CLO1	27	clock output $768f_{so}$	OPF40
CLO2	28	clock output $384f_{so}$	OPF40
V_{SSD}	29	digital ground; note 2	–
CLO3	30	clock output $256f_{so}$	OPF40
CLO4	31	clock output $128f_{so}$;	OPF40
V_{DDD}	32	digital supply voltage; note 1	–
V_{SSD}	33	digital ground; note 2	–
BS	34	block sync; channel status/user channel/CD subcode	OPF40
CEN	35	data enable; channel status/user channel/CD subcode	OPF40
CUS	36	data bit; channel status/user channel/CD subcode	OPF40
EM	37	IEC 958 source pre-emphasis flag	OPF20

SYMBOL	PIN	DESCRIPTION	TYPE
$\overline{RST}$	38	power-on reset input (active LOW)	HPP07
V_{DDD}	39	digital supply voltage; note 1	–
V_{SSD}	40	digital ground; note 2	–
TST2	41	test pin 2 (LOW for normal operation)	HPP01
TST1	42	test pin 1 (LOW for normal operation)	HPP01
SA	43	Stand-alone/microcontroller operated selection; SA = 1 for stand-alone operation	HPP01
MU	44	mute flag (active HIGH)	OPF40
LD	45	SA = 0 (microcontroller operated) microcontroller interface; load (read/write); SA = 1 (stand-alone control) NSD control line; note 4	HPP01
DA	46	SA = 0 (microcontroller operated) microcontroller interface (data); SA = 1 (stand-alone control) DI2 control line; note 4	HOF41
CL	47	SA = 0 (microcontroller operated) microcontroller interface (clock); SA = 1 (stand-alone control) QU1/QU0 control line; note 4	HPP01
LOCK	48	ADIC lock flag (active HIGH)	OPF40
DO1W	49	serial digital audio output 1; word select input/output (f_{so})	HOF41
DO1D	50	serial digital audio output 1; data	OPF43
DO1C	51	serial digital audio output 1; bit clock input/output ($48f_{so}$)	HOF41
V_{DDD}	52	digital supply voltage; note 1	–
V_{SSD}	53	digital ground; note 2	–
FOW	54	serial digital audio feature output; word select	OPF43
FOD	55	serial digital audio feature output; data	OPF43
FOC	56	serial digital audio feature output; bit clock ($64f_{so}$)	OPF43
DI2D	57	serial digital audio input 2; data	HPP01
V_{SSD}	58	digital ground; note 2	–
DI2W	59	serial digital audio input 2; word select	HOF21
DI2C	60	serial digital audio input 2; bit clock output	HOF21
V_{SSD}	61	digital ground; note 2	–
DI1D	62	SA = 0 (microcontroller operated) IEC 958 digital audio input ‘D’ (CMOS level); SA = 1 (stand-alone control) MSO control line; note 4	HPP01
DI1O	63	IEC 958 digital audio input ‘O’ (CMOS level)	HPP01
V_{SSD}	64	digital ground; note 2	–

Notes

1. All V_{DDD} pins are internally connected.
2. All V_{SSD} pins are internally connected.
3. DLO is a command flag from register 4 (see Section “Command registers”).
4. SA is the stand-alone/microcontroller operated pin (pin 43). DI11, NSD, DI2, QU1, QU0 and MS0 are command flags to control the operation of the device. For more information see Section “Controlling the GDIN”.

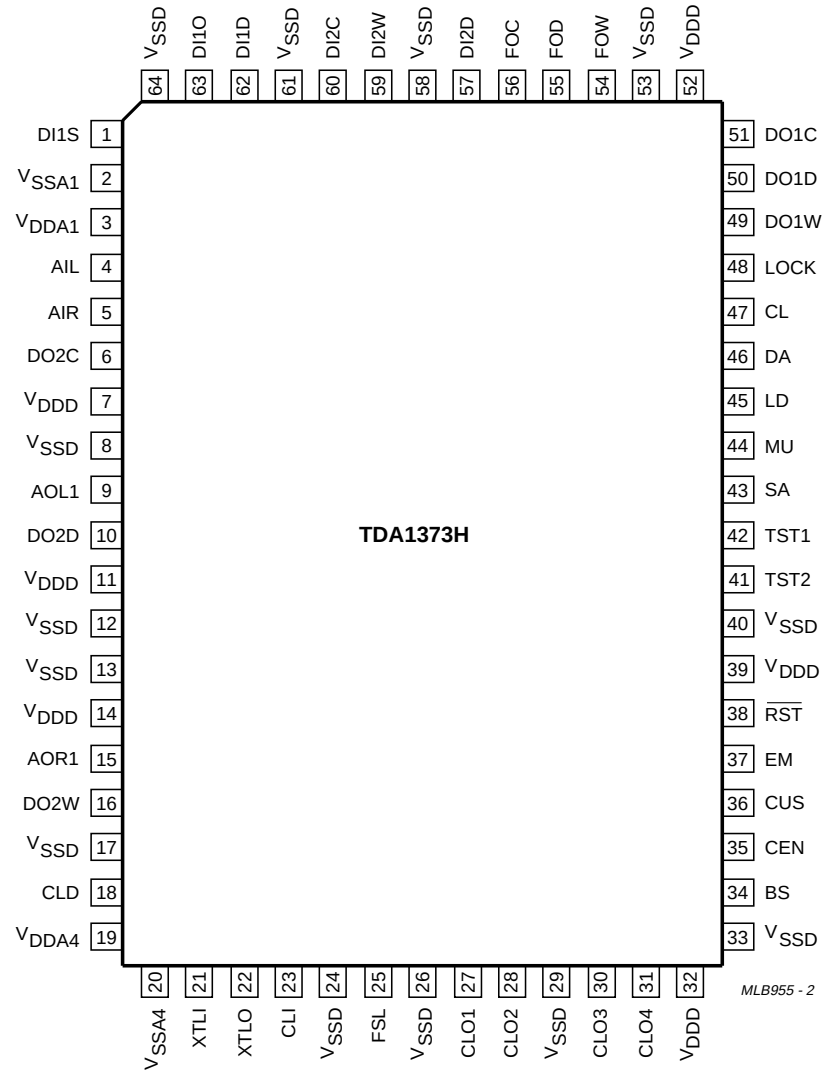


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Operating modes

SAMPLE RATE CONVERSION (SRC) MODE

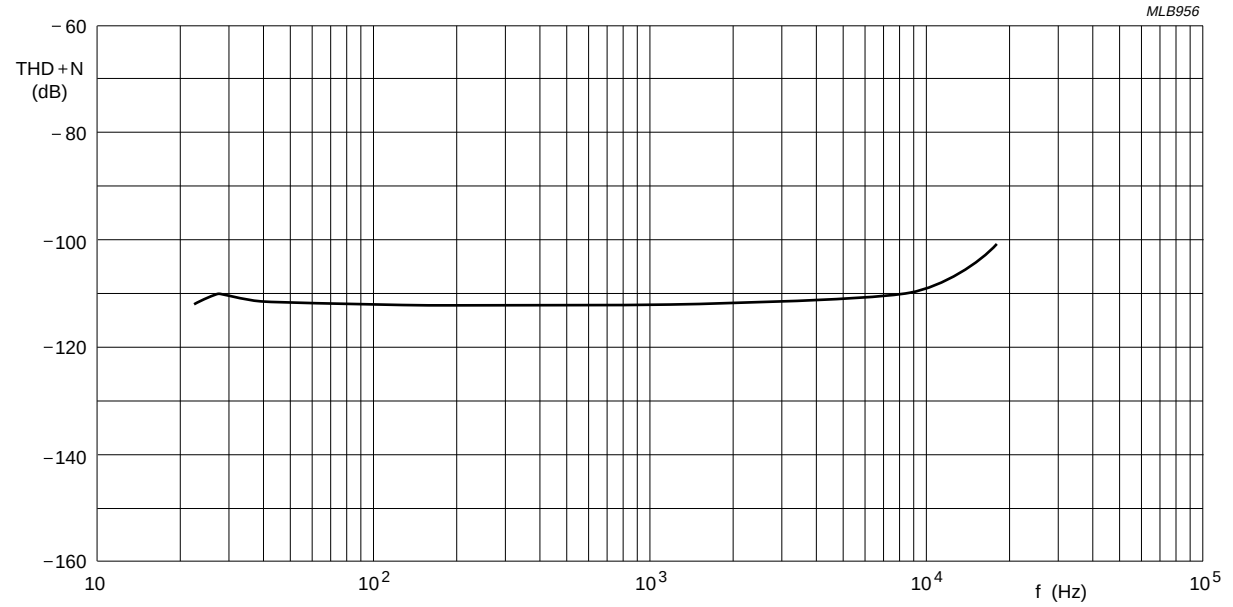
The output sample rate is determined by a crystal and can be chosen up to 49 kHz. The range of input sample rates for a given output sample rate is given in Table 1. A pitch variation ('Varispeed') of ±12% around the nominal input sample rate can be tracked.

Data path (see Fig.4)

The input signal at sample frequency f_{si} comes in via one of the DI1 inputs (IEC 958) or via the serial input DI2X. The signal passes through the FIFO/GAIN part and is interpolated in the up-sampling filters. The actual sample rate conversion takes place in the variable hold block. The down-sampling filters decimate the sample frequency to f_{so} and after in-band noise shaping, the output signal is present at serial output DO1. Additionally the converted signal is available at the 'analog' Bitstream outputs AOL, AOR and at the serial digital output DO2 ($4f_{so}$).

Table 1 Input sample rates

OUTPUT SAMPLE RATE (kHz)	I^2S INPUT (kHz) 0.3 to $1.7f_{so}$	IEC 958 INPUT (kHz) 0.35 to $1.45f_{so}$
48	13 to 83	16 to 68
44.1	12 to 76	15 to 62
32	9 to 55	12 to 45



Measurement done with 'Audio Precision'.
SRC mode; 48 to 44.1 kHz; 20-bit output.

Fig.3 Total harmonic distortion plus noise as a function of frequency.

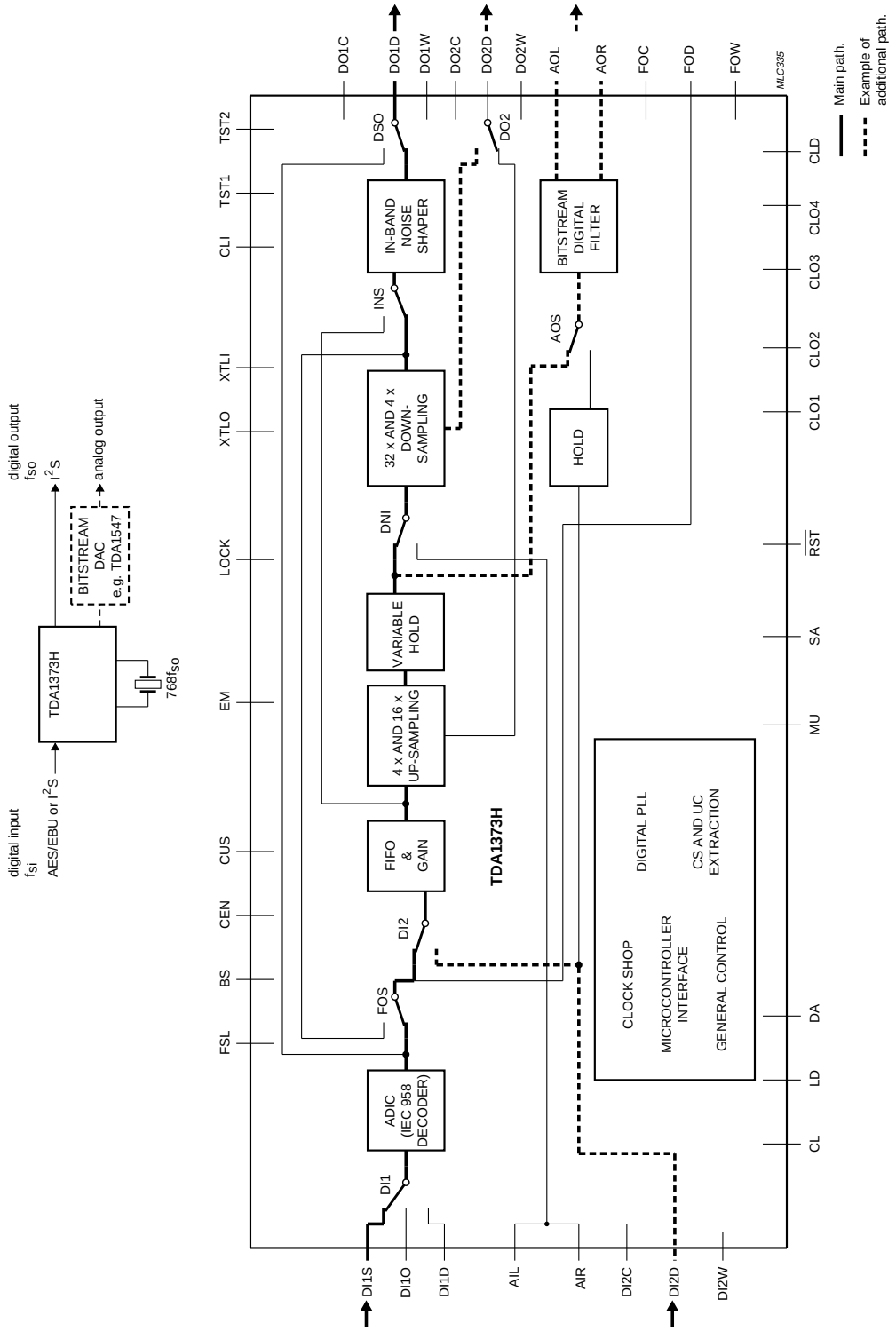


Fig.4 Standard data path in the SRC mode.

SLAVE-VCO AND SLAVE-VCXO MODES

In the SLAVE-VCO and SLAVE-VCXO modes, the GDIN can pass an exact copy of the incoming samples to the output, e.g. for storage on a digital medium such as CD-R. The output sample rate tracks any input sample rate within the frequency range of the external VC(X)O ($f_{so} = f_{si}$).

In the SLAVE-VCO mode a pitch variation of ±12.5% around the nominal sample frequency can be tolerated.

Data path (see Fig.5)

The signal at input sample frequency f_{si} comes in via one of the DI1 inputs (IEC 958).

The ADIC signal passes through the FIFO/GAIN block and can be fed through the IN-BAND NOISE SHAPER to the serial output DO1. Additionally, the signal is present at DO2 ($4f_{so}$) and at the Bitstream outputs AOL and AOR.

Exact copies for digital use (e.g. write to a disk) from the input signal can be retrieved at output FO (this signal might be affected by jitter since it has not passed through the FIFO/GAIN block). By means of data path switch DSO, this direct output of the ADIC block can also be fed to output DO1. Note that in this event the DO1 serial format becomes equal to the FO format (see Table 3).

AD/DA MODE

In this mode, the GDIN supports an economic realization of analog-to-digital and digital-to-analog conversion, in accordance with the Bitstream principle. This requires a Bitstream sigma-delta modulator and a Bitstream DAC, since the up-sampling and down-sampling filters of the sample rate convertor are reused. ADC and DAC can be simultaneously performed.

Data path DA conversion (see Fig.6)

The signal at sample frequency f_{so} comes in via serial input DI2X or via one of the DI1 inputs (IEC 958). The signal passes through the FIFO/GAIN part and is interpolated in the up-sampling filters. A Bitstream digital filter converts this signal into a Bitstream signal at outputs AOL and AOR, after which it can be filtered by a Bitstream DAC like the TDA1547.

Data path AD conversion (see Fig.6)

The Bitstream signal from the sigma-delta modulator enters the GDIN at inputs AIL and AIR. The down-sampling filters decimate this signal to f_{so} and after in-band noise shaping (selectable), the output signal is present at serial output DO1.

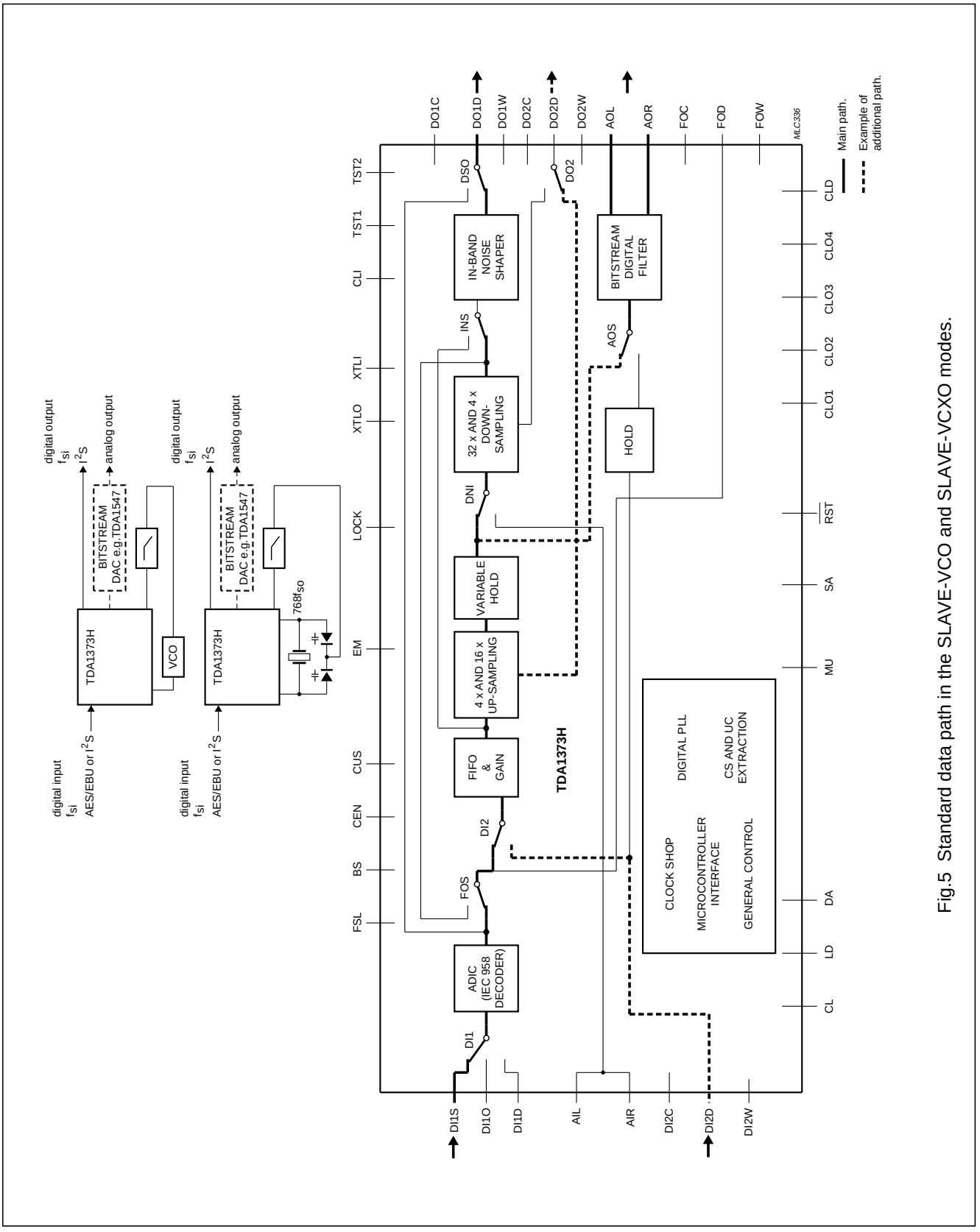


Fig.5 Standard data path in the SLAVE-VCO and SLAVE-VCXO modes.

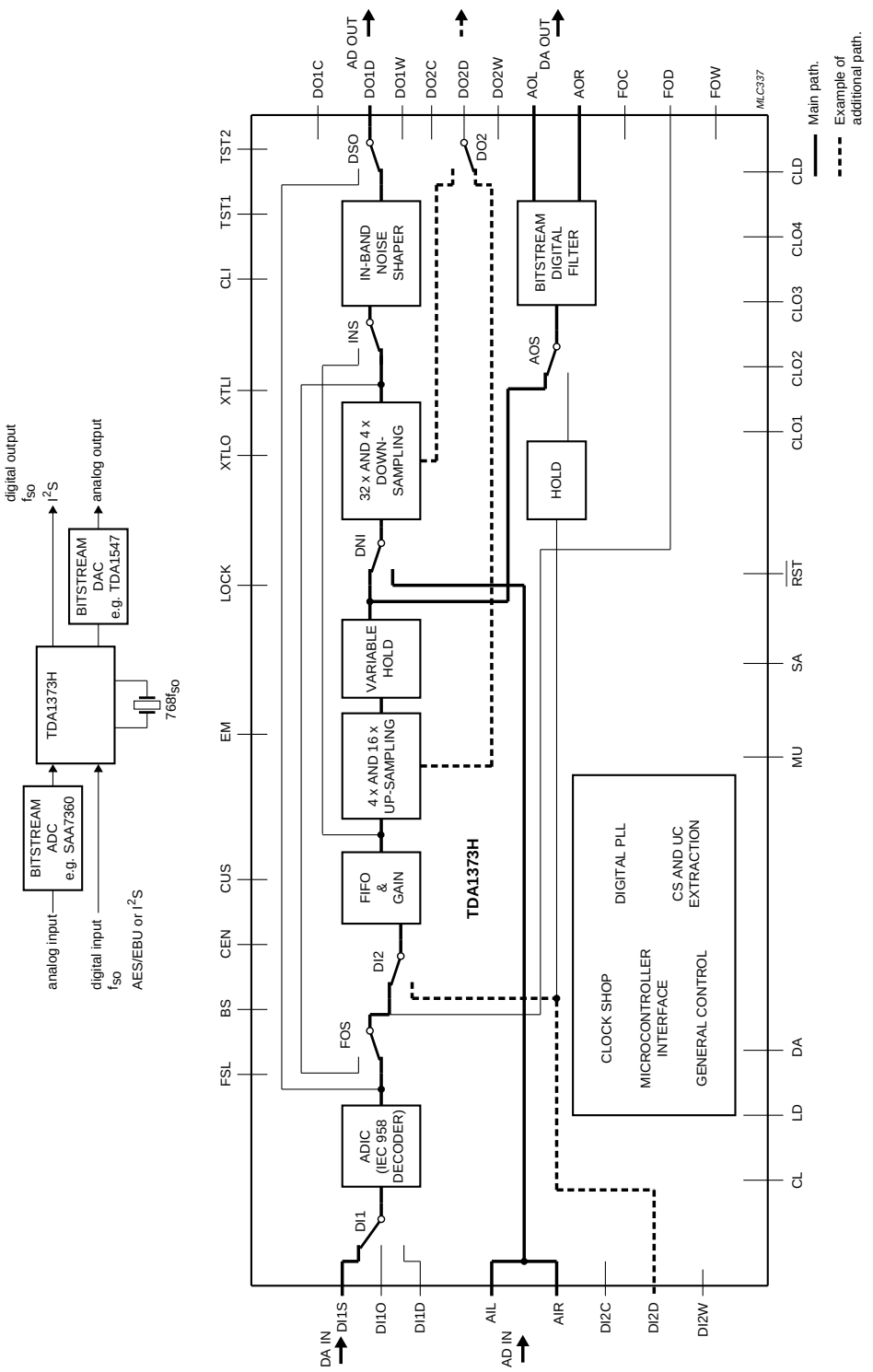


Fig.6 Standard data paths in the AD/DA mode.

Description of functional blocks

IEC 958 AUDIO DIGITAL INPUT CIRCUIT

The TDA1373H has three IEC 958 inputs:

1. DI1S.
2. DI1O.
3. DI1D.

DI1S accepts IEC 958 line signals (minimum 200 mV peak-to-peak value and maximum 5 V peak-to-peak value), DI1O and DI1D accept only CMOS level signals. The input sample rate range that can be handled depends on the output sample frequency (f_{so}) of the device.

The maximum useful word length of the incoming samples is 20 bits.

The internal ADIC retrieves the stereo audio samples, the V, U, C and P data bits, the ADIC word clock and the bit clock from the selected IEC 958 input signal. The digital ADIC locks in less than 1 ms for a 44.1 kHz input signal. During this lock-in time the word clock is stopped and the audio bits are muted.

The validity flag (VA), pre-emphasis flag and pin (EM), lock flag (LCK) and lock pin (LOCK) are available to check the status of the ADIC. This validity flag is an OR-ing of the incoming validity (V) bit and the own error detection of the ADIC. The actions which take place in case of detected errors are listed in Table 2.

SERIAL DIGITAL INPUTS DI2W, DI2D AND DI2C

The serial digital input DI2 can be used as standard input instead of the DI1 IEC 958 input or can be used together with the FO-output to switch a DSP IC in the input data path. A third possibility is to use DI2 as direct input to the GDIN Bitstream digital filter. In that case the DI2 input signal should be 4× oversampled externally. The serial formats supported are shown in Fig.7 and Table 3.

Table 2 Error concealment in the IEC 958 decoder

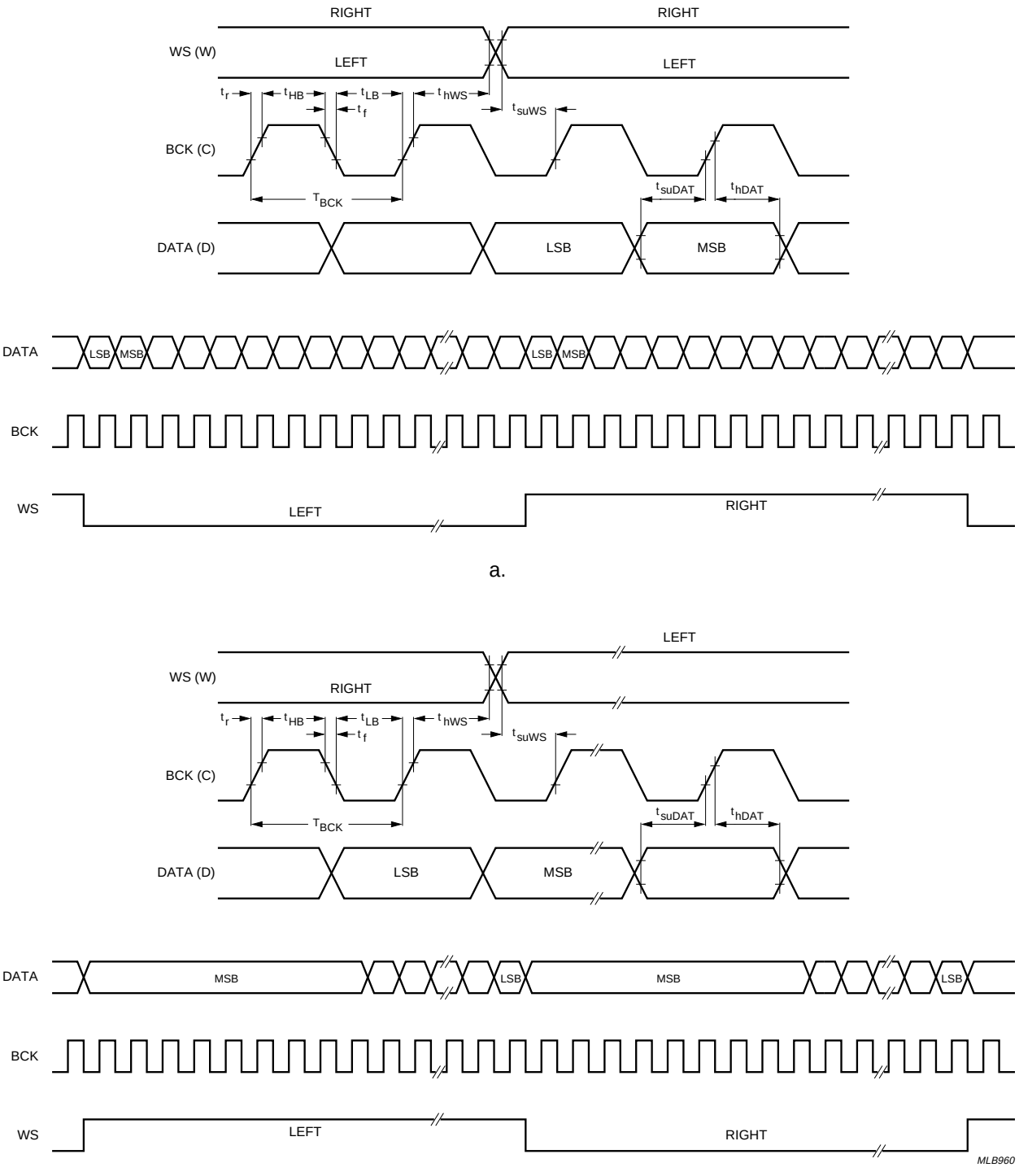
ERROR	ACTION DATA	ACTION WORD CLOCK
Validity (V-bit) error	pass sample	no action
Parity (P-bit) error	repeat last correct sample	
Number of data bits ≠32		
Missing pre-amble(s)		
Extra pre-amble(s)		
More than 4 pre-ambles missing or extra	mute output; restart	stop ADIC word clock

Table 3 Serial input and output formats (see note 1)

INPUT OUTPUT	f_{WS}	f_{BCK}	I^2S	JAPANESE 16-BIT	JAPANESE 18-BIT	JAPANESE 20-BIT	3-STATE	CONTROL BITS
DI2	f_{si}	$\leq 128f_{si}$	S	S	S	S	no	DI2, DI21 and DI22
	$4f_{so}$	$192f_{so}$	M	S	S	S	no	DI2
DO1	f_{so}	$48f_{so}$	M	M	M	–	yes	DO1S, DO11 and DO12
		$\leq 128f_{so}$	S	–	–			
DO2	$4f_{so}$	$192f_{so}$	M	M	M	–	no	DO2, DO21 and DO22
FO	f_{si}	$64f_{so}$	M	–	–	–	yes	FO and FO1

Note

1. S = slave; M = master.



a. I^2S input format.
b. Japanese input format.

Fig.7 Timing diagram for the serial input and output formats.

SERIAL DIGITAL OUTPUTS DO1W, DO1D AND DO1C

Depending on the operating mode and data path switching, DO1 can contain the output of the in-band noise shaper or can be directly connected to the output of the internal ADIC. The supported serial formats and modes of this interface are given in Table 3.

In case the GDIN goes out-of-lock the output data is muted and if the output is configured as master transmitter, the word clock slips half a word clock period. If this is undesirable, use the serial output as a slave transmitter.

SERIAL DIGITAL OUTPUTS DO2W, DO2D AND DO2C

The additional digital audio output DO2 operates at $4f_{so}$. DO2 can contain data of the up-sampling (not in SRC mode) or down-sampling filters. The formats supported are shown in Table 3.

SERIAL FEATURE OUTPUTS FOW, FOD AND FOC

The internal ADIC output is directly available in I^2S format at this output. This makes it possible to switch a DSP featuring IC in the data path before SRC (at f_{si}). See Table 3 for the formats supported.

BITSTREAM INPUTS AIL AND AIR

The Bitstream input receives data at $128f_{so}$ from a 1-bit sigma-delta modulator. Possible Bitstream inputs at $64f_{so}$ are held twice. The timing diagram for the Bitstream inputs and outputs is given in Fig.8.

BITSTREAM OUTPUTS AOL1 AND AOR1

The Bitstream output generates a 128 (SRC and SLAVE modes) or 192 (AD/DA mode) times oversampled Bitstream and can be connected to a Bitstream DAC (e.g. TDA1547) for high-quality DAC. It is also possible to get the inverted Bitstream signals on the complementary Bitstream outputs $\overline{AOL1}$ (pin DO2D) and $\overline{AOR1}$ (pin DO2W) by setting the DLO control bit. By using a simple low-pass filter, this symmetrical Bitstream output can be used to make an inexpensive analog monitor output. In that event the serial digital output DO2 cannot be used.

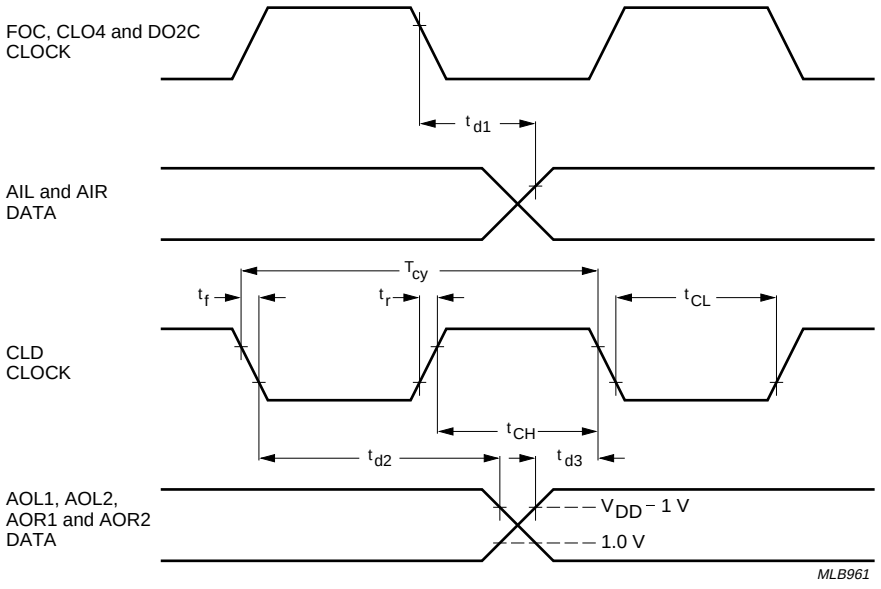


Fig.8 Timing diagram for the Bitstream inputs and outputs.

FIRST-IN FIRST-OUT (FIFO)

The incoming samples are buffered in a FIFO. The depth of this FIFO determines the transients that can be allowed in the input frequency, as they may occur during pitch control. The FIFO has a depth of 8 samples, which makes GDIN support a tracking speed of up to 4 kHz/ms. FIFO overflow detection is provided to detect out-of-lock situations.

GAIN CONTROL

At the begin of the data path, the signal level can be controlled over a gain/attenuation range from 2 to 0 with a step size of 2E-7. This gain control can be used for volume control, gain correction and fade-in or fade-out. For normal operation, the gain level should be set to 1-2E-7 (–0.068 dB) to avoid pass band ripple clipping in the digital filters. Whenever a new gain value is set, the gain level is increased or decreased by one step per input sample until the new entered value is reached.

Setting the MMU control bit forces the GDIN to start a soft muting. The gain is decreased, by one step per input sample, to zero. Clearing the MMU bit will increase the gain back to its original value. Only those outputs, for which the signal passes through the 'gain control' part, are muted.

64× UP-SAMPLING FILTER

A 64× (4× and 16×) oversampling filter is incorporated in the GDIN for the SRC process. This filter can also be used as the up-sampling filter for a Bitstream digital-to-analog conversion in the AD/DA mode, in combination with the Bitstream digital filter and Bitstream DAC (e.g. TDA1547). Two filter characteristics can be chosen by the control bit SS (see Table 4).

The 50 dB stop band suppression mode is especially suited for 32 kHz input sources like Digital Satellite Radio (DSR), where a very narrow transition band is required to obtain 0 to 15 kHz pass band.

VARIABLE HOLD

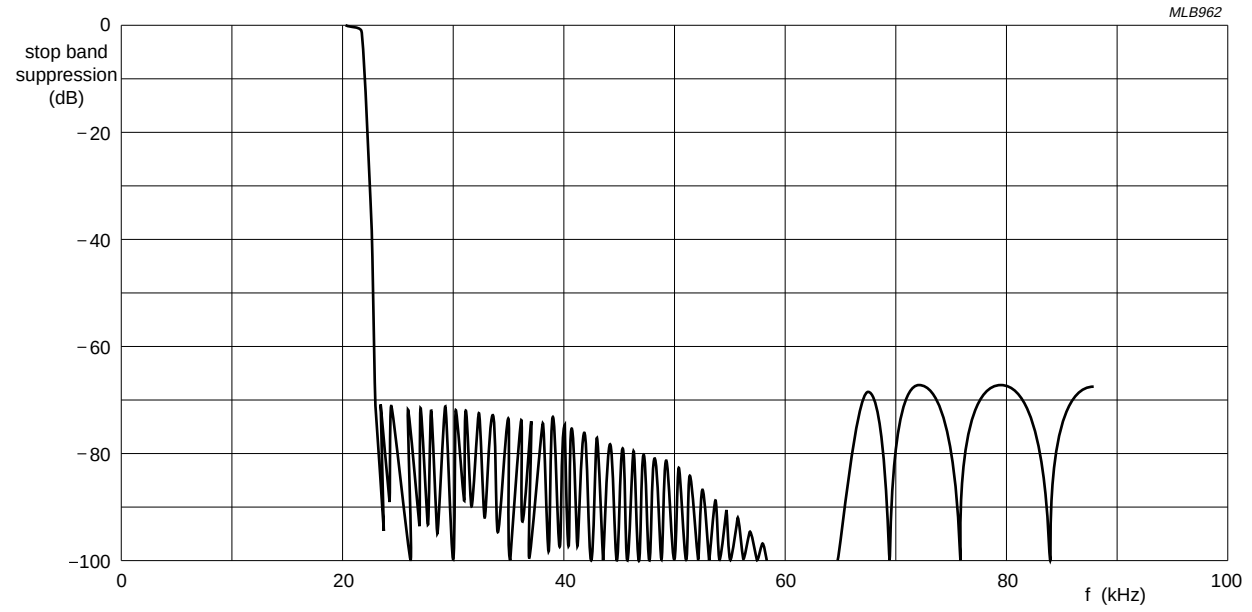
In SRC mode, the variable hold is the interface between the 64× up-sampling filters ($64f_{si}$) and the 128× down-sampling filters ($128f_{so}$). In SLAVE and AD/DA modes, the variable hold holds each sample twice from $64f_{si}$ to $128f_{si}$ ($f_{si} = f_{so}$).

128× DOWN-SAMPLING FILTER (see Fig.10)

After SRC, a 128× (32× + 4×) down-sampling filter decimates the signal to f_{so}. In the AD/DA mode, this filter is used as the ADC down-sampling filter for a Bitstream sigma-delta modulator. The stop band suppression is 80 dB from $0.54648f_{so}$ (e.g. 24.1 kHz at f_{so} = 44.1 kHz).

Table 4 Filter characteristics 64× up-sampling filter

SS	PASS BAND		STOP BAND	
0	0 to $0.45351f_{si}$	±0.004 dB	$0.54648f_{si}$ to $1f_{si}$	–70 dB
1	0 to $0.46875f_{si}$	±0.004 dB	$0.53125f_{si}$ to $1f_{si}$	–50 dB



SS = 0; 70 dB stop band suppression.

Fig.9 Filter characteristic 64× up-sampling filter.

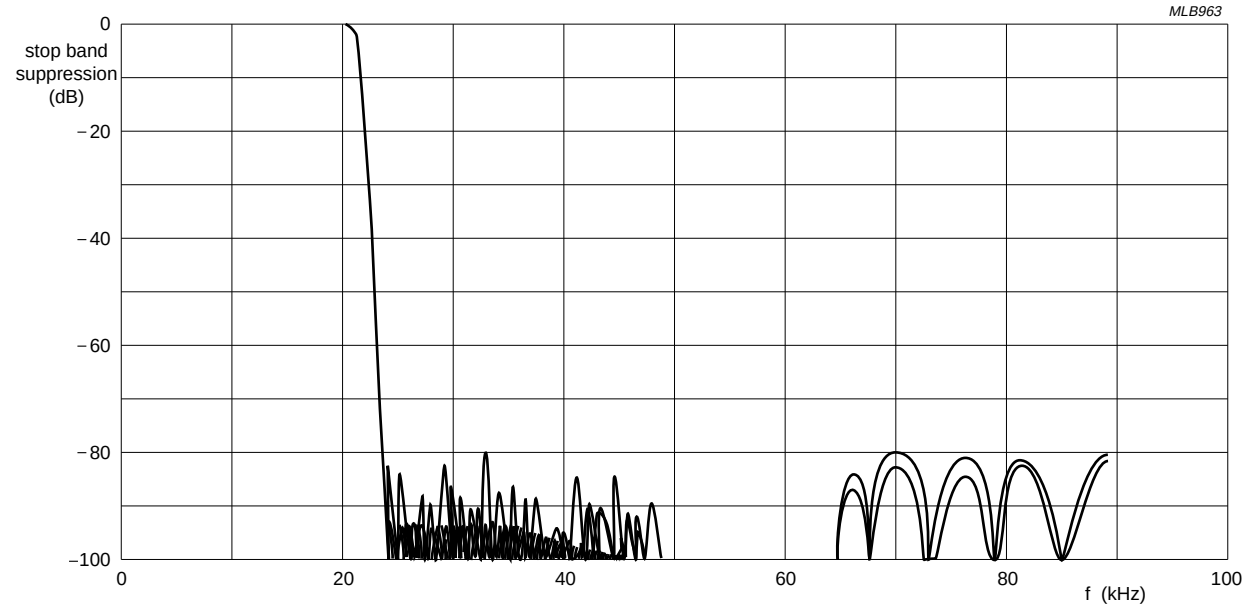


Fig.10 Filter characteristic 128× down-sampling filter.

IN-BAND NOISE SHAPING (INS)

The standard 20-bit output word length can be reduced to 16 or 18 bits to match digital consumer equipment. Normally 16 bit output re-quantization at audio-band sample rates drops the signal-to-noise ratio (S/N) inevitably to 95 dB, because of the re-quantization noise at −98 dB.

It is possible however to shape the re-quantization noise in a psycho-acoustical way. This reduces the re-quantization noise at the frequencies where the human ear is most sensitive and stores the bulk of re-quantization noise at high frequencies, where the human ear is quite insensitive.

The In-band Noise Shaping function (to 16 or 18 bits) results in a subjective quality improvement of about 2 bits below the actual quantization level.

It is also possible to re-quantize the 20 bit output to 16 bits without noise shaping but by a simple rounding operation. Table 5 gives an overview of the 4 possible settings.

Table 5 Selectable output word lengths

QU1	QU0	WORD LENGTH
0	0	16 bit (rounded)
0	1	20 bit
1	0	16 bit INS(1)
1	1	18 bit INS(1)

Note

1. INS = In-band Noise Shaping.

BITSTREAM DIGITAL FILTER

The Bitstream digital filter generates a Bitstream signal which should be filtered by a Bitstream DAC (e.g. TDA1547) to become a high-quality analog signal. The input for this block can be selected from the output of the up-sample path or directly from serial input DI2. In this case, the input signal applied to DI2 should be externally oversampled to $4f_{so}$ and further oversampling will be carried out by the hold function. The Bitstream signal has a frequency of $128f_{so}$ (SRC and SLAVE modes) or $192f_{so}$ (AD/DA mode).

To prevent idle patterns in the audio band, it is strongly advised to add out-of-band dither by setting control bit NSD.

DIGITAL PLL

The digital PLL controls the variable hold function which steers the actual SRC process. An adaptive loop filter allows fast locking to the input frequency and a small bandwidth during steady-state. At start-up, the bandwidth of the 3-step digital loop filter is gradually reduced to 0.5 Hz. A difference frequency of 1 Hz is reached within 512 input samples (10 ms at 44.1 kHz), which allows to start the SRC. At this moment the outputs are de-muted, indicated at pin MU and status flag MUT.

The FIFO position is continuously monitored to control the adaptive loop filter. The loop filter switches back to a fast state when the FIFO tends to drift, e.g. during pitch control on the input signal. It is possible to fix the loop filter in one of the three states. In the adaptive mode, the actual state can be monitored by the microcontroller (ST1 and ST0). In SRC mode, the microcontroller can retrieve the exact input sample frequency via the status registers STS3 and STS4.

Table 6 PLL operation modes

LC1	LC0	PLL OPERATION	PLL BANDWIDTH (Hz)
0	0	adaptive	500, 50 or 0.5
0	1	state 1 fixed	500
1	0	state 2 fixed	50
1	1	state 3 fixed	0.5

In both SLAVE modes, a pulse modulated signal at pin FSL is present to control the external VC(X)O. In SLAVE-VCO mode, CLI is the clock input of the GDIN and in SLAVE-VCXO mode XTLI is the clock input. An external 1000 Hz low-pass filter retrieves the control voltage for the VC(X)O. To get the loop characteristics as described above, the centre frequency of the VCO should be at $\frac{1}{2}V_{DD}$ and the sensitivity should be:

$$g_v = \frac{768f_{so(c)}}{\frac{1}{2}V_{DD}} \text{ Hz/V.}$$

The maximum VCO frequency range is:
$(768 \times 0.3)f_{so(c)} < 768f_{si}\ (=f_{so}) < (768 \times 1.7)f_{so(c)}$ (49 kHz).

IEC 958 CHANNEL STATUS AND USER CHANNEL EXTRACTOR (CUP)

The internal ADIC retrieves also the Channel Status (CS) and User Channel (UC) bits from the IEC 958 signal. The C/U processing function block can be programmed for 4 different functions (see Table 7).

Table 7 Overview of selectable CUP functions

SM1	SM0	LR[1]	CUP FUNCTION	RAM BUFFER
0	1	0	extract full C-block left (192 bits/block)	80H to 97H
0	1	1	extract full C-block right (192 bits/block)	80H to 97H
1	0	X	extract full U-block (384 bits/block)	80H to AFH
0	0	X	decode CD-Subcode Q-information (80 bits/CD frame) from U-bits	80H to 89H

Note

1. X = don't care.

The extracted or decoded information can be read in three ways:

- From the internal RAM buffer by a microcontroller (see Section "The RAM buffer")
- At the output pins CUS, BS and CEN (see Fig.11)
- In status registers STS5 and STS6 (permanent 16 'consumer mode' C-bits, see Table 9).

During CD subcode Q extraction, a 16-bit CRC is done over the Q-channel (CRC flag). This flag is only meaningful when the ADIC is locked (LCK flag).

THE RAM BUFFER

A double RAM buffer is present in the device. While reading one buffer, the other buffer is filled with the new incoming data. The RAM buffer can be read in two ways:

1. Interrupt protocol (UIP = 0).
2. User request protocol (UIP = 1).

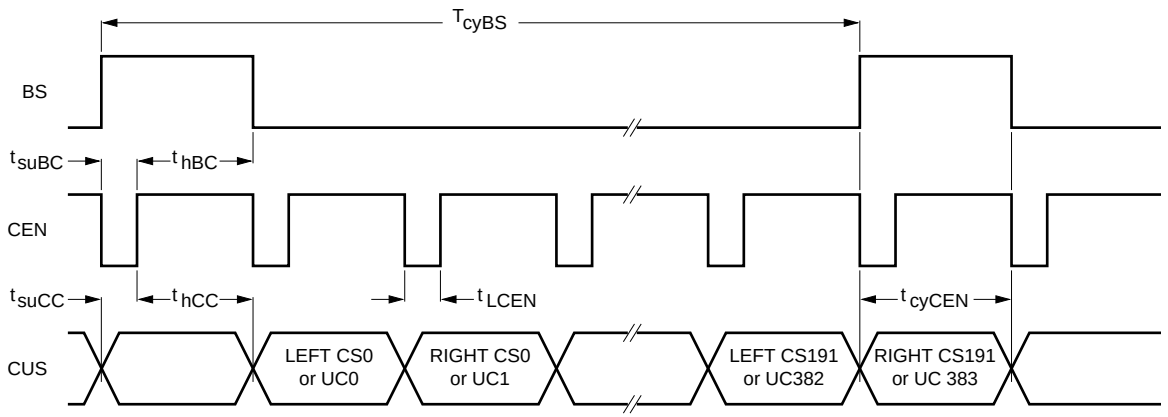
Interrupt protocol (UIP = 0)

A C-block, a U-block or CD Subcode frame is read in the time between two Block Sync (output pin BS) pulses, which can be used as the interrupt for a microcontroller. At a sample rate of 44.1 kHz, the microcontroller must be able to read a C-block or U-block within $\frac{192}{44100}$ = 4.35 ms.

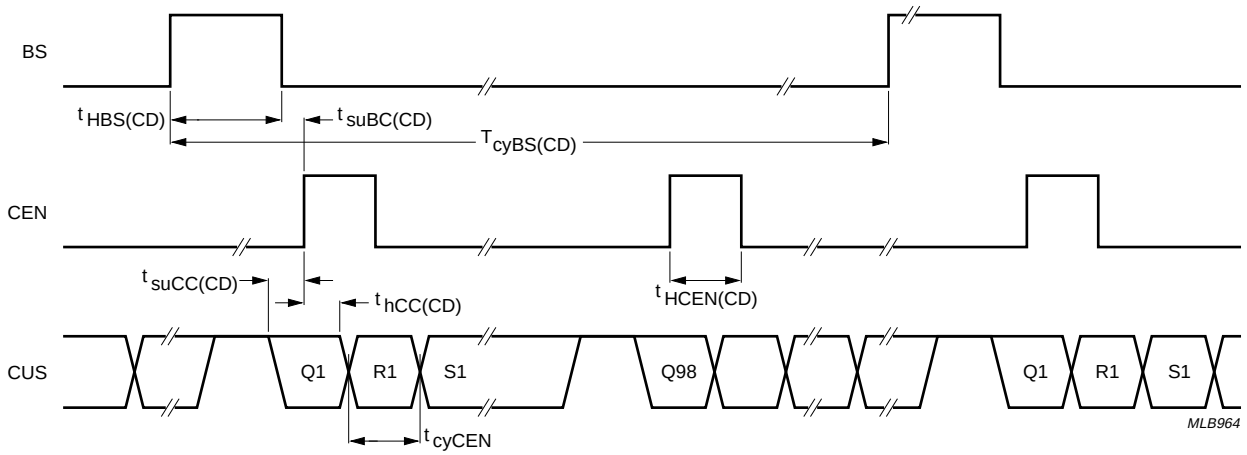
CD Subcode frames are received at a data rate of 75 Hz or 13.3 ms/frame.

User request protocol (UIP = 1)

The microcontroller requests for a C, U and CD-Q block or frame, which will then become available at the next block preamble, indicated by BS. The information is not updated until the next user request, which means the microcontroller can take any time to read the information. The CD Subcode CRC check flag always shows the CRC over the last received CD Subcode Q frame and is not stored with the present Q frame in the buffer. Figure 12 shows the user request read procedure.



a.



b.

a. Channel Status (CS) or User Channel (UC) extraction.
b. CD subcode demodulation.

Fig.11 Timing of the CUS, CEN and BS output pins.

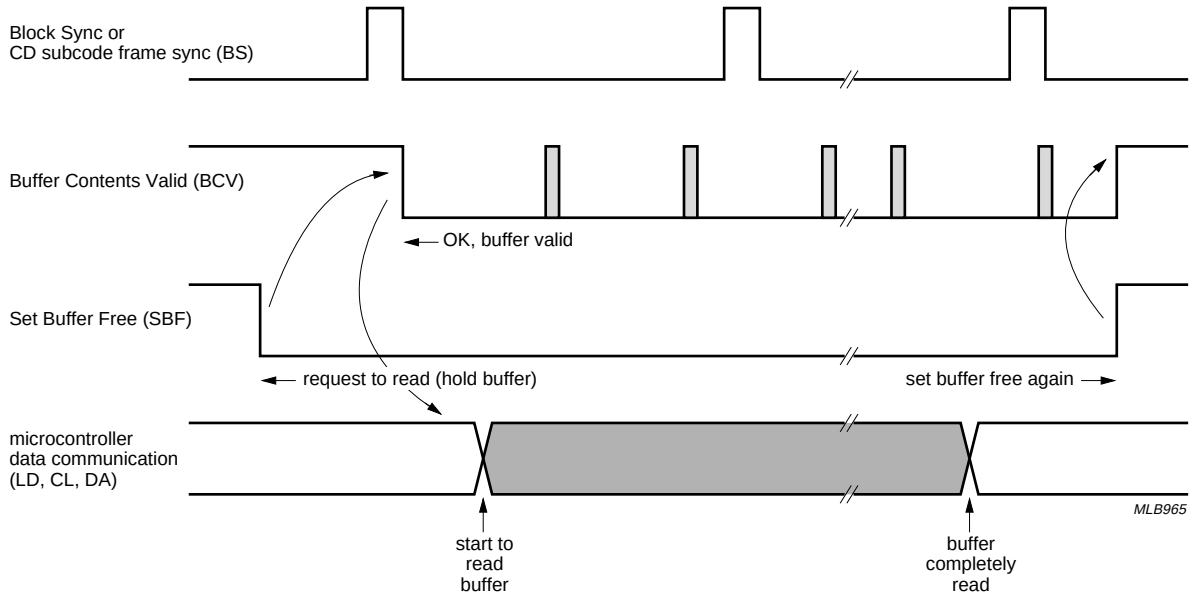


Fig.12 C, U and CD-Q user request procedure.

THE MICROCONTROLLER INTERFACE/ STAND-ALONE CONTROL BLOCK

If pin SA is LOW, a microcontroller controls and monitors the operation of the GDIN and reads C, U and CD-Q information. A 3-line bidirectional serial interface with data (DA), load (LD) and clock (CL) line is present. For both a write and read operation the microcontroller generates the clock and load signals.

A single byte is written by setting the LD signal active HIGH during transmission of the serial data. At the rising edge of the serial clock, the GDIN clocks in the serial data. At the end of the 8-bit data word a ‘load pulse’ should be given to enable the internal serial-to-parallel conversion.

Write operations are always two-byte operations. First, the register address is sent to the GDIN, then the corresponding data is send (see Fig.13):

1. Write Address.
2. Write Data byte.

A single byte read-operation is initialized by pulling LD LOW. When the serial clock is started, the GDIN will transmit serial data on the DA line. The information is read by the microcontroller at the rising edges of the clock CL.

Read operations are at least two-byte operations with multi-byte reads possible. The address is sent to the GDIN and then one or more bytes are read from the GDIN with each additional byte coming from an incrementally higher address:

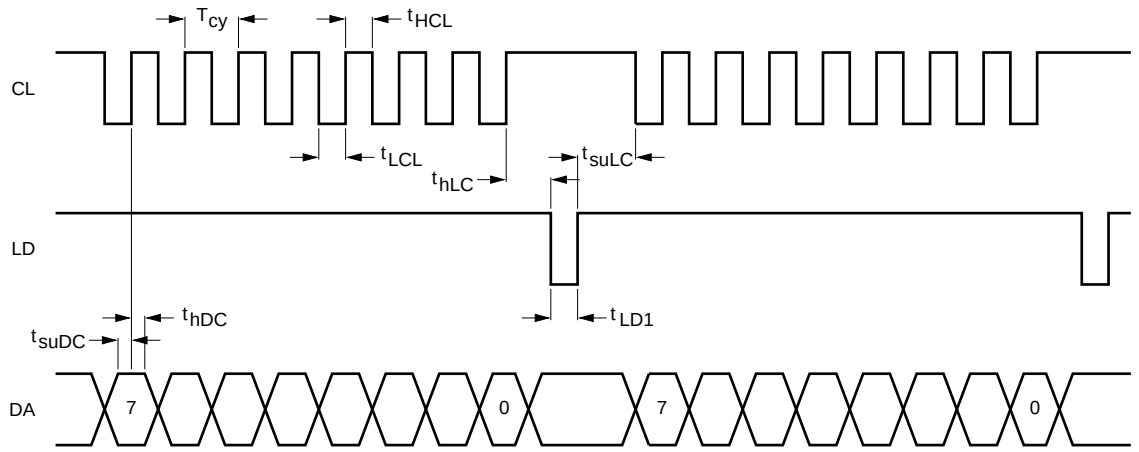
1. Write Address.
2. Read Data byte.
3. Read Data byte.
4. Read Data byte.
5. Etc.

Multi-read operations continue to cycle through the given Register Address Range until the read operation is completed.

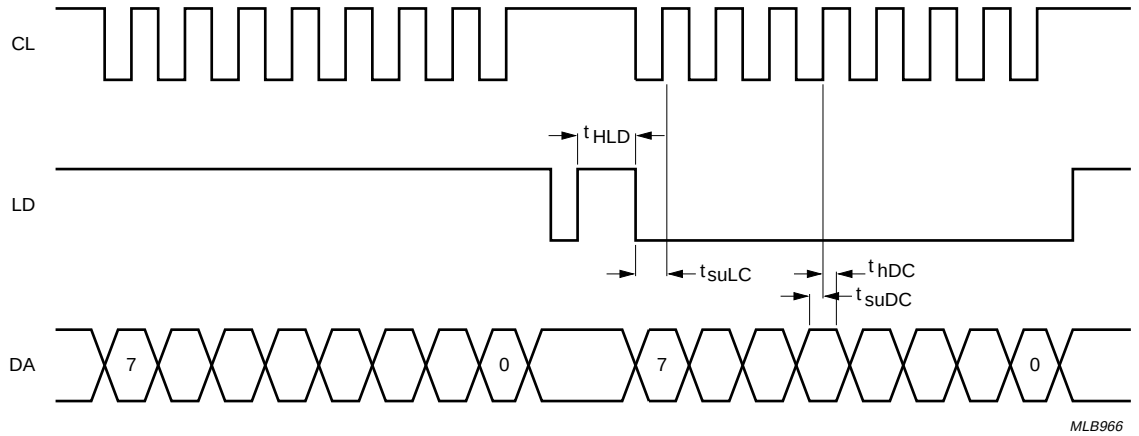
If pin SA is HIGH, the GDIN can operate without an external microcontroller. In this event, only the SRC mode and the AD/DA mode can be selected. A number of pins are reconfigured to control some of the internal switches of the device. For more information see Chapter “Pinning” and Section “Controlling the GDIN”.

Table 8 TDA1373H memory map

REGISTER ADDRESS RANGE	REGISTER NAME	TYPE
00H to 05H	CMD1 to CMD6	command; read/write
40H to 45H	STS1 to STS6	status; read
80H to 97H	RAM buffer; C-block	read
80H to AFH	RAM buffer; U-block	read
80H to 89H	RAM buffer; CD-Q frame	read



a.



b.

a. A complete write operation.
b. A complete read operation.

Fig.13 Timing for the microcontroller read and write operations.

Controlling the GDIN

MICROCONTROLLER OPERATED

Status registers

Table 9 Status registers

REGISTER	BIT	FLAG	DESCRIPTION	EXPLANATION
STS1 (40H) GDIN status information	7	–	reserved	–
	6	–	reserved	–
	5	–	reserved	–
	4	–	reserved	–
	3	LCK	internal ADIC lock status	0 = not locked; 1 = locked
	2	CRC	CD-Q channel; CRC check(1)	0 = OK; 1 = error
	1	VA	validity bit(2)	0 = valid; 1 = not valid
	0	BCV	RAM buffer contents	0 = valid; 1 = not valid
STS2 (41H) GDIN status information	7	–	reserved	–
	6	–	reserved	–
	5	–	reserved	–
	4	–	reserved	–
	3	–	reserved	–
	2 and 1	ST1 and ST0	PLL operating status(3)	00 = reserved; 01 = state 1; 10 = state 2; 11 = state 3
	0	MUT	mute status(4)	0 = mute OFF; 1 = mute ON
STS3 (42H)	7 to 0	LF15 to LF8	LF15 to LF0: input sample rate(5)	$f_{si} = f_{so} \times (1 - (0.75 \times LF15\ to\ LF0))$
STS4 (43H)	7 to 0	LF7 to LF0		
STS5 (44H)(6) AES/EBU channel status	7 and 6	CA1 and CA0	clock accuracy	00 = level 2; 01 = level 1; 10 = level 3; 11 = reserved
	5 and 4	FS1 and FS0	input sample rate	00 = 44.1 kHz; 01 = reserved; 10 = 48 kHz; 11 = 32 kHz
	3	EM	pre-emphasis	0 = OFF; 1 = ON
	2	CPY	copyright protection	0 = YES; 1 = NO
	1	AN	audio or data	0 = audio; 1 = data
	0	CPF	consumer or professional use	0 = consumer; 1 = professional
STS6 (45H)(6) AES/EBU channel status	7	CAT7	CAT7 to CAT0: category code	some examples: 00000000 = general 10000000 = CD 1100001L = DCC 1100000L = DAT 0100100L = mixer 0101100L = SRC 1001000L = MD
	6	CAT6		
	5	CAT5		
	4	CAT4		
	3	CAT3		
	2	CAT2		
	1	CAT1		
	0	CAT0(7)		

Notes

1. Only valid when the internal ADIC is in lock (bit 3 of register STS1; LCK = 1).

2. VA = IEC 958 V-bit or ADIC error detector.
3. Only valid when the digital PLL works in adaptive mode.
4. After approximately 512 stereo input samples (approximately 10 ms when f_{si} = 44.1 kHz).
5. Only valid in SRC mode. LF15 to LF0 are in two's complement notation.
6. Only valid when IEC 958 input format is consumer (bit 0 of register STS5; CPF = 0). When the input format is professional (CPF = 1) the STS5 and STS6 registers contain the first 16 bits of C-block.
7. Generation status (L-bit).

Command registers

Table 10 Command registers

REGISTER	BIT	FLAG	DESCRIPTION	EXPLANATION
CMD1 (00H) ADIC control	7 and 6	DI12 and DI11	ADIC input selector	00 = DI1S; 01 = DI1O; 10 = DI1D; 11 = reserved
	5	UIP	user interface protocol	0 = interrupt; 1 = user requirement
	4	SBF	set internal RAM buffer free	0 = hold buffer; 1 = set buffer free
	3 and 2	SM1 and SM0	channel decoding	00 = CD-Q; 01 = C-block; 10 = U-block; 11 = reserved
	1	LRS	C-block left/right selector	0 = left; 1 = right
	0	DBA	RAM buffer mode	0 = normal; 1 = test
CMD2 (01H) loop and mode control	7	–	reserved	–
	6	–	reserved	–
	5 and 4	LC1 and LC0	PLL control; note 1	00 = adaptive; 01 = state 1 fixed; 10 = state 2 fixed; 11 = state 3 fixed
	3 and 2	MS1 and MS0	mode selector; notes 1 and 2	00 = SRC mode; 01 = AD/DA mode; 10 = SLAVE-VCXO mode; 11 = SLAVE-VCO mode
	1	RTR	enable 3-state outputs; note 3	0 = 3-state; 1 = enabled
	0	MRS	reset (hardware reset); note 4	0 = no reset; 1 = reset
CMD3 (02H) data path[5]	7	DSO	DO1 output selector	0 = INS; 1 = ADIC
	6	–	reserved	–
	5	FOS	FO output selector	0 = ADIC; 1 = 128× filter
	4	DI2	FIFO input selector	0 = FOW, FOD and FOC; 1 = DI2W, DI2D and DI2C
	3	DNI	input selector 128× filter	0 = variable hold; 1 = AIL/AIR
	2	INS	In-band Noise Shaper input selector	0 = output 128× down; 1 = output FIFO/GAIN
	1	AOS	Bitstream digital filter input selector	0 = variable hold; 1 = DI2W, DI2D and DI2C
	0	DO2	DO2 output selector	0 = 128× down; 1 = 64× up

REGISTER	BIT	FLAG	DESCRIPTION	EXPLANATION
CMD4 (03H) control	7	–	reserved	–
	6	–	reserved	–
	5	MMU	soft mute function; note 7	0 = OFF; 1 = ON
	4 and 3	QU1 and QU0	in-band noise shaper	00 = 16-bit; 01 = 20-bit; 10 = 16-bit INS; 11 = 18-bit INS
	2	NSD	dither Bitstream digital filter; note 8	0 = OFF; 1 = ON
	1	DLO	symmetrical Bitstream output	0 = OFF; 1 = ON
	0	SSP	stop band suppression 64× filter; note 9	0 = 70 dB; 1 = 50 dB
CMD5 (04H) input/output formats	7 and 6	DI22 and DI21	serial format DI2 input	00 = I^2S; 01 = Japanese 16-bit; 10 = Japanese 18-bit; 11 = Japanese 20-bit
	5 and 4	DO22 and DO21	serial format DO2 output	00 = I^2S; 01 = Japanese 16-bit; 10 = Japanese 18-bit; 11 = reserved
	3 and 2	DO12 and DO11	serial format DO1 output	00 = I^2S; 01 = Japanese 16-bit; 10 = Japanese 18-bit; 11 = 3-stated
	1	DO1M	DO1 master/slave selector	0 = master; 1 = slave
	0	FOT	FO output 3-state selector	0 = I^2S; 1 = 3-stated
CMD6 (05H)	7	GAIN7	GAIN7 to GAIN0: gain of the GCM block[10]; maximum = 2; step = $1/128$	some examples: 11111111 = ×2 (maximum) 10000000 = ×1 01111111 = ×0.992 00000001 = ×0.0078
	6	GAIN6		
	5	GAIN5		
	4	GAIN4		
	3	GAIN3		
	2	GAIN2		
	1	GAIN1		
	0	GAIN0		

Notes

1. In the SLAVE-VCXO mode, the PLL should be fixed in state 2 until locked.
2. A mode change will always invoke a restart of the GDIN.
3. At power-on the DO1 and FO outputs are ‘3-state’ to avoid I^2S bus conflicts. This bit overrides the serial I/O control bits.
4. A MRS or hardware reset clears all command registers, also the MRS flag itself.
5. See Section “Data path switching” for possible settings of the data path switches in the different modes.
6. Set all reserved flags to 0.
7. Setting MMU starts a soft-mute from current gain value to 0 by $1/128$ per input sample. Clearing MMU starts the inverse process from 0 to current gain value.
8. To prevent idle patterns in the audio band, it is strongly advised to add out-of-band dither by setting control bit NSD.
9. Set this bit for 32 kHz input sources.
10. Use ‘01111111’ for normal operation to avoid pass band ripple clipping.

Data path switching

All data path switches are freely controllable, although not all combinations make sense in the different operating modes. Table 11 shows the preferred settings of the CMD3 control register.

Table 11 Preferred settings of the CMD3 control register

REGISTER	BIT	FLAG	DATA PATH SWITCH	SRC(1)	SLAVE(1)	AD/DA(1)
CMD3 (02H) data path	7	DSO	DO1 output selector; note 2	0	A	A
	6	–	reserved	–	–	–
	5	FOS	FO output selector; note 2	A	A	A
	4	DI2	FIFO input selector	A	A	A
	3	DNI	input selector 128× filter	0	1	1
	2	–	reserved	–	–	–
	1	AOS	AOL and AOR output selector	A	A	A
	0	DO2	DO2 output selector	0	A	A

Notes

1. Level 0 or 1 indicates to set the flag in this position. A = application dependent.
2. When the output of the internal ADIC is fed directly to DO1 or FO, the serial output format is I^2S, the word select jitters (by one $384f_{so}$ clock cycle) and the number of bit clocks per word select is not fixed.

STAND-ALONE CONTROL

When pin SA is HIGH, the GDIN operates under stand-alone control. Some basic settings can be controlled in this event by changing the level at the control pins. Table 12 shows which command bits are pin-controllable during stand-alone operation. The command bits which are not pin-controllable are automatically set to their appropriate value in accordance with the selected mode (SRC or AD/DA). All control bits not shown get the value 0 in the event of stand-alone control.

Table 12 Command registers

REGISTER	FLAG	PIN	DESCRIPTION	EXPLANATION
CMD1 (00H) ADIC control	DI11	FSL	ADIC input selector	0 = DI1S; 1 = DI1O
CMD2 (01H) loop and mode control	MS0	DI1D	mode selector; note 1	0 = SRC mode; 1 = AD/DA mode
	RTR	–	enable 3-state outputs; note 2	RTR is always 1 in stand-alone mode
CMD3 (02H) data path	DI2	DA	FIFO input selector	0 = FOW, FOD and FOC; 1 = DI2W, DI2D and DI2C
	DNI	–	input selector 128× filter	SRC mode = 0: variable hold; AD/DA mode = 1: AIL/AIR
CMD4 (03H) control	QU0/QU1	CL	in-band noise shaper	0 = 20 bit; 1 = 16 bit INS
	NSD	LD	dither Bitstream digital	0 = OFF; 1 = ON
CMD6 (05H)	GAIN	–	gain of the FIFO/GAIN block	gain = 01111111 = ×0.992

Notes

1. When the device operates in stand-alone control, only the SRC mode and AD/DA mode are available.
2. This means that all 3-state outputs are permanently enabled during stand-alone operation.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		–0.5	–	+6.5	V
I_{DD}	supply current		–	–	200	mA
V_i	input voltage		–0.5	–	V_{DD} + 0.5	V
$I_{i(max)}$	maximum input current		–	–	10	mA
$I_{o(max)}$	maximum output current		–	–	10	mA
P_{tot}	total power dissipation		–	1030	–	mW
T_{stg}	storage temperature		–65	–	+150	°C
T_{amb}	operating ambient temperature		0	–	+70	°C
V_{es}	electrostatic handling	HBM; note 1	–3000	–	+3000	V
		MM; note 2	–300	–	+300	V

Notes

1. Human Body Model (HBM): C = 100 pF; R = 1.5 kΩ; 3 zaps positive and 3 zaps negative.
2. Machine Model (MM): C = 200 pF; L = 2.5 μH; R = 25 Ω; 3 zaps positive and 3 zaps negative.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	46	K/W

CHARACTERISTICS

V_{DD} = 5 V ±10%; T_{amb} = 0 to +70 °C; C_L = 50 pF; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		–0.5	–	6.5	V
I_{DDD}	digital supply current		–	148	180	mA
I_{DDA1}	analog supply current IEC 958 data slicer		–	0.65	1	mA
I_{DDA4}	analog supply current clock oscillator		–	4	6	mA
P_{tot}	total power dissipation	f_{so} = 44.1 kHz	–	775	–	mW
$I_{q(tot)}$	total quiescent supply current	T_{amb} = 25 °C; note 2	–	–	10	µA
DC characteristics						
INPUT PINS TYPE HPP01 (AIL, AIR, CLI, TST2, TST1, SA, LD, CL, DI2D, DI1D AND DI1O)						
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
$\|I_{IL}\|$	input leakage current		–	–	1.0	µA
INPUT PIN TYPE HPP07 (SCHMITT-TRIGGER; $\overline{RST}$)						
V_{IL}	LOW level input voltage		–	–	$0.2V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.8V_{DD}$	–	–	V
V_{hys}	hysteresis voltage		–	$0.33V_{DD}$	–	V
$\|I_{IL}\|$	input leakage current		–	–	1.0	µA
INPUT PIN DI1S (IEC 958 INPUT)						
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
I_i	input current		–	–	1.9	mA
OUTPUT PINS TYPE OPF40 (DO2C, AOL1, DO2D, AOR1, DO2W, CLO1, CLO2, CLO3, CLO4, BS, CEN, CUS, MU AND LOCK; 4 mA OUTPUTS)						
V_{OL}	LOW level output voltage		–	–	0.5	V
V_{OH}	HIGH level output voltage		V_{DD} – 0.5	–	–	V
OUTPUT PIN TYPE OPF20 (EM; 2 mA OUTPUT)						
V_{OL}	LOW level output voltage		–	–	0.5	V
V_{OH}	HIGH level output voltage		V_{DD} – 0.5	–	–	V
OUTPUT PINS TYPE OPF43 (CLD, DO1D, FOW, FOD AND FOC; 4 mA 3-STATE OUTPUTS)						
V_{OL}	LOW level output voltage		–	–	0.5	V
V_{OH}	HIGH level output voltage		V_{DD} – 0.5	–	–	V
I_{OZ}	3-state leakage current		–	–	5.0	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
INPUT/OUTPUT PINS TYPE HOF21 (FSL, DI2W AND DI2C; 2 mA OUTPUTS)						
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
$\|I_{OZ}\|$	3-state leakage current		–	–	5.0	μA
V_{OL}	LOW level output voltage		–	–	0.5	V
V_{OH}	HIGH level output voltage		$V_{DD} - 0.5$	–	–	V
INPUT/OUTPUT PINS TYPE HOF41 (DA, DO1W AND DO1C; 4 mA OUTPUTS)						
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
$\|I_{OZ}\|$	3-state leakage current		–	–	5.0	μA
V_{OL}	LOW level output voltage		–	–	0.5	V
V_{OH}	HIGH level output voltage		$V_{DD} - 0.5$	–	–	V
Characteristics per block and pin; note 1						
INPUT PINS TYPE HPP01 AND HPP07						
C_i	input capacitance		–	10	–	pF
t_r	rise time (unless otherwise specified)		–	–	T_{cy}	ns
t_f	fall time (unless otherwise specified)		–	–	T_{cy}	ns
OUTPUT PINS TYPE OPF40 AND OPF43						
t_r	rise time (unless otherwise specified)		–	5	10	ns
t_f	fall time (unless otherwise specified)		–	5	10	ns
CRYSTAL OSCILLATOR						
g_m	mutual conductance		0.007821	–	0.03913	mA/V
Z_O	output impedance		405	–	3200	Ω
$\|I_{IL}\|$	input leakage current		–	–	1.0	μA
C_I	input capacitance		–	3.1	–	pF
C_O	output capacitance		–	–	18	pF
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
IEC 958 INTERFACE (FOR TIMING SEE SECTION 13 OF REFERENCE 1 IN CHAPTER “References”)						
$V_{i(p-p)}$	AC input voltage (peak-to-peak value)		0.2	–	V_{DD}	V
C_i	input capacitance		–	25	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SERIAL INPUT INTERFACES (see Fig.7)						
t_r	rise time (unless otherwise specified)		–	–	25	ns
t_f	fall time (unless otherwise specified)		–	–	25	ns
t_{suDAT}	set-up time data (D) to clock (C)		T_{cy}	–	–	ns
t_{hDAT}	hold time data (D) to clock (C)		0	–	–	ns
t_{suWS}	set-up time word select (W) to clock (C)		T_{cy}	–	–	ns
t_{hWS}	hold time word select (W) to clock (C)		0	–	–	ns
T_{BCK}	clock period time	see Table 3	–	$1/f_{BCK}$	–	ns
t_{HB}	bit clock HIGH time		T_{cy}	–	–	ns
t_{LB}	bit clock LOW time		T_{cy}	–	–	ns
SERIAL OUTPUT INTERFACES						
t_r	rise time (unless otherwise specified)		–	–	10	ns
t_f	fall time (unless otherwise specified)		–	–	10	ns
t_{suDAT}	set-up time data (D) to clock (C)		$0.5t_{BCK}$	–	–	ns
t_{hDAT}	hold time data (D) to clock (C)		T_{cy}	–	–	ns
t_{suWS}	set-up time word select (W) to clock (C)		$0.5t_{BCK}$	–	–	ns
t_{hWS}	hold time word select (W) to clock (C)		T_{cy}	–	–	ns
T_{BCK}	clock period time	see Table 3	–	$1/f_{BCK}$	–	ns
t_{HB}	bit clock HIGH time		$0.4t_{BCK}$	–	–	ns
t_{LB}	bit clock LOW time		$0.4t_{BCK}$	–	–	ns
BITSTREAM INPUTS AIL AND AIR (see Fig.8)						
t_{d1}	delay time after HIGH-to-LOW clock transition		–	–	100	ns
BITSTREAM OUTPUTS AOL1, AOR1 AND CLD (see Fig.8)						
t_r	data output rise time		–	10	15	ns
t_f	data output fall time		–	10	15	ns
t_{su}	data output set-up time		0	–	–	ns
t_h	data output hold time		25	–	–	ns
t_r	clock output rise time		–	5	10	ns
t_f	clock output fall time		–	5	10	ns
t_{CH}	clock output HIGH time		40	–	–	ns
t_{CL}	clock output LOW time		40	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MICROCONTROLLER INTERFACE (see Fig.13)						
T_{cyCL}	CL cycle time		$6T_{cy}$	–	–	ns
t_{HCL}	CL HIGH time		$3T_{cy}$	–	–	ns
t_{LCL}	CL LOW time		$3T_{cy}$	–	–	ns
t_{suLC}	set-up time LD to CL	write operation	$9T_{cy}$	–	–	ns
t_{hLC}	hold time LD to CL	write operation	$3T_{cy}$	–	–	ns
t_{LD1}	write pulse period LD		$3T_{cy}$	–	–	ns
T_{cyLD}	LD cycle time	read operation	$3T_{cy}$	–	–	ns
t_{hLC}	hold time LD to CL	read operation	$3T_{cy}$	–	–	ns
t_{LD2}	read enable LD pulse period		$6T_{cy}$	–	–	ns
t_{suDC}	set-up time DA to CL	write operation	T_{cy}	–	–	ns
t_{hDC}	hold time DA to CL	write operation	$3T_{cy}$	–	–	ns
t_{suDC}	set-up time DA to CL	read operation	T_{cy}	–	–	ns
t_{hDC}	hold time DA to CL	read operation	$3T_{cy}$	–	–	ns
OUTPUT PINS CUS, CEN AND BS (see Fig.11)						
Channel status or channel mode						
T_{cyBS}	BS cycle time		–	$192 \times \frac{1}{f_{si}}$	–	ms
t_{CEN}	CEN enable time		–	$\frac{1}{2}f_{si}$	–	µs
t_{LCEN}	CEN LOW time		1.5	–	–	µs
t_{suBC}	set-up time BS to CEN		1.5	–	–	µs
t_{hBC}	hold time BS to CEN		8	–	–	µs
t_{suCC}	set-up time CUS to CEN		1.5	–	–	µs
t_{hCC}	hold time CUS to CEN		8	–	–	µs
CD-Q subcode demodulation mode						
$T_{cyBS(CD)}$	frame sync BS cycle time		–	13.3	–	ms
$t_{HBS(CD)}$	frame sync BS HIGH time		–	408	–	µs
t_{CEN}	CEN enable time		–	136	–	µs
$t_{HCEN(CD)}$	CEN enable HIGH time		–	$\frac{1}{2}f_{si}$	–	ms
$t_{suBSCEN}$	set-up time BS to CEN		8	–	–	µs
$t_{suCC(CD)}$	set-up time CUS to CEN		1.5	–	–	µs
$t_{hCC(CD)}$	hold time CUS to CEN		8	–	–	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RESET						
t_{PWRES}	reset pulse width		$10T_{cy}$	–	–	ns
t_{iRES}	internal reset time after reset pulse		–	–	$40T_{cy}$	ns

Notes

1. Most timing specifications are referenced to the system clock $T_{cy} = {}^{1}\!/_{384}f_{so}$.
2. The (I_{DD}) quiescent current is checked on as much active gate area as possible, therefore outputs are chosen reference. Each output is I_{DD} tested in HIGH and LOW state. The minimum number of test vectors on which I_{DD} quiescent current is tested is 2 and the maximum is N + 1 (N = number of outputs). These test vectors also define fixed conditions in the core. I_{DD} quiescent current test is not allowed on test vectors which may result in additional quiescent current caused by pull-up/down resistors, I/Os, internal bus-structures, etc. In total this I_{DD} quiescent current test contributes highly to the (functional) fault coverage.

QUALITY SPECIFICATION

- General quality in accordance with *"SNW-FQ-611 part E"* and can be found in the *"Quality Reference Handbook"* (order number 9398 510 63011).

REFERENCES

1. *"Digital audio interface"*, first edition 1989-03 International standard *"IEC 958"*.
2. *"I^2S bus specification"*, release 2-86, Philips Export B.V. (order number 9398 332 10011).

TEST DIAGRAM

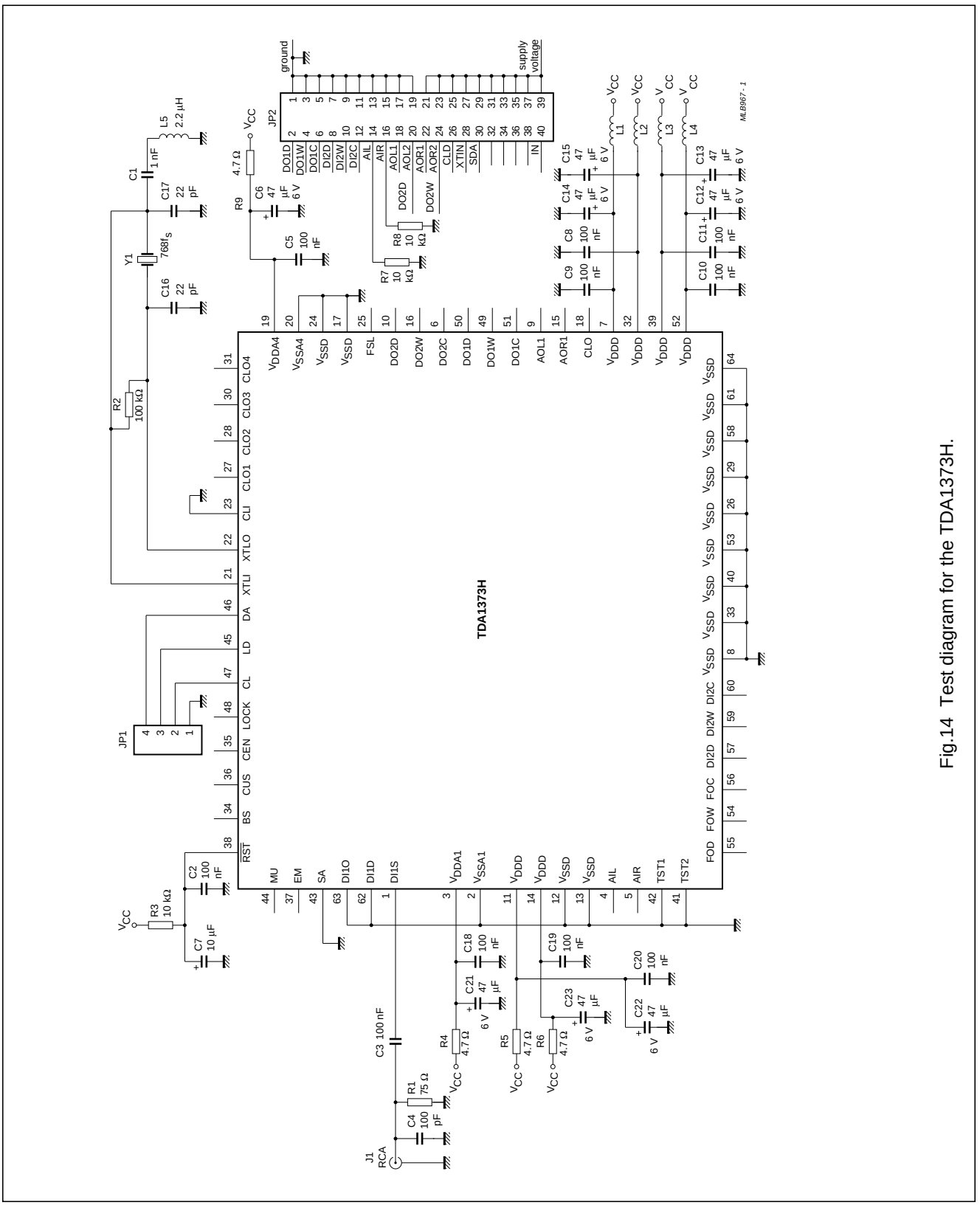
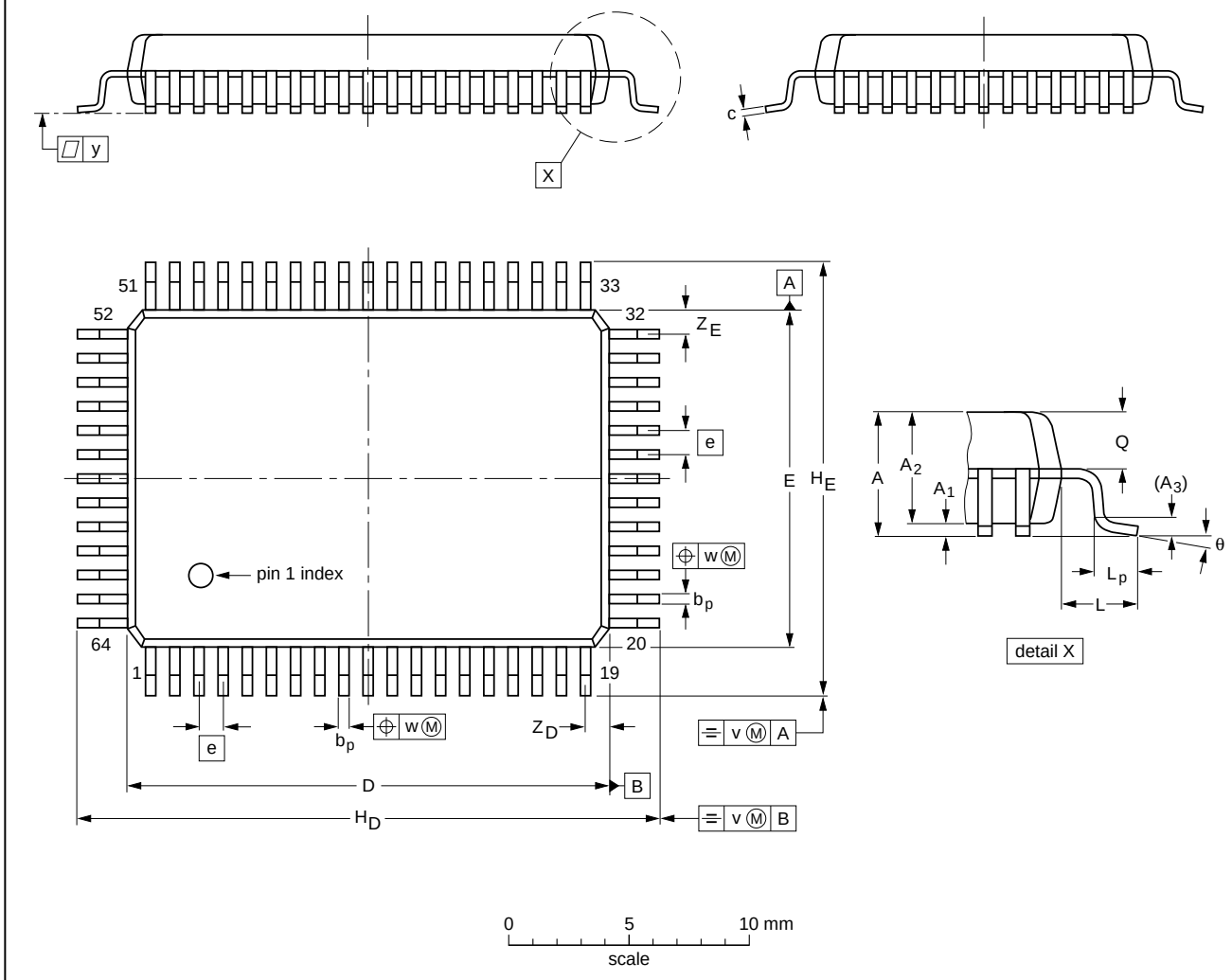


Fig.14 Test diagram for the TDA1373H.

PACKAGE OUTLINE

QFP64: plastic quad flat package;
64 leads (lead length 1.95 mm); body 14 x 20 x 2.7 mm; high stand-off height **SOT319-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.3	0.36 0.10	2.87 2.57	0.25	0.50 0.35	0.25 0.13	20.1 19.9	14.1 13.9	1	24.2 23.6	18.2 17.6	1.95	1.0 0.6	1.43 1.23	0.2	0.2	0.1	1.2 0.8	1.2 0.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT319-1						~~92-11-17~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9398 510 63011).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
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Where application information is given, it is advisory and does not form part of the specification.	

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