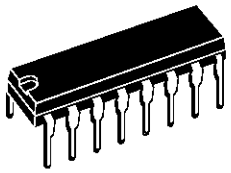
SGS-THOMSON MICROELECTRONICS

STV9420
STV9421

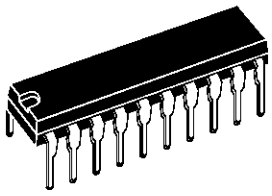
MULTISYNC ON-SCREEN DISPLAY FOR MONITOR

- CMOS SINGLE CHIP OSD FOR MONITOR
- BUILT IN 1 KBYTE RAM HOLDING :
  - PAGES' DESCRIPTORS
  - CHARACTER CODES
  - USER DEFINABLE CHARACTERS
- 128 ALPHANUMERIC CHARACTERS OR GRAPHIC SYMBOLS IN INTERNAL ROM (12 x 18 DOT MATRIX)
- UP TO 26 USER DEFINABLE CHARACTERS
- INTERNAL HORIZONTAL PLL (15 TO 120kHz)
- PROGRAMMABLE VERTICAL HEIGHT OF CHARACTER WITH A SLICE INTERPOLATOR TO MEET MULTI-SYNCH REQUIREMENTS
- PROGRAMMABLE VERTICAL AND HORIZONTAL POSITIONING
- FLEXIBLE SCREEN DESCRIPTION
- CHARACTER BY CHARACTER COLOR SELECTION (UP TO 8 DIFFERENT COLORS)
- PROGRAMMABLE BACKGROUND (COLOR, TRANSPARENT OR WITH SHADOWING)
- CHARACTER BLINKING
- 2-WIRES ASYNCHRONOUS SERIAL MCU INTERFACE (I^2C PROTOCOL)
- 4 x 8 BITS PWM DAC OUTPUTS ON THE STV9421
- SINGLE POSITIVE 5V SUPPLY



DIP16
(Plastic Package)

ORDER CODE : STV9420



DIP20
(Plastic Package)

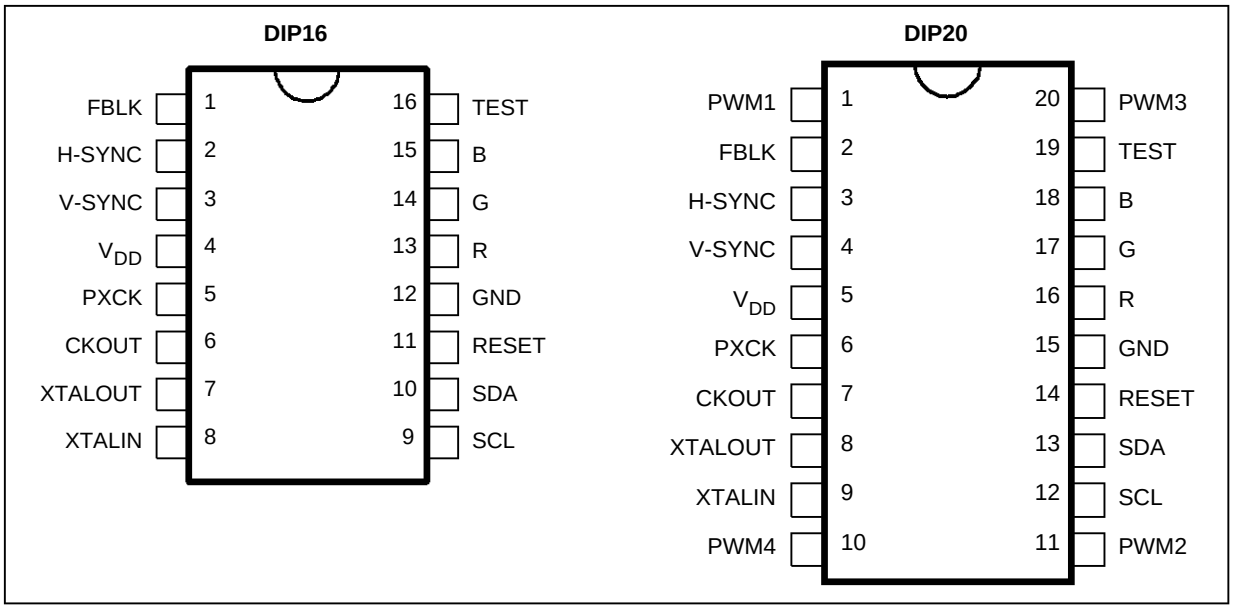
ORDER CODE : STV9421

DESCRIPTION

The STV9420/21 is an ON SCREEN DISPLAY for monitor. It is built as a slave peripheral connected to a host MCU via a serial I^2C bus. It includes a display memory, controls all the display attributes and generates pixels from the data read in its on chip memory. The line PLL and a special slice interpolator allow to have a display aspect which does not depend on the line and frame frequencies. I^2C interface allows MCU to make transparent internal access to prepare the next pages during the display of the current page. Toggle from one page to another by programming only one register.

4 x 8 bits PWM DAC are available (STV9421) to provide DC voltage control to other peripherals. The STV9420/21 provides the user an easy to use and cost effective solution to display alphanumeric or graphic information on monitor screen.

PIN CONNECTIONS



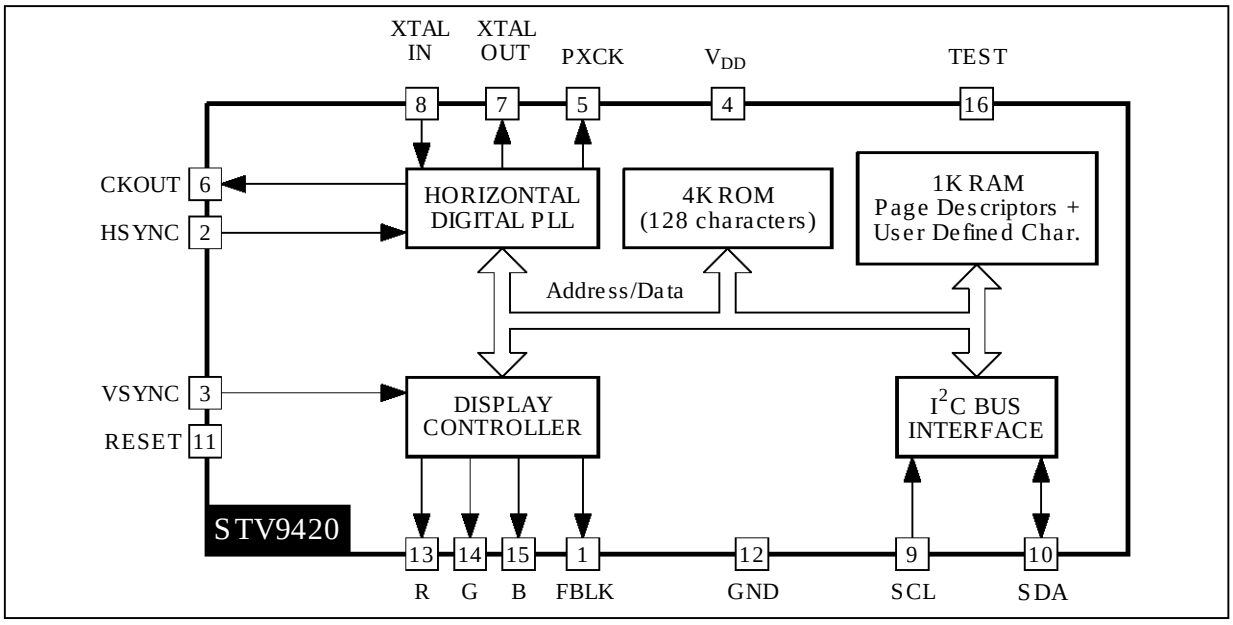
PIN DESCRIPTION

Symbol	Pin Number		I/O	Description
	DIP16	DIP20		
PWM1		1	O	DAC1 Output
FBLK	1	2	O	Fast Blanking Output
H-SYNC	2	3	I	Horizontal Sync Input
V-SYNC	3	4	I	Vertical Sync Input
V_{DD}	4	5	S	+5V Supply
PXCK	5	6	O	Pixel Frequency Output
CKOUT	6	7	O	Clock Output
XTALOUT	7	8	O	Crystal Output
XTALIN	8	9	I	Crystal or Clock Input
PWM4		10	O	DAC4 Output
PWM2		11	O	DAC2 Output
SCL	9	12	I	Serial Clock
SDA	10	13	I/O	Serial Input/output Data
RESET	11	14	I	Reset Input
GND	12	15	S	Ground
R	13	16	O	Red Output
G	14	17	O	Green Output
B	15	18	O	Blue Output
TEST	16	19	I	Reserved (grounded in Normal Operation)
PWM3		20	O	DAC3 Output

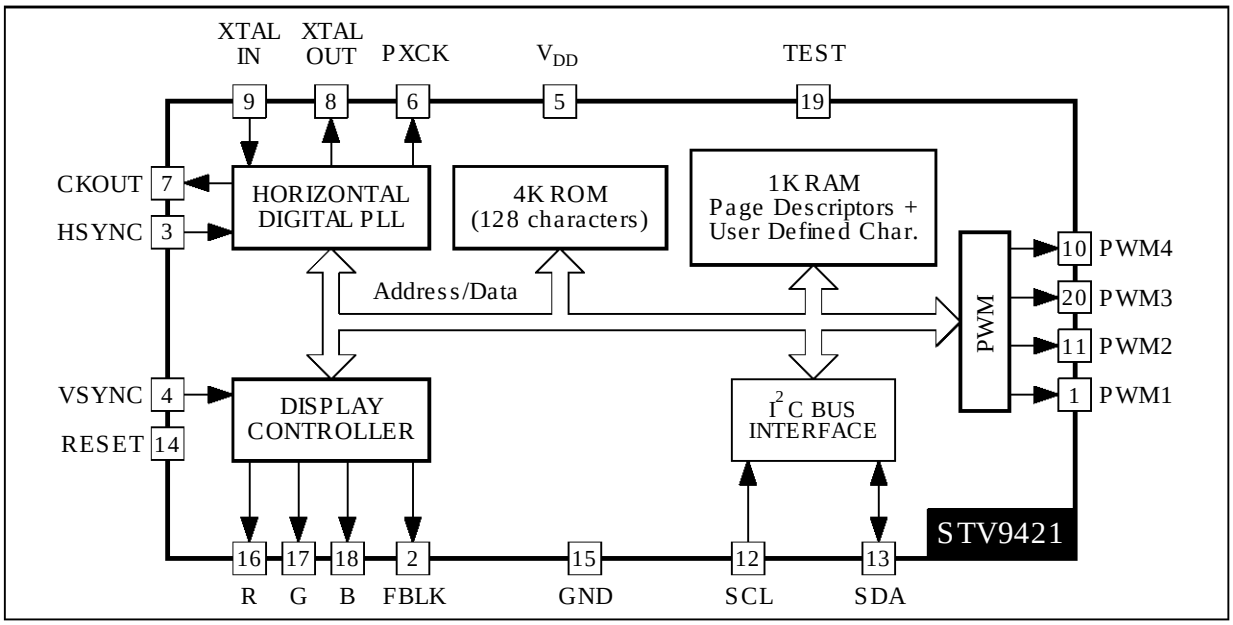
9420-01.TBL

BLOCK DIAGRAMS

STV9420



STV9421



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3, +7.0	V
V_{IN}	Input Voltage	-0.3, +7.0	V
T_{oper}	Operating Ambient Temperature	0, +70	°C
T_{stg}	Storage Temperature	-40, +125	°C

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ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V, V_{SS} = 0V, T_A = 0 to 70°C, F_{XTAL} = 8 to 15MHz, TEST = 0 V, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SUPPLY					
V_{DD}	Supply Voltage	4.75	5	5.25	V
I_{DD}	Supply Current	-	-	50	mA
INPUTS					
SCL, SDA, TEST, RESET, V-SYNC and H-SYNC					
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage	0.8 V_{DD}			V
I_{IL}	Input Leakage Current	-20		+20	µA
OUTPUTS					
R, G, B, FBLK, SDA, CKOUT, PXCK and PWMi (i = 1 to 4)					
V_{OL}	Output Low Voltage (I_{OL} = 1.6mA)	0		0.4	V
V_{OH}	Output High Voltage (I_{OL} = -0.1mA)	0.8 V_{DD}		V_{DD}	V

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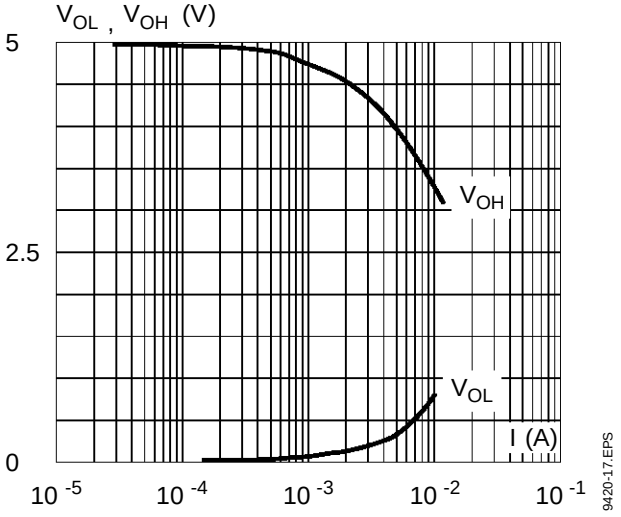
For R, G, B and FBLK outputs, see Figure 1.

Figure 1 : Typical R, G, B Outputs Characteristics



TIMINGS

Symbol	Parameter	Min.	Typ.	Max.	Unit
OSCILATOR INPUT : XTI (see Figure 2)					
t_{WH}	Clock High Level	35			ns
t_{WL}	Clock Low Level	35			ns
f_{XTAL}	Clock Frequency	6		15	MHz
f_{PXL}	Pixel Frequency			30	MHz
RESET					
t_{RES}	Reset High Level Pulse	4			µs
R, G, B, FBLK (C_{LOAD} = 30pF)					
t_R	Rise Time (Note 1)		5		ns
t_F	Fall Time (Note 1)		5		ns
t_{SKEW}	Skew between R, G, B, FBLK (Note 1)		5		ns
I^2C INTERFACE : SDA AND SCL (see Figure 3)					
f_{SCL}	SCL Clock Frequency	0		1	MHz
t_{BUF}	Time the bus must be free between 2 access	500			ns
t_{HDS}	Hold Time for Start Condition	500			ns
t_{SUP}	Set up Time for Stop Condition	500			ns
t_{LOW}	The Low Period of Clock	400			ns
t_{HIGH}	The High Period of Clock	400			ns
t_{HDAT}	Hold Time Data	0			ns
t_{SUDAT}	Set up Time Data	375			ns
t_F	Fall Time of SDA			20	ns
t_R	Rise Time of Both SCL and SDA	Depend on the pull-up resistor and the load capacitance			

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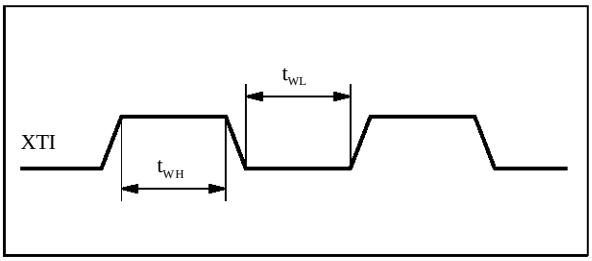
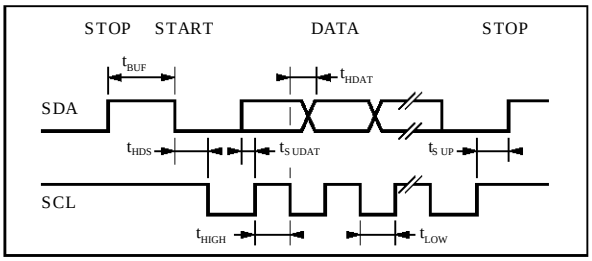
Note 1 : These parameters are not tested on each unit. They are measured during our internal qualification procedure which includes characterization on batches comming from corners of our processes and also temperature characterization.

Figure 2



9420-03.EPS

Figure 3



9420-04.EPS

FUNCTIONAL DESCRIPTION

The STV9420/21 display processor operation is controlled by a host MCU via the I^2C interface. It is fully programmable through 8 internal read/write registers (12 for STV9421) and performs all the display functions by generating pixels from data stored in its internal memory. After the page downloading from the MCU, the STV9420/21 refreshes screen by its built in processor, without any MCU control (access).In addition, the host MCU has a direct access to the on chip 1Kbytes RAM during the display of the current page to make any update of its contents.

With the STV9420/21, a page displayed on the screen is made of several strips which can be of 2 types : spacing or character and which are described by a table of descriptors and character codes in RAM. Several pages can be downloaded at the same time in the RAM and the choice of the current display page is made by programming the CONTROL register.

I - Serial Interface

The 2-wires serial interface is an I^2C interface. To be connected to the I^2C bus, a device must own its slave address ; the slave address of the STV9420/21 is BA (in hexadecimal).

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	1	1	1	0	1	

I.1 - Data Transfer in Write Mode

The host MCU can write data into the STV9420/21 registers or RAM.

To write data into the STV9420/21, after a start, the MCU must send (Figure 3) :

- First, the I^2C address slave byte with a low level for the R/W bit,
- The two bytes of the internal address where the MCU wants to write data(s),
- The successive bytes of data(s).

All bytes are sent MS bit first and the write data transfer is closed by a stop.

I.2 - Data Transfer in Read Mode

The host MCU can read data from the STV9420/21 registers, RAM or ROM.

To read data from the STV9420/21 (Figure 4), the MCU must send 2 different I^2C sequences.
The first one is made of I^2C slave address byte with R/W bit at low level and the 2 internal address bytes.

The second one is made of I^2C slave address byte with R/W bit at high level and all the successive data bytes read at successive addresses starting from the initial address given by the first sequence.

Figure 3 : STV9420/I^2C Write Operation

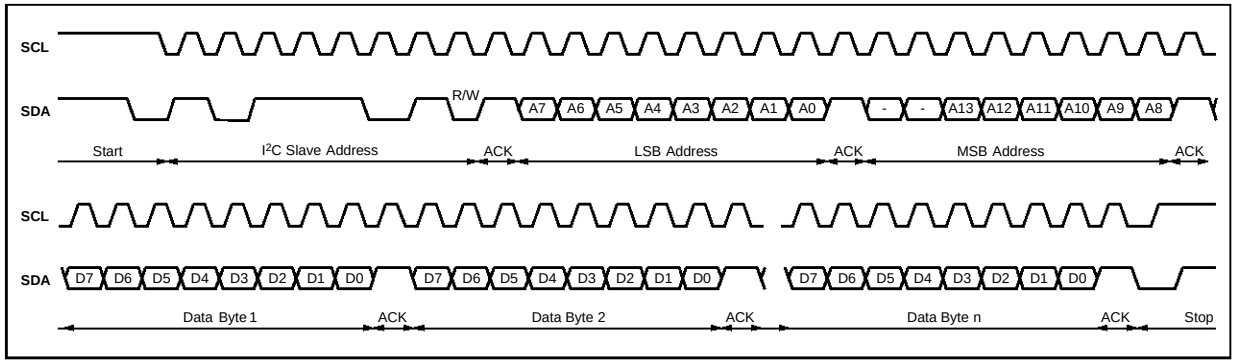
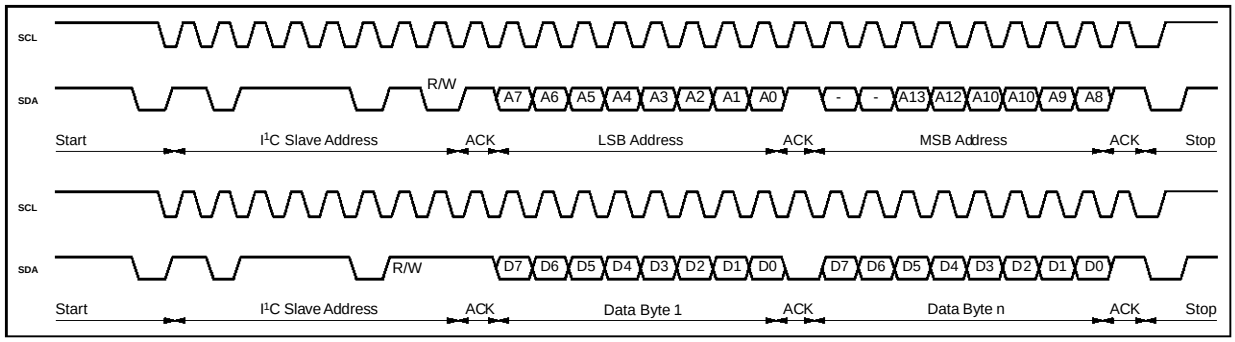


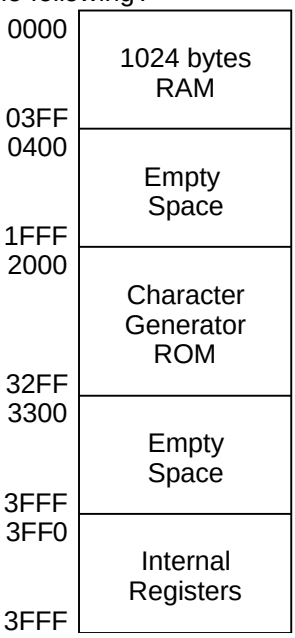
Figure 4 : STV9420/I^2C Read Operation



FUNCTIONAL DESCRIPTION (continued)

I.3 - Addressing Space

STV9420/21 registers, RAM and ROM are mapped in a 16Kbytes addressing space. The mapping is the following :



I.4 - Register Set

LINE DURATION

3FF0	-	-	LD5	LD4	LD3	LD2	LD1	LD0
*	-	-	1	1	1	1	1	1

LD[5:0] : LINE DURATION (number of character period, 1LSB = 12 pixel periods).

HORIZONTAL DELAY

3FF1	DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0
*	0	0	0	0	1	0	0	0

DD[7:0] : HORIZONTAL DISPLAY DELAY from the H-SYNC reference falling edge to the 1st pixel position of the character strips.
Unit = 3 pixel periods.

CHARACTERS HEIGHT

3FF2	-	-	CH5	CH4	CH3	CH2	CH1	CH0
*	-	-	0	1	0	0	1	0

CH[5:0] : HEIGHT of the character strips in scan lines. For each scan line, the number of the slice which is displayed is given by :

$$\text{SLICE-NUMBER} = \text{round}\left(\frac{\text{SCAN-LINE-NUMBER} \times 18}{\text{CH[5:0]}}\right)$$

SCAN-LINE-NUMBER = Number of the current scan line of the strip.

DISPLAY CONTROL

3FF3	OSD	FBK	FL1	FL0	-	P8	P7	P6
*	0	0	0	0	-	0	0	0

OSD : ON/OFF (if 0, R, G, B and FBLK are 0).

FBK : Fast blanking control :
= 1 : FBLK = 1, forcing black where these is no display,
= 0 : FBLK is active only during character display.

FL[1:0] : Flashing mode :
- 00 : No flashing. The character attribute is ignored,
- 01 : 1/1 flashing (a duty cycle = 50%),
- 10 : 1/3 flashing,
- 11 : 3/1 flashing.

P[8:6] : Address of the 1st descriptor of the current displayed pages.
P[13:9] and P[5:0] = 0 ; up to 8 different pages can be stored in the RAM.

LOCKING CONDITION TIME CONSTANT

3FF4	FR	AS2	AS1	AS0	-	BS2	BS1	BS0
*	0	0	1	0	-	0	1	0

FR : Free Running ; if = 1 PLL is disabled and the pixel frequency keeps its last value.

AS[2:0] : Phase constant during locking conditions.

BS[2:0] : Frequency constant during locking conditions.

CAPTURE PROCESS TIME CONSTANT

3FF5	-	AF2	AF1	AF0	-	BF2	BF1	BF0
*	-	0	1	1	-	0	1	1

AF[2:0] : Phase constant during the capture process.

BF[2:0] : Frequency constant during the capture process.

INITIAL PIXEL PERIOD

3FF6	PP7	PP6	PP5	PP4	PP3	PP2	PP1	PP0
*	0	0	1	0	1	0	0	0

PP[7:0] : Value to initialize the pixel period of the PLL.

FREQUENCY MULTIPLIER

3FF7	-	-	-	-	FM3	FM2	FM1	FM0
*	-	-	-	-	1	0	1	0

FM[3:0] : Frequency multiplier of the crystal frequency to reach the high frequency used by the PLL to derive the pixel frequency.

FUNCTIONAL DESCRIPTION (continued)

The last fourth registers described below are only available with the STV9421 :

PULSE WIDTH MODULATOR 1

3FF8	V17	V16	V15	V14	V13	V12	V11	V10
*	0	0	0	0	0	0	0	0

V1[7:0] : Digital value of the 1st PWM D to A converter (Pin1).

PULSE WIDTH MODULATOR 2

3FF9	V27	V26	V25	V24	V23	V22	V21	V20
*	0	0	0	0	0	0	0	0

V2[7:0] : Digital value of the 2d PWM DAC (Pin11).

PULSE WIDTH MODULATOR 3

3FFA	V37	V36	V35	V34	V33	V32	V31	V30
*	0	0	0	0	0	0	0	0

V3[7:0] : Digital value of the 3rd PWM DAC (Pin20).

PULSE WIDTH MODULATOR 4

3FFB	V47	V46	V45	V44	V43	V42	V41	V40
*	0	0	0	0	0	0	0	0

V4[7:0] : Digital value of the 4th PWM DAC (Pin10).

Note : * is power on reset value.

II - Descriptors

SPACING

MSB	0	-	-	-	-	-	-	-
LSB	SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0

SL[7:0] : The number of the scan lines of the spacing strip (1 to 255).

CHARACTER

MSB	1	DE	-	ZY	-	-	C9	C8
LSB	C7	C6	C5	C4	C3	C2	C1	0

C[9:0] : The address of the first character code of the strip (even).

DE : Display enable :
- DE = 0, R = G = B = 0 and FBLK = FBK (display control register) on whole strip,
- DE = 1, display of the characters.

ZY : Zoom, ZY = 1 all the scan lines are repeated once.

III - Code Format

MSB	SET	CHARACTER NUMBER						
LSB	BK3	BK2	BK1	BK0	FL	RF	GF	BF

FL : Flashing attribute (the flashing mode is defined in the DISPLAY CONTROL register).

SET : The set CHARACTER NUMBER
- If SET = 0 : ROM character,
- If SET = 1 :
  - If CHARACTER NUMBER is 0 to 25, a user redefinable character (UDC) located in RAM at the address equal to : 38 x CHARACTER NUMBER,
  - If CHARACTER NUMBER is 26 to 63, space character,
  - If CHARACTER NUMBER >63, end of line.

RF, GF, BF : Foreground color.

BK[3:0] : Background :
- If BK3 = 0, BK[2:0] = background color R, G and B,
- If BK3 = 1, shadowing :
  - BK2 : vertival shadowing,
  - BK1 : horizontal shadowing.

(if BK2 = BK1 = 0, the background is transparent).

IV - Clock and Timing

The whole timing is derived from the XTALIN and the SYNCHRO (horizontal and vertival) input frequencies. The XTALIN input frequency can be an external clock or a crystal signal thanks to XTALIN/XTALOUT pins. The value of this frequency can be chosen between 8 and 15MHz, it is available on the CKOUT pin and is used by the PLL to generate a pixel clock locked on the horizontal synchro input signal.

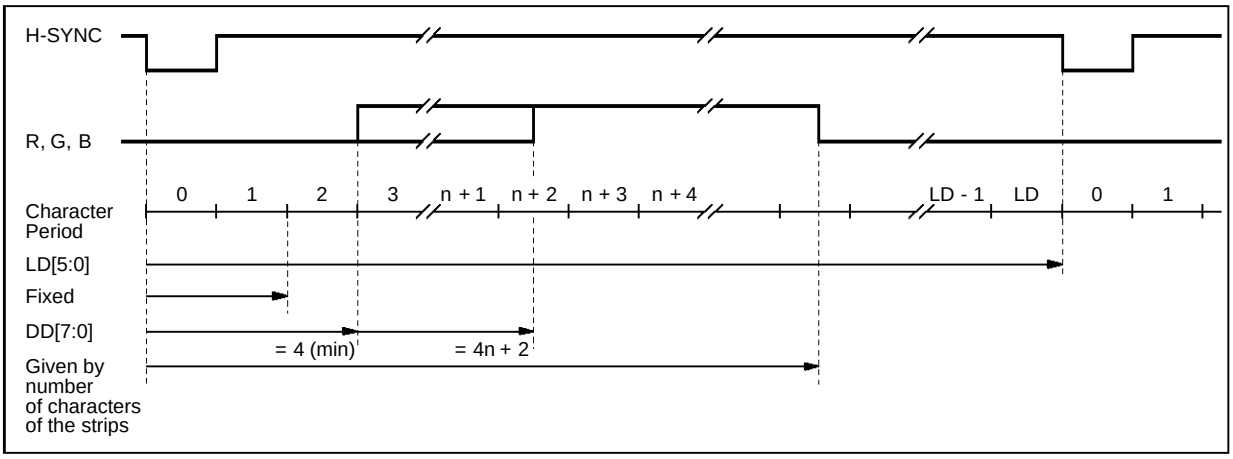
IV.1 - Horizontal Timing

The number of pixel periods is given by the LINE DURATION register and is equal to :
[LD[5:0] + 1] x 12
(LD[5:0] : value of the LINE DURATION register).
This value allows to choose the horizontal size of the characters.

The horizontal left margin is given by the HORIZONTAL DELAY register and is equal to :
[DD[7:0] + 8] x 3 x t_{PXCK}
(DD[7:0] : value of the DISPLAY DELAY register and T_{PXCK} : pixel period).
This value allows to choose the horizontal position of the characters on the screen. The value of DD[7:0] must be equal or greater than 4 (the minimum value of the horizontal delay is 36 x t_{PXCK} = 3 character periods). The length of the active area, where R, G, B are different from 0, depends on the number of characters of the strips.

FUNCTIONAL DESCRIPTION (continued)

Figure 5 : Horizontal Timing



IV.2 - D to A Timing (STV9421)

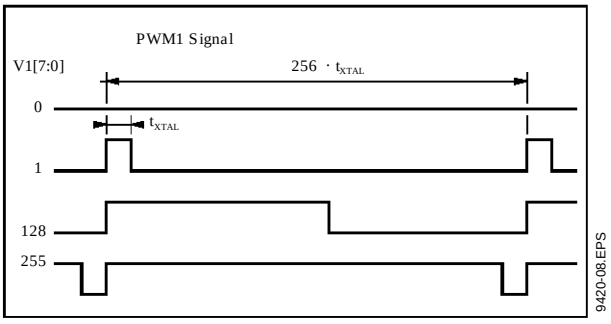
The D to A converters of the STV9421 are pulse width modulater converter.

The frequency of the output signal is : $\frac{F_{XTAL}}{256}$

and the duty cycle is : $\frac{V1[7:0]}{256}$ per cent.

After a low pass filter, the average value of the output is : $\frac{V1\,[7:0]}{256} \cdot V_{DD}$

Figure 6 : PWM Timing



V - Display Control

A screen is composed of successive scanlines gathered in several strips. Each strip is defined by a descriptor stored in memory. A table of descriptors allows screen composition and different tables can be stored in memory at the page addresses (8 possible ≠ addresses).

Two types of strips are available :

- Spacing strip : its descriptor (see II) gives the number of black (FBK = 1 in DISPLAY CONTROL register) or transparent (FBK = 0) lines.
- Character strip : its descriptor gives the memory address of the character codes corresponding to the 1st displayed character. The characters and attributes (see code format III) are defined by a succession of codes stored in the RAM at addresses starting from the 1st one given by the descriptor. A character strip can be displayed or not by using the DE bit of its descriptor. A zoom can be made on it by using the ZY bit.

After the falling edge on V-SYNC, the first strip descriptor is read at the top of the current table of descriptors at the address given by P[8:6] (see DISPLAY CONTROL register) ; if it is a spacing strip, SL[7:0] black or transparent scan lines are displayed ; if it is a character strip, during CH[5:0] x (I + ZY) scan lines (CH[5:0] given by the CHARACTER HEIGHT register), the character codes are read at the addresses starting from the 1st one given by the descriptor until a end of line character or the end of the scan line ; the next descriptor is then read and the same process is repeated until the next falling edge on V-SYNC.

FUNCTIONAL DESCRIPTION (continued)

Figure 7 : Relation between Screen/Address Page/Character Code in RAM

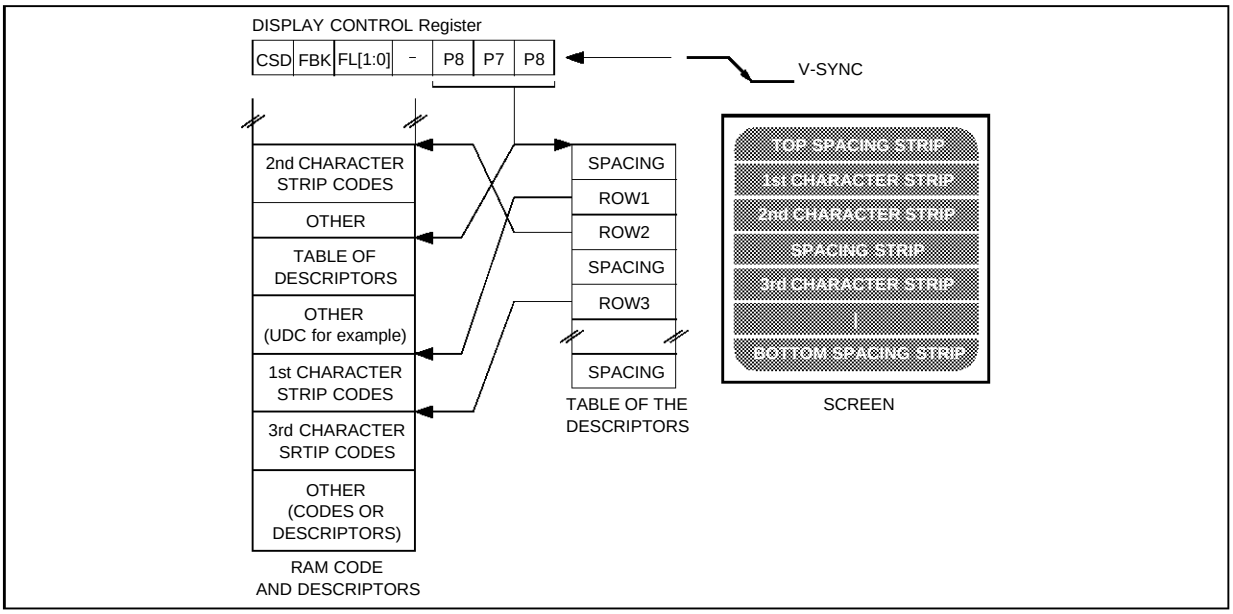
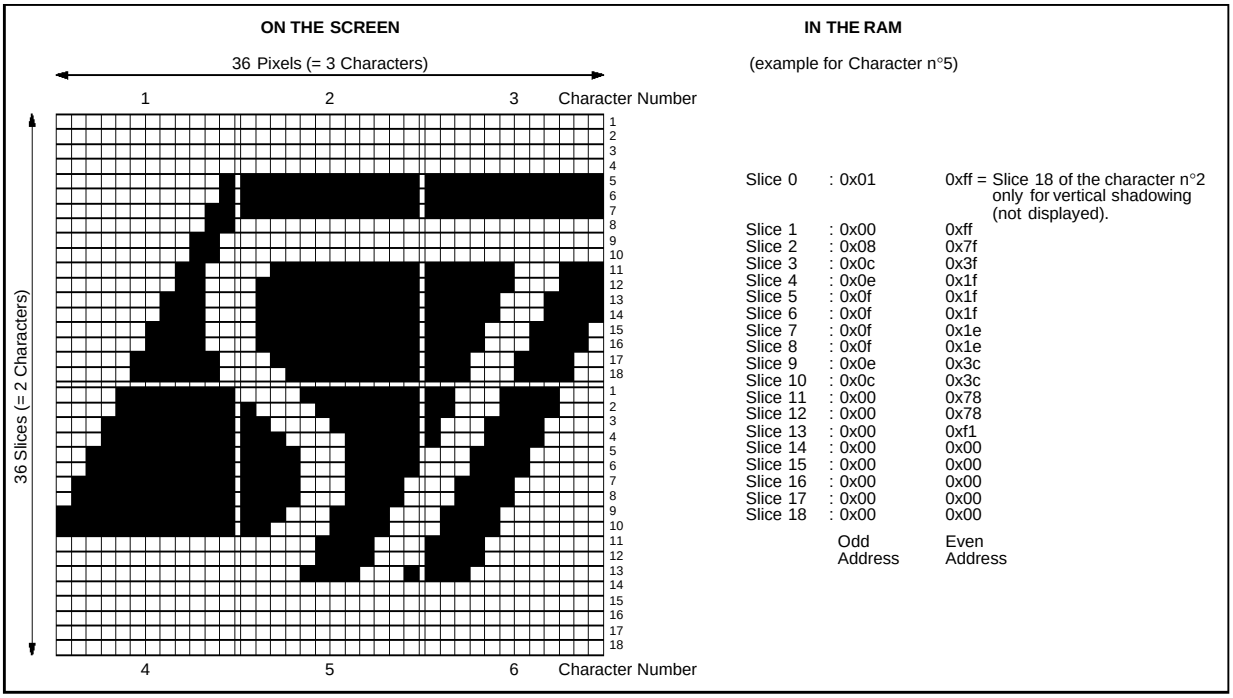
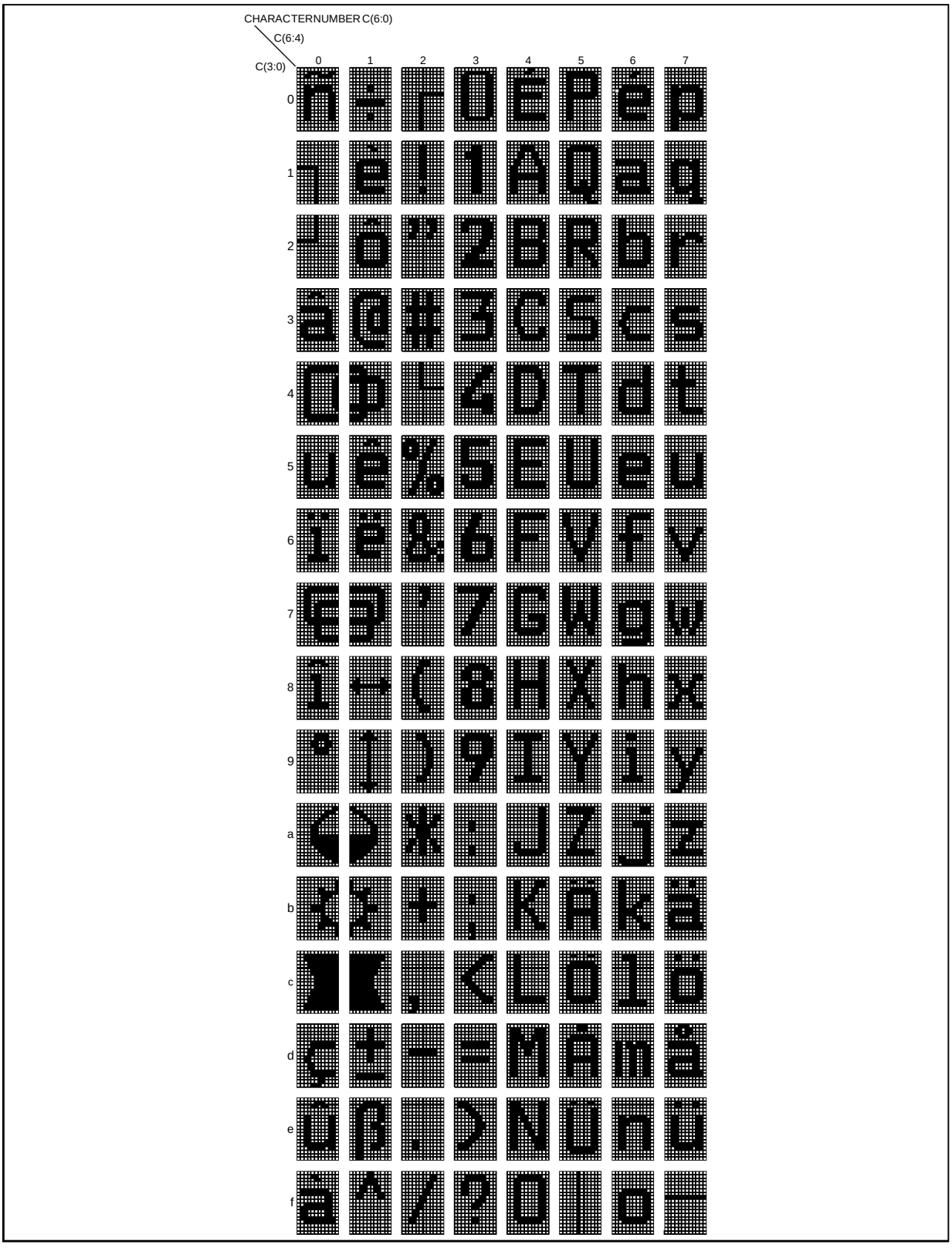


Figure 8 : User Definable Character



FUNCTIONAL DESCRIPTION (continued)

Table 1 : ROM Character Generator



FUNCTIONAL DESCRIPTION (continued)

VI - User Definable Character

The STV9420/21 allows the user to dynamically define character(s) for his own needs (for a special LOGO for example). Like the ROM characters, a UDC is made of a 12 pixels x 18 slices dot matrix, but one more slice is added for the vertical shadowing when several UDCs are gathered to make a special great character (see Figure 8).

In a UDC, each pixel is defined with a bit, 1 refers to foreground, and 0 to background color. Each slice of a UDC uses 2 bytes :

add + 1	-	-	-	-	PX11	PX10	PX9	PX8
add (even)	PX7	PX6	PX5	PX4	PX3	PX2	PX1	PX0

PX11 is the left most pixel. Character slice address : SLICE ADDRESS = 38 x (CHARACTER NUMBER) + (SLICE NUMBER).

Where :
- CHARACTER NUMBER is the number given by the character code,
- SLICE NUMBER is the number given by the slice interpolator (n° of the current slice of the strip : 1 < <18)

VII - ROM Character Generator

The STV9420/21 includes a ROM character generator which is made of 128 alphanumeric or graphic characters (see Table 1)

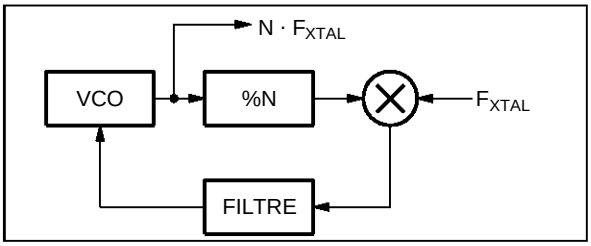
VIII - PLL

The PLL function of the STV9420/21 provides the internal pixel clock locked on the horizontal synchro signal and used by the display processor to generate the R, G, B and fast blancking signals. It is made of 2 PLLs. The first one analogic (see Figure 9), provides a high frequency signal locked on the crystal frequency. The frequency multiplier is given by :

$N = 2 \cdot (FM[3:0] + 3)$

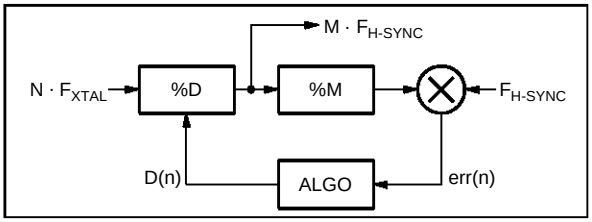
Where FM[3:0] is the value of the FREQUENCY MULTIPLIER register.

Figure 9 : Analogic PLL



The second PLL, full digital (see Figure 10), provides a pixel frequency locked on the horizontal synchro signal. The ratio between the frequencies of these 2 signals is :M = 12 x (LD[5:0] + 1)
Where LD[5:0] is the value of the LINE DURATION register.

Figure 10 : Digital PLL



VIII.1 - Programming of the PLL Registers

Frequency Multiplier (@3FF7)
This register gives the ratio between the crystal frequency and the high frequency of the signal used by the 2nd PLL to provide, by division, the pixel clock. The value of this high frequency must be near to 200MHz (for example if the crystal is a 8MHz, the value of FM must be equal to 10) and greater than 6 x (pixel frequency).

Initial Pixel Period (@3FF6)
This register allows to increase the speed of the convergence of the PLL when the horizontal frequency changes (new graphic standart). The relationship between FM[3:0], PP[7:0], LD[5:0], F_{HSYNC} and F_{XTAL} is :

$$PP[7:0] = \text{round}\left(8 \cdot \frac{2 \cdot (FM[3:0] + 3) \cdot F_{XTAL}}{12 \cdot LD[5:0] \cdot F_{HSYNC}} \pm 24\right)$$

Locking Condition Time Constant (@ 3FF4)
This register gives the constants AS[2:0] and BS[2:0] used by the algo part of the PLL (see Figure 10) to calculate, from the phase error, err(n), the new value, D(n), of the division of the high frequency signal to provide the pixel clock. These two constants are used only in locking condition, which is true, if the phase error is less than a fixed value during at least, 4 scan lines. If The phase error becomes greater than the fixed value, the PLL is not in locking condition but in capture process. In this case, the algo part of the PLL used the other constants, AF[2:0] and BF[2:0], given by the next register.

Capture Process Time Constant (@ 3FF5)
The choice between these two time constants (locking condition or capture process) allows to decrease the capture process time by changing the time response of the PLL.

FUNCTIONAL DESCRIPTION (continued)

VIII.2 - How to choose the value of the time constant ?

The time response of the PLL is given by its characteristic equation which is :

$$(x \pm 1)^2 + (\alpha + \beta) \cdot (x \pm 1) + \beta = 0.$$

Where :

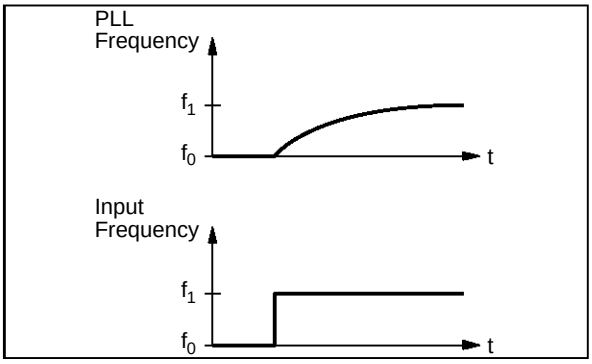
$\alpha = 3 \cdot LD[5:0] \cdot 2^{A \pm 11}$ and $\beta = 3 \cdot LD[5:0] \cdot 2^{B \pm 19}$.

(LD[5:0] = value of the LINE DURATION register, A = value of the 1st time constant, AF or AS and B = value of the 2^d time constant, BF or BS).

As you can see, the solution depend only on the LINE DURATION and the TIME CONSTANTS given by the I^2C registers.

If $(\alpha + \beta)^2 \pm 4\beta \geq 0$ and $2\alpha \pm \beta < 4$, the PLL is stable and its response is like this presented on Figure 11.

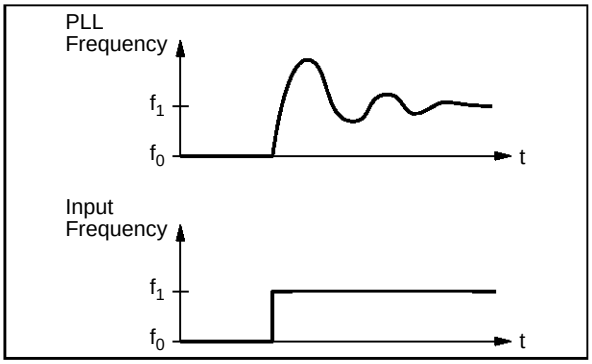
Figure 11 : Time Response of the PLL/Characteristic Equation Solutions (with Real Solutions)



If $(\alpha + \beta)^2 \pm 4\beta \leq 0$, the response of the PLL is like this presented on Figure 12.

In this case the PLL is stable if $\tau > 0.7$ (damping coefficient).

Figure 12 : Time Response of the PLL/Characteristic Equation Solutions (with Complex Solutions)



The Table 2 gives some good values for A and B constants for different values of the LINE DURATION.

Summary

For a good working of the PLL :

- A and B time constants must be chosen among values for which the PLL is stable,
- B must be equal or greater than A and the difference between them must be less than 3,
- The greater (A, B) are, the faster the capture is.

An optimal choice for the most of applications might be :

- For locking condition : AS = 0 and BS = 1,
- For capture process : AS = 2 and BS = 4.

But for each application the time constants can be calculated by solving the characteristic equation and choosing the best response.

Table 2 : Valid Time Constants Examples

B \ A	0	1	2	3	4	5	6
0	YYYY	YYYY	YYYY	YYYN	YNNN	NNNN	NNNN
1	YYYY	YYYY	YYYY	YYYN	YNNN	NNNN	NNNN
2	NYYY	YYYY	YYYY	YYYN	YNNN	NNNN	NNNN
3	NNNY	YYYY	YYYY	YYYN	YNNN	NNNN	NNNN
4	NNNN	NYYY(1)	YYYY	YYYN	YNNN	NNNN	NNNN
5	NNNN	NNNY	YYYY	YYYN	YNNN	NNNN	NNNN
6	NNNN	NNNN	NYYY	YYYN	YNNN	NNNN	NNNN
7	NNNN	NNNN	NNNY	YYYN	YNNN	NNNN	NNNN

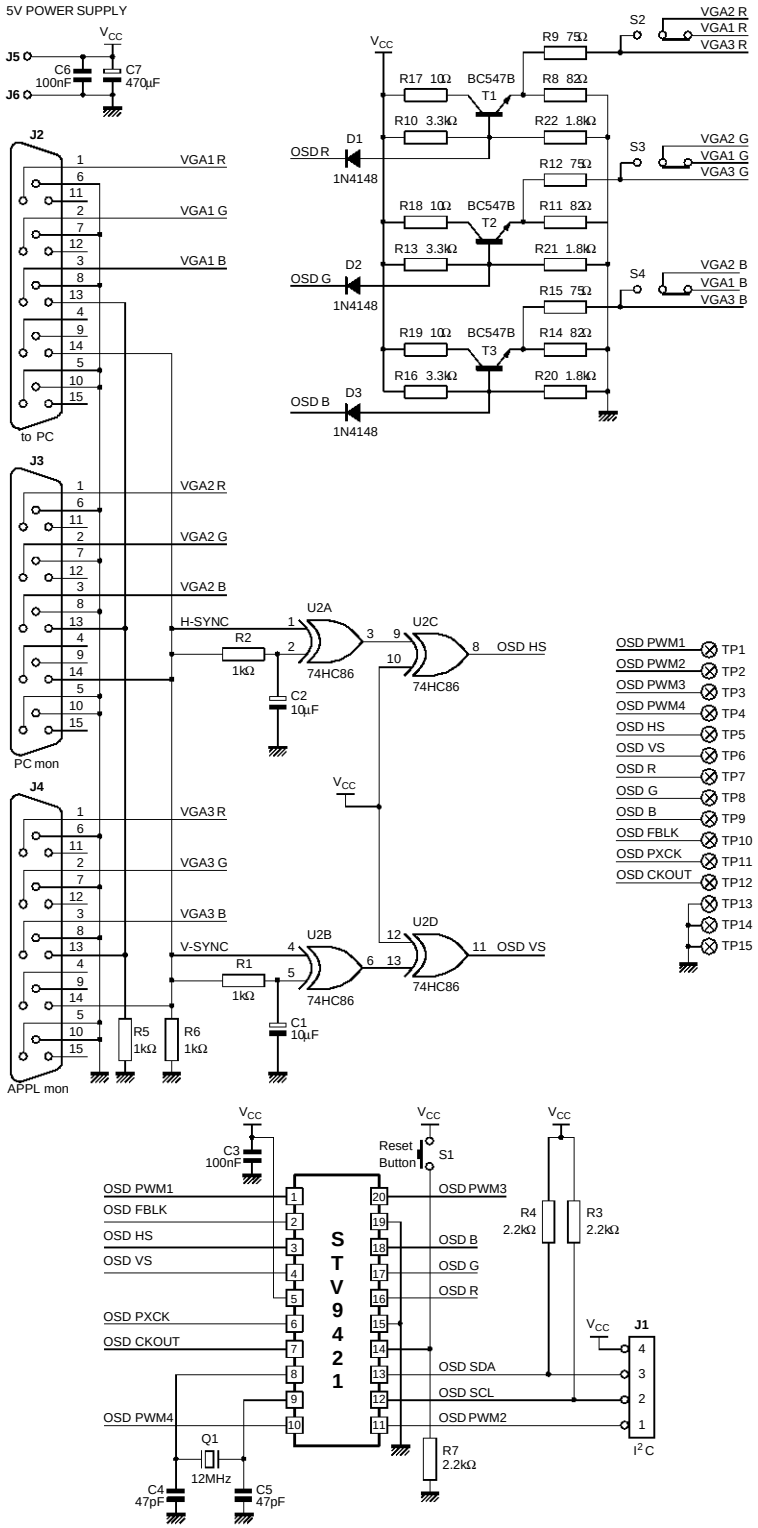
9420-05.TBL

Note : 1. Case of A[2:0] = 1 (001) and B[2:0] = 4 (100) :

LD	16	32	48	63
Valid Time Constants	N	Y	Y	Y

Value of LINE DURATION Register (@ 3FF0) :
LD = 16 : LD[5:0] = 010000
LD = 32 : LD[5:0] = 100000
LD = 48 : LD[5:0] = 110000
LD = 63 : LD[5:0] = 111111
Table meaning :
N = No possible capture
Y = PLL can lock

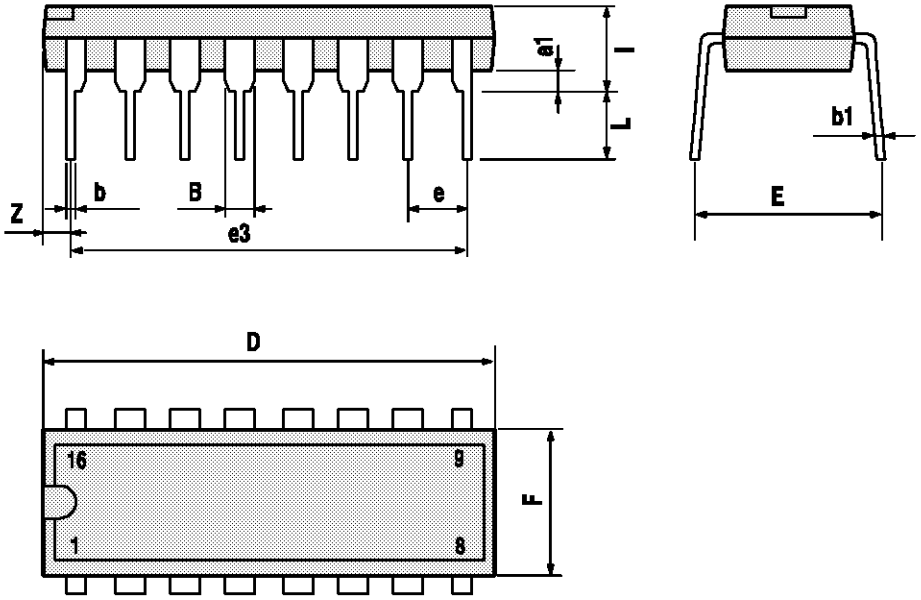
DEMO KIT



A demonstration board is available through your usual SGS-THOMSON Sales Office.
This demonstration board alllows to test very easily the STV9420/21 performances on any personnal computer. The board is delivered together with a "page maker" software which allows to easily generate pages of text or graphics on the PC monitor, or on a second monitor. The I^2C sequences are generated by the PC parallel port and send to the demobaord through an I^2C interface which is also delivered together with demoboard. Of course, a small manual is also inside the kit.

9420-16.EPS

PACKAGE MECHANICAL DATA (STV9420)
16 PINS - PLASTIC DIP

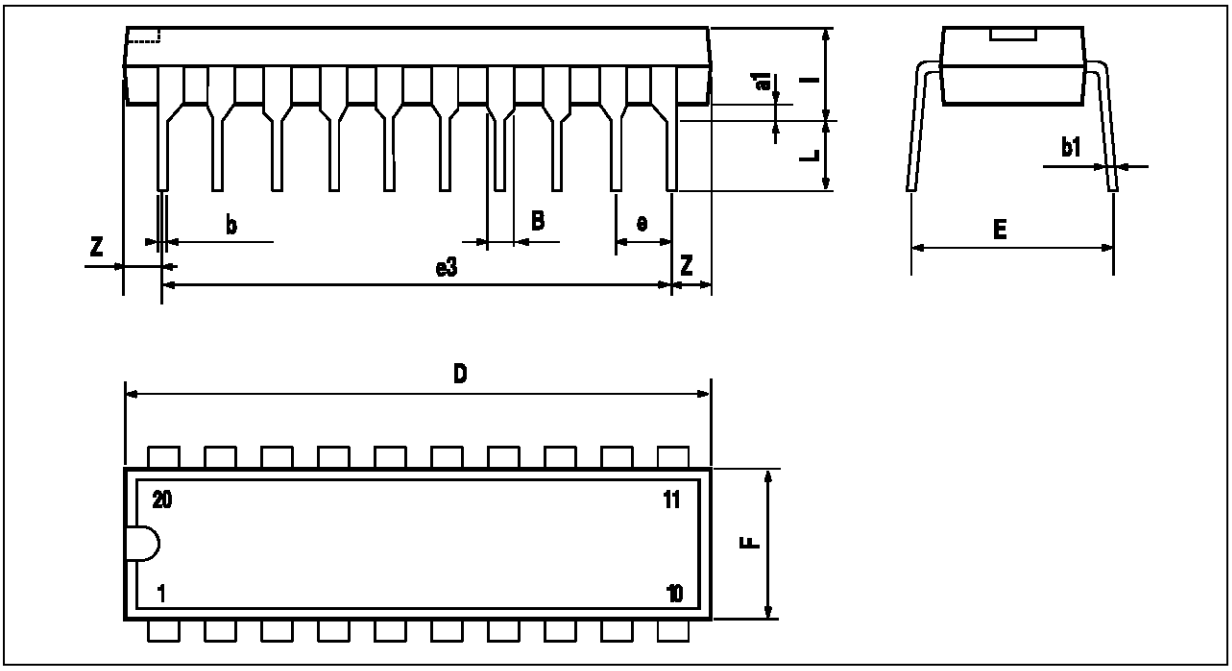


PM-DIP16.WMF

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

DIP16.TBL

PACKAGE MECHANICAL DATA (STV9421)
20 PINS - PLASTIC DIP



PM-DIP20.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053

DIP20.TBL