



STP50NE10

N - CHANNEL 100V - 0.021Ω - 50A - D²PAK STripFET™ POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STP50NE10	100 V	<0.027 Ω	50 A

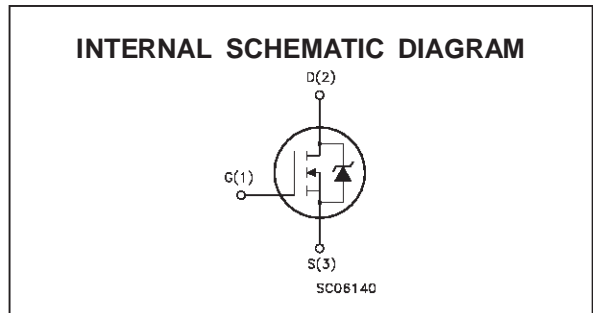
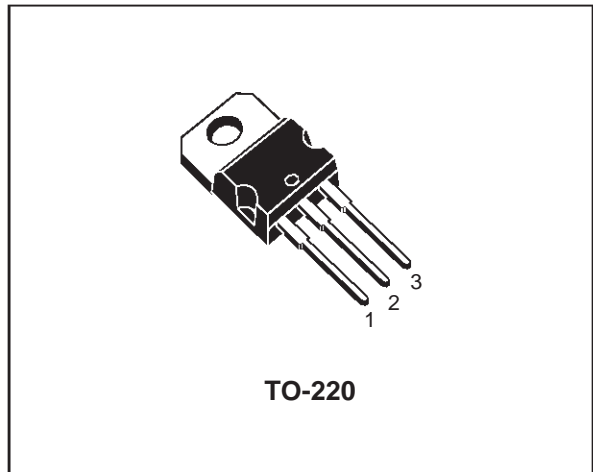
- TYPICAL R_{DS(on)} = 0.021 Ω
- EXCEPTIONAL dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- LOW GATE CHARGE AT 100 °C
- APPLICATION ORIENTED CHARACTERIZATION

DESCRIPTION

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RELAY DRIVERS
- MOTOR CONTROL, AUDIO AMPLIFIERS
- DC-DC & DC-AC CONVERTERS
- AUTOMOTIVE ENVIRONMENT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	100	V
V _{DGR}	Drain- gate Voltage (R _{GS} = 20 kΩ)	100	V
V _{GS}	Gate-source Voltage	± 20	V
I _D	Drain Current (continuous) at T _c = 25 °C	50	A
I _D	Drain Current (continuous) at T _c = 100 °C	35	A
I _{DM} (•)	Drain Current (pulsed)	200	A
P _{tot}	Total Dissipation at T _c = 25 °C	150	W
	Derating Factor	1	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	6	V/ns
T _{stg}	Storage Temperature	-65 to 175	°C
T _j	Max. Operating Junction Temperature	175	°C

(•) Pulse width limited by safe operating area

(1) I_{SD} ≤ 50 A, di/dt ≤ 300 A/μS, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}

STP50NE10

THERMAL DATA

R _{thj-case}	Thermal Resistance Junction-case	Max	1	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient	Max	62.5	°C/W
R _{thc-sink}	Thermal Resistance Case-sink	Typ	0.5	°C/W
T _l	Maximum Lead Temperature For Soldering Purpose		300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	50	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	300	mJ

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA V _{GS} = 0	100			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating T _c = 125 °C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20 V			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} I _D = 250 μA	2	3	4	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V I _D = 25 A		0.021	0.027	Ω
I _{D(on)}	On State Drain Current	V _{DS} > I _{D(on)} × R _{DS(on)max} V _{GS} = 10 V	50			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (*)	Forward Transconductance	V _{DS} > I _{D(on)} × R _{DS(on)max} I _D = 25 A	20	35		S
C _{iss}	Input Capacitance	V _{DS} = 25 V f = 1 MHz V _{GS} = 0		4350	6000	pF
C _{oss}	Output Capacitance			500	675	pF
C _{rss}	Reverse Transfer Capacitance			175	238	pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Time	$V_{DD} = 50\text{ V}$ $I_D = 25\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (see test circuit, figure 3)		25	34	ns
t_r	Rise Time			100	135	ns
Q_g	Total Gate Charge	$V_{DD} = 80\text{ V}$ $I_D = 50\text{ A}$ $V_{GS} = 10\text{ V}$		123	166	nC
Q_{gs}	Gate-Source Charge			24		nC
Q_{gd}	Gate-Drain Charge			47		nC

SWITCHING OFF

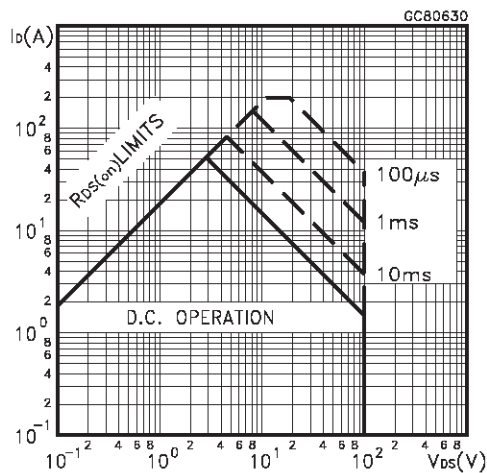
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 80\text{ V}$ $I_D = 50\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (see test circuit, figure 5)		45	61	ns
t_f	Fall Time			35	48	ns
t_c	Cross-over Time			65	88	ns

SOURCE DRAIN DIODE

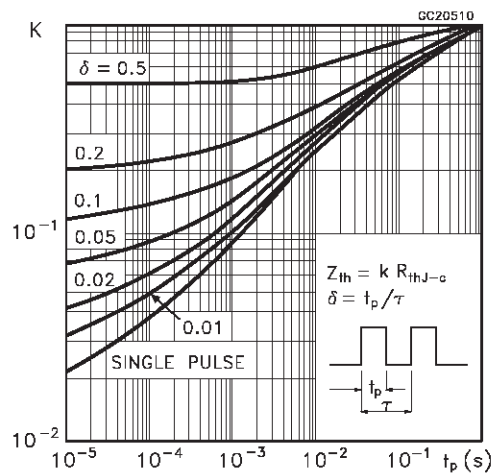
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				50	A
$I_{SDM}(\bullet)$	Source-drain Current (pulsed)				200	A
$V_{SD}(\ast)$	Forward On Voltage	$I_{SD} = 50\text{ A}$ $V_{GS} = 0$			1.5	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 50\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}$ $T_j = 150\text{ }^\circ\text{C}$ (see test circuit, figure 5)		155	210	ns
Q_{rr}	Reverse Recovery Charge			815	1100	nC
I_{RRM}	Reverse Recovery Current			10.5	15	A

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %
 (•) Pulse width limited by safe operating area

Safe Operating Area

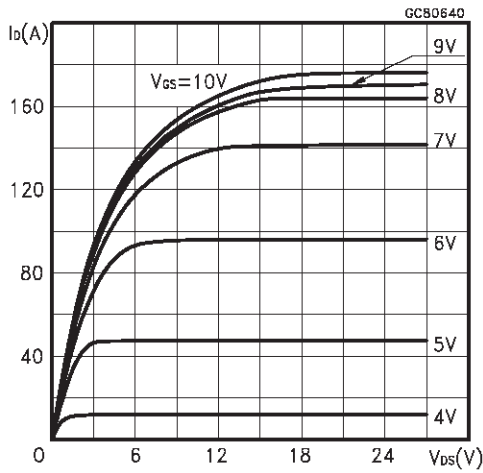


Thermal Impedance

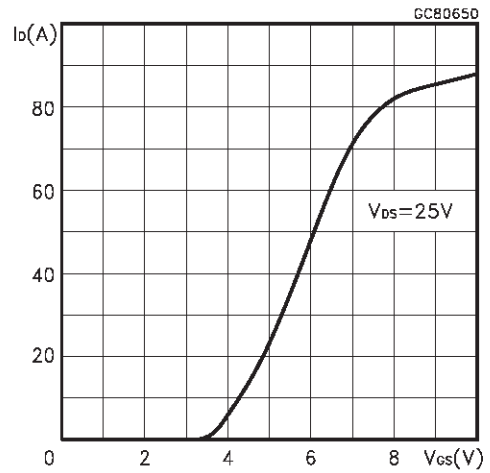


STP50NE10

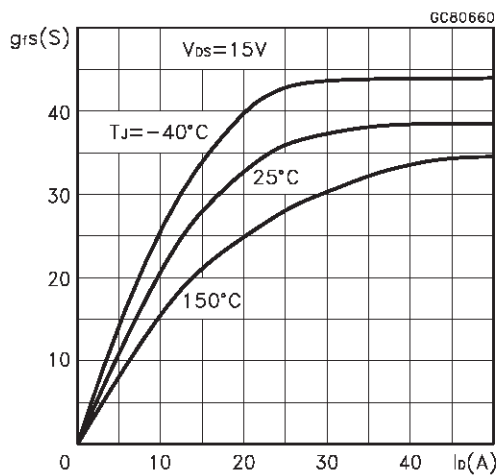
Output Characteristics



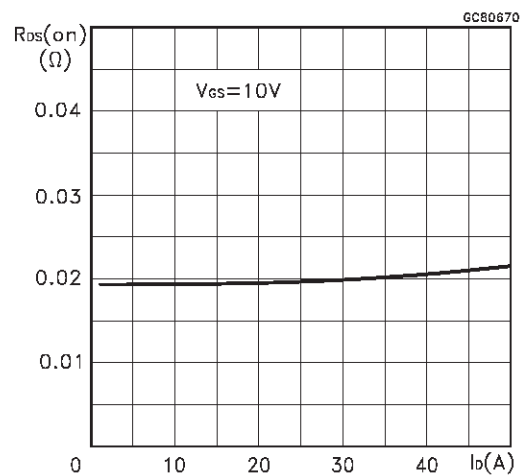
Transfer Characteristics



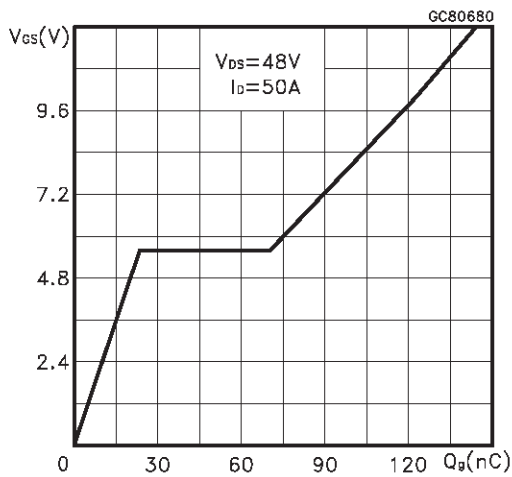
Transconductance



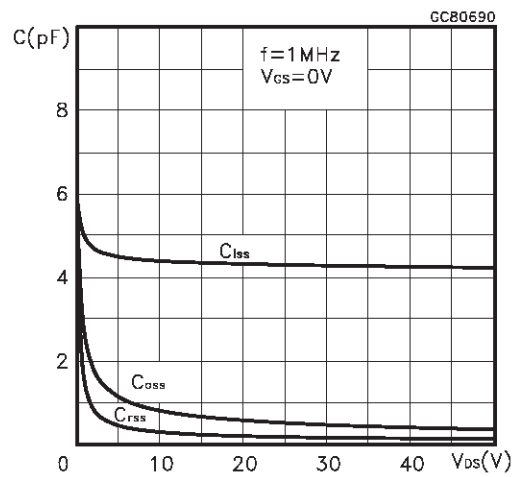
Static Drain-source On Resistance



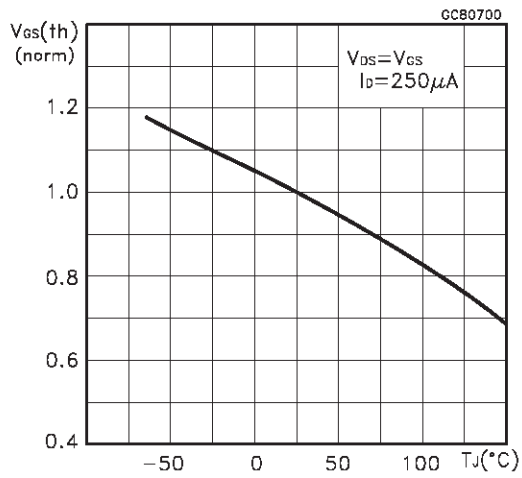
Gate Charge vs Gate-source Voltage



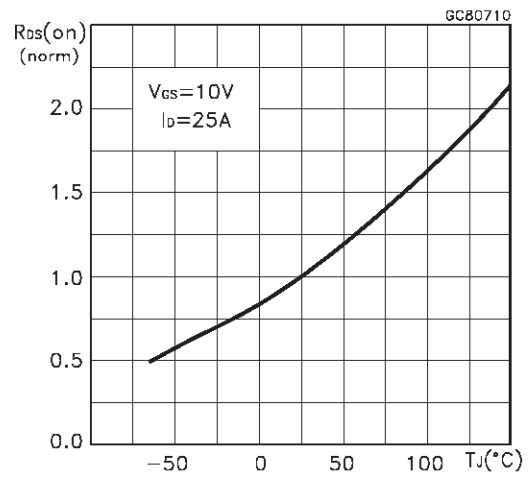
Capacitance Variations



Normalized Gate Threshold Voltage vs Temperature



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

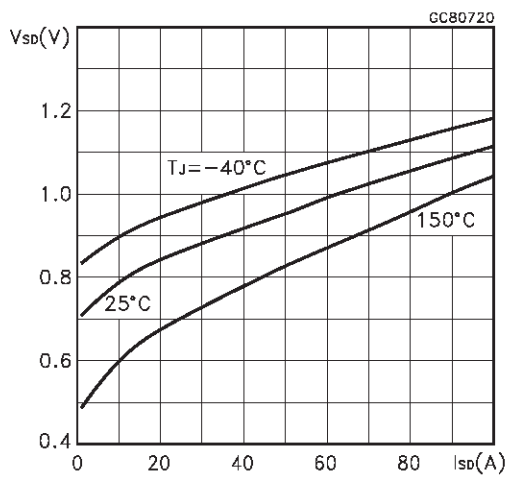


Fig. 1: Unclamped Inductive Load Test Circuit



Fig. 2: Unclamped Inductive Waveform



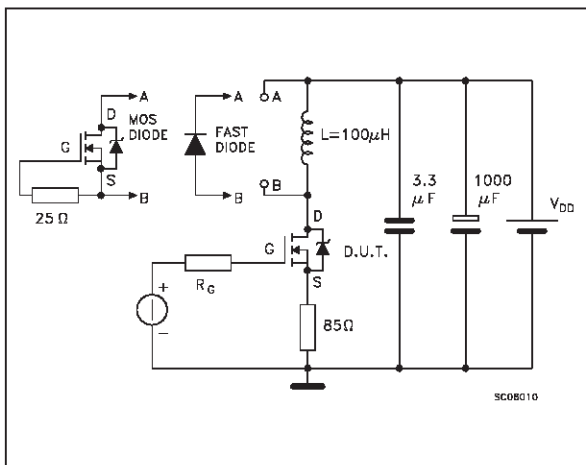
Fig. 3: Switching Times Test Circuits For Resistive Load



Fig. 4: Gate Charge test Circuit

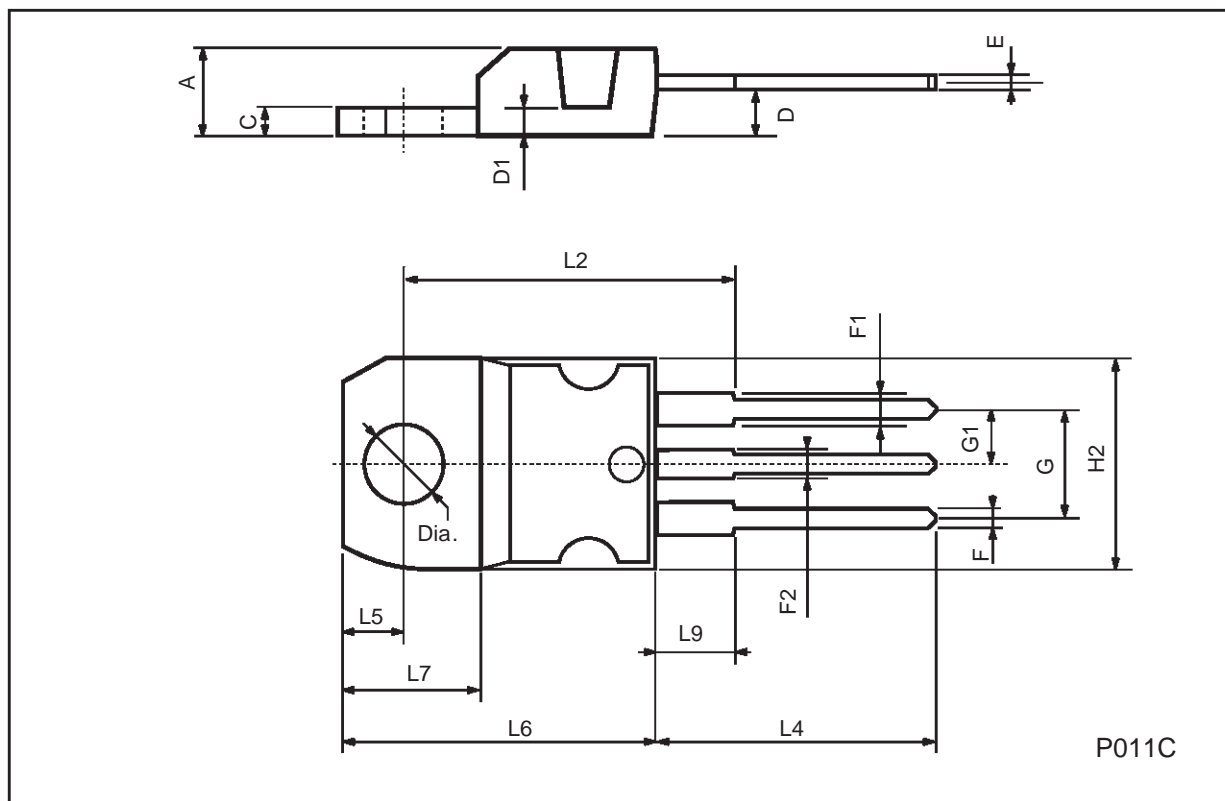


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a trademark of STMicroelectronics

© 1998 STMicroelectronics – Printed in Italy – All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - France - Germany - Italy - Japan - Korea - Malaysia - Malta - Mexico - Morocco - The Netherlands -
Singapore - Spain - Sweden - Switzerland - Taiwan - Thailand - United Kingdom - U.S.A.

<http://www.st.com>