Ordering number : EN4793A

Thick-Film Hybrid IC

# STK301-220

## 7-band, 2-channel Electronic Graphic Equalizer

## Overview

The STK301-220 is a hybrid IC (HIC) for electronically controlled graphic equalizer applications and is equipped with on-chip electronic volume control for 7-band, 2-channel graphic equalization, thereby permitting one-touch up-down control of all band gains. The STK301-220 is a hybrid IC which combines SC system and photoresist techniques with folded board construction while incorporating Sanyo's unique insulated metal substrate technology (IMST) to the base.

## Applications

- Car stereos
- Portable radio-cassette players
- Home stereos

## Features

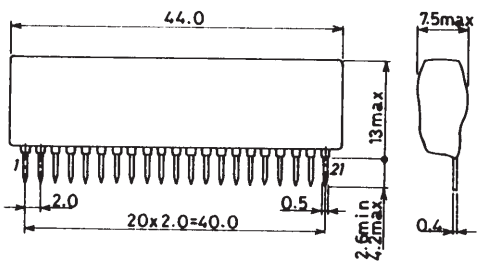
- All bands are set for L/R simultaneous 2 dB incremental operation (typ).
- All bands are equipped with 13 positions and range between +12 dB maximum boost to –12 dB maximum cut.
- Crossover frequencies include fo; 60 Hz, 150 Hz, 400 Hz, 1 kHz, 2.5 kHz, 6 kHz and 15 kHz.
- The following features can be made available with an electronic graphic equalizer system which incorporates the 3-IC construction consisting of the STK301-220, a controller (universal microcontroller) along with the display LSI (LC75821→LCD, LC7565→FLT, LED):
  - — One-touch up-down control of all band gains.
  - — Immediate recall of preferred frequency levels tailored to suit musical selections. This is possible using preset functions to retrieving items from one-touch memory.
  - — Such functions as setting all bands to 0 dB (flat function), or switching frequency characteristics from 0 dB to center (reverse function) may be simply performed with supported software.
  - — Dual control lines permit mutual use with display LSI and help to simplify wiring between microcontroller and LSI.
- Minimal operating shock noise when boost or cut is used.

## Package Dimensions

unit : mm

**4143**

[STK301-220]




## Specifications

### Maximum Ratings at Ta = 25°C, $V_{SS}$ = 0 V

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Maximum supply voltage | $V_{DD}$-$V_{EE}$ max | | 16 | V |
| | $V_{CC}$1 max | | ±18 (36) | V |
| | $V_{CC}$2 max | | 7 | V |
| Input voltage | $V_I$1 | CLK, DI, IN1, IN2 | 0 to $V_{CC}$2 + 0.3 | V |
| | $V_I$2 | CLK, DI, IN1, IN2 | $V_{EE}$ – 0.3 to $V_{DD}$ + 0.3 | V |
| Allowable power dissipation | Pd max | | 920 | mW |
| Operating temperature | Topr | | –20 to +70 | °C |
| Storage temperature | Tstg | | –40 to +100 | °C |

## Recommended Operational Voltage at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{DD}/V_{EE}$ | $V_{SS}$ = 0 V | ±7 (14) | V |
| | $V_{CC}1$ | $V_{SS}$ = 0 V | ±7 (14) | V |
| | $V_{CC}2$ | $V_{SS}$ = 0 V | 5 | V |

## Allowable Operating Ranges at Ta = 25°C, $V_{SS}$ = 0 V

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{DD}$-$V_{EE}$ | | 7.5 to 15.0 | V |
| | $V_{CC}1$ | | ±4 to ±18 (8 to 36) | V |
| | $V_{CC}2$ | | 4.5 to 5.5 | V |
| Input high level voltage | $V_{IH}$ | CLK, DI | 0.8 $V_{CC}2$ to $V_{CC}2$ | V |
| Input low level voltage | $V_{IL}$ | CLK, DI | 0.2 $V_{CC}2$ | V |
| Input pulse width | $t_{\O W}$ | CLK | from 1 | µs |
| Setup time | $t_{setup}$ | DI | from 1 | µs |
| Hold time | $t_{hold}$ | DI | from 1 | µs |
| Operating frequency | $f_{opg}$ | CLK | up to 330 | kHz |

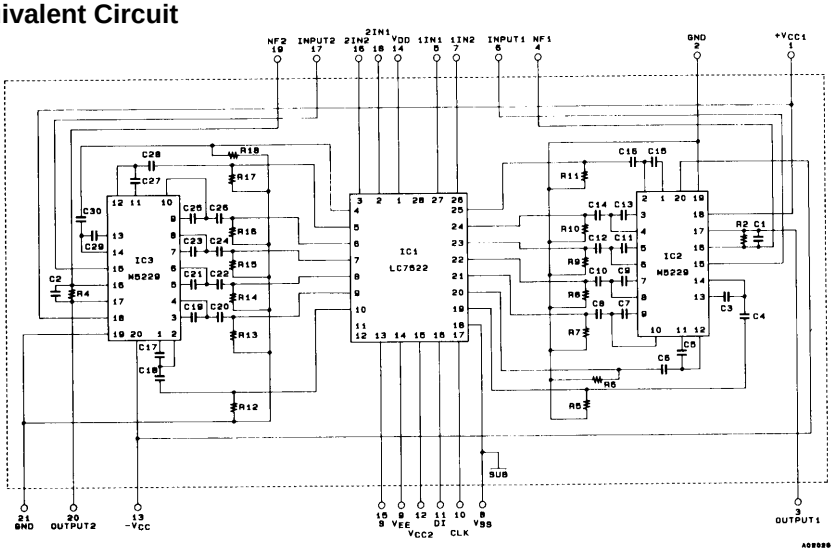
## Operating Characteristics at Ta = 25°C, $V_{SS}$ = 0 V, $V_{DD}/V_{EE}$ = ±7 V, $V_{CC}1$ = ±7 V, $V_{CC}2$ = 5 V, f = 1 kHz

All bands flat, using the specified test circuit

| Parameter | Symbol | Conditions | | Ratings min | Ratings typ | Ratings max | Unit |
|---|---|---|---|---|---|---|---|
| Current dissipation | $I_{DD}$ | $V_{DD}/V_{EE}$ = ±7 V, $V_{CC}1$ = ±7 V, $V_{SS}$ = 0 V<br>$V_{CC}2$ = 5 V | | | | 1 | mA |
| | $I_{CC}1$ | | | | 20 | 30 | mA |
| | $I_{CC}2$ | | | | | 1 | mA |
| Voltage gain | VG | $V_{IN}$ = –10 dB–4.0 | | –1.0 | +2.0 | | dB |
| Total harmonic distortion | THD | f = 1 kHz, $V_O$ = 1V, 30 kHz L.P.F | | | 0.005 | 0.1 | % |
| Crosstalk | C.T. | f = 20 kHz, $V_{IN}$ = 0 dB | | 45 | 55 | | dB |
| Output noise voltage | $V_{NO}$ | Rg = 0 Ω, 10 Hz to 30 kHz B.P.F | | | 9 | 25 | µV |
| Setting error | ΔB | | | –1 | | +1 | dB |
| Frequency response | f (1) | f = 60 Hz | When operating at f = 1 kHz, all bands are flat and $V_O$ = –10 dB set at 0 dB. | ±10 | ±12 | ±14 | dB |
| | f (2) | f = 150 Hz | | ±10 | ±12 | ±14 | dB |
| | f (3) | f = 400 Hz | | ±10 | ±12 | ±14 | dB |
| | f (4) | f = 1 kHz | | ±10 | ±12 | ±14 | dB |
| | f (5) | f = 2.5 kHz | | ±10 | ±12 | ±14 | dB |
| | f (6) | f = 6 kHz | | ±10 | ±12 | ±14 | dB |
| | f (7) | f = 15 kHz | | ±10 | ±12 | ±14 | dB |

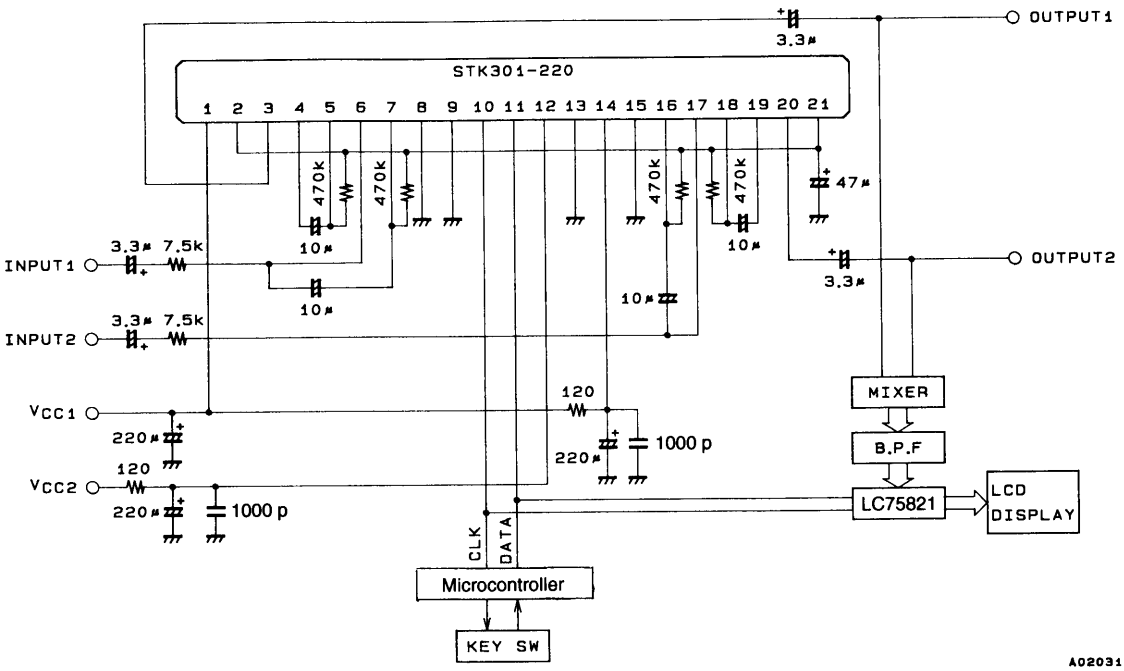
Note: With constant voltage power supply.
The supply voltage figures in parentheses indicate the voltages when a single voltage power supply is used.

## Internal Equivalent Circuit



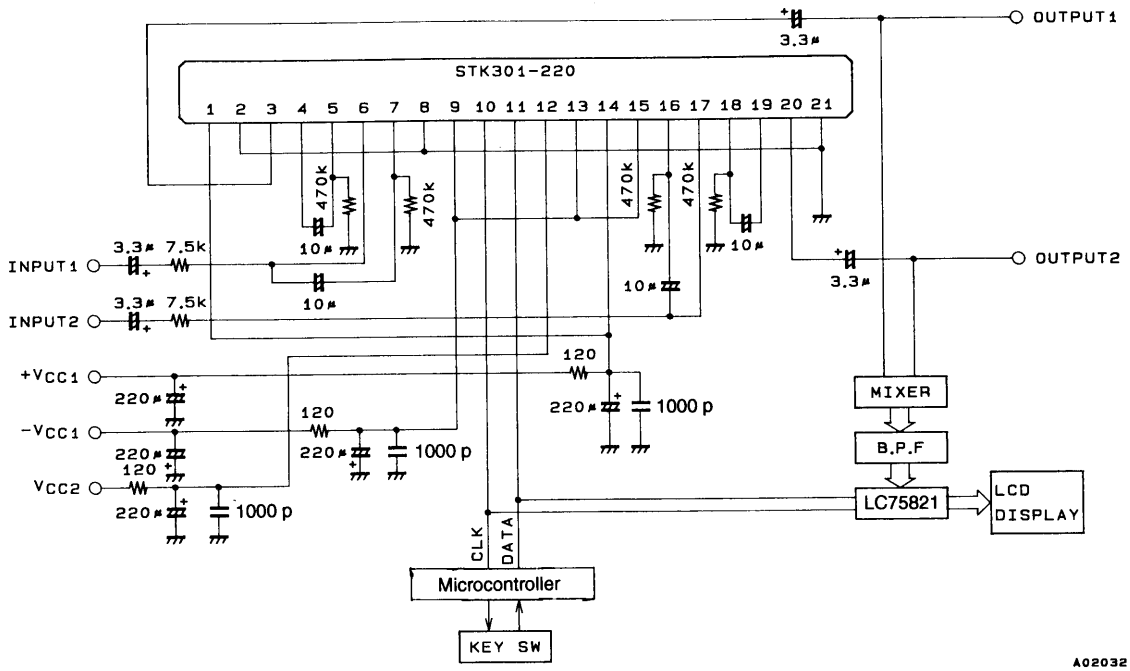
## Sample Application Circuit

### Single Power Supply




Unit (resistance: Ω, capacitance:F)

### Split Power Supply




Unit (resistance: Ω, capacitance:F)

## Pin Descriptions

| Pin No. | Pin name | Functions | |
|---|---|---|---|
| 1 | $+V_{CC}1$ | Power supply pin used for + power supply to IC2 and IC3 graphic equalizer. | |
| 2, 21 | DC | Pin for 1/2 $V_{CC}1$ decoupling capacitor of graphic equalizer IC. When shortened, power supply becomes more effective and ripples are vulnerable. | |
| 3 | OUTPUT 1 | Output pin 1. | |
| 4 | NF 1 | Inverting input for the graphic equalizer IC2 internal operational amplifier. | |
| 5 | 1IN 1 | Audio signal input 1 (INPUT1) for electronic volume control IC1 | |
| 6 | INPUT 1 | Input impedance for input pin 1 rated at approximately 60 kΩ (1 kHz, flat). | |
| 7 | 1IN 2 | Audio signal input 2 (INPUT1) for electronic volume control IC1 | |
| 8 | $V_{SS}$ | Power supply pin connected to ground (GND). | |
| 9 | $V_{EE}$ | Power supply pin used for audio signal power supply to electronic volume control section. When single power supply is used, connect to $V_{SS}$. | |
| 10 | CLK | | Input pin for data from CPU according to Schmitt inverter format. |
| 11 | DI | | Input pin for clock from the CPU according to Schmitt inverter format. |
| 12 | $+V_{CC}2$ | Power supply pin rated at +5 V (typ). Make sure that $V_{CC}2$ does not onset before $V_{DD}$. | |
| 13 | GND ($-V_{CC}1$) | Power supply pin for ground (- power supply) of IC2 and IC3 graphic equalizer. | |
| 14 | $V_{DD}$ | Power supply pin used for audio signal power supply to electronic volume control section. | |
| 15 | S | | Select pin for applications using two ICs. Input “1” to initiate key code 7C3 for connecting to $V_{DD}$. Input “0” to initiate key code 7C2 for connecting to $V_{EE}$. |
| 16 | 2IN 2 | Audio signal input 2 (INPUT2) for electronic volume control IC1 | |
| 17 | INPUT 2 | Input impedance for input pin 2 rated at approximately 60 kΩ (1 kHz, flat). | |
| 18 | 2IN 1 | Audio signal input 1 (INPUT2) for electronic volume control IC1 | |
| 19 | NF 2 | Inverting input for the graphic equalizer IC3 internal operational amplifier. | |
| 20 | OUTPUT 2 | Output pin 2. | |

Note: Refer to LC7522 or LC7523 specifications concerning pins which do not appear here and are hybrid IC (HIC) pins connected directly to a LC7522 or LC7523 pins.

## Description of Operation

The STK301-220 is a hybrid IC (HIC) with a 7-component 2-channel construction for electronically controlled graphic equalizer applications. It employs an LC7522 for graphic equalizer electronic volume control and an M5229 for 7-component graphic equalizer functions.

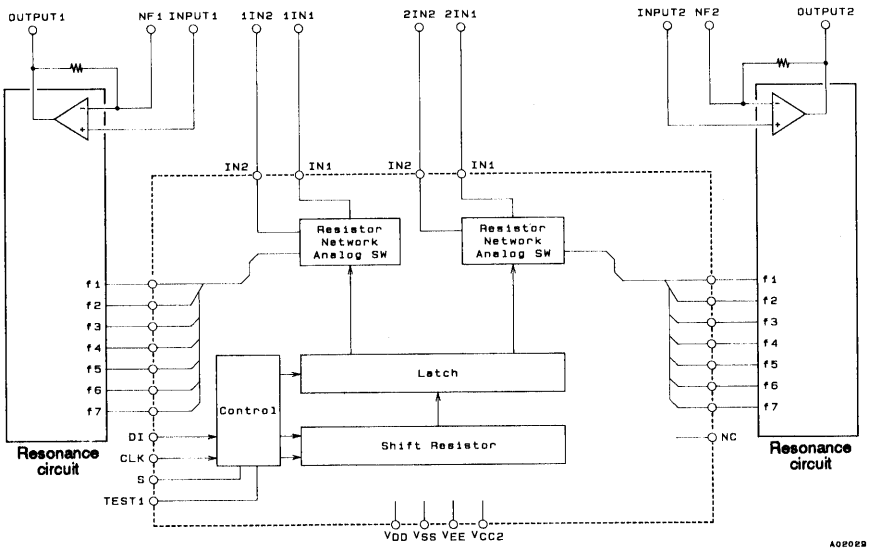
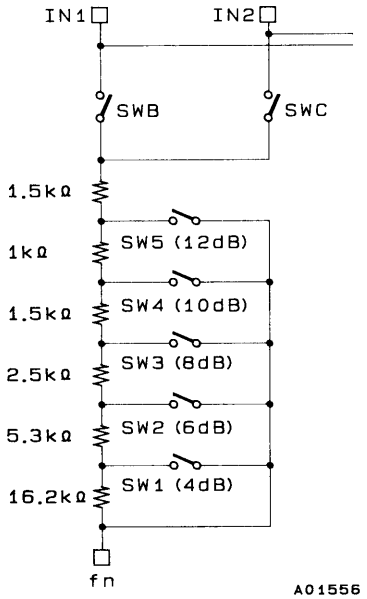



**Figure 1 Equivalent Circuit Block Diagram**

Pins f (1) through f (7) are used as pin connections for the LC7522 band filter. Supported frequencies and their pin assignments are listed in the following.

| Pin Name | Frequency |
|---|---|
| f (1) | 60Hz |
| f (2) | 150Hz |
| f (3) | 400Hz |
| f (4) | 1kHz |
| f (5) | 2.5kHz |
| f (6) | 6kHz |
| f (7) | 15kHz |

In order to minimize the noise which occurs during changeover, connections are made using 1 MΩ resistors from pins f (1) through f (7) to 1/2 $V_{CC}$1.




**Resistor Equivalent Circuit (single band)**

## Principles of Operation

The graphic equalizer section is constructed from 7 resonance circuits and output buffer amplifiers (every channel); variable resistors (LC7522) and resonance circuit capacitors C1 and C2 are built-in. Resonance circuits utilize semiconductor inductors and apply resonation to reduced impedance; all frequency gains are altered.

1. Resonance Circuit

   Semiconductor inductors replace the L of the R, L, C series resonance circuit with a CR element passing through the buffer function of active elements such as the transistor and op-amp (operational amplifier), thereby effecting the equivalent operation of a R, L, C series resonance circuit. The STK301-220 resonance circuit buffer is constructed using transistors and arranged as illustrated in Figure 2.

   Resonance frequency fo is determined using the following formula:

$$fo = \frac{1}{2\pi \sqrt{C1 \cdot C2 \cdot R1 \cdot R2}}$$

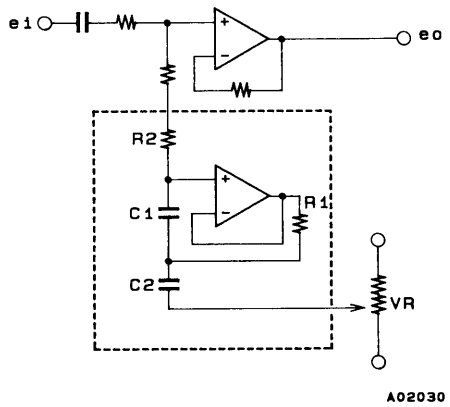
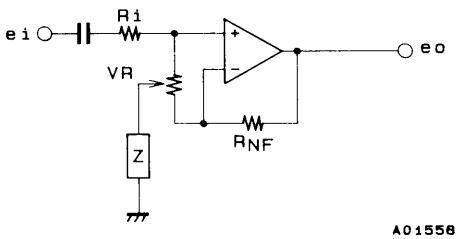



**Figure 2 Resonance Circuit**

2. Flat, Boost and Cut

   Gains matching resonance circuit frequency gains are altered by altering the built-in resonance circuits and electronic volume control. Figure 3 is presented to describe the equivalent circuit. Z represents the impedance of the resonance circuit in Figure 2.




Z : Resonance circuit impedance
VR : Equivalent to LC7522

**Figure 3 Equivalent Circuit**

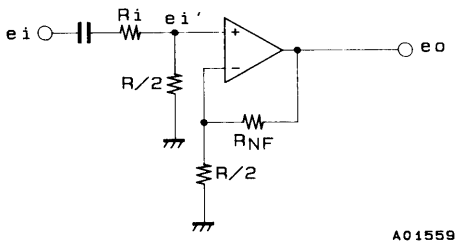
3. Flat

When the volume control is set to the midrange position and Ri=$R_{NF}$, the following relationships are established:

$$ei' = \frac{R/2}{Ri = R/2} \cdot ei$$

$$A_V = \frac{R_{NF} + R/2}{R/2} \text{ in which}$$

$$eo = A_V \cdot ei' = ei$$




with no relation to the resonance circuit and frequency characteristics become flat.

When VR is set to R, the resistance value using the VR center position becomes R/2.

4. Boost

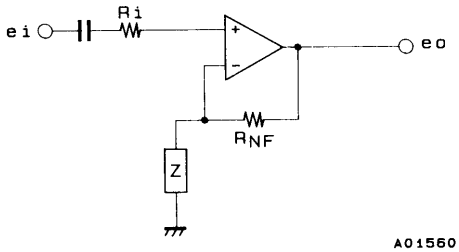
When the volume control is set to the boost position, the resonance circuit is linked to the NF loop of the output buffer amplifier. Under these circumstances and when R»Ri and $R_{NF}$, the following relationship exist:

$$A_V = \frac{R_{NF} + Z}{Z}$$

is established and output voltage eo is calculated as

$$eo = A_V \cdot ei = \frac{R_{NF} + Z}{Z} \cdot ei$$

The gain becomes a minimum when the resonance circuit has Z at a minimum so that the frequency option is boosted.




5. Cut

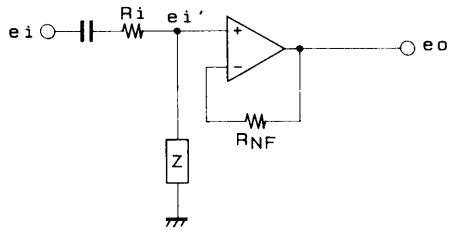
When volume is set to the cut side, resonance circuit is linked to the input side of the output buffer amplifier. Under these circumstances and when ignoring R similarly to boost, the following relationship exist:

$$ei' = \frac{Z}{Ri+Z} \cdot ei,\ A_V = 1$$

is established and output voltage eo is calculated as

$$eo = A_V \cdot ei' = \frac{Z}{Ri+Z} \cdot ei$$

The gain becomes a minimum when the resonance circuit has Z at a minimum so that the frequency option is cut.

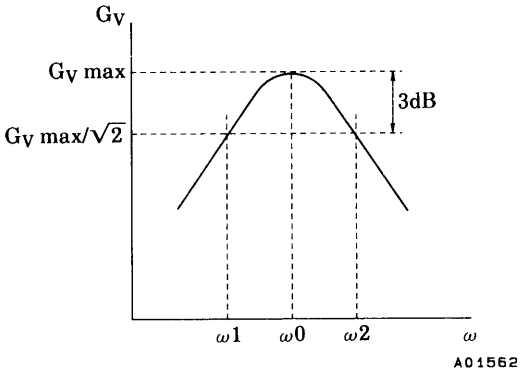



6. Resonance Circuit Crest Acuteness (Q)

Resonance circuit crest acuteness is determined by comparing frequency widths ω2 - ω1 for $G_V$ max/$\sqrt{2}$ where $G_V$ max represents point ω0 as the maximum value of the resonance circuit crest.

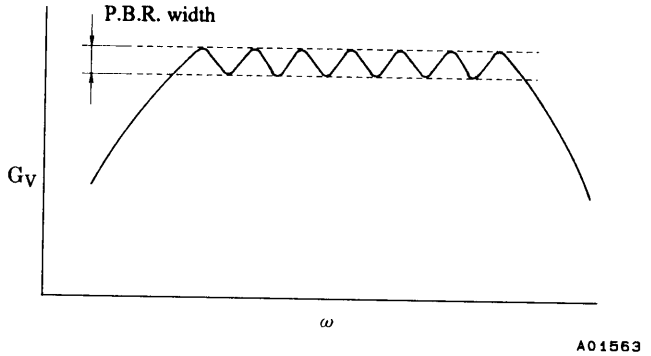
The following formula is used to calculate the value for Q:

$$Q = \sqrt{\frac{C1 \cdot R2}{C2 \cdot R1}}$$



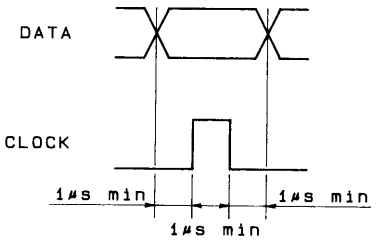

As the value for Q becomes larger, the participating frequency bandwidth of the resonance circuit becomes narrower. Although neighboring bands distinction is precise, the swell of frequency characteristics under total boost is larger while the peak of the resultant frequency is lowered.

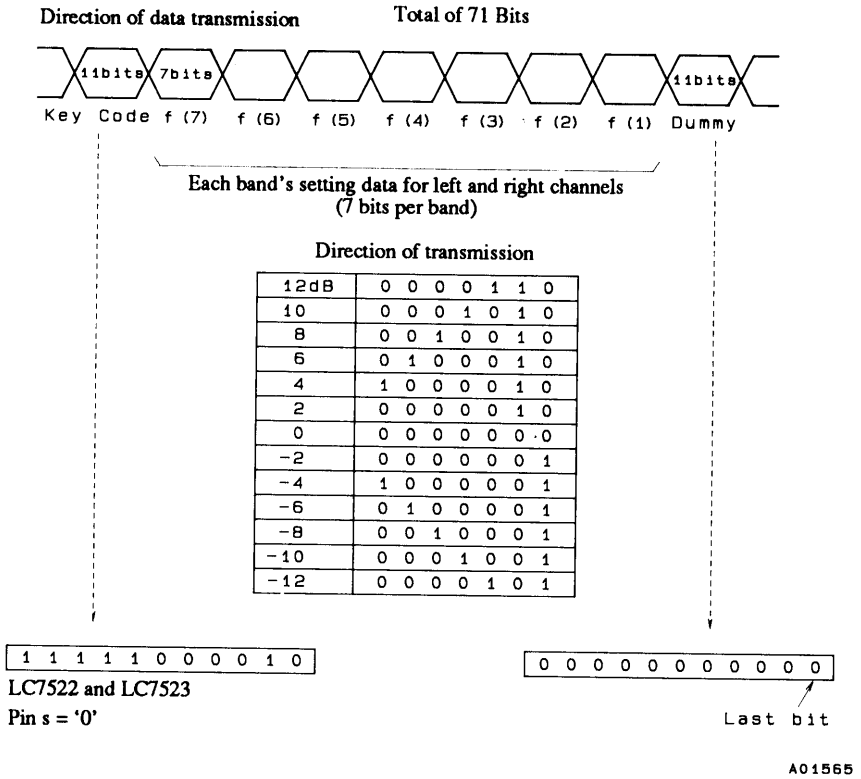
With the STK301-220, few crossover bands exist with an increase in swell during total boost. Pass-band-ripple (P.B.R.) width at this time is 4 dB with Q set at 3.5 fore and aft.




## Data Code

1. Turning on the power initiates a process which transmits no data (0) for 60 clock cycles (initialization clock). When data is stopped en route, the remaining data is sent only after the clock has been initialized.
2. Using DI and CLK in conjunction with LC75821 (or equivalent) involves the transmission of the maximum initialization clock to those devices involved.

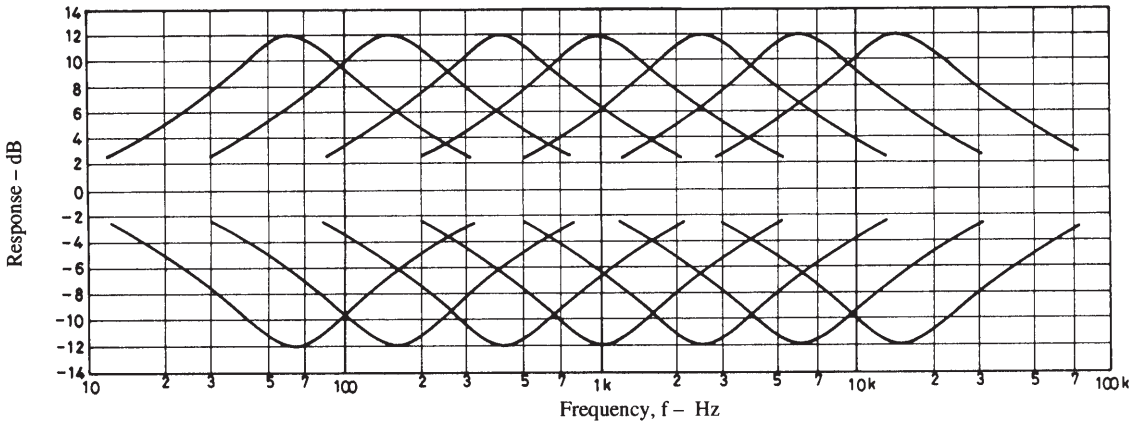


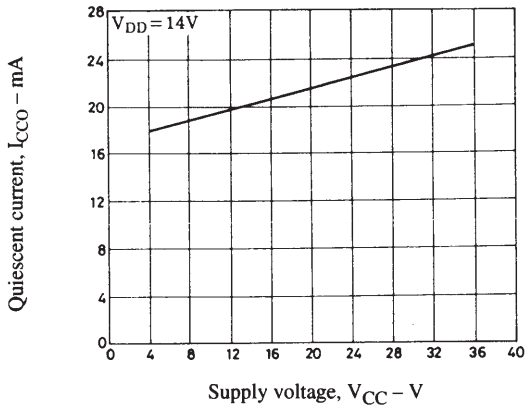

## Things to Note

1. A 1000pF rated capacitor (or higher) should be installed between the current pin and $V_{SS}$.
2. When the control signal on the microcontroller side onsets faster than STK301-220's $V_{DD}$, a resistor rated at 2 kΩ or more should be placed on the DI and CLK line.
3. Since the STK301-220 is equipped with a built-in CMOS LSI, sufficient caution should be extended to damage caused by static electricity.
4. Refer to the specification sheet for itemized details about the LC7522.

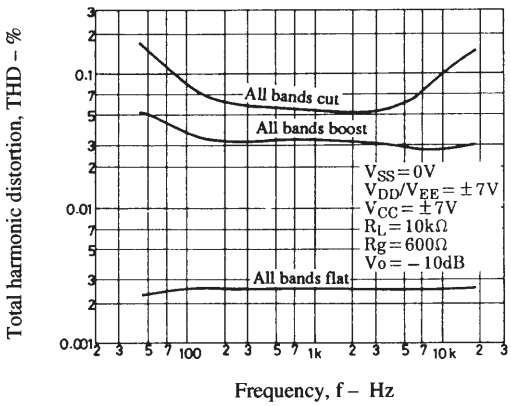
f Response




$I_{CCO} - V_{CC}$




THD – f




THD – $V_O$