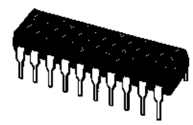
SGS-THOMSON MICROELECTRONICS

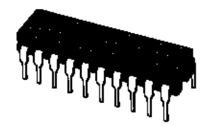
M54/74HCT374
M54/74HCT534

OCTAL D-TYPE FLIP FLOP WITH 3 STATE OUTPUT
HCT374 NON INVERTING - HCT534 INVERTING

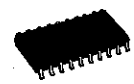
- HIGH SPEED
  f_{MAX} = 62 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $I_{OL} = |I_{OH}|$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS374/534



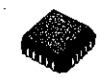
B1R
(Plastic Package)



F1R
(Ceramic Package)



M1R
(Micro Package)



C1R
(Chip Carrier)

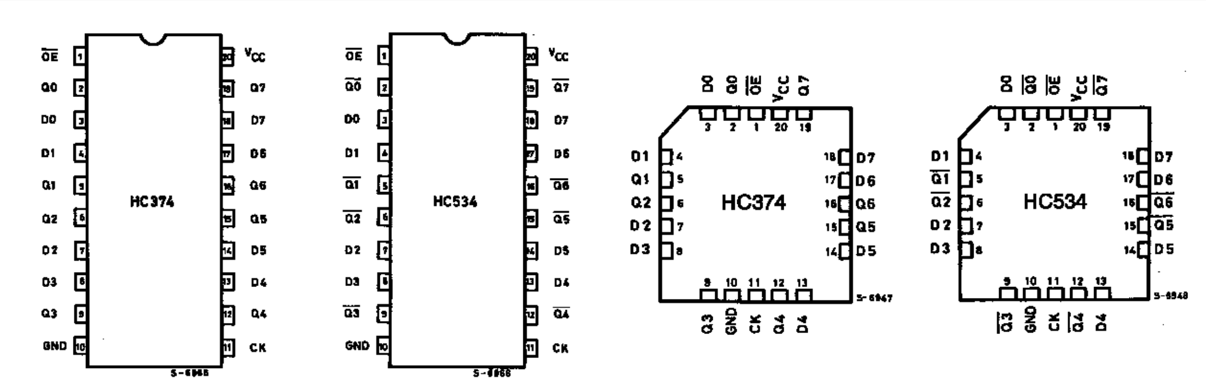
ORDER CODES :

M54HCTXXXF1R M74HCTXXXM1R
M74HCTXXXB1R M74HCTXXXC1R

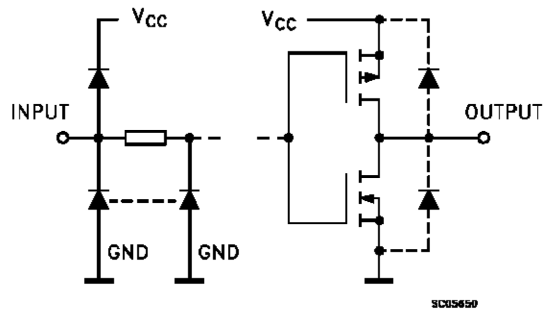
DESCRIPTION

The M54/74HCT374, M54/74HCT534, are high speed CMOS OCTAL D-TYPE FLIP FLOP WITH 3-STATE OUTPUTS fabricated with in silicon gate C^2MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power comsuption. These8-bit D-type flip-flops are controlled by a clock input (CK) and an ouput enable input ($\overline{OE}$). On the positive transition of the clock, the Q outputs will be set to the logic state that were setup at the D inputs (HCT374) or their complements (HCT534).
While the $\overline{OE}$ input is low, the eight outputs will be in a normal logic state (high or low logic level), and while high level, the outputs will be in a high impedance state. The output control does not affect the internal operation of flip-flops. That is, the old data can be retained or the new data can be entered even while the outputs are off. The application engineer has a choice of combination of inverting and non-inverting outputs. The 3-state output configuration and the wide choice of outline make bus-organized systems simple. All inputs are equipped with protection circuits against static discharge and transient excess voltage. This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC^{2}MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.

PIN CONNECTION (top view)



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION (HCT374)

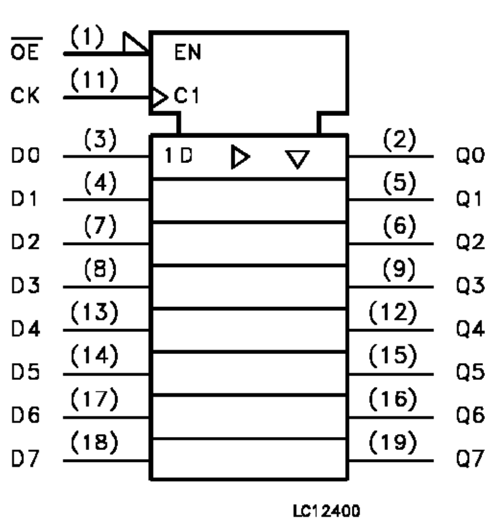
PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3 State output Enable Input (Active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q0 to Q7	3 State outputs
3, 4, 7, 8, 13, 14, 17, 18	D0 to D7	Data Inputs
11	CLOCK	Clock Input (LOW to HIGH, edge triggered)
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

PIN DESCRIPTION (HCT534)

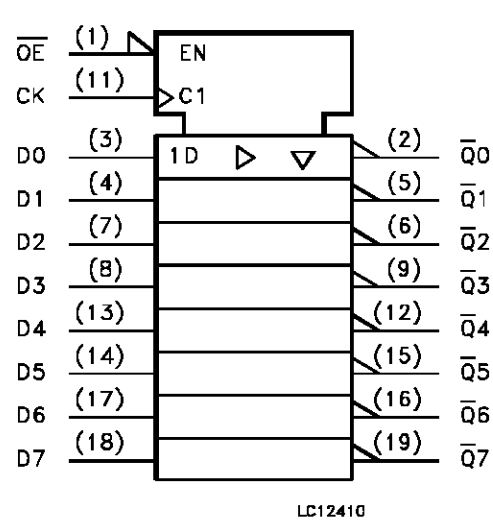
PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3 State output Enable Input (Active LOW)
2, 5, 6, 9, 12, 15, 16, 19	$\overline{Q0}$ to $\overline{Q7}$	3 State outputs
3, 4, 7, 8, 13, 14, 17, 18	D0 to D7	Data Inputs
11	CLOCK	Clock Input (LOW to HIGH, edge triggered)
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS

HCT374



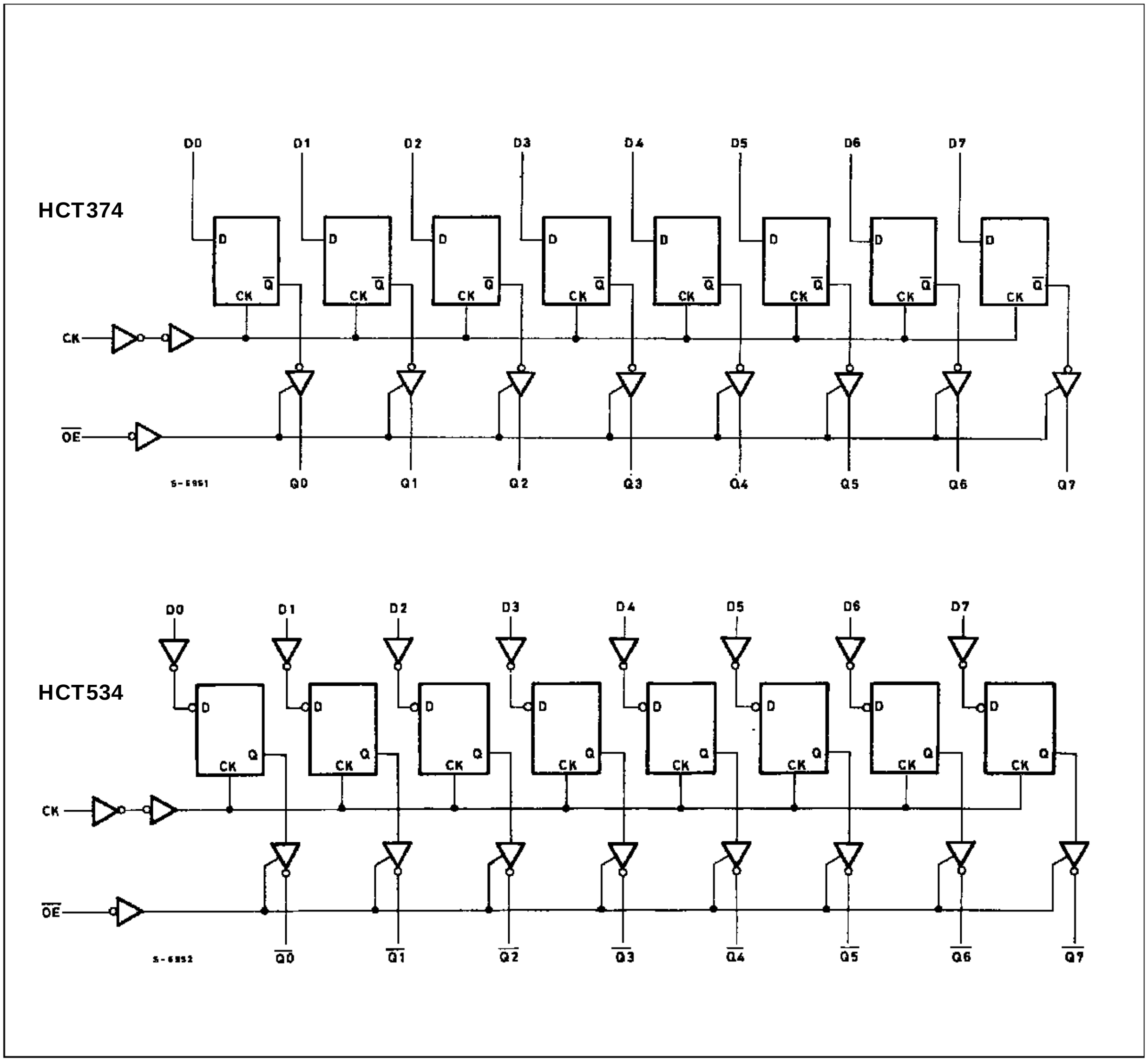
HCT534



TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	CK	D	Q (HC374)	$\overline{Q}$ (HC534)
H	X	X	Z	Z
L	↓	X	NO CHANGE	NO CHANGE
L	↑	L	L	H
L	↑	H	H	L

LOGIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	^oC
T_L	Lead Temperature (10 sec)	300	^oC

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 ^oC derate to 300 mW by 10mW/^oC: 65 ^oC to 85 ^oC

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	^oC ^oC
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-6.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 6.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				4		40		80	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND I_O= 0				2.0		2.9		3.0	mA

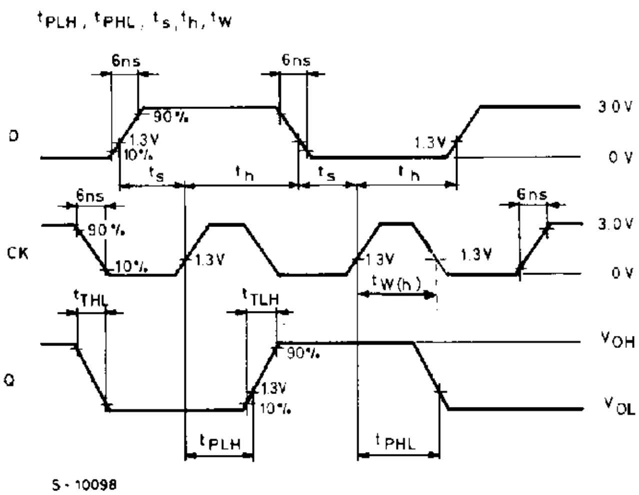
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	Test Conditions V_{CC} (V)	Test Conditions C_L (pF)	Test Conditions	Value T_A = 25 °C 54HC and 74HC Min.	Typ.	Max.	-40 to 85 °C 74HC Min.	Max.	-55 to 125 °C 54HC Min.	Max.	Unit
t_{TLH} t_{THL}	Output Transition Time	4.5	50			7	12		15		18	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Q, $\overline{Q}$)	4.5	50			20	30		38		45	ns
		4.5	150			25	38		48		57	ns
t_{PZL} t_{PZH}	Output Enable Time	4.5	50	R_L = 1 KΩ		17	30		38		45	ns
		4.5	150	R_L = 1 KΩ		25	38		48		57	ns
t_{PZL} t_{PZH}	Output Disable Time	4.5	50	R_L = 1 KΩ		16	28		35		42	ns
f_{MAX}	Maximum CLock Frequency	4.5	50		31	50		25		21		ns
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width (CLOCK)	4.5	50				15		19		23	ns
t_s	Minimum Set-up Time	4.5	50				15		19		23	ns
t_h	Minimum Hold Time	4.5	50				0		0		0	ns
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{OUT}	Out put Capacitance					10						pF
C_{PD} (*)	Power Dissipation Capacitance					48						pF

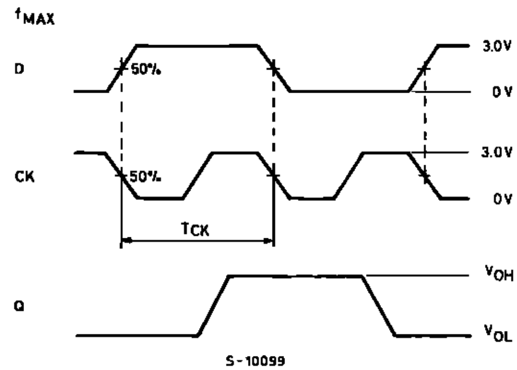
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}/8$ (per FLIP-FLOP) and C_{PD} when N pcs of FLIP-FLOP operate, can be gained by following equation: C_{PD} (TOTAL) = 38 + 18 x N (pF)

SWITCHING CHARACTERISTICS TEST WAVEFORM

t_{PLH}, t_{PHL}, t_s, t_h, t_w



f_{MAX}



t_{PLZ}, t_{PZL}

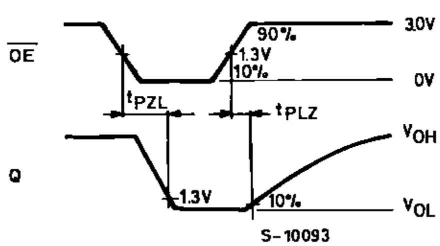
The 1KΩ load resistors should be connected between outputs and V_{CC} line and the 50pF load capacitors should be connected between outputsand GND line.

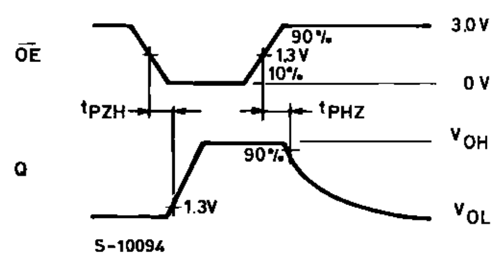
All inputs except $\overline{OE}$ input should be connected to V_{CC} line or GND line such that outputs will be in low logic level while $\overline{OE}$ input is held low.

t_{PHZ}, t_{PZH}

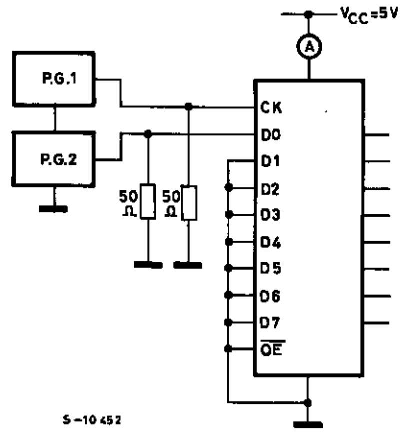
The 1KΩ load resistors and the 50pF load capacitors should be connected between each output and GND line.

All inputs except $\overline{OE}$ input should be connected to V_{CC} or GND line such that output will be in high logic level while $\overline{OE}$ input is held low.





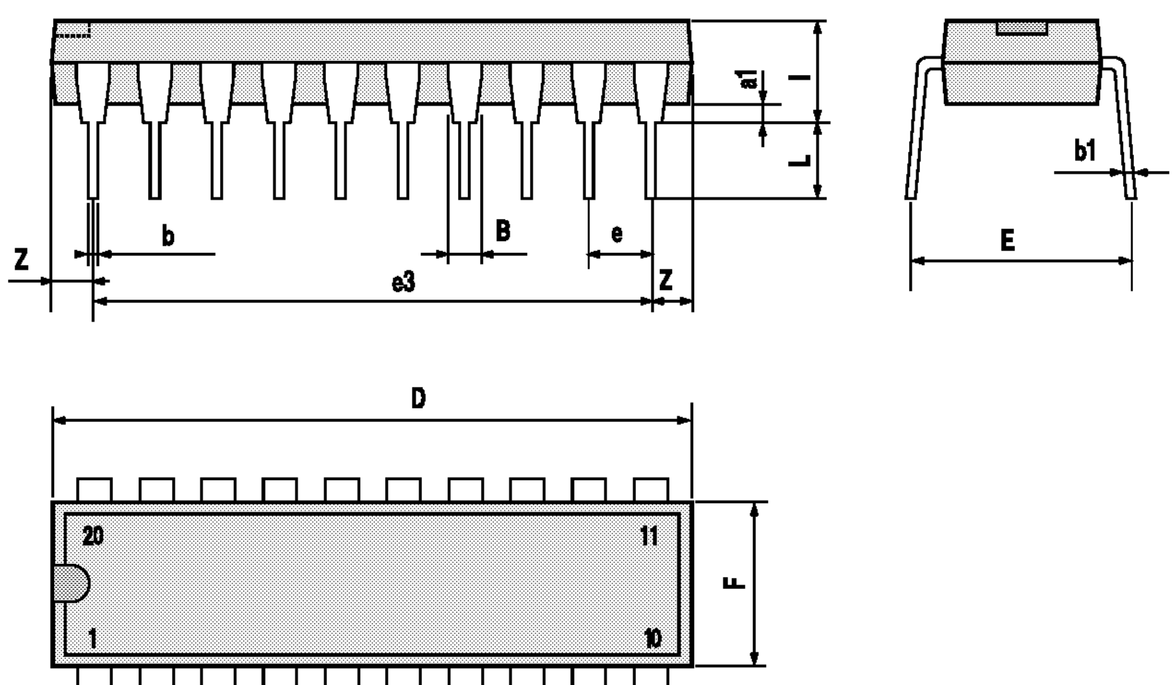
TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

Plastic DIP20 (0.25) MECHANICAL DATA

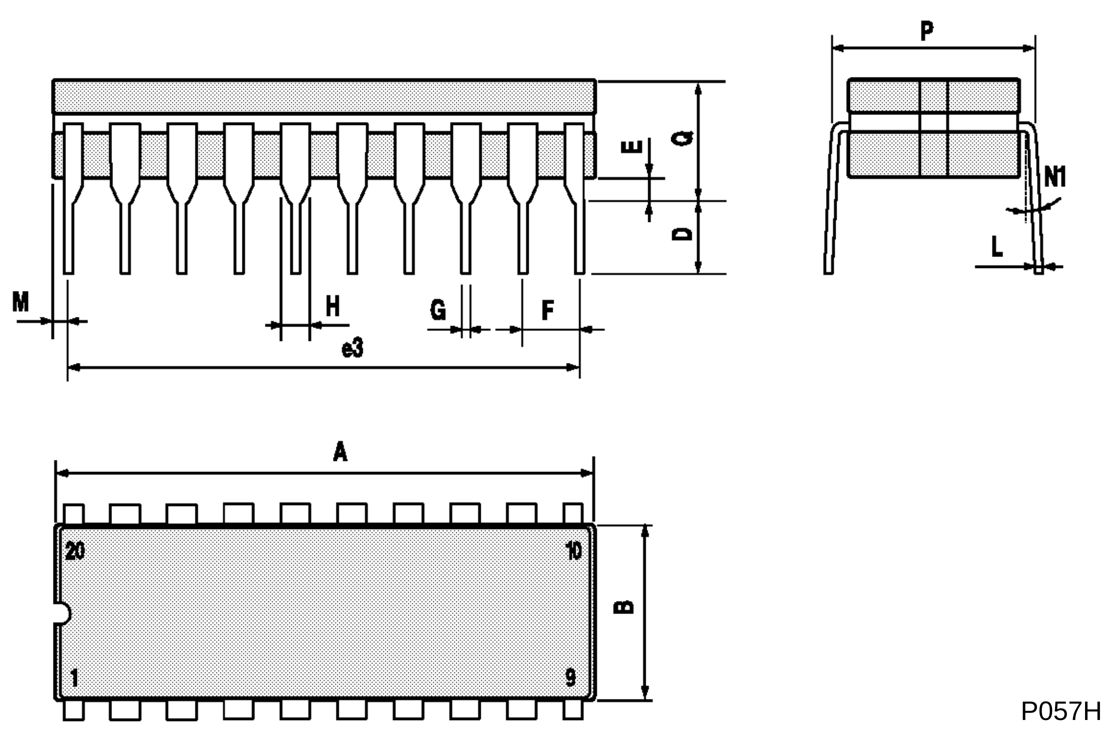
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053



P001J

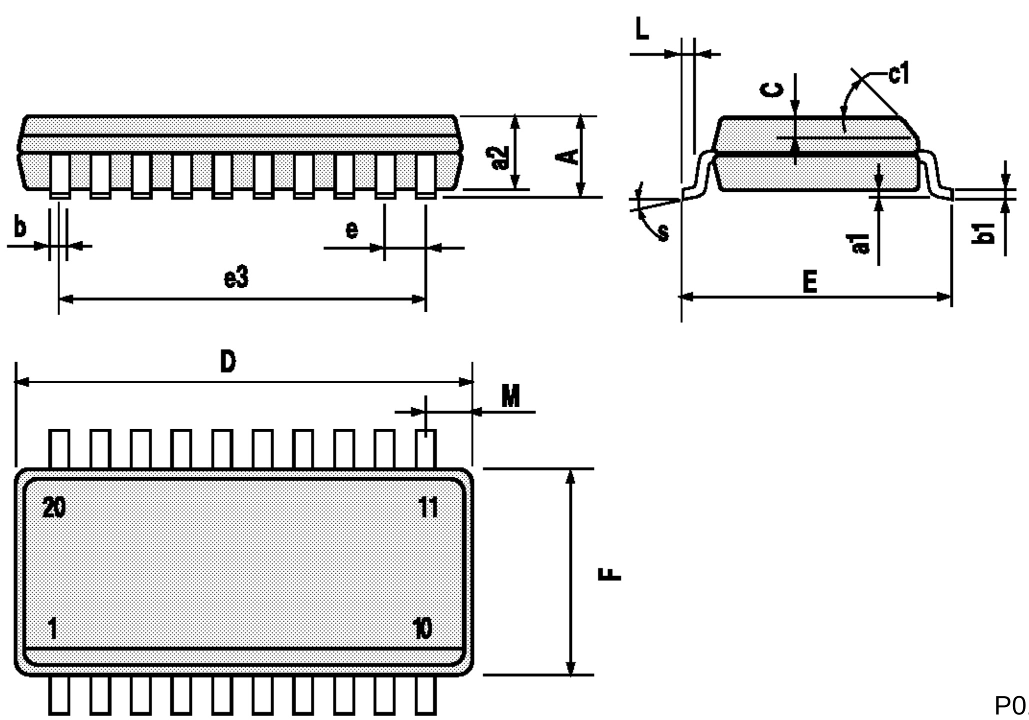
Ceramic DIP20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			25			0.984
B			7.8			0.307
D		3.3			0.130	
E	0.5		1.78	0.020		0.070
e3		22.86			0.900	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
I	1.27		1.52	0.050		0.060
L	0.22		0.31	0.009		0.012
M	0.51		1.27	0.020		0.050
N1	4° (min.), 15° (max.)					
P	7.9		8.13	0.311		0.320
Q			5.71			0.225



SO20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.20	0.004		0.007
a2			2.45			0.096
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45° (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.19		0.050
M			0.75			0.029
S	8° (max.)					



P013L

PLCC20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045