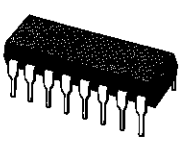
SGS-THOMSON MICROELECTRONICS

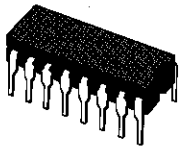
M54HCT165
M74HCT165

8 BIT PISO SHIFT REGISTER

- HIGH SPEED
  t_{PD} = 17 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- SYMMETRICAL OUTPUT IMPEDANCE
  $I_{OL} = |I_{OH}| = 4$ mA (MIN.)
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2 V (MIN.) V_{IL} = 0.8 V (MAX.)
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS165



B1R
(Plastic Package)



F1R
(Ceramic Package)

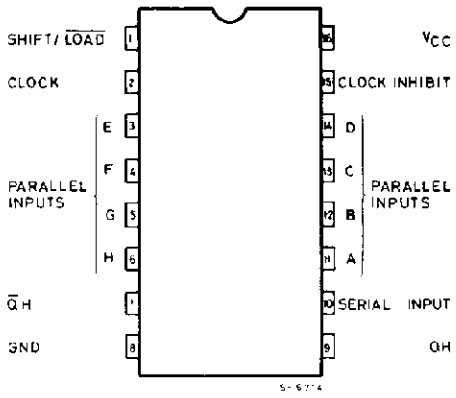
M1R
(Micro Package)

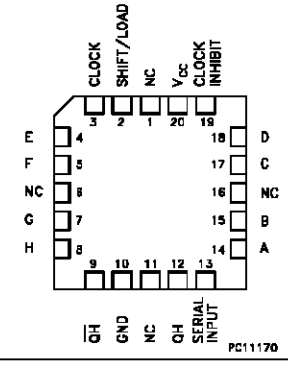
C1R
(Chip Carrier)

ORDER CODES :

M54HCT165F1R M74HCT165M1R
M74HCT165B1R M74HCT165C1R

PIN CONNECTIONS (top view)





NC =
No Internal
Connection

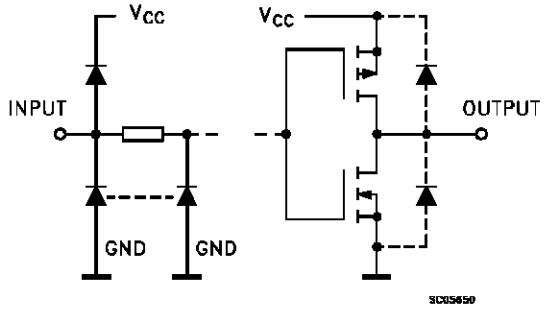
DESCRIPTION

The M54/74HCT165 is a high speed CMOS 8 BIT PISO SHIFT REGISTER fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. It achives the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

This device contains eight clocked master slave RS flip-flops connected as a shift register, with auxiliary gating to provide over-riding asynchronous parallel entry. Parallel data entrens when the shift/load input is low. The parallel data can change while shift/load is low, provided that the recommended set-up and hold times are observed. For clocked operation, shift/load must be high. The two clock input perform identically; one can be used as a clock inhibit by applying a high signal; to permit this operation clocking is accomplished through a 2 input nor gates.

To avoid double clocking, however, the inhibit signal should only go high while the clock is high. Otherwise the rising inhibit signal will cause the same response as rising clock edge.This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSCMOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT

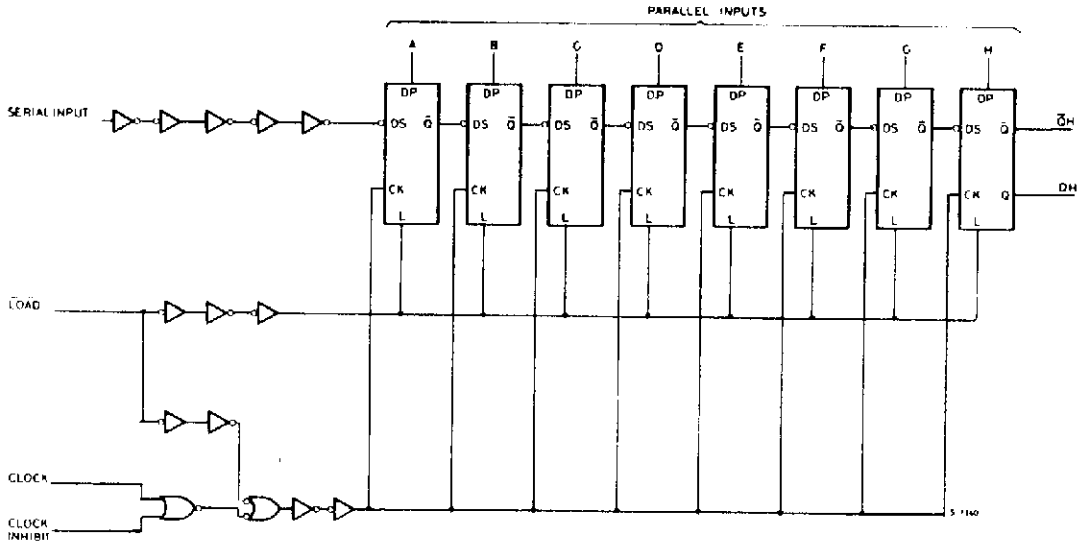


TRUTH TABLE

INPUTS					INTERNAL OUTPUTS		OUTPUS	OUTPUS
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL IN	A .....H	QA	QB	QH	$\overline{QH}$
L	X	X	X	a.....h	a	b	h	$\overline{h}$
H	L	⎍	H	X	H	QAn	QGn	$\overline{QGn}$
H	L	⎍	L	X	L	QAn	QGn	$\overline{QGn}$
H	⎍	L	H	X	H	QAn	QGn	$\overline{QGn}$
H	⎍	L	L	X	L	QAn	QGn	$\overline{QGn}$
H	X	H	X	X	NO CHANGE			
H	H	X	X	X	NO CHANGE			

a.....h: The level of steady input voltage at inputs A through H respectively
QAn - QGn : The level of QA -QG, respectively, before the most-recent transition of the clock.

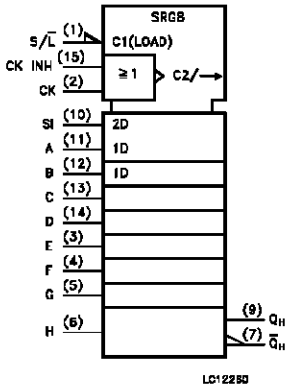
LOGIC DIAGRAM



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{S/L}$	Asynchronous Parallel Load Input
2	$\overline{QH}$	Complementary Output
7	QH	Serial Output
9	CLOCK	Clock Input (LOW to HIGH edge triggered)
10	SI	Serial Data Input
11, 12, 13, 14, 3, 4, 5, 6	A to H	Parallel Data Inputs
15	CLOCK INH	CLock Inhibit
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

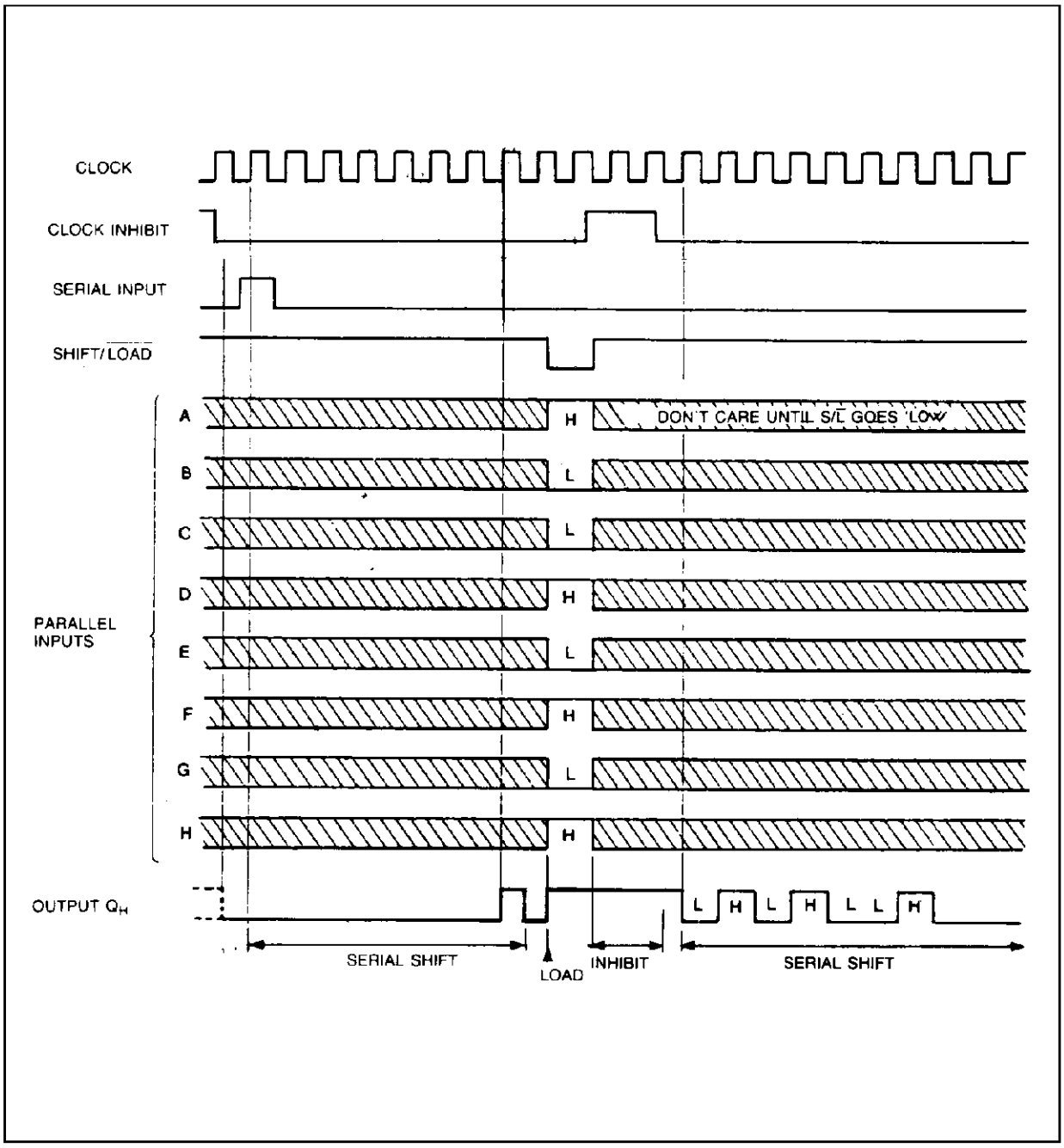
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-4.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 4.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				4		40		80	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND I_O= 0				2.0		2.9		3.0	mA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5			8	15		19		22	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CK - QH, $\overline{QH}$)	4.5			24	37		46		56	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CKINH - QH, $\overline{QH}$)	4.5			24	37		46		56	ns
t_{PLH} t_{PHL}	Propagation Delay Time (S/L - QH, $\overline{QH}$)	4.5			26	40		50		60	ns
t_{PLH} t_{PHL}	Propagation Delay Time (H - QH, $\overline{QH}$)	4.5			22	34		43		51	ns
f_{MAX}	Maximum Clock Frequency	4.5		30	46		24				MHz
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CK, CKINH)	4.5			8	15		19		22	ns
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width ($\overline{S/L}$)	4.5			8	15		19			ns
t_s	Minimum Set-up Time (PI - $\overline{S/L}$)	4.5			7	15		19		22	ns
t_s	Minimum Set-up Time (S/L -CK, CHINH)	4.5			7	15		19		22	ns
t_s	Minimum Set-up Time (S -CK, CHINH)	4.5			7	15		19		22	ns
t_h	Minimum Hold Time (PI - $\overline{S/L}$) (S/L -CK, CHINH)	4.5				0		0		0	ns
t_{REM}	Minimum Removal Time (CK - CKINH) (CKINH - CK)	4.5			5	15		19		22	ns
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				96						pF

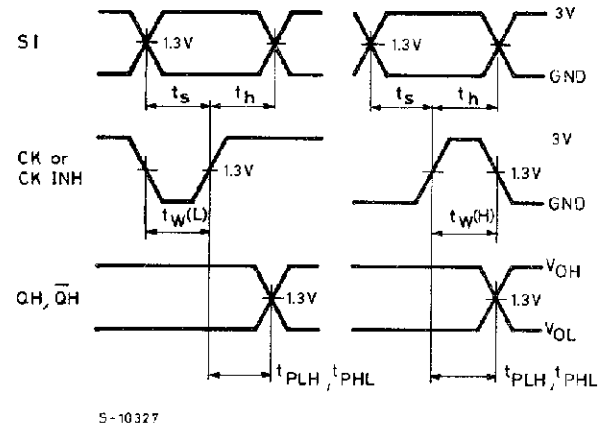
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}$

TIMING CHART

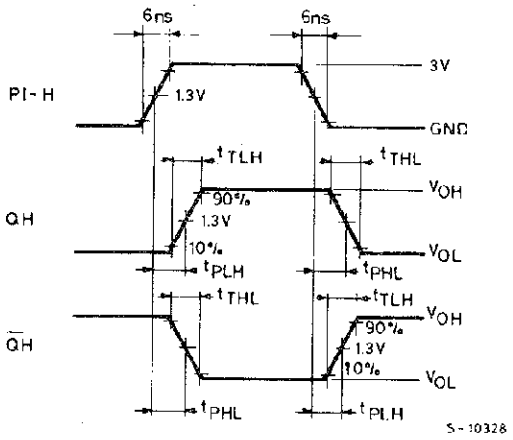


SWITCHING CHARACTERISTICS TEST WAVEFORM

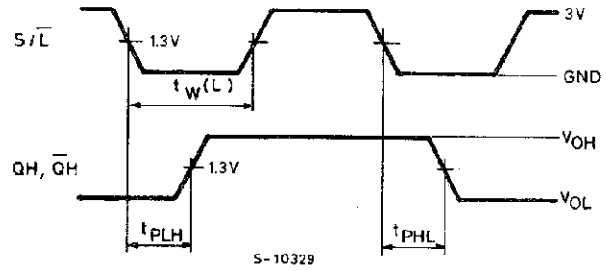
SERIAL MODE



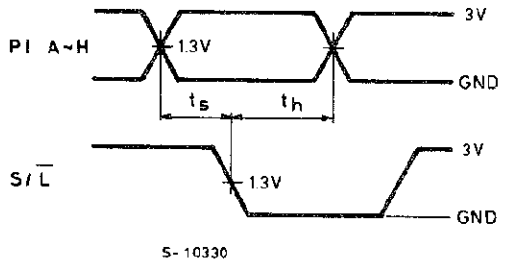
PARALLEL MODE



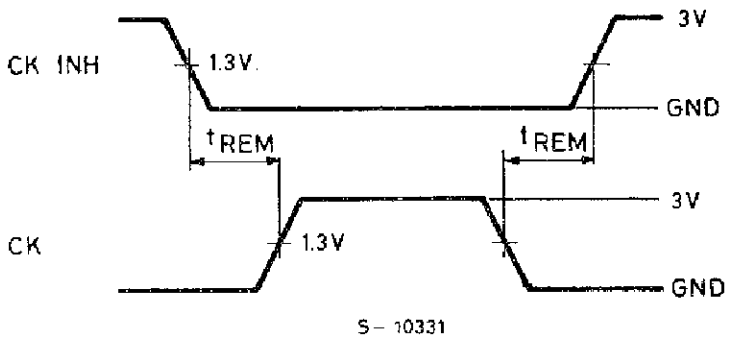
PARALLEL MODE



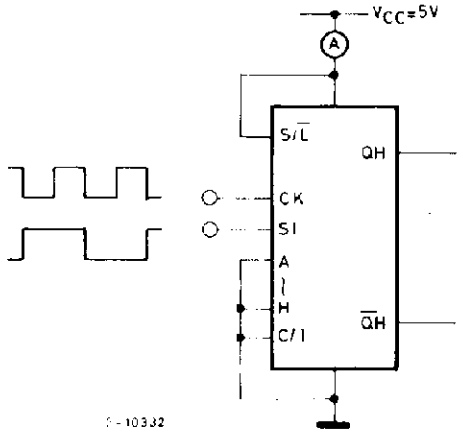
PARALLEL MODE



PARALLEL MODE



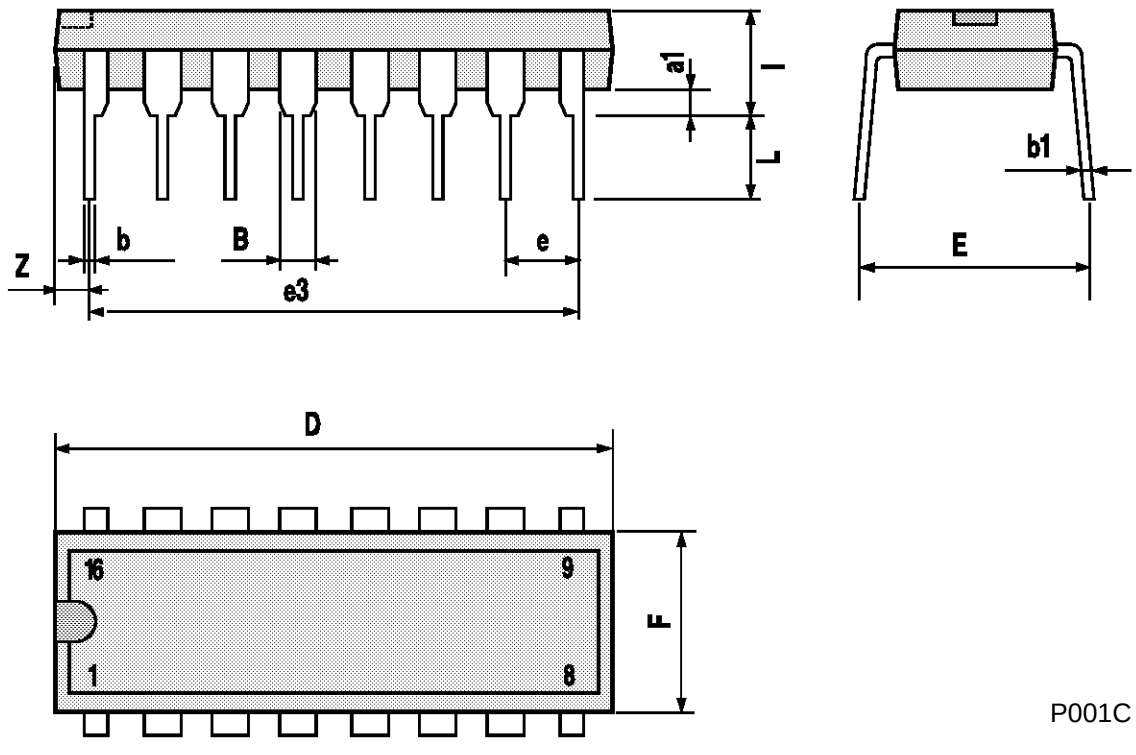
TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

Plastic DIP16 (0.25) MECHANICAL DATA

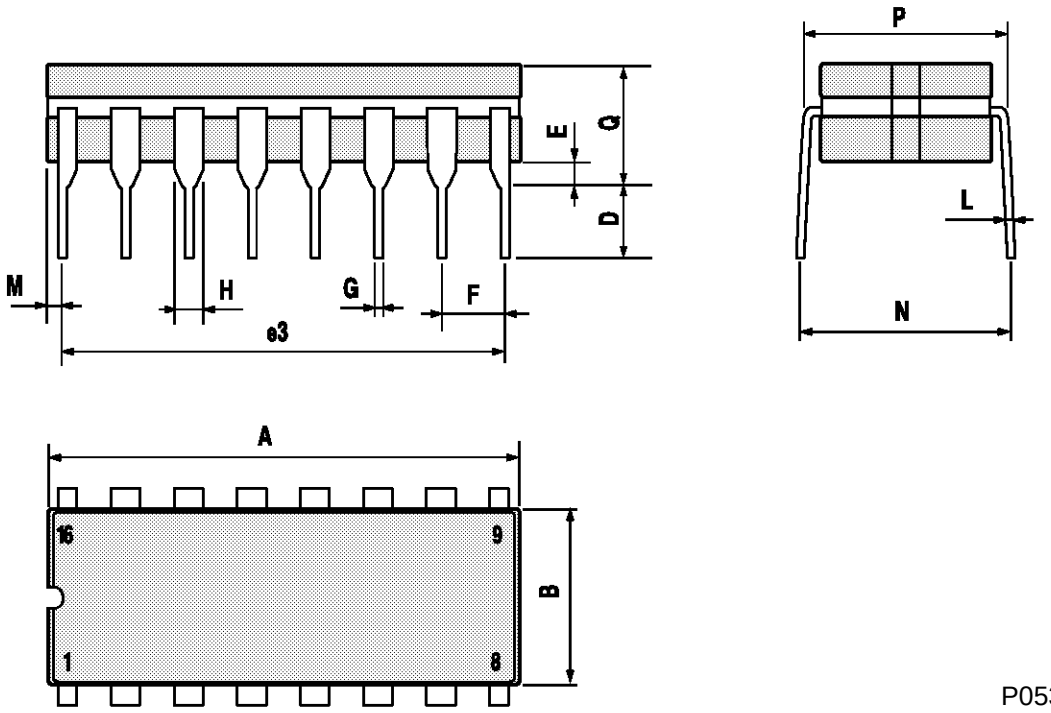
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

Ceramic DIP16/1 MECHANICAL DATA

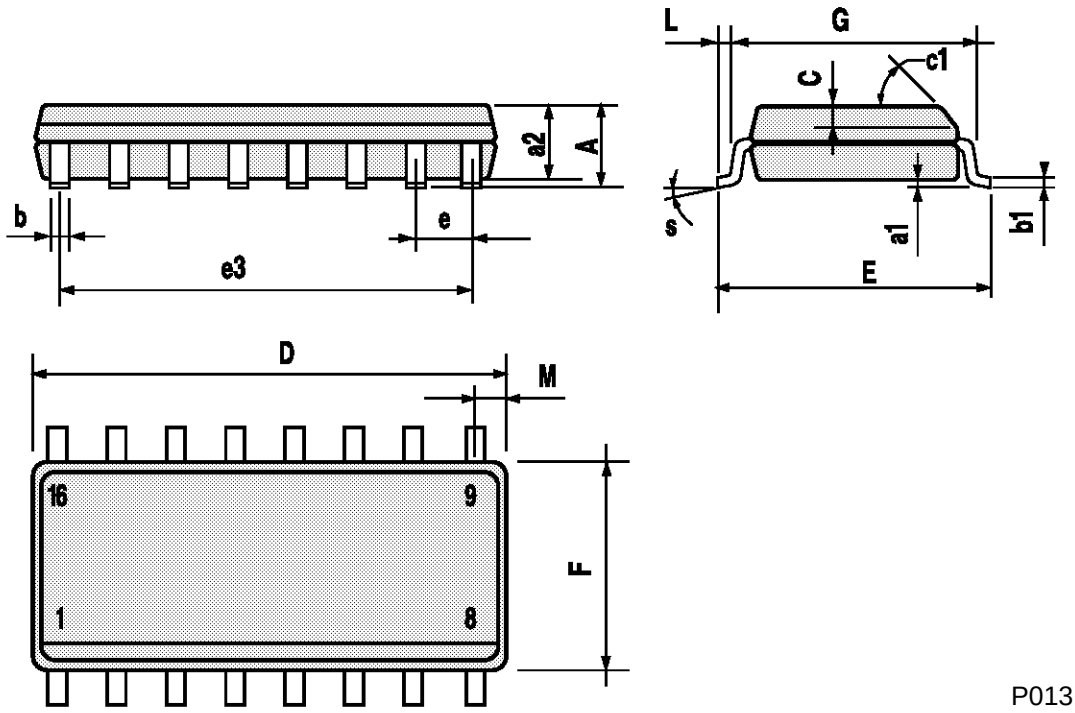
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			20			0.787
B			7			0.276
D		3.3			0.130	
E	0.38			0.015		
e3		17.78			0.700	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
H	1.17		1.52	0.046		0.060
L	0.22		0.31	0.009		0.012
M	0.51		1.27	0.020		0.050
N			10.3			0.406
P	7.8		8.05	0.307		0.317
Q			5.08			0.200



P053D

SO16 (Narrow) MECHANICAL DATA

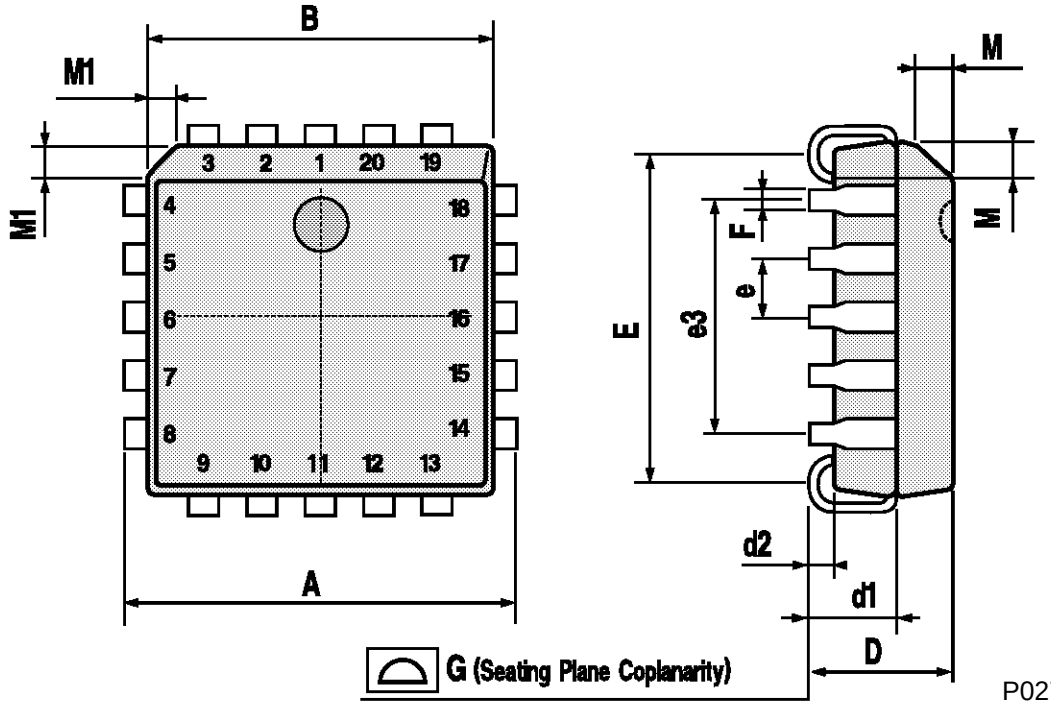
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



P013H

PLCC20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	



P027A