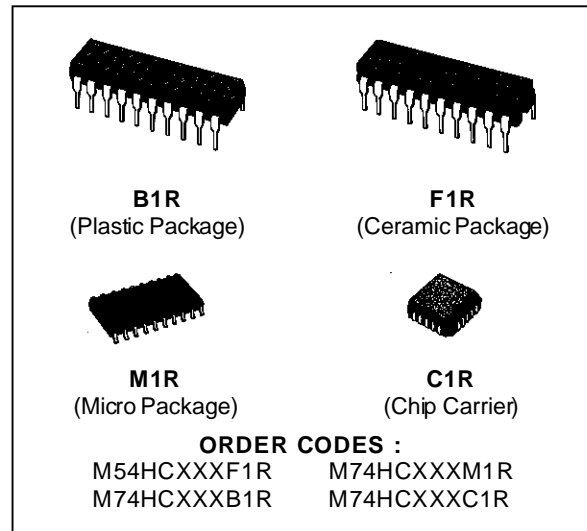


HC696/698 U/D DECADE COUNTER/REGISTER (3-STATE) HC697/699 U/D 4 BIT BINARY COUNTER/REGISTER (3-STATE)

- HIGH SPEED
f_{MAX} = 50 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
V_{NIH} = V_{NIL} = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
15 LSTTL LOADS (for Q_A to Q_D)
10 LSTTL LOADS (for RCO)
- SYMMETRICAL OUTPUT IMPEDANCE
|I_{OH}| = I_{OL} = 6 mA (MIN.) FOR Q_A TO Q_D
|I_{OH}| = I_{OL} = 4 mA (MIN.) FOR RCO OUTPUT
- BALANCED PROPAGATION DELAYS
t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
WITH LSTTL 54/74LS696/697/698/699



DESCRIPTION

The HC696/697 are high speed CMOS up/down counters fabricated with silicon gate C²MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. The HC696/698 are BCD DECADE COUNTER, and the HC697/699 are 4-BIT BINARY COUNTER. Both devices have register.

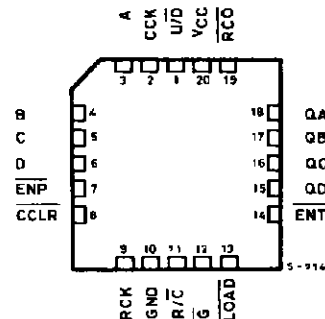
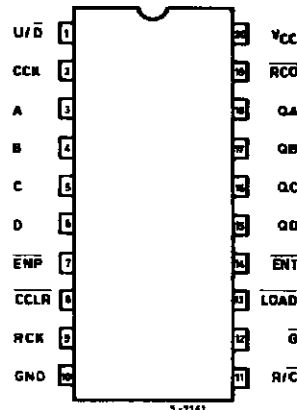
They count on the positive edge of the counter clock input (CCK) when selected by the "Counter Mode". If the input U/D is held "H", the internal counter counts up, and held "L", counts down. The internal counter's outputs are stored in the output register at the positive edge of register clock (RCK).

The counter features enable P and enable T and a ripple-carry output for easy expansion. the register/counter select input, R/C, selects the counter when low or the register when high for the three state outputs, Q_A, Q_B, Q_C and Q_D.

Both the counter clock CCK and register clock RCK are positive-edge triggered. The counter clear CCLR is active low and is synchronous for HC698/699, and asynchronous for HC696/697.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTIONS (top view)

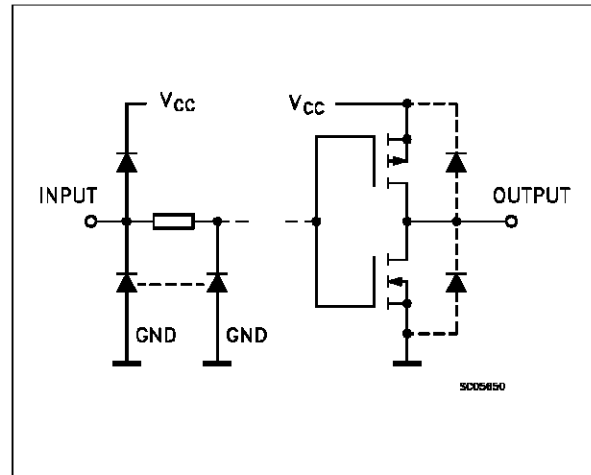


NC =
No Internal
Connection

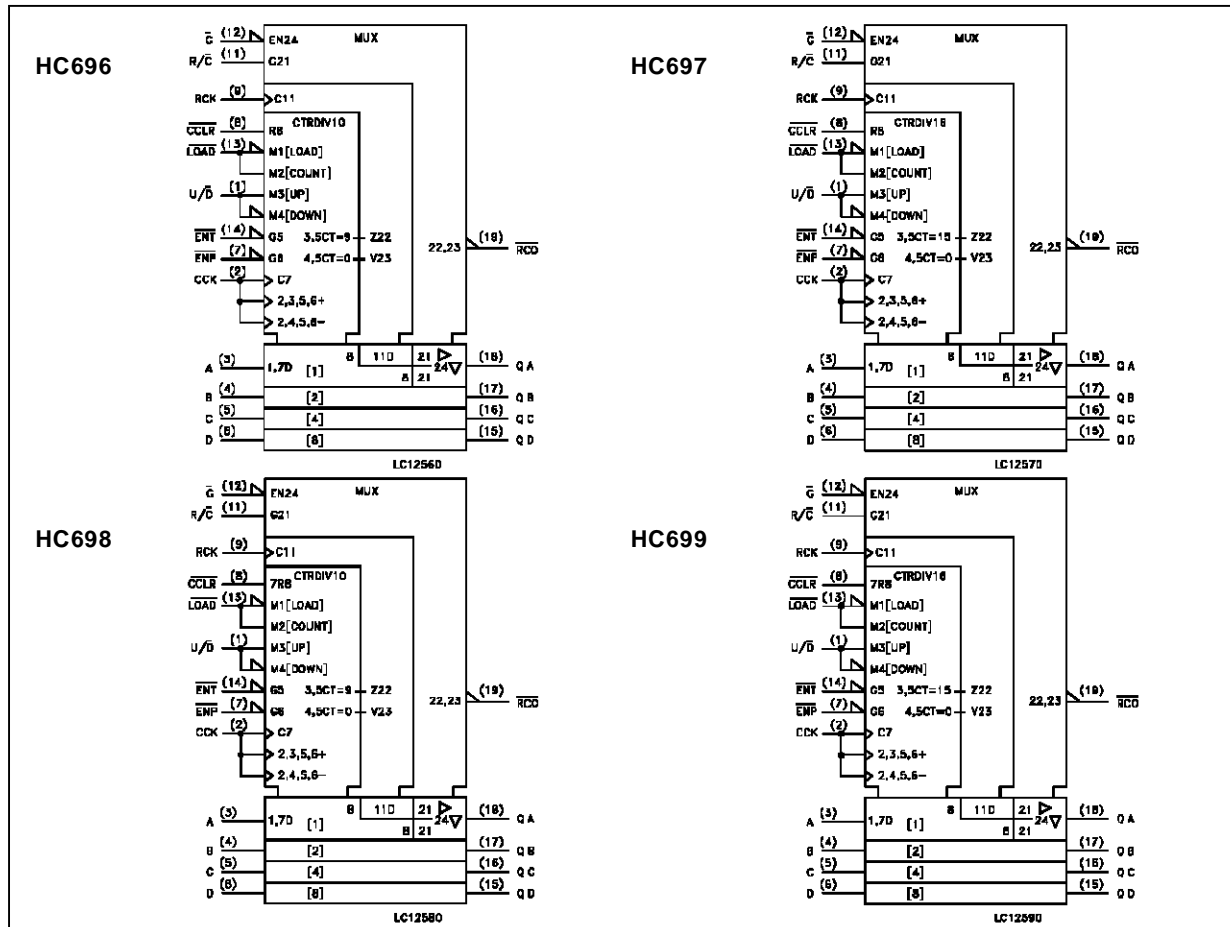
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	U/D	Up Down Counter Selector
2	CCK	Counter Clock
3, 4, 5, 6	A to D	Data Inputs
7, 14	EMP/ENT	Enable \bar{P} and \bar{T}
8	CCLR	Counter Clear (Active LOW)
9	RCK	Register Clock
11	R/C	Register Counter Selector
12	\bar{G}	Enable Input
13	LOAD	Load Counter (Active LOW)
15, 16, 17, 18	QA to QD	Data Outputs
19	RCO	Load Counter (Active HIGH)
10	GND	Ground (0V)
20	V _{CC}	Positive Supply Voltage

INPUT AND OUTPUT EQUIVALENT CIRCUIT



IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS									OUTPUTS				FUNCTION
CCLR	LOAD	ENP	ENT	CCK	U/D	RCK	R/C	G	QA	QB	QC	QD	
X	X	X	X	X	X	X	X	H	Z	Z	Z	Z	HIGH IMPEDANCE
L	X	X	X	X (*)	X	X	L	L	L	L	L	L	CLEAR COUNTER
H	L	X	X		X	X	L	L	a	b	c	d	LOAD COUNTER
H	H	H	X		X	X	L	L	NO CHANGE			NO COUNT	
H	H	X	H		X	X	L	L	NO CHANGE			NO COUNT	
H	H	L	L		H	X	L	L	COUNT UP			COUNT UP	
H	H	L	L		L	X	L	L	COUNT DOWN			COUNT DOWN	
H	X	X	X		X	X	L	L	NO CHANGE			NO COUNT	
X	X	X	X	X	X		H	L	a'	b'	c'	d'	LOAD REGISTER
X	X	X	X	X	X		H	L	NO CHANGE			NO LOAD	

(*) : For HC698/699

X : Don't care

Z : High impedance

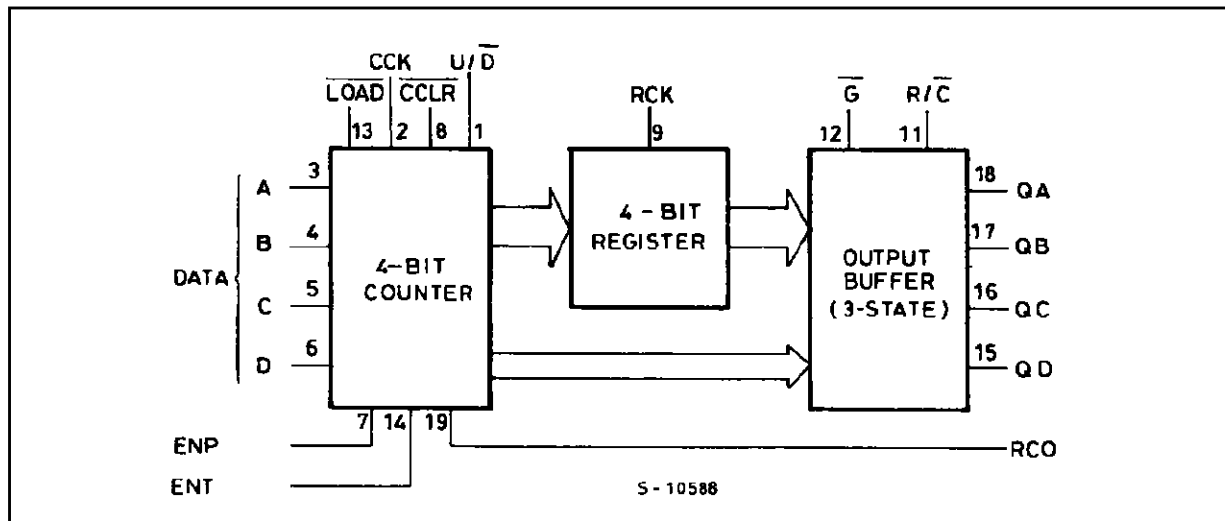
a-d : The level of steady state input at inputs a through D respectively

a'-d' : The level of steady state outputs at internal counter outputs QA' through QD' respectively

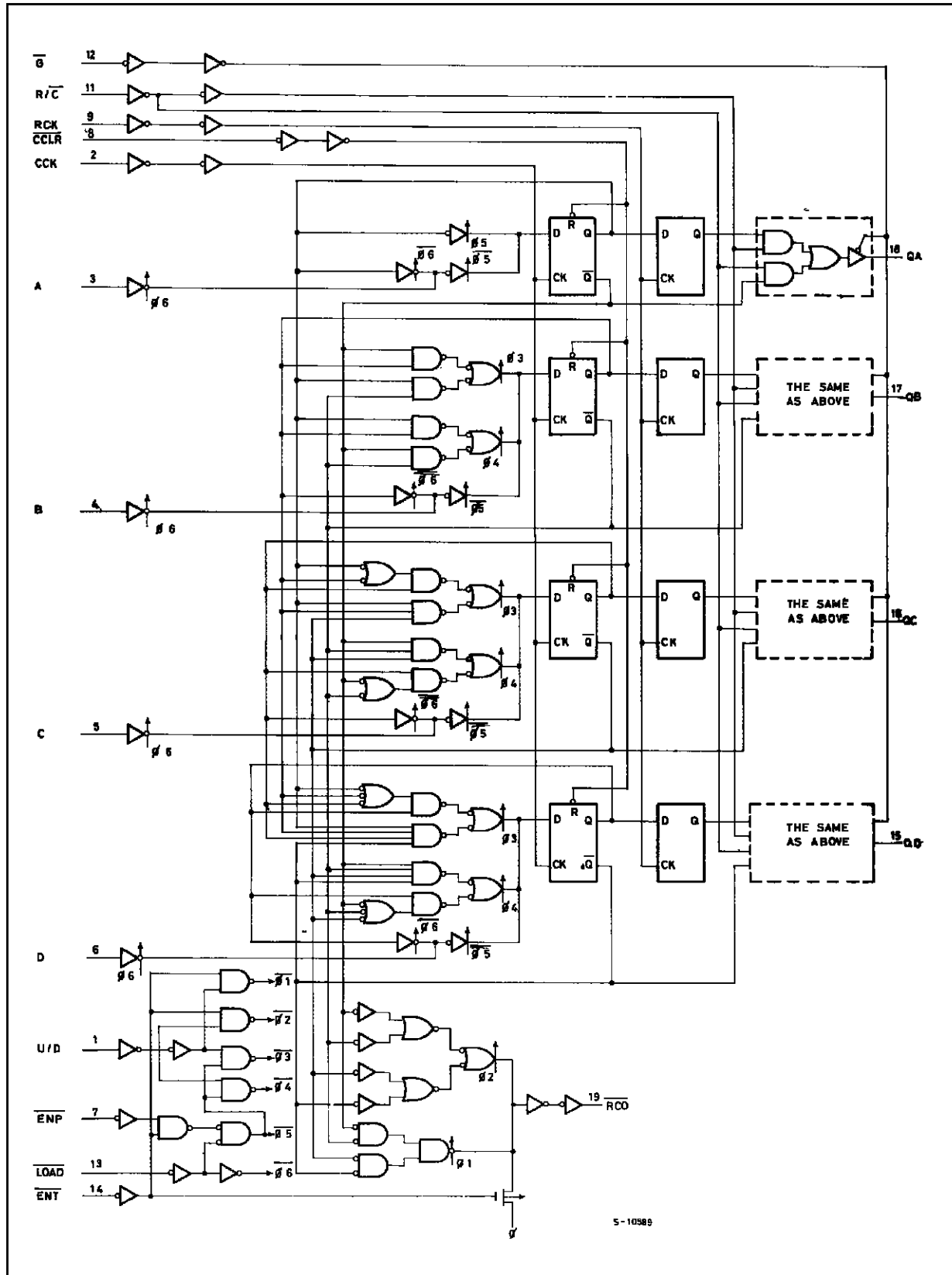
RCO function : HC696/8 - $\overline{RCO} = (\overline{UP} \cdot QA \cdot QD \cdot ENT + \overline{UP} \cdot \overline{QA} \cdot \overline{QD} \cdot ENT)$

HC697/9 - $\overline{RCO} = (\overline{UP} \cdot QA \cdot QB \cdot QC \cdot QD \cdot ENT + \overline{UP} \cdot \overline{QA} \cdot \overline{QB} \cdot \overline{QC} \cdot \overline{QD} \cdot ENT)$

BLOCK DIAGRAM

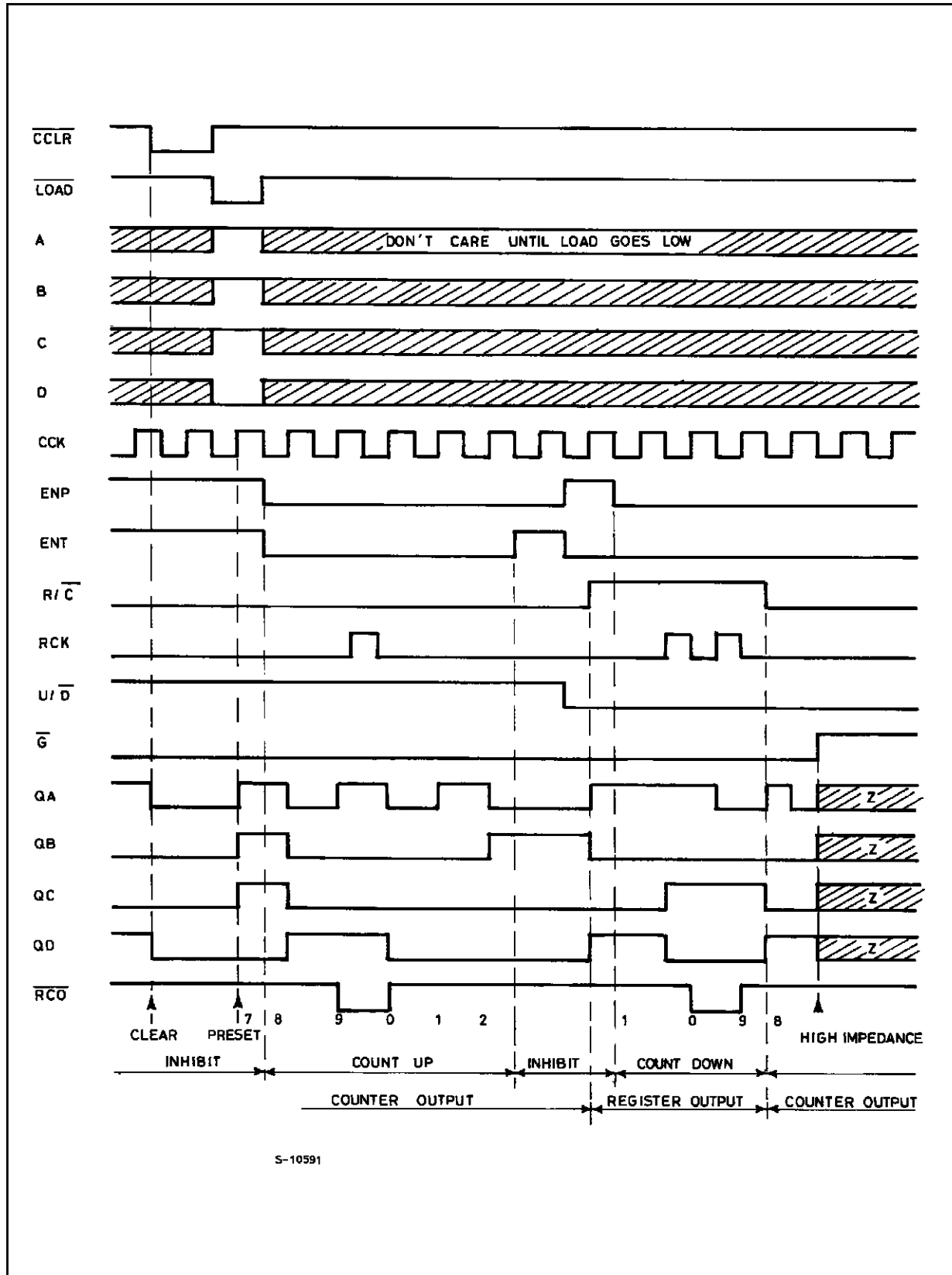


LOGIC DIAGRAM (HC696)

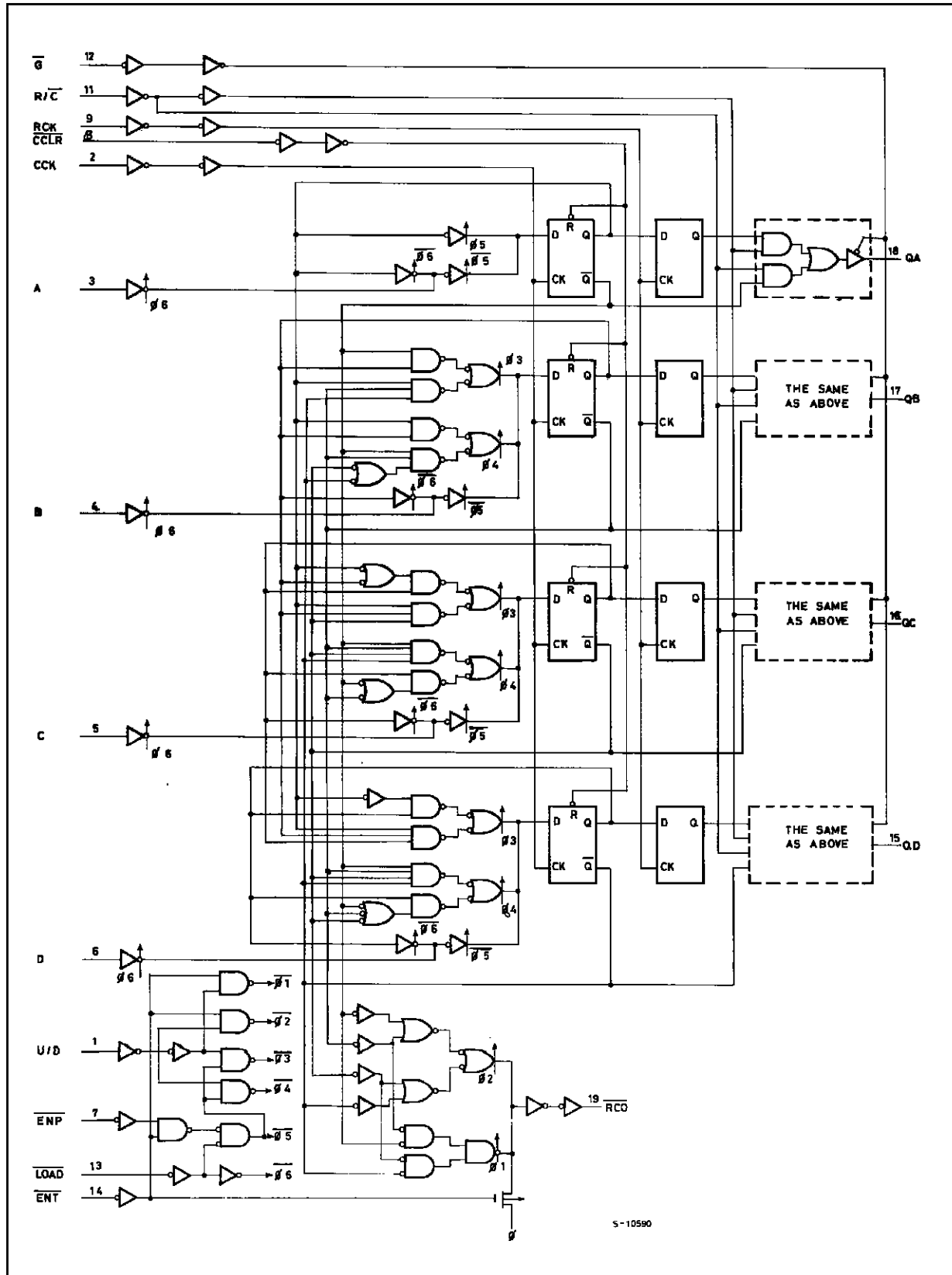


5-10989

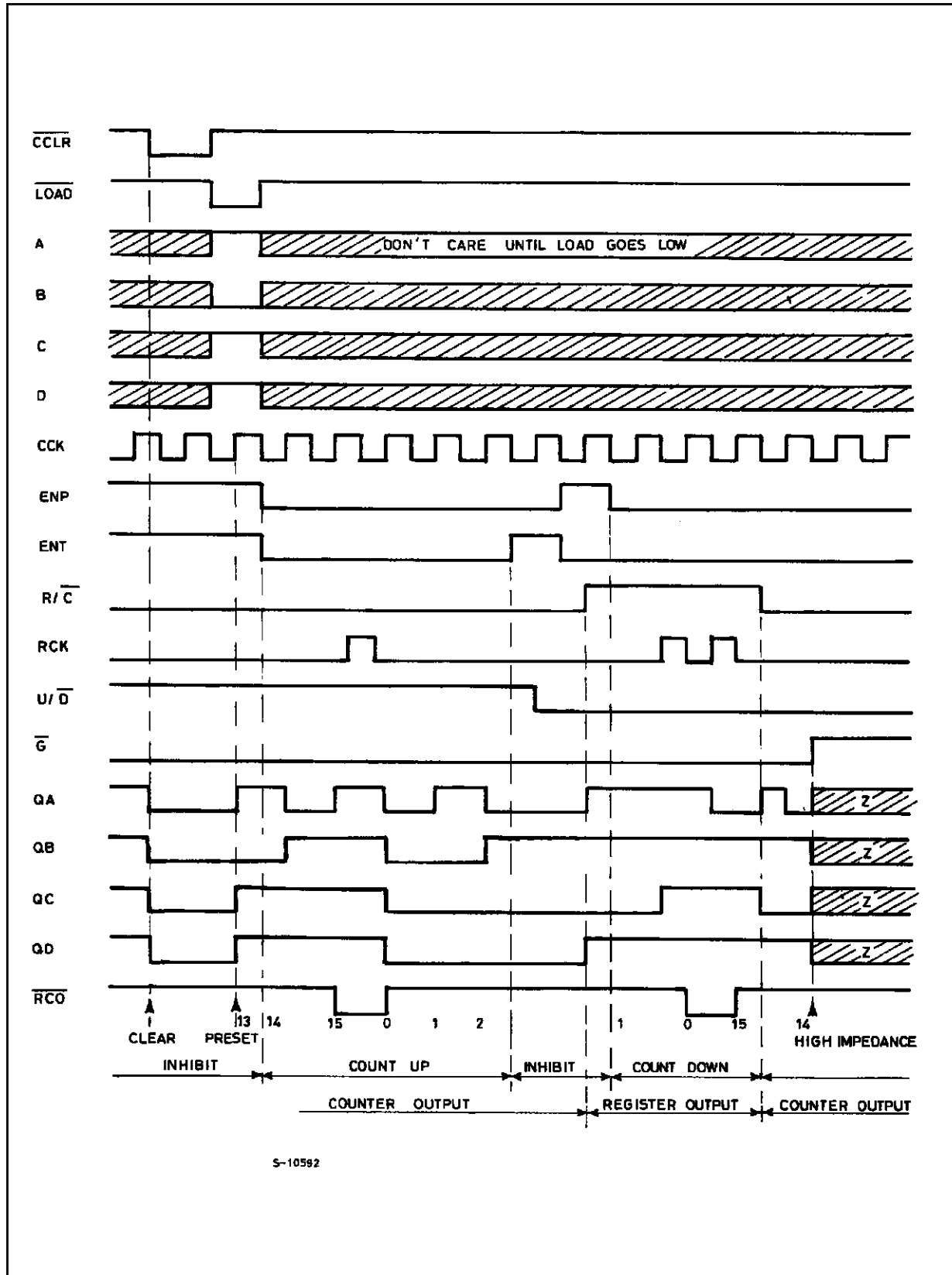
TIMING CHART (HC696)



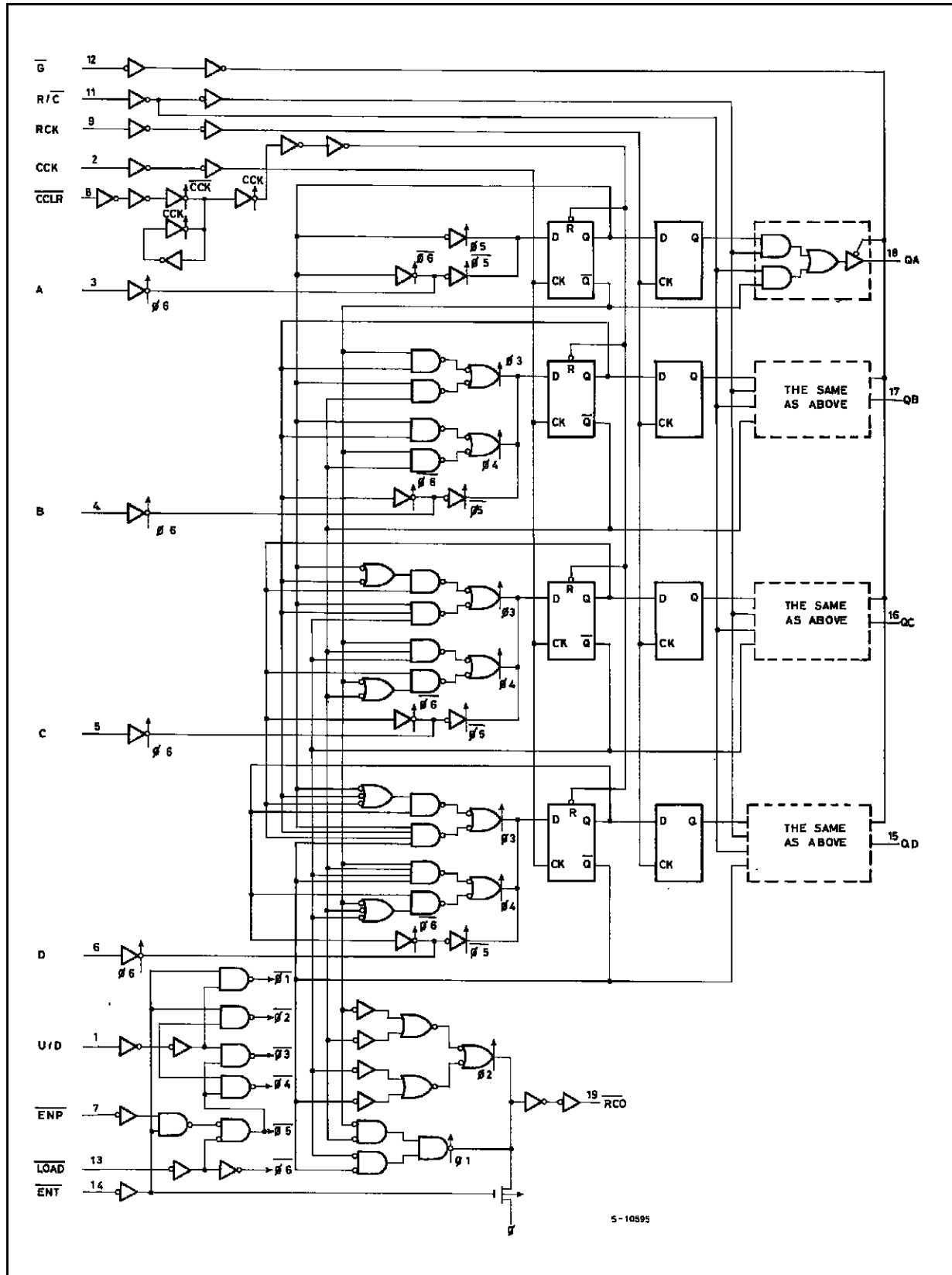
LOGIC DIAGRAM (HC697)



TIMING CHART (HC697)

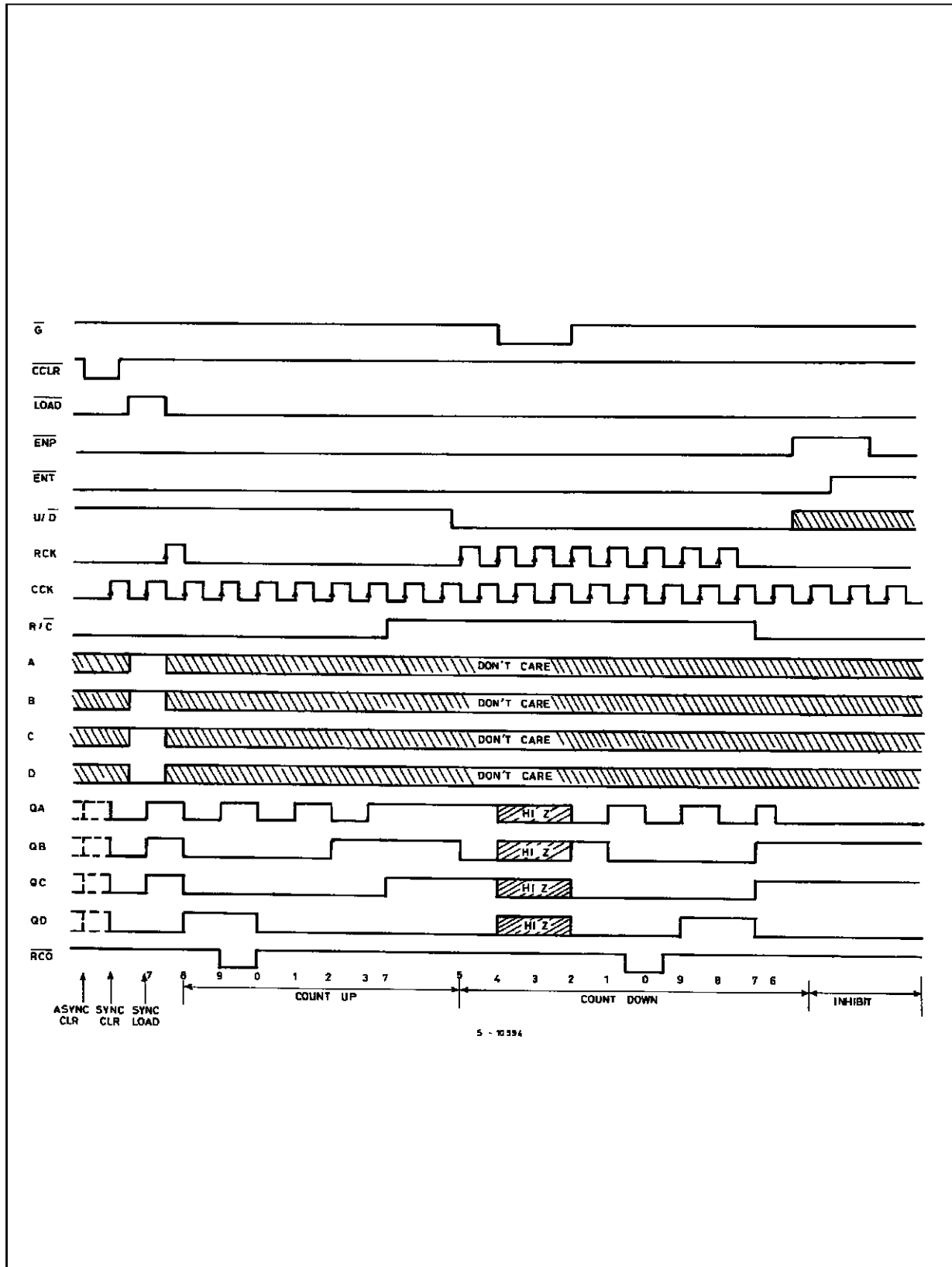


LOGIC DIAGRAM (HC698)

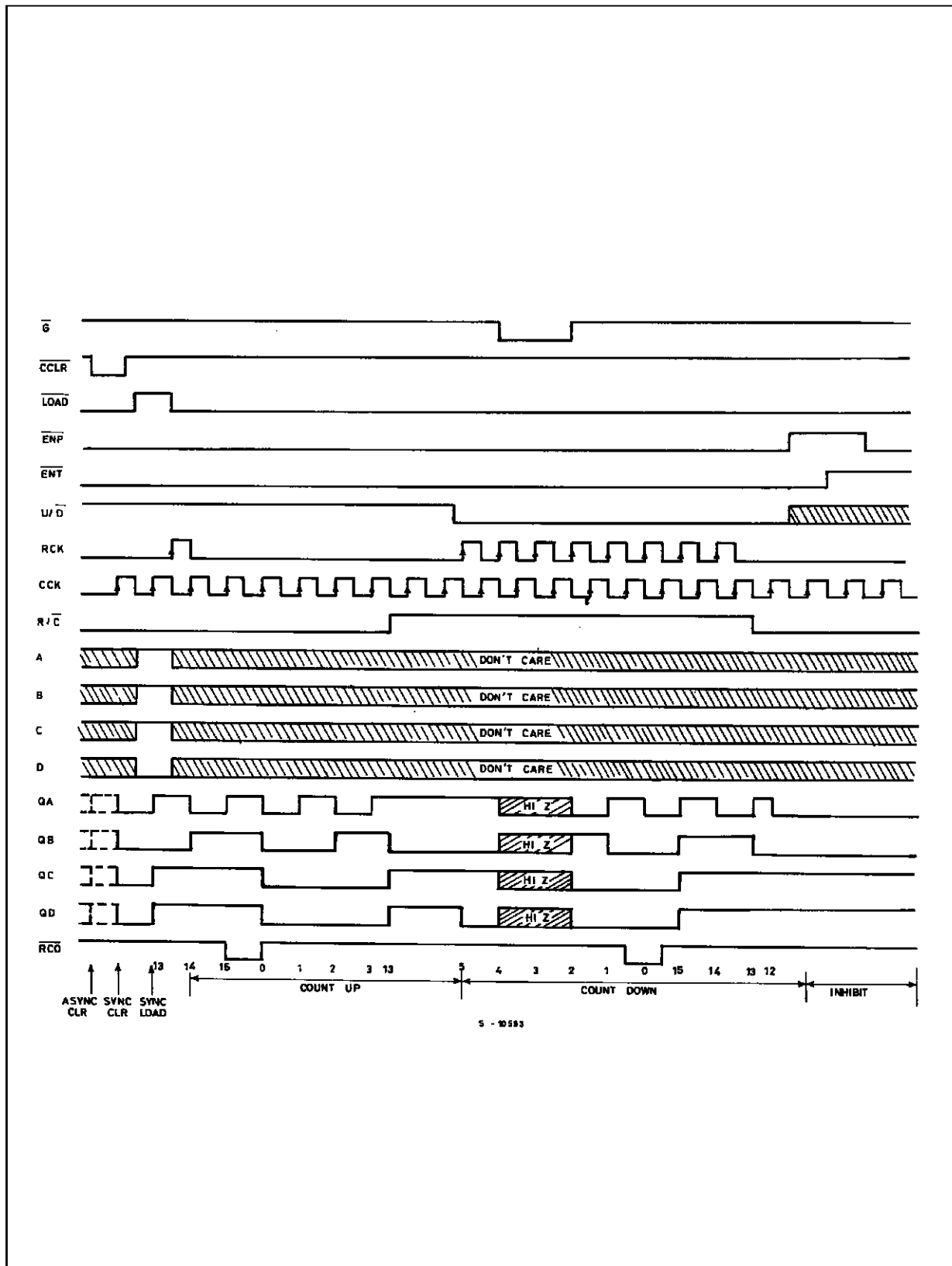


5-10595

DECADE COUNTER, SYNCHRONOUS CLEAR (HC698)



BINARY COUNTER, SYNCHRONOUS CLEAR (HC699)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to +7	V
V _I	DC Input Voltage	-0.5 to V _{CC} + 0.5	V
V _O	DC Output Voltage	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	± 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Source Sink Current Per Output Pin (RCO) (QA to QD)	± 25 ± 35	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 70	mA
P _D	Power Dissipation	500 (*)	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
 (*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit	
V _{CC}	Supply Voltage	2 to 6	V	
V _I	Input Voltage	0 to V _{CC}	V	
V _O	Output Voltage	0 to V _{CC}	V	
T _{op}	Operating Temperature:	M54HC Series M74HC Series	-55 to +125 -40 to +85	°C °C
t _r , t _f	Input Rise and Fall Time	V _{CC} = 2 V V _{CC} = 4.5 V V _{CC} = 6 V	0 to 1000 0 to 500 0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions		Value						Unit		
		V _{CC} (V)		T _A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC			
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.	
V _{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V	
		4.5		3.15			3.15		3.15			
		6.0		4.2			4.2		4.2			
V _{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V	
		4.5				1.35		1.35		1.35		
		6.0				1.8		1.8		1.8		
V _{OH}	High Level Output Voltage (RCO)	2.0	V _I = V _{IH} or V _{IL}	I _O = -20 μA	1.9	2.0		1.9		1.9	V	
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I _O = -4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I _O = -5.2 mA	5.68	5.8		5.63		5.60		
V _{OH}	High Level Output Voltage (QA - QD)	2.0	V _I = V _{IH} or V _{IL}	I _O = -20 μA	1.9	2.0		1.9		1.9	V	
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I _O = -6.0 mA	4.18	4.31		4.13		4.10		
		6.0		I _O = -7.8 mA	5.68	5.8		5.63		5.60		
V _{OL}	Low Level Output Voltage (RCO)	2.0	V _I = V _{IH} or V _{IL}	I _O = 20 μA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I _O = 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I _O = 5.2 mA		0.18	0.26		0.33		0.40	
V _{OL}	Low Level Output Voltage (QA - QD)	2.0	V _I = V _{IH} or V _{IL}	I _O = 20 μA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I _O = 6.0 mA		0.17	0.26		0.33		0.40	
		6.0		I _O = 7.8 mA		0.18	0.26		0.33		0.40	
I _I	Input Leakage Current	6.0	V _I = V _{CC} or GND			±0.1		±1		±1	μA	
I _{OZ}	3 State Output Off State Current	6.0	V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND			±0.5		±5		±10	μA	
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND			4		40		80	μA	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6$ ns)

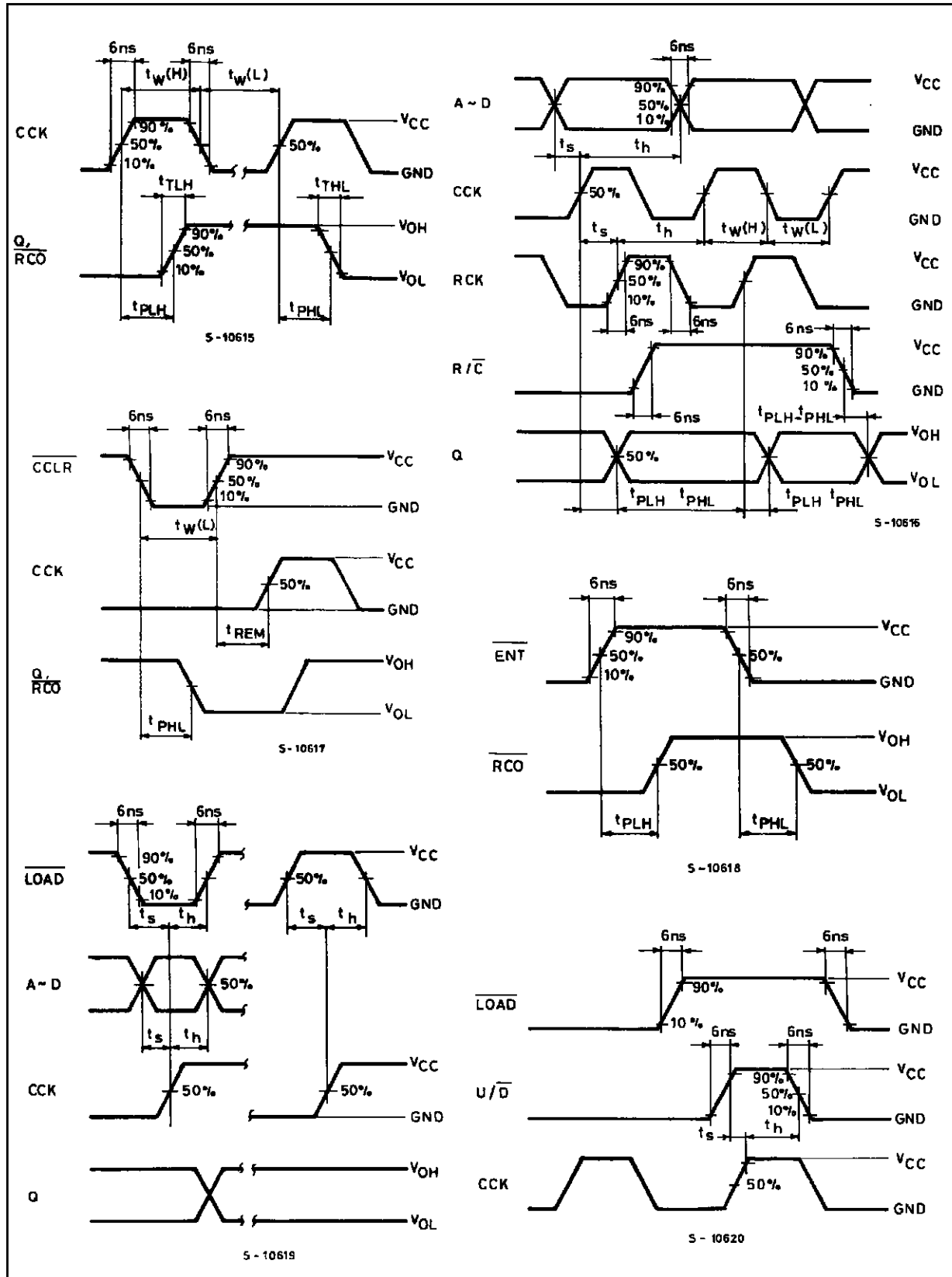
Symbol	Parameter	Test Conditions			Value						Unit	
		V _{CC} (V)	C _L (pF)		T _A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t _{TLH} t _{THL}	Output Transition Time (Qn)	2.0	50		25	60		75		90	ns	
		4.5		7	12		19		18			
		6.0		6	10		13		15			
t _{TLH} t _{THL}	Output Transition Time (RCO)	2.0	50		30	75		95		115	ns	
		4.5		8	15		19		23			
		6.0		7	13		16		20			
t _{PLH} t _{PHL}	Propagation Delay Time (CCK - Q)	2.0	50		90	215		270		325	ns	
		4.5		28	43		54		65			
		6.0		24	37		46		55			
		2.0	150		103	245		305		370	ns	
		4.5		32	49		61		74			
		6.0		27	42		52		63			
t _{PLH} t _{PHL}	Propagation Delay Time (RCK - Q)	2.0	50		82	185		230		280	ns	
		4.5		24	37		46		56			
		6.0		20	31		39		48			
		2.0	150		95	215		270		325	ns	
		4.5		28	43		54		65			
		6.0		24	37		46		55			
t _{PLH} t _{PHL}	Propagation Delay Time (CCK - RCO)	2.0	50		109	245		305		370	ns	
		4.5		32	49		61		74			
		6.0		27	42		52		63			
		2.0	150		61	155		195		235	ns	
		4.5		20	31		39		47			
		6.0		17	26		33		40			
2.0	150		73	185		230		280	ns			
4.5		24	37		46		56					
6.0		20	31		39		48					
t _{PLH} t _{PHL}	Propagation Delay Time (ENT - RCO)	2.0	50		63	140		175		210	ns	
		4.5		18	28		35		42			
		6.0		15	24		30		36			
t _{PLH} t _{PHL}	Propagation Delay Time (CCLR - Q)	2.0	50	for HC696 HC697	78	195		245		295	ns	
		4.5			26	39		49		59		
		6.0			22	33		42		50		
		2.0	150		90	235		295		355	ns	
		4.5			30	47		59		71		
		6.0			26	40		50		60		
t _{PLH} t _{PHL}	Propagation Delay Time (CCLR - RCO)	2.0	50	for HC696 HC697	98	220		275		330	ns	
		4.5			29	44		55		66		
		6.0			25	37		47		56		
f _{MAX}	Maximum Clock Frequency	2.0	50		5	12		4		3.4	MHz	
		4.5		25	45		20		17			
		6.0		30	53		24		20			

AC ELECTRICAL CHARACTERISTICS (Continued)

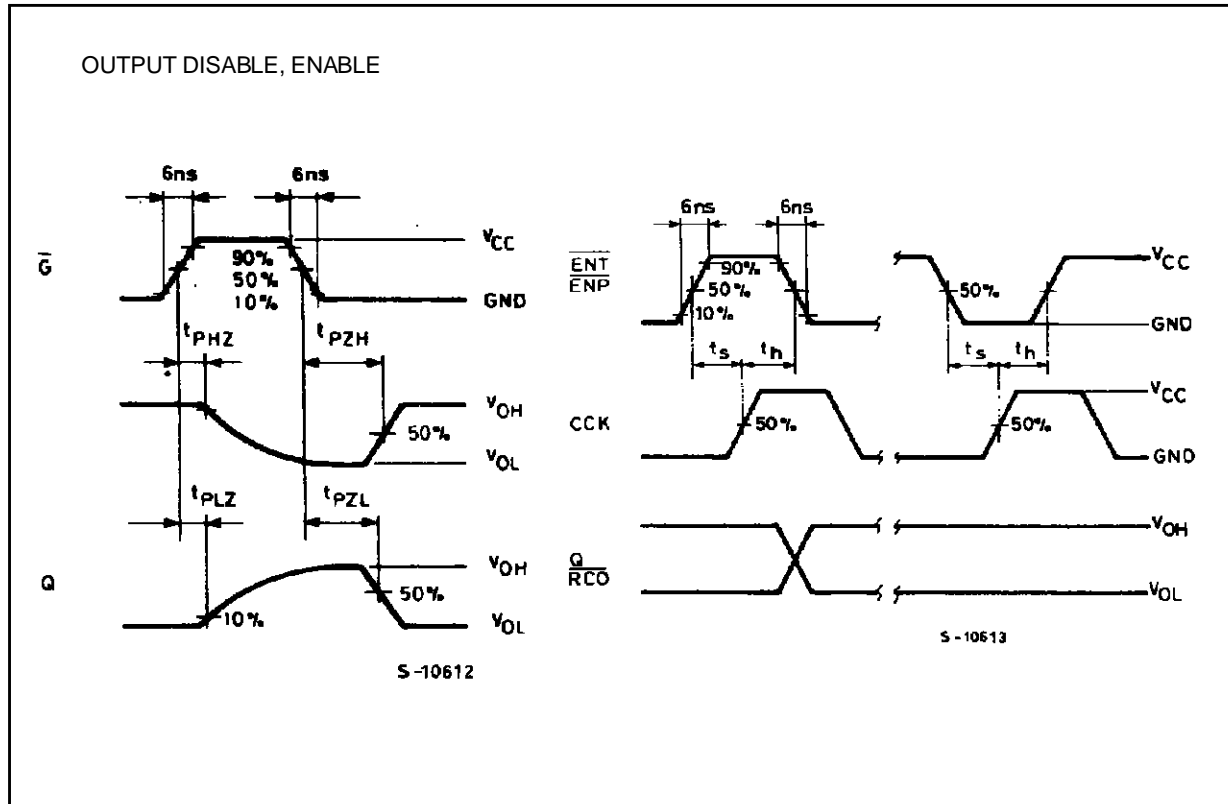
Symbol	Parameter	Test Conditions			Value						Unit		
		V _{CC} (V)	C _L (pF)		T _A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC			
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.	
t _{PZL} t _{PZH}	Output Enable Time	2.0	50	R _L = 1KΩ		45	120		150		180	ns	
		4.5				15	24		30		36		
		6.0				13	20		26		31		
		2.0	150	R _L = 1KΩ		57	150		190		225	ns	
		4.5				19	30		38		45		
		6.0				16	26		32		38		
t _{PLZ} t _{PHZ}	Output Disable Time	2.0	50	R _L = 1KΩ		32	115		145		175	ns	
		4.5				17	23		29		35		
		6.0				14	20		25		30		
t _{W(H)} t _{W(L)}	Minimum Pulse Width (CCK, RCK)	2.0	50			40	75		95		110	ns	
		4.5				8	15		19		22		
		6.0				7	13		16		19		
t _{W(L)}	Minimum Pulse Width (CCLR)	2.0	50	for HC696 HC697		40	75		95		110	ns	
		4.5				8	15		19		22		
		6.0				7	13		16		19		
t _s	Minimum Set-up Time (CCLR)	2.0	50	for HC698 HC699		16	50		65		75	ns	
		4.5				4	10		13		15		
		6.0				3	9		11		13		
t _s	Minimum Set-up Time (LOAD, ENT, ENP)	2.0	50			64	150		190		220	ns	
		4.5				16	30		38		44		
		6.0				14	26		32		37		
t _s	Minimum Set-up Time (A, B, C, D)	2.0	50			16	50		65		75	ns	
		4.5				4	10		13		15		
		6.0				3	9		11		13		
t _s	Minimum Set-up Time (CCK, RCK)	2.0	50			44	100		125		150	ns	
		4.5				11	20		25		30		
		6.0				9	17		21		26		
t _s	Minimum Set-up Time (U/D)	2.0	50			44	100		125		145	ns	
		4.5				11	20		25		29		
		6.0				9	17		21		25		
t _h	Minimum Hold Time	2.0	50				5		5		5	ns	
		4.5					5		5		5		
		6.0					5		5		5		
t _{REM}	Minimum Removal Time	2.0	50	for HC696 HC697			5		5		5	ns	
		4.5					5		5		5		
		6.0					5		5		5		
C _{IN}	Input Capacitance					5	10		10		10	pF	
C _{PD} (*)	Power Dissipation Capacitance			HC696/697/699 HC698		71 77							pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. I_{CC(opr)} = C_{PD} • V_{CC} • f_{IN} + I_{CC}/2 (per circuit)

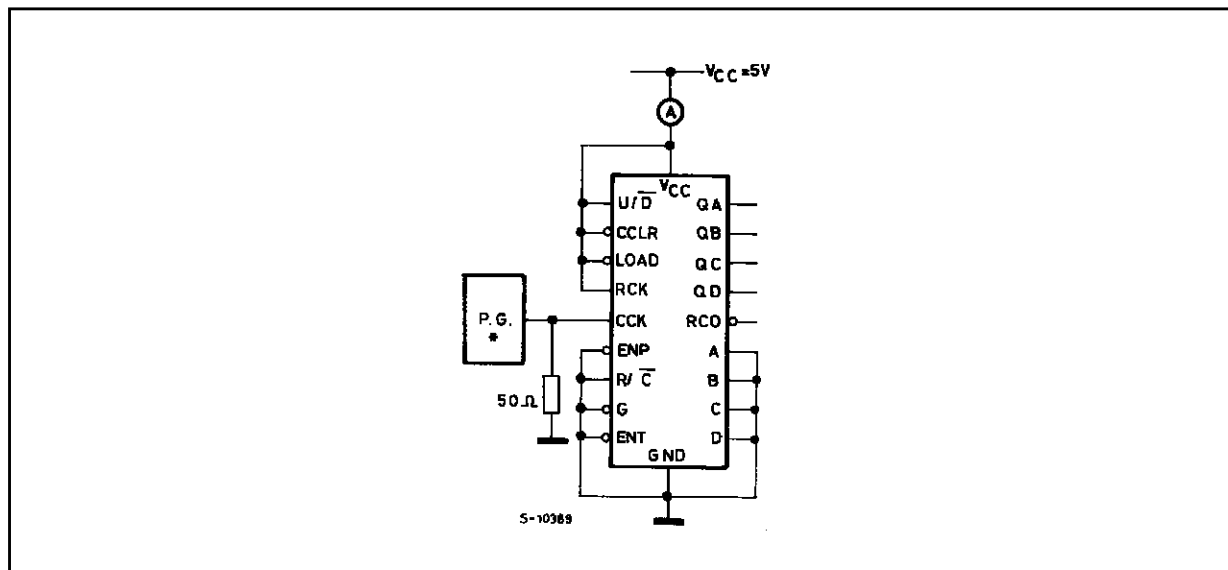
SWITCHING CHARACTERISTICS TEST WAVEFORM (HC696/697)



SWITCHING CHARACTERISTICS TEST WAVEFORM (continued)

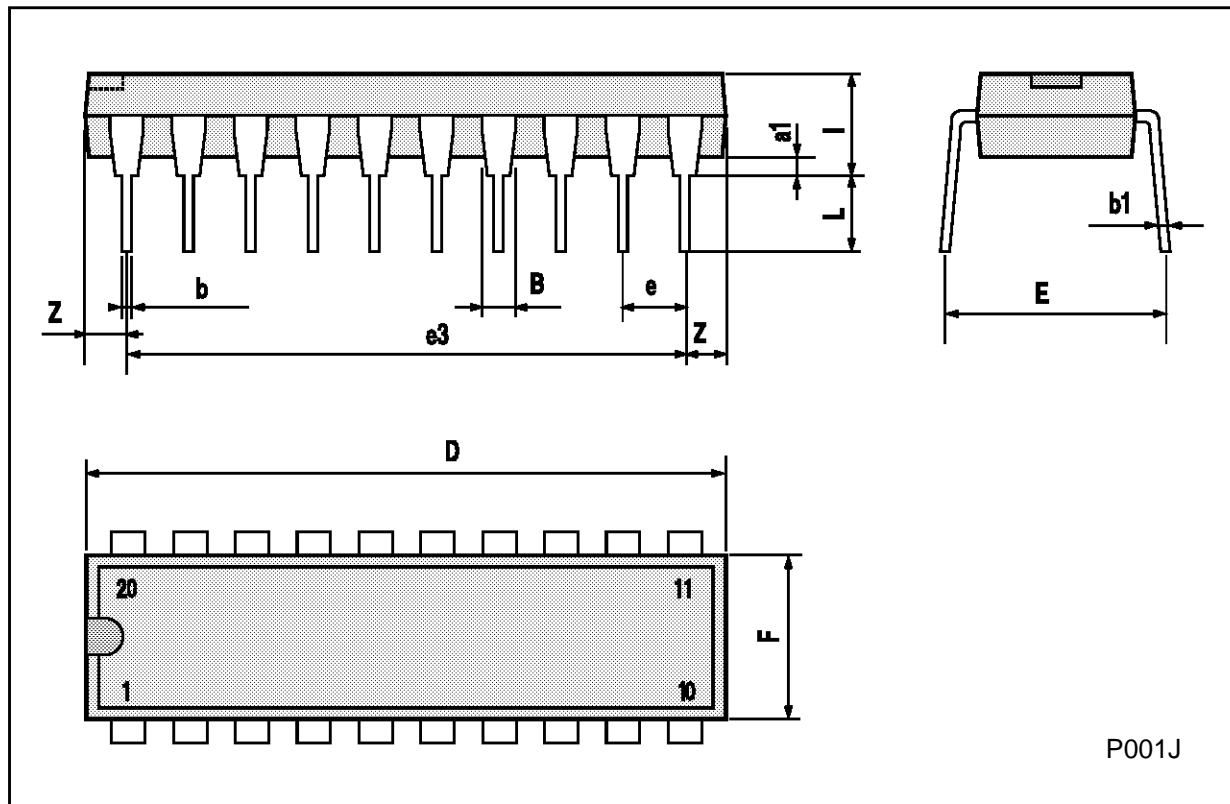


TEST CIRCUIT I_{CC} (Opr.)



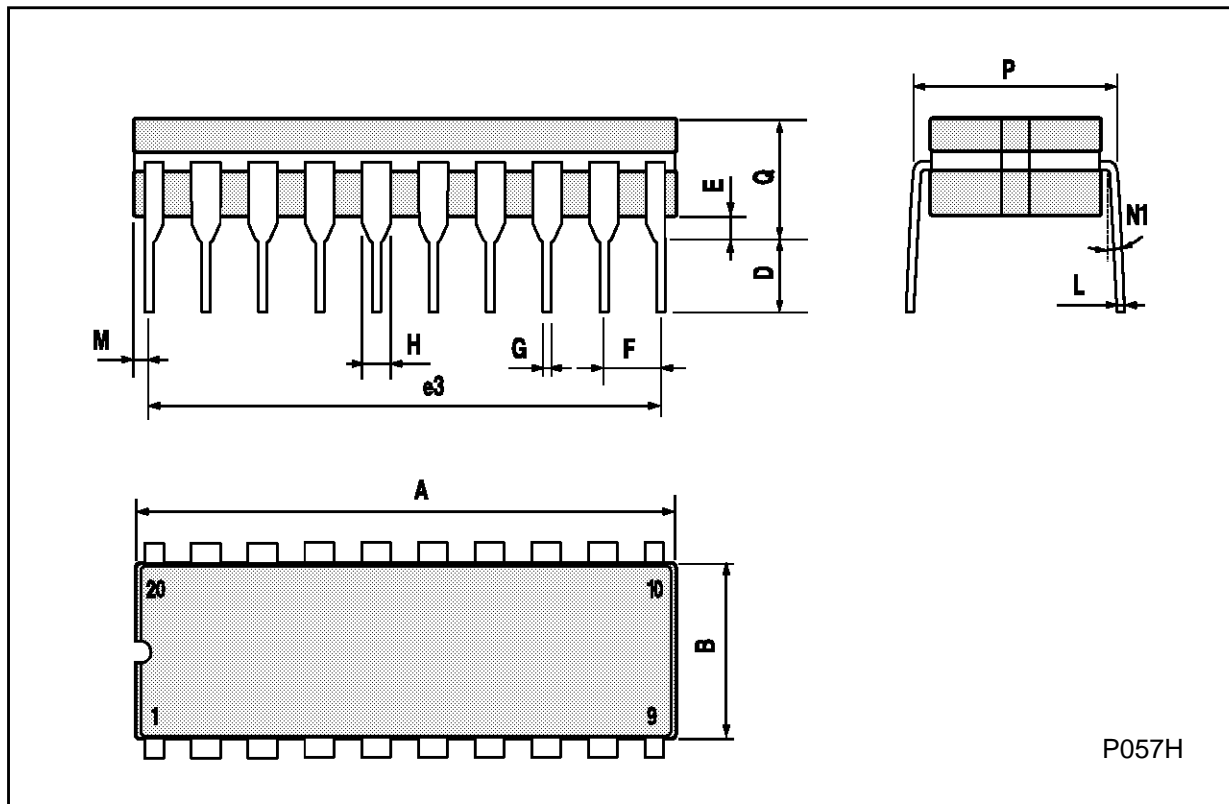
Plastic DIP20 (0.25) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053



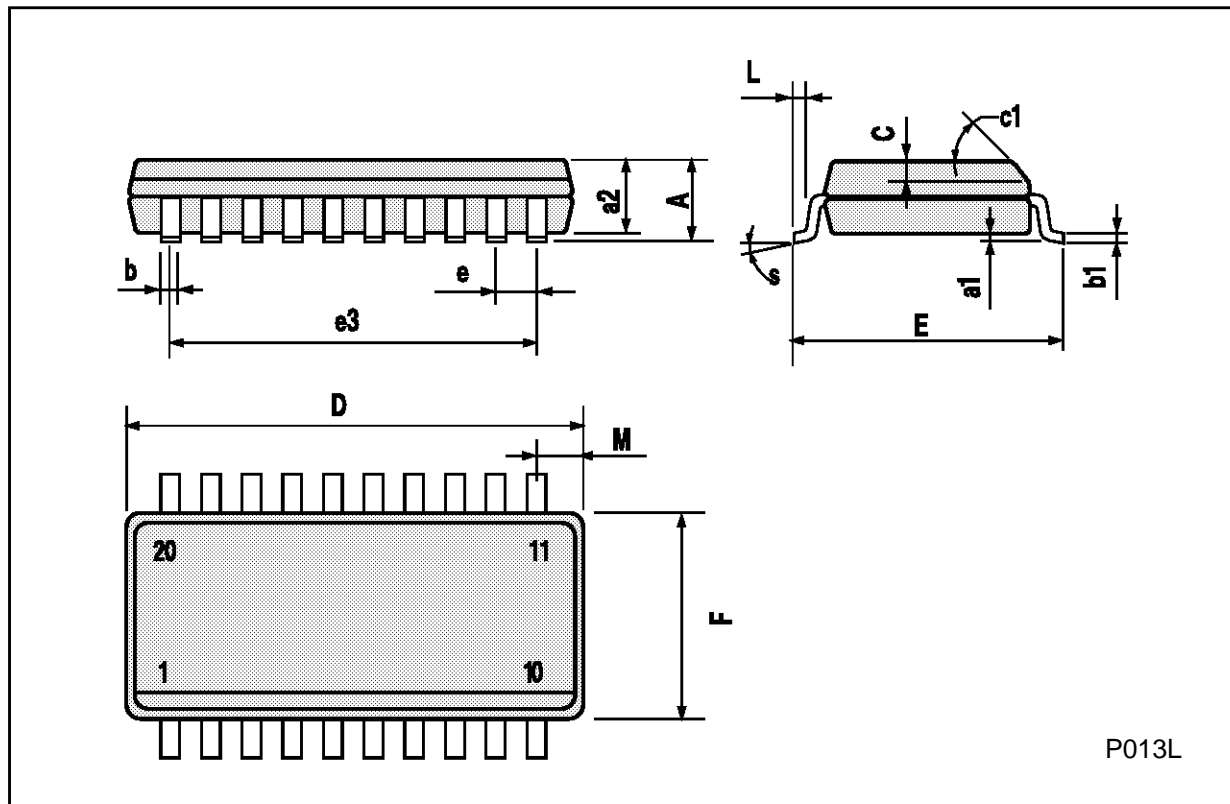
Ceramic DIP20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			25			0.984
B			7.8			0.307
D		3.3			0.130	
E	0.5		1.78	0.020		0.070
e3		22.86			0.900	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
I	1.27		1.52	0.050		0.060
L	0.22		0.31	0.009		0.012
M	0.51		1.27	0.020		0.050
N1	4° (min.), 15° (max.)					
P	7.9		8.13	0.311		0.320
Q			5.71			0.225



SO20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.20	0.004		0.007
a2			2.45			0.096
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45° (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.19		0.050
M			0.75			0.029
S	8° (max.)					



P013L

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