

## 3 TO 8 LINE DECODER (INVERTING)

- HIGH SPEED  
 $t_{PD} = 16 \text{ ns (TYP.) AT } V_{CC} = 5 \text{ V}$
- LOW POWER DISSIPATION  
 $I_{CC} = 4 \mu\text{A AT } T_A = 25 \text{ }^\circ\text{C}$
- OUTPUT DRIVE CAPABILITY  
 10 LSTTL LOADS
- BALANCED PROPAGATION DELAYS  
 $t_{PLH} = t_{PHL}$
- SYMMETRICAL OUTPUT IMPEDANCE  
 $|I_{OH}| = I_{OL}$
- HIGH NOISE IMMUNITY  
 $V_{NIH} = V_{NIL} = 28 \% V_{CC} \text{ (MIN.)}$
- WIDE OPERATING VOLTAGE RANGE  
 $V_{CC} \text{ (OPR)} = 2 \text{ V TO } 6 \text{ V}$
- PIN AND FUNCTION COMPATIBLE  
 WITH 54/74LS138

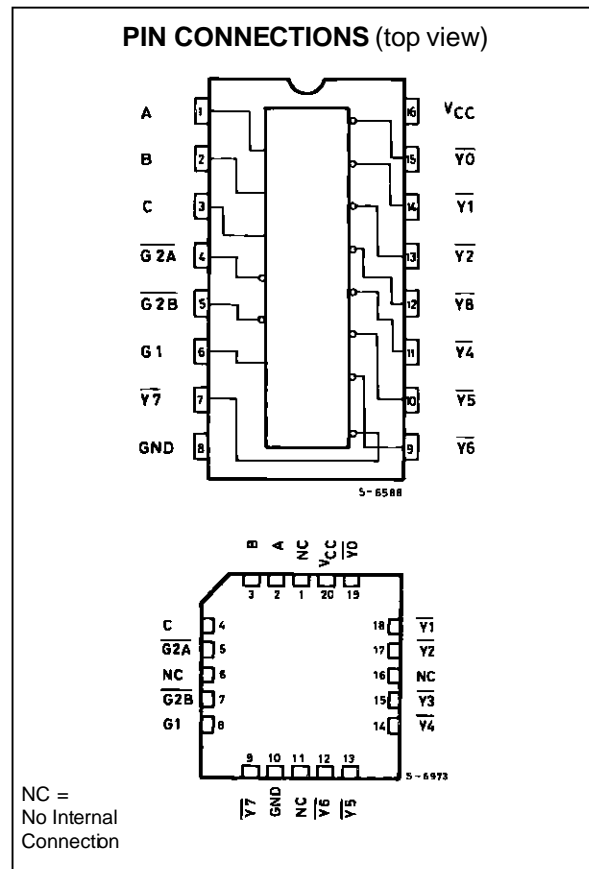
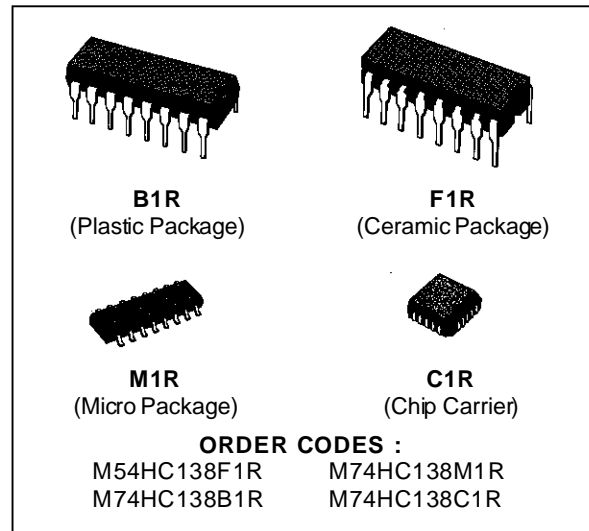
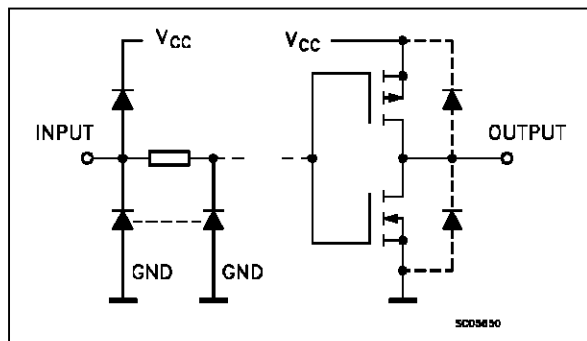
### DESCRIPTION

The M54/74HC138 is a high speed CMOS 3 TO 8 LINE DECODER fabricated in silicon gate C<sup>2</sup>MOS technology.

It has the same high speed performance of LSTTL combined with true CMOS low power consumption. If the device is enabled, 3 binary select inputs (A, B and C) determine which one of the outputs will go low. If enable input G1 is held low or either  $\overline{G2A}$  or  $\overline{G2B}$  is held high, the decoding function is inhibited and all the 8 outputs go high.

Three enable inputs are provided to ease cascade connection and application of address decoders for memory systems. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

### INPUT AND OUTPUT EQUIVALENT CIRCUIT



# M54/M74HC138

## TRUTH TABLE

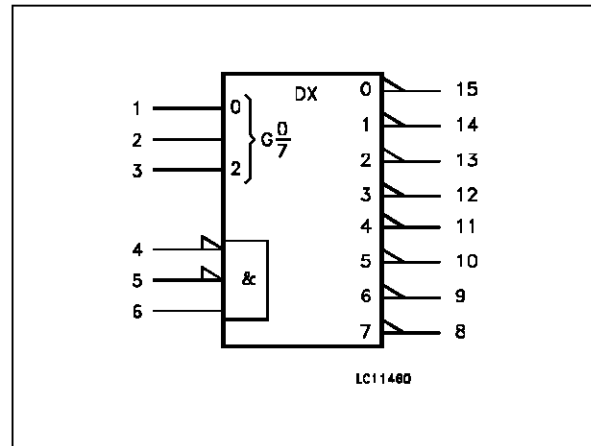
INPUTS						OUTPUTS							
ENABLE			SELECT			$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
$\overline{G2B}$	$\overline{G2A}$	G1	C	B	A								
X	X	L	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	X	X	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

X: Don't Care

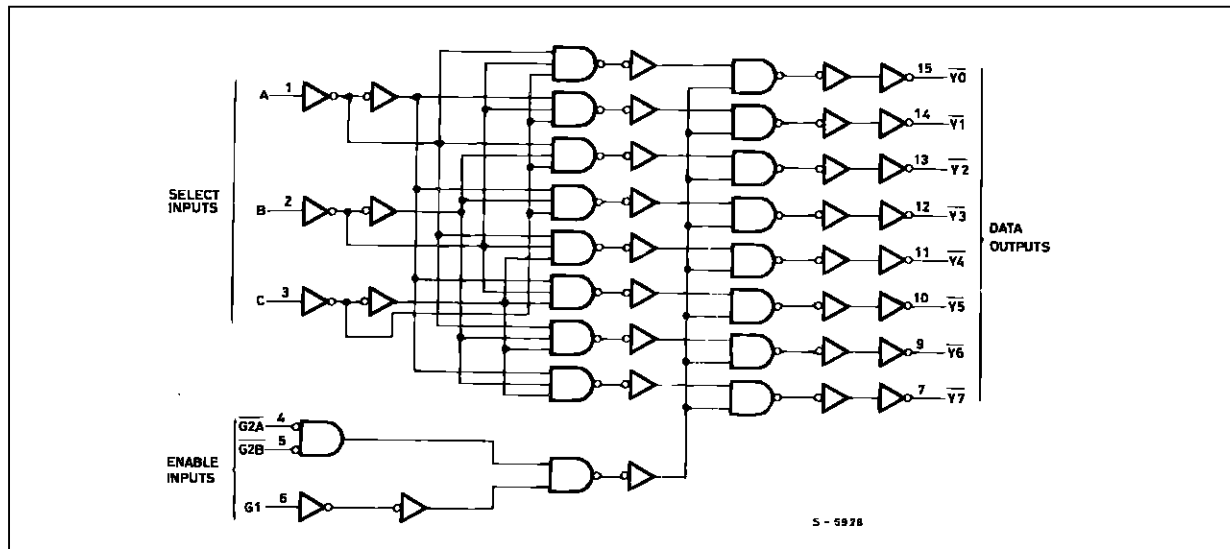
## PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 3	A, B, C	Address Inputs
4, 5	$\overline{G2A}$ , $\overline{G2B}$	Enable Inputs
6	G1	Enable Input
15, 14, 13, 12, 11, 10, 9, 7	$\overline{Y0}$ to $\overline{Y7}$	Outputs
8	GND	Ground (0V)
16	V <sub>CC</sub>	Positive Supply Voltage

## IEC LOGIC SYMBOL



## LOGIC DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage	-0.5 to +7	V
V <sub>I</sub>	DC Input Voltage	-0.5 to V <sub>CC</sub> + 0.5	V
V <sub>O</sub>	DC Output Voltage	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	DC Input Diode Current	± 20	mA
I <sub>OK</sub>	DC Output Diode Current	± 20	mA
I <sub>O</sub>	DC Output Source Sink Current Per Output Pin	± 25	mA
I <sub>CC</sub> or I <sub>GND</sub>	DC V <sub>CC</sub> or Ground Current	± 50	mA
P <sub>D</sub>	Power Dissipation	500 (*)	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(\*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit	
V <sub>CC</sub>	Supply Voltage	2 to 6	V	
V <sub>I</sub>	Input Voltage	0 to V <sub>CC</sub>	V	
V <sub>O</sub>	Output Voltage	0 to V <sub>CC</sub>	V	
T <sub>op</sub>	Operating Temperature: <b>M54HC Series</b> <b>M74HC Series</b>	-55 to +125 -40 to +85	°C °C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time	V <sub>CC</sub> = 2 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6 V	0 to 1000 0 to 500 0 to 400	ns

**DC SPECIFICATIONS**

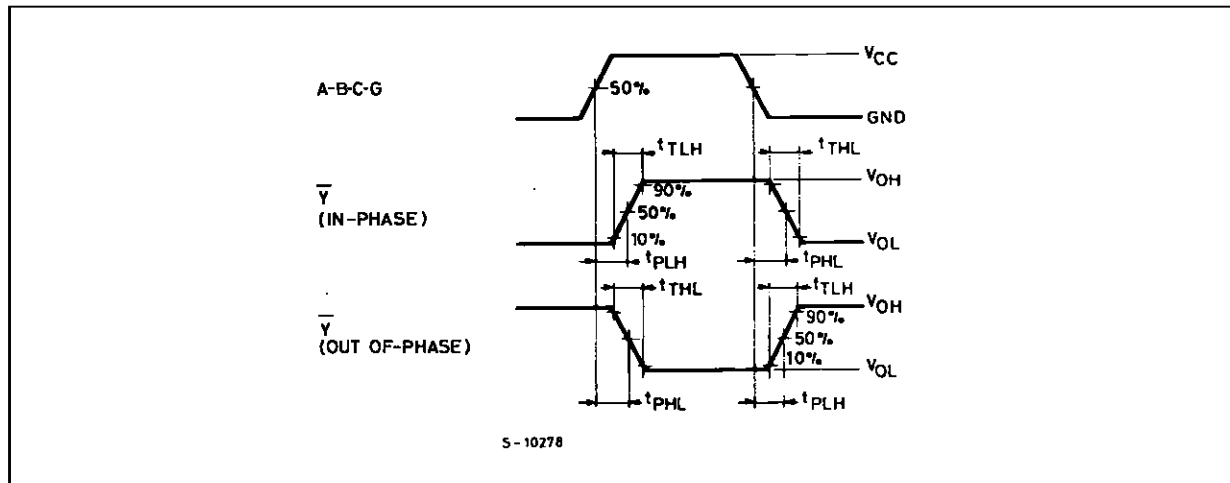
Symbol	Parameter	Test Conditions		Value						Unit		
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC			
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.	
V <sub>IH</sub>	High Level Input Voltage	2.0		1.5			1.5		1.5		V	
		4.5		3.15			3.15		3.15			
		6.0		4.2			4.2		4.2			
V <sub>IL</sub>	Low Level Input Voltage	2.0				0.5		0.5		0.5	V	
		4.5				1.35		1.35		1.35		
		6.0				1.8		1.8		1.8		
V <sub>OH</sub>	High Level Output Voltage	2.0	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = -20 μA	1.9	2.0		1.9		1.9	V	
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5	I <sub>O</sub> = -4.0 mA	4.18	4.31		4.13		4.10			
		6.0		I <sub>O</sub> = -5.2 mA	5.68	5.8		5.63		5.60		
V <sub>OL</sub>	Low Level Output Voltage	2.0	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 20 μA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I <sub>O</sub> = 4.0 mA	0.17	0.26		0.33		0.40		
		6.0			I <sub>O</sub> = 5.2 mA	0.18	0.26		0.33		0.40	
I <sub>I</sub>	Input Leakage Current	6.0	V <sub>I</sub> = V <sub>CC</sub> or GND			±0.1		±1		±1	μA	
I <sub>CC</sub>	Quiescent Supply Current	6.0	V <sub>I</sub> = V <sub>CC</sub> or GND			4		40		80	mA	

AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

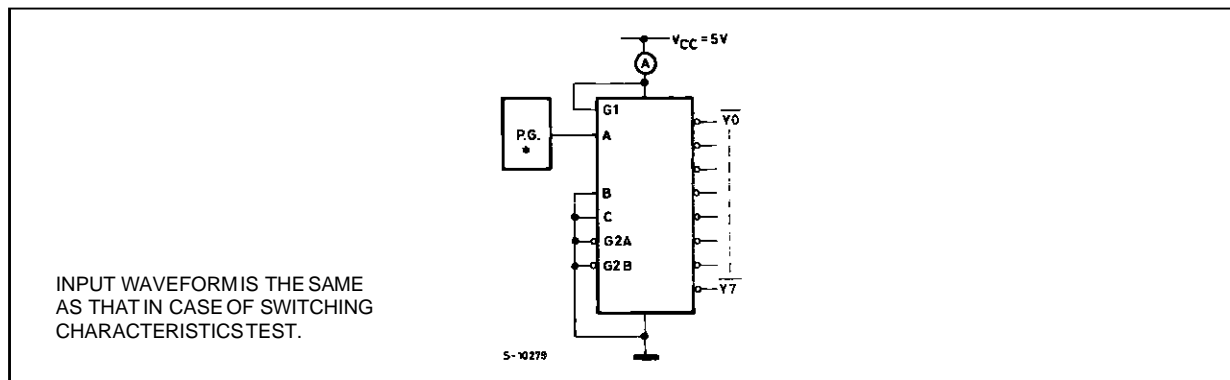
Symbol	Parameter	Test Conditions		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t <sub>TLH</sub> t <sub>THL</sub>	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (A, B, C - $\bar{Y}$ )	2.0			60	125		155		190	ns
		4.5			15	25		31		38	
		6.0			13	21		26		32	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (G, $\bar{G}$ - $\bar{Y}$ )	2.0			56	120		150		180	ns
		4.5			14	24		30		36	
		6.0			12	20		26		31	
C <sub>IN</sub>	Input Capacitance				5	10		10		10	pF
C <sub>PD</sub> (*)	Power Dissipation Capacitance				47						pF

(\*) C<sub>PD</sub> is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. I<sub>cc(opr)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>IN</sub> + I<sub>cc</sub>

SWITCHING CHARACTERISTICS TEST WAVEFORM

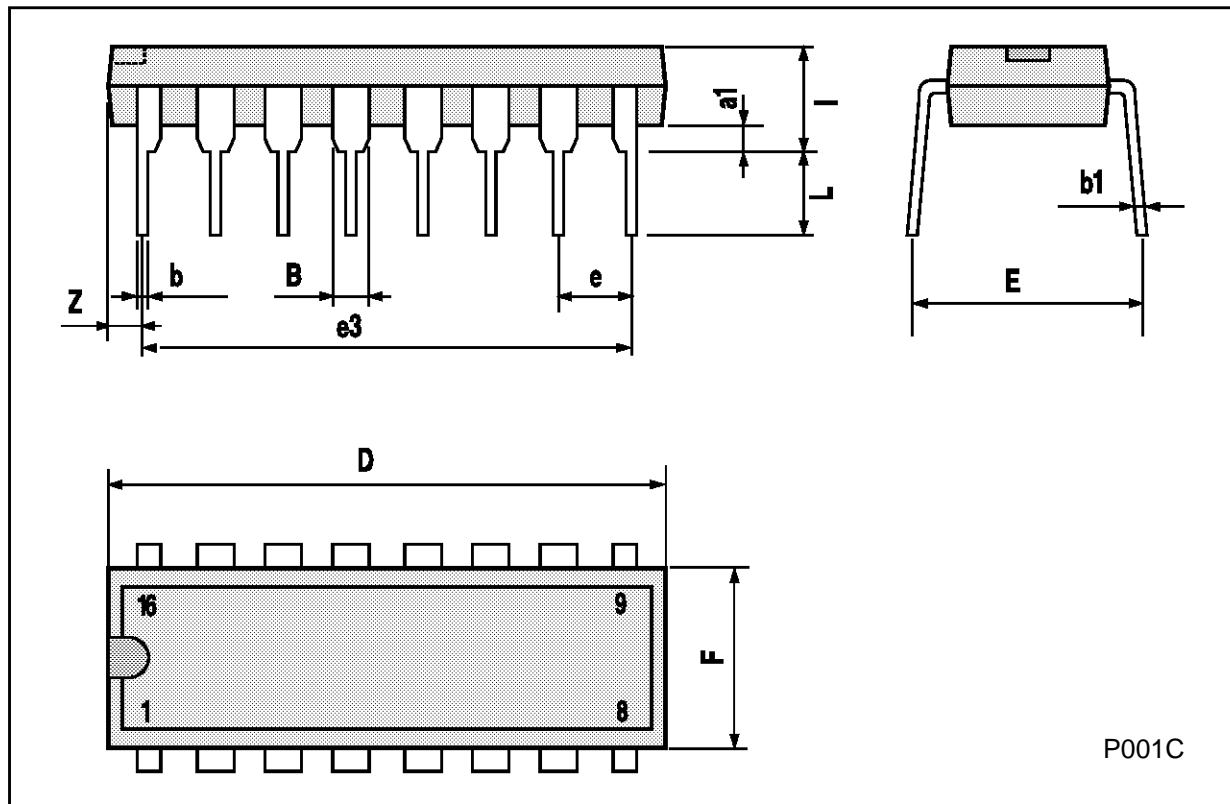


TEST CIRCUIT I<sub>cc</sub> (Opr.)



**Plastic DIP16 (0.25) MECHANICAL DATA**

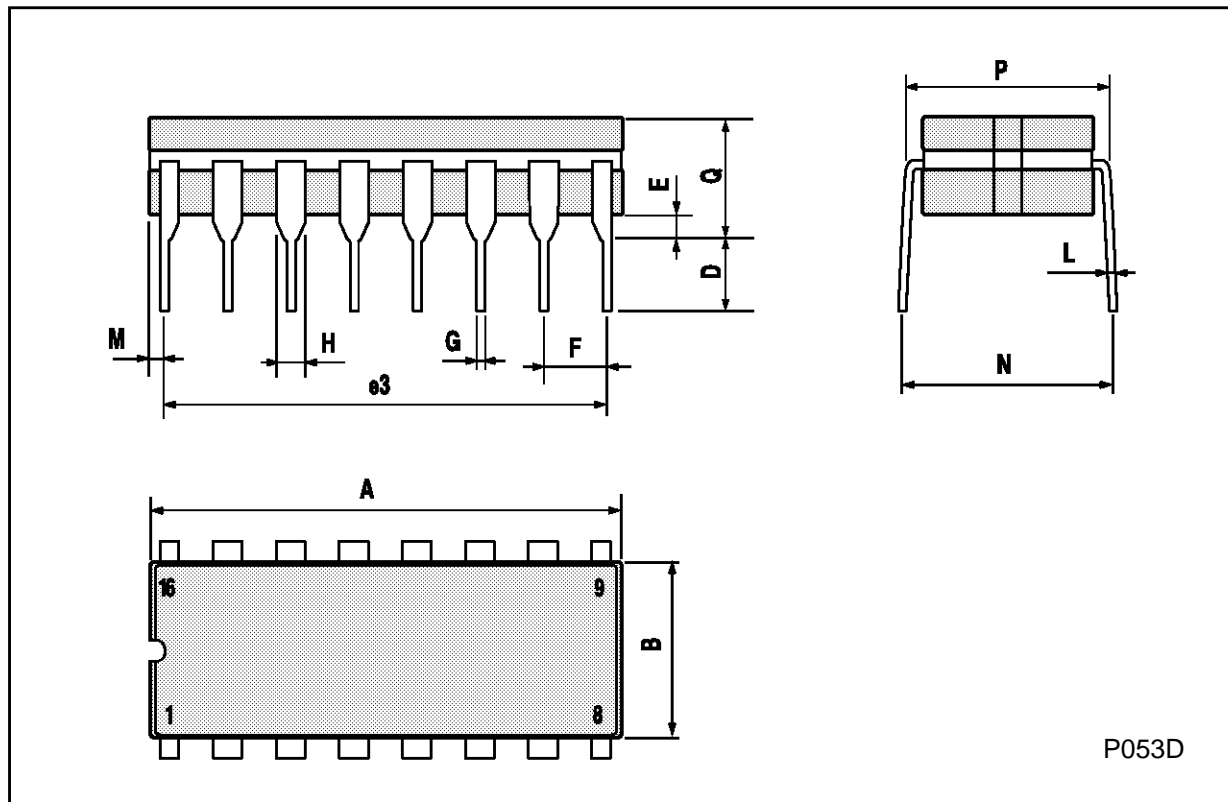
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

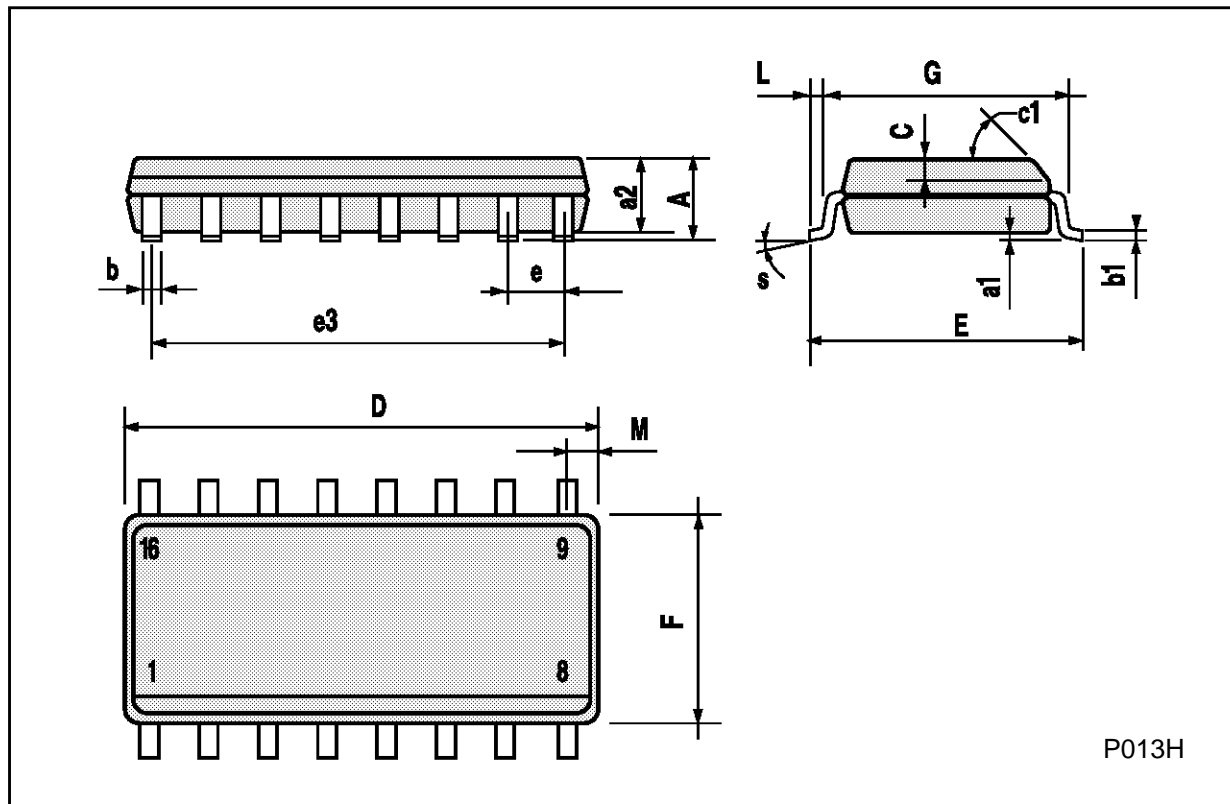
## Ceramic DIP16/1 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			20			0.787
B			7			0.276
D		3.3			0.130	
E	0.38			0.015		
e3		17.78			0.700	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
H	1.17		1.52	0.046		0.060
L	0.22		0.31	0.009		0.012
M	0.51		1.27	0.020		0.050
N			10.3			0.406
P	7.8		8.05	0.307		0.317
Q			5.08			0.200



SO16 (Narrow) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



P013H



## PLCC20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	



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