

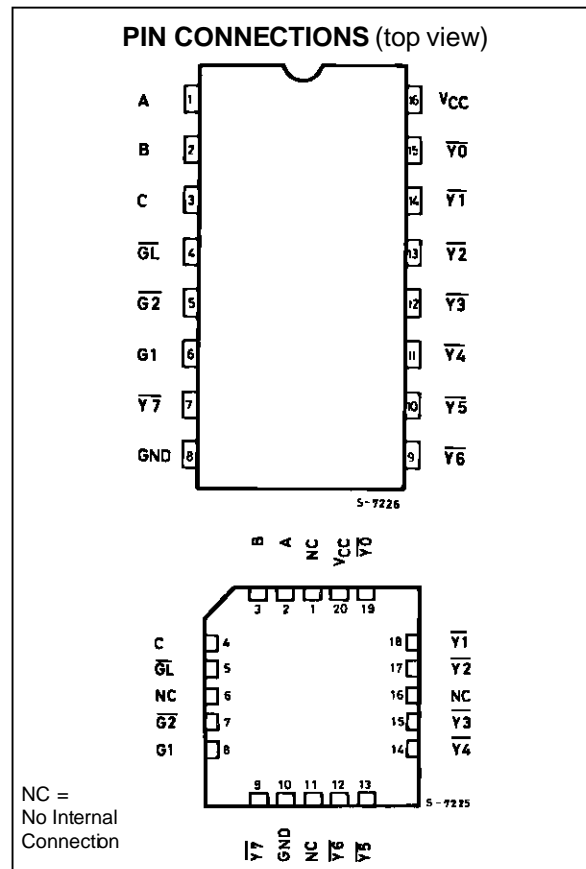
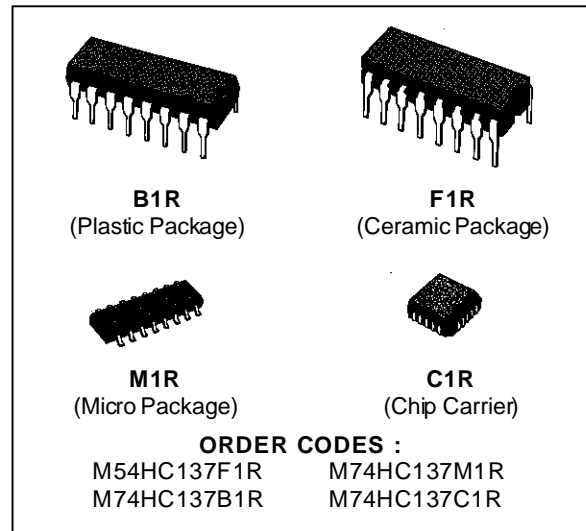
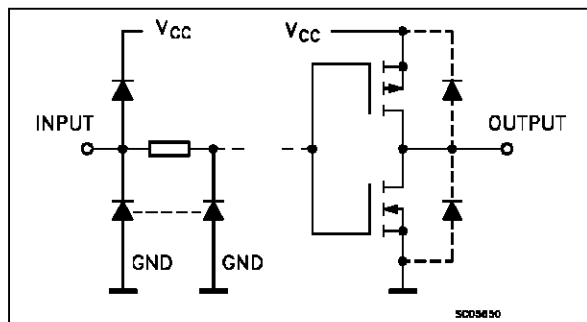
3 TO 8 LINE DECODER/LATCH (INVERTING)

- HIGH SPEED
 $t_{PD} = 11 \text{ ns (TYP.) AT } V_{CC} = 5 \text{ V}$
- LOW POWER DISSIPATION
 $I_{CC} = 4 \mu\text{A (MAX.) AT } T_A = 25 \text{ }^\circ\text{C}$
- HIGH NOISE IMMUNITY
 $V_{NIH} = V_{NIL} = 28 \% V_{CC} \text{ (MIN.)}$
- OUTPUT DRIVE CAPABILITY
 10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
 $|I_{OH}| = I_{OL} = 4 \text{ mA (MIN.)}$
- BALANCED PROPAGATION DELAYS
 $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
 $V_{CC} \text{ (OPR)} = 2 \text{ V TO } 6 \text{ V}$
- PIN AND FUNCTION COMPATIBLE
 WITH 54/74LS137

DESCRIPTION

The M54/74HC137 is a high speed CMOS 3 TO 8 LINE DECODER/LATCH (INVERTING) fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This device is a 3 to 8 line decoder with latches on the three address inputs. When \overline{GL} goes from low to high, the address present at the select inputs (A, B and C) is stored in the latches. As long as \overline{GL} remains high no address changes will be recognized. Output enable pins G1 and $\overline{G2}$ control the state of the outputs independently of the select or latch-enable inputs. All the outputs are high unless G1 is high and $\overline{G2}$ is low. The HC137 is ideally suited for the implementation of glitch-free decoders in stored-address applications in bus oriented systems. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

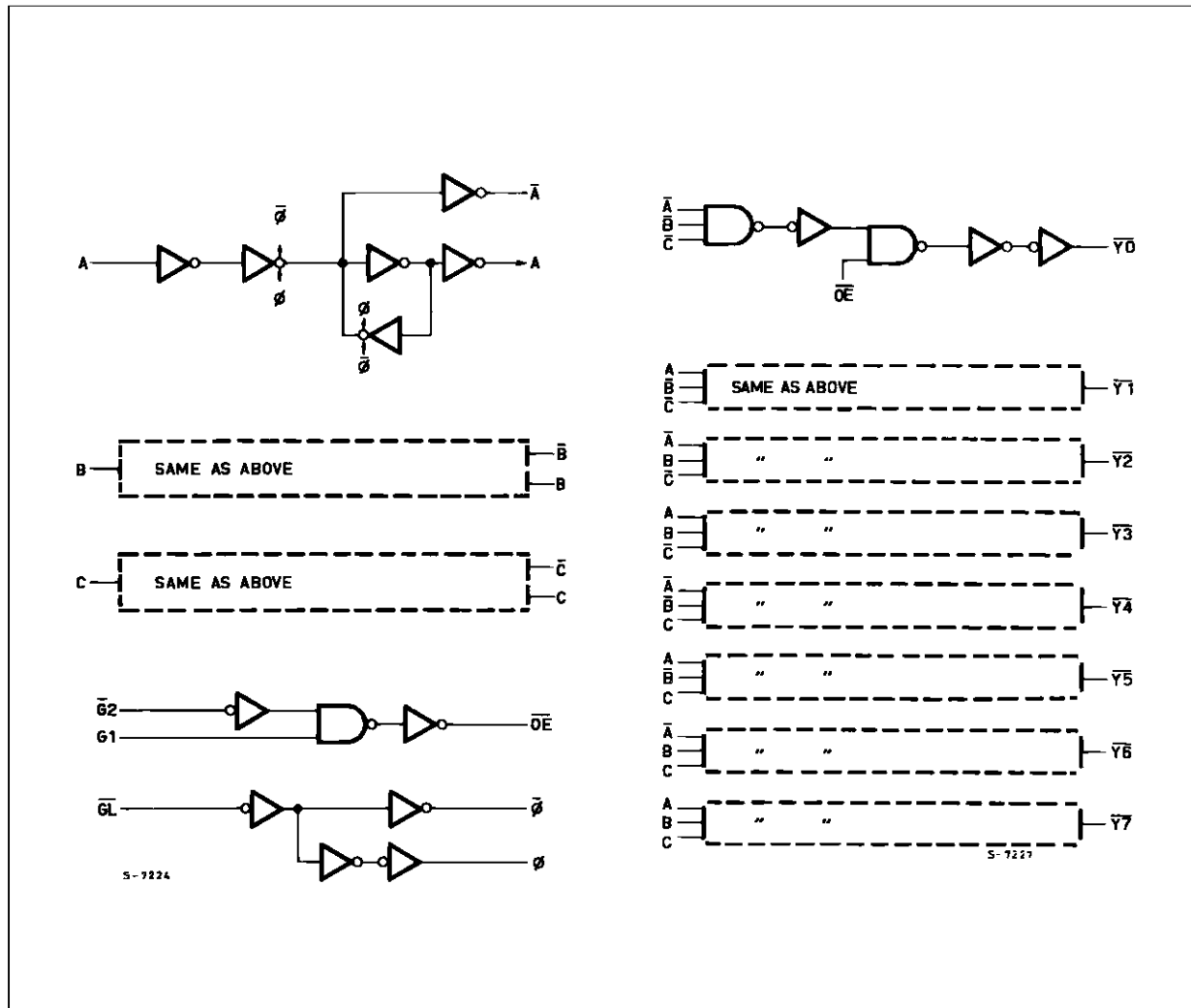
INPUT AND OUTPUT EQUIVALENT CIRCUIT



TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{G1}$	G1	$\overline{G2}$	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Outputs corresponding to stored address L: all others H							

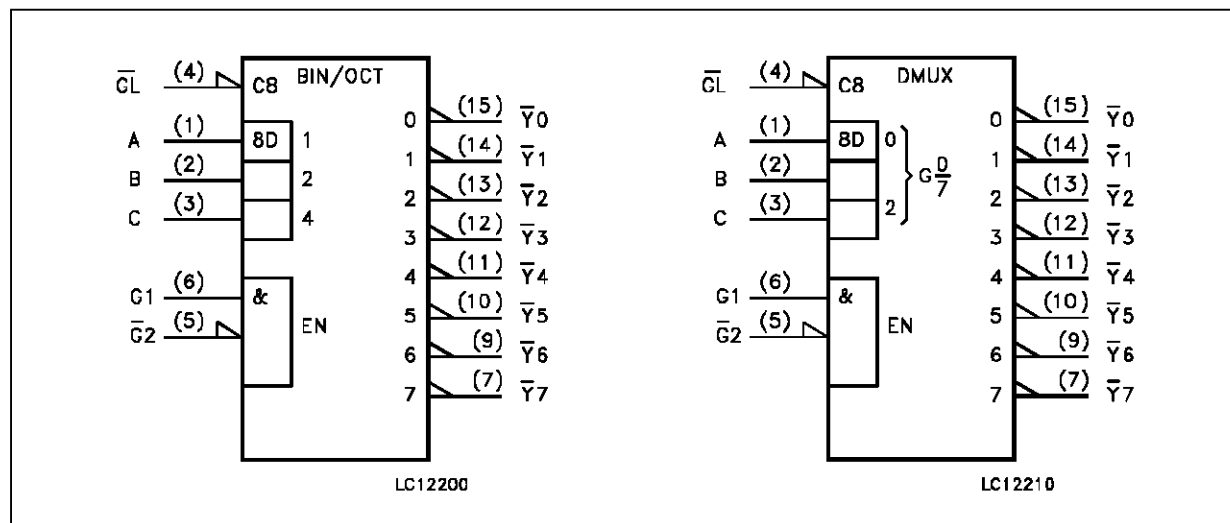
LOGIC DIAGRAM



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 3	A to C	Data Inputs
4	\overline{GL}	Latch Enable Input (Active LOW)
5	$\overline{G2}$	Data Enable Input (Active LOW)
6	G1	Data Enable Input (Active HIGH)
15, 14, 13, 12, 11, 10, 9, 7	$\overline{Y0}$ to $\overline{Y7}$	Multiplexer Outputs
8	GND	Ground (0V)
16	V _{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to +7	V
V _I	DC Input Voltage	-0.5 to V _{CC} + 0.5	V
V _O	DC Output Voltage	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	± 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Source Sink Current Per Output Pin	± 25	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 50	mA
P _D	Power Dissipation	500 (*)	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit	
V_{CC}	Supply Voltage	2 to 6	V	
V_I	Input Voltage	0 to V_{CC}	V	
V_O	Output Voltage	0 to V_{CC}	V	
T_{op}	Operating Temperature: M54HC Series M74HC Series	-55 to +125 -40 to +85	°C °C	
t_r, t_f	Input Rise and Fall Time	$V_{CC} = 2\text{ V}$	0 to 1000	ns
		$V_{CC} = 4.5\text{ V}$	0 to 500	
		$V_{CC} = 6\text{ V}$	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions		Value						Unit		
				$T_A = 25\text{ °C}$ 54HC and 74HC			$-40\text{ to }85\text{ °C}$ 74HC		$-55\text{ to }125\text{ °C}$ 54HC			
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.	
V_{IH}	High Level Input Voltage	V_{CC} (V)		1.5			1.5		1.5		V	
				3.15			3.15		3.15			
				4.2			4.2		4.2			
V_{IL}	Low Level Input Voltage	V_{CC} (V)				0.5		0.5		0.5	V	
						1.35		1.35		1.35		
						1.8		1.8		1.8		
V_{OH}	High Level Output Voltage	V_{CC} (V)	$V_I = V_{IH}$ or V_{IL}	$I_O = -20\text{ }\mu\text{A}$	1.9	2.0		1.9		1.9	V	
					4.4	4.5		4.4		4.4		
					5.9	6.0		5.9		5.9		
				4.5	$I_O = -4.0\text{ mA}$	4.18	4.31		4.13			4.10
						5.68	5.8		5.63			5.60
V_{OL}	Low Level Output Voltage	V_{CC} (V)	$V_I = V_{IH}$ or V_{IL}	$I_O = 20\text{ }\mu\text{A}$		0.0	0.1		0.1		0.1	V
						0.0	0.1		0.1		0.1	
						0.0	0.1		0.1		0.1	
				4.5	$I_O = 4.0\text{ mA}$	0.17	0.26		0.33		0.40	
						0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	V_{CC} (V)	$V_I = V_{CC}$ or GND			± 0.1		± 1		± 1	μA	
						2		20		40		
I_{CC}	Quiescent Supply Current	V_{CC} (V)	$V_I = V_{CC}$ or GND			2		20		40	μA	

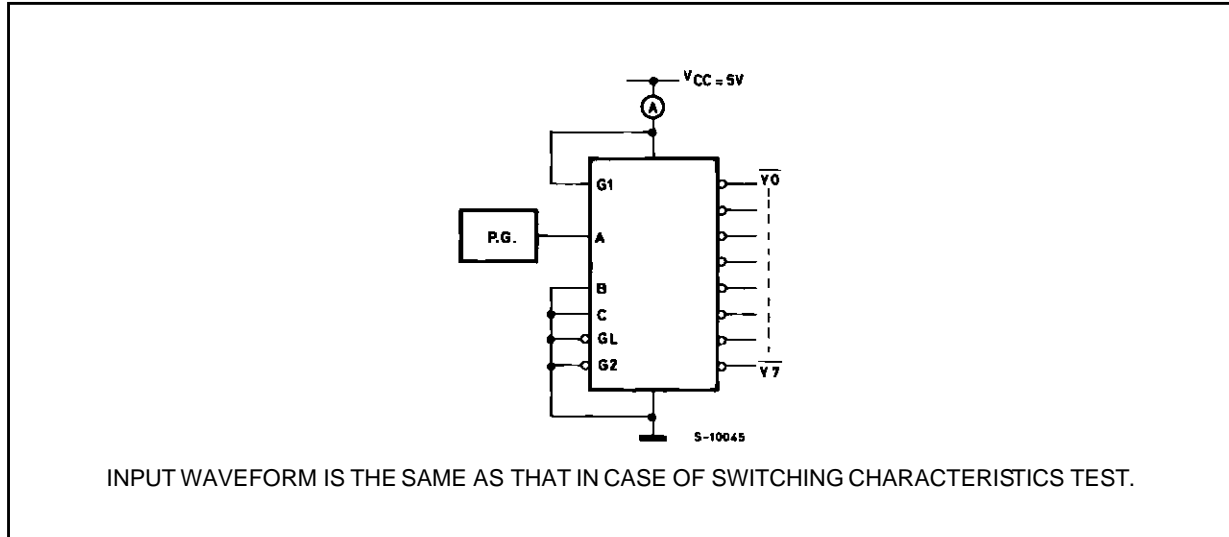
AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	Test Conditions		Value						Unit	
		V _{CC} (V)		T _A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t _{TLH} t _{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t _{PLH} t _{PHL}	Propagation Delay Time (G1 - \bar{Y})	2.0			45	115		145		175	ns
		4.5			14	23		29		35	
		6.0			12	20		25		30	
t _{PLH} t _{PHL}	Propagation Delay Time (G2 - Y)	2.0			50	115		145		175	ns
		4.5			15	23		29		35	
		6.0			13	20		25		30	
t _{PLH} t _{PHL}	Propagation Delay Time (GL - Y)	2.0			70	170		215		250	ns
		4.5			22	34		43		50	
		6.0			19	29		37		43	
t _{PLH} t _{PHL}	Propagation Delay Time (A, B, C - \bar{Y})	2.0			70	165		205		110	ns
		4.5			21	33		41		22	
		6.0			18	28		35		19	
t _{W(L)}	Minimum Pulse Width (GL)	2.0			12	50		65		75	ns
		4.5			3	10		13		15	
		6.0			3	9		11		13	
t _s	Minimum Set-up Time (A, B, C - \bar{GL})	2.0			8	50		60		75	ns
		4.5			2	10		12		15	
		6.0			2	9		10		13	
t _h	Minimum Hold Time (A, B, C - \bar{GL})	2.0				5		5		5	ns
		4.5				5		5		5	
		6.0				5		5		5	
C _{IN}	Input Capacitance				5	10		10		10	pF
C _{PD} (*)	Power Dissipation Capacitance				55						pF

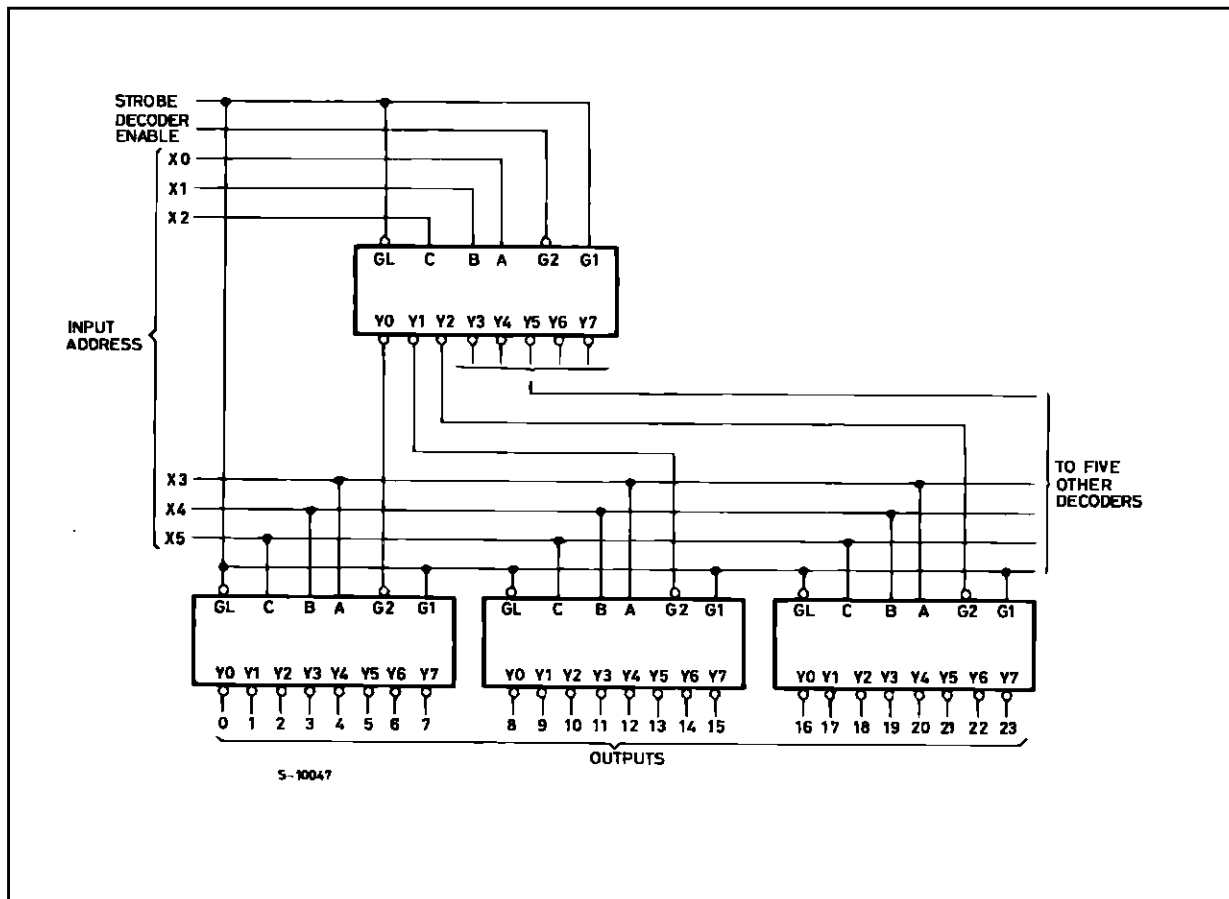
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

M54/M74HC137

TEST CIRCUIT I_{cc} (Opr.)



TYPICAL APPLICATION



Plastic DIP16 (0.25) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



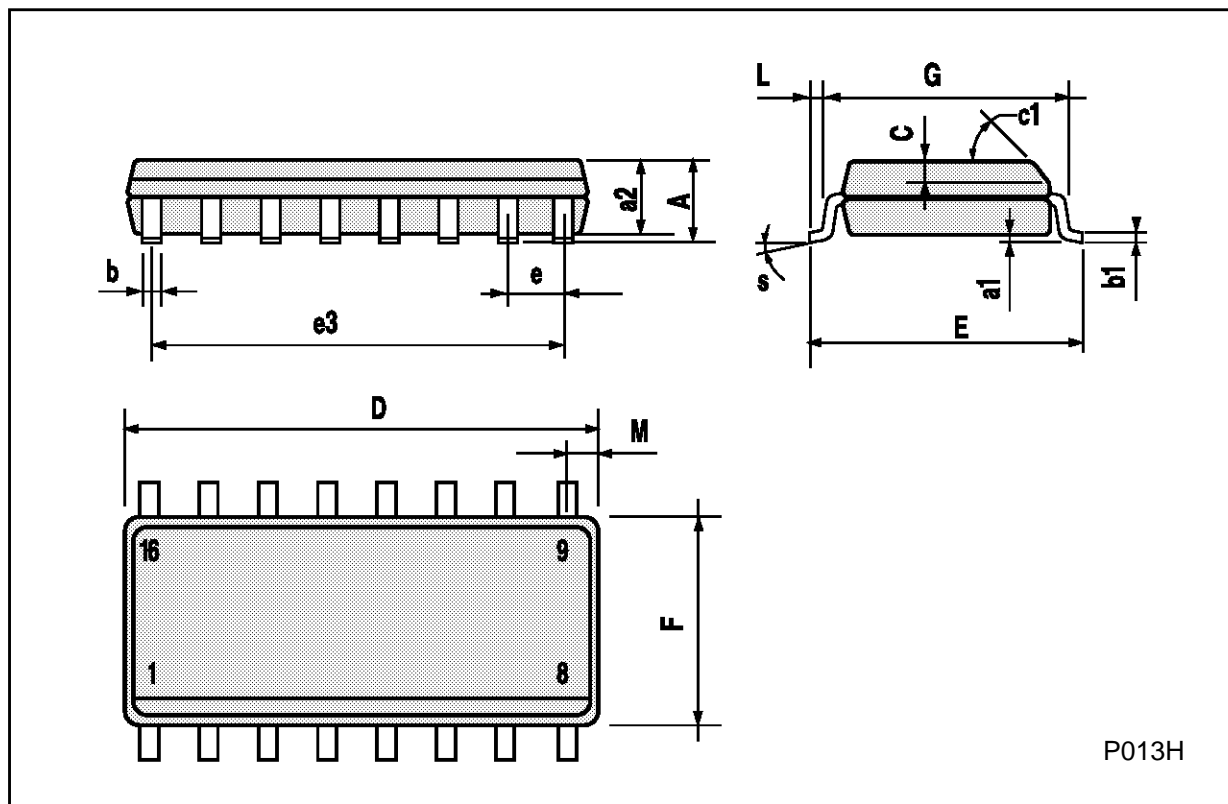
Ceramic DIP16/1 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			20			0.787
B			7			0.276
D		3.3			0.130	
E	0.38			0.015		
e3		17.78			0.700	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
H	1.17		1.52	0.046		0.060
L	0.22		0.31	0.009		0.012
M	0.51		1.27	0.020		0.050
N			10.3			0.406
P	7.8		8.05	0.307		0.317
Q			5.08			0.200



SO16 (Narrow) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



P013H

PLCC20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	



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