

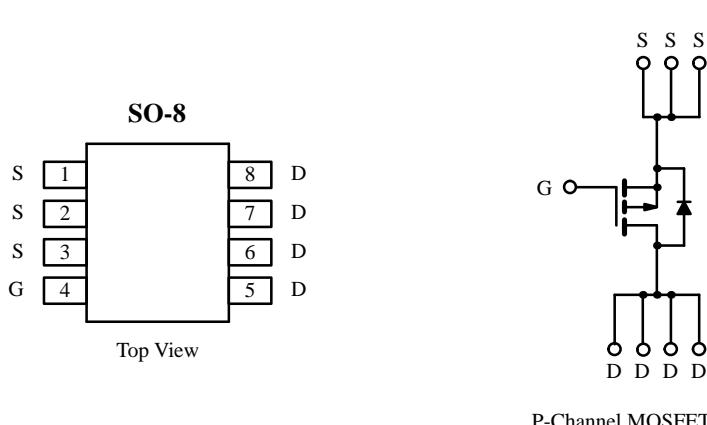
P-Channel Enhancement-Mode MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-20	0.065 @ $V_{GS} = -4.5$ V	± 5.4
	0.100 @ $V_{GS} = -2.7$ V	± 4.2

Recommended upgrade: Si9424DY

Lower profile/smaller size—see LITE FOOT® equivalent: Si6433DQ



P-Channel MOSFET

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage		± 12	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	± 5.4	A
		± 4.4	
Pulsed Drain Current	I_{DM}	± 10	A
Continuous Source Current (Diode Conduction) ^a	I_S	-2.6	
Maximum Power Dissipation ^a	P_D	2.5	W
		1.6	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	50	°C/W

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Subsequent updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #1207.

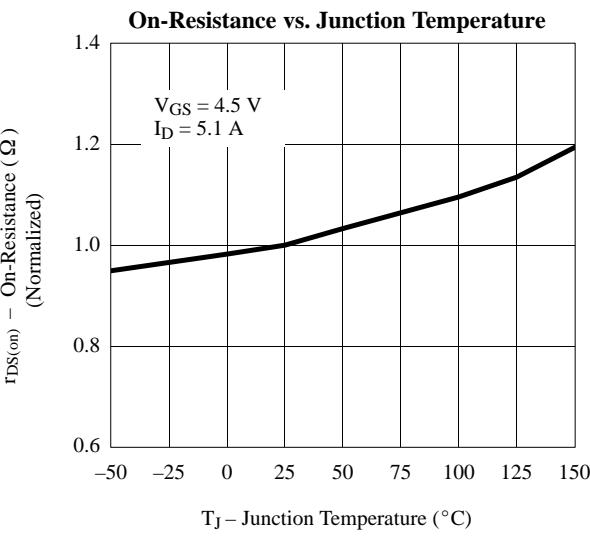
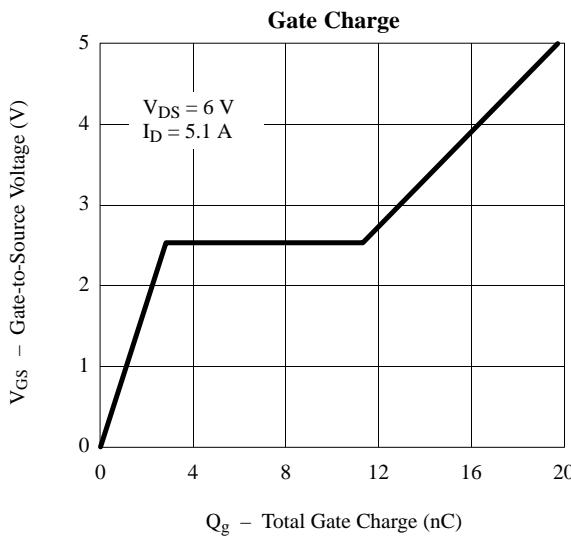
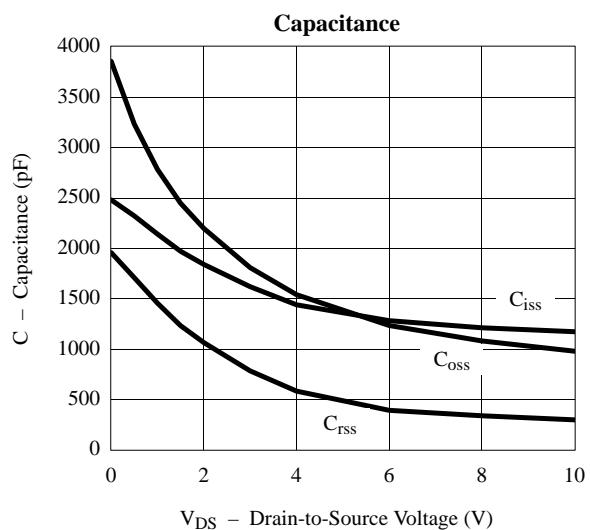
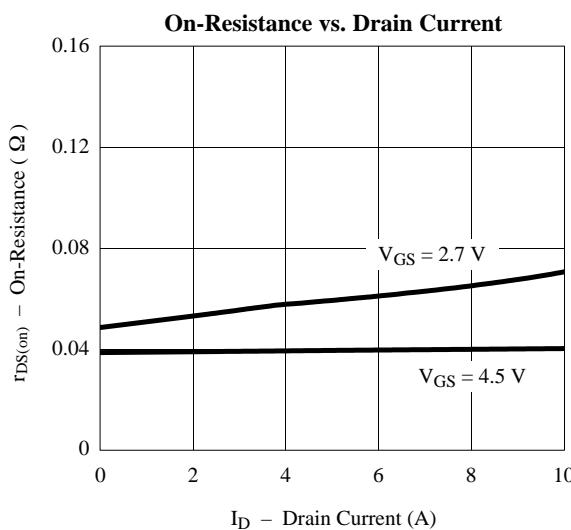
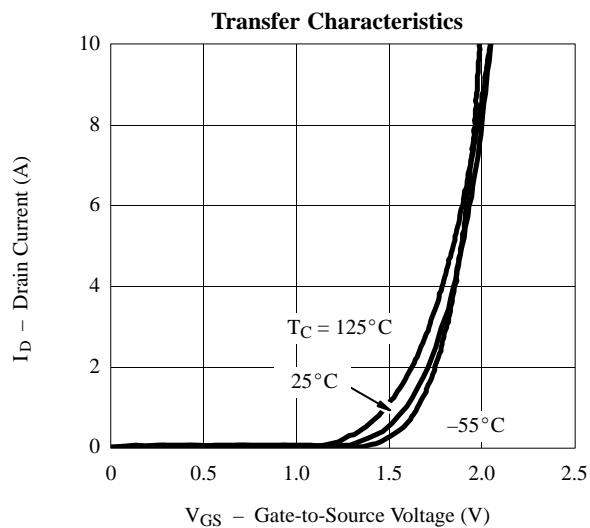
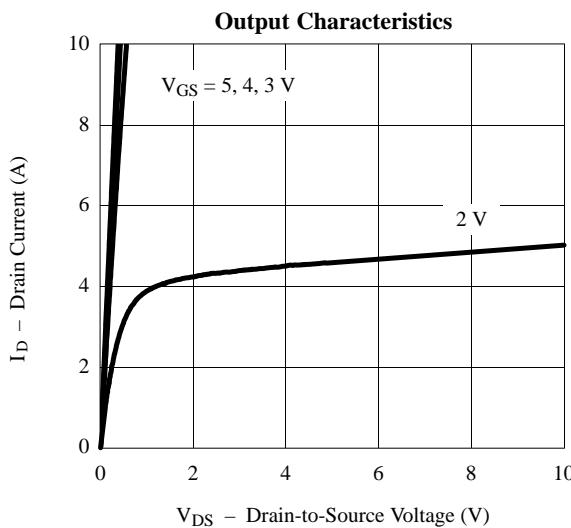
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	-0.8			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$		-1		μA
		$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 70^\circ\text{C}$		-5		
On-State Drain Current ^b	$I_{D(\text{on})}$	$V_{DS} \leq -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	-10			A
		$V_{DS} \leq -5 \text{ V}, V_{GS} = -2.7 \text{ V}$	-4			
Drain-Source On-State Resistance ^b	$r_{DS(\text{on})}$	$V_{GS} = -4.5 \text{ V}, I_D = -5.1 \text{ A}$		0.045	0.065	Ω
		$V_{GS} = -2.7 \text{ V}, I_D = -2.0 \text{ A}$		0.060	0.100	
Forward Transconductance ^b	g_{fs}	$V_{DS} = -9 \text{ V}, I_D = -5.1 \text{ A}$		11		S
Diode Forward Voltage ^b	V_{SD}	$I_S = -2.6 \text{ A}, V_{GS} = 0 \text{ V}$		-1.0	-1.2	V
Dynamic^a						
Total Gate Charge	Q_g	$V_{DS} = -6 \text{ V}, V_{GS} = -4.5 \text{ V}, I_D = -5.1 \text{ A}$		20	60	nC
Gate-Source Charge	Q_{gs}			3		
Gate-Drain Charge	Q_{gd}			10		
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = -6 \text{ V}, R_L = 6 \Omega$ $I_D \cong -1 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_G = 6 \Omega$		30	60	ns
Rise Time	t_r			55	100	
Turn-Off Delay Time	$t_{d(\text{off})}$			80	180	
Fall Time	t_f			50	100	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -2.6, di/dt = 100 \text{ A}/\mu\text{s}$		60	80	

Notes

- a. For design aid only; not subject to production testing.
- b. Pulse test: pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

Typical Characteristics (25°C Unless Otherwise Noted)



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