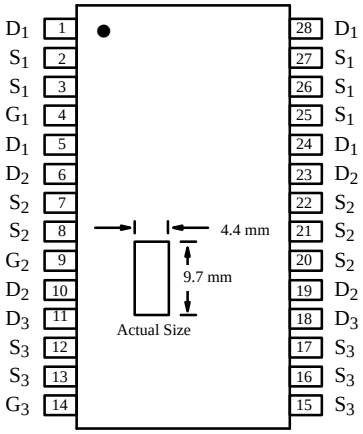
# Triple P-Channel Enhancement-Mode MOSFET

## Product Summary

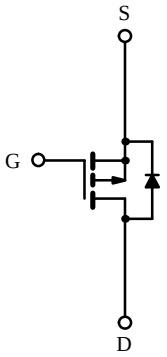
| $V_{DS}$ (V) | $r_{DS(on)}$ (Ω) | $I_D$ (A) |
|---|---|---|
| –30 | 0.040 @ $V_{GS}$ = –10 V | ±4.5 |
| | 0.070 @ $V_{GS}$ = –4.5 V | ±3.4 |

TrenchFET™ Power MOSFETs

**TSSOP-28**




Top View




P-Channel MOSFET

*Source Pins 2, 3, 25, 26, and 27 must be tied common.

Source Pins 7, 8, 20, 21, and 22 must be tied common.

Source Pins 12, 13, 15, 16, and 17 must be tied common.

## Absolute Maximum Ratings ($T_A$ = 25°C Unless Otherwise Noted)

| Parameter | | Symbol | Limit | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | –30 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±20 | |
| Continuous Drain Current ($T_J$ = 150°C)[a] | $T_A$ = 25°C | $I_D$ | ±4.5 | A |
| | $T_A$ = 70°C | | ±3.6 | |
| Pulsed Drain Current | | $I_{DM}$ | ±30 | |
| Continuous Source Current (Diode Conduction)[a] | | $I_S$ | –1.25 | |
| Maximum Power Dissipation[a] | $T_A$ = 25°C | $P_D$ | 1.5 | W |
| | $T_A$ = 70°C | | 1.0 | |
| Operating Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | –55 to 150 | °C |

## Thermal Resistance Ratings

| Parameter | Symbol | Limit | Unit |
|---|---|---|---|
| Maximum Junction-to-Ambient[a] | $R_{thJA}$ | 83 | °C/W |

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Subsequent updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #1817.

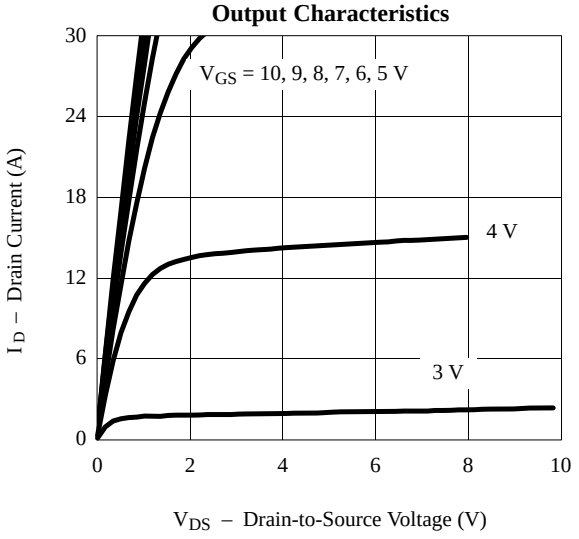
## Specifications ($T_J$ = 25°C Unless Otherwise Noted)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = –250 µA | –1 | | | V |
| Gate-Body Leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ±20 V | | | ±100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = –30 V, $V_{GS}$ = 0 V | | | –1 | µA |
| | | $V_{DS}$ = –30 V, $V_{GS}$ = 0 V, $T_J$ = 55°C | | | –25 | |
| On-State Drain Current[a] | $I_{D(on)}$ | $V_{DS}$ = –5 V, $V_{GS}$ = –10 V | –20 | | | A |
| Drain-Source On-State Resistance[a] | $r_{DS(on)}$ | $V_{GS}$ = –10 V, $I_D$ = –4.5 A | | 0.029 | 0.040 | Ω |
| | | $V_{GS}$ = –4.5 V, $I_D$ = –3.5 A | | 0.045 | 0.070 | |
| Forward Transconductance[a] | $g_{fs}$ | $V_{DS}$ = –15 V, $I_D$ = –4.5 A | | 9.0 | | S |
| Diode Forward Voltage[a] | $V_{SD}$ | $I_S$ = –1.25 A, $V_{GS}$ = 0 V | | –0.8 | –1.2 | V |
| **Dynamic[b]** | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = –15 V, $V_{GS}$ = –10 V, $I_D$ = –4.5 A | | 20 | 35 | nC |
| Gate-Source Charge | $Q_{gs}$ | | | 4.0 | | |
| Gate-Drain Charge | $Q_{gd}$ | | | 3.3 | | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = –15 V, $R_L$ = 15 Ω<br>$I_D$ ≅ –1 A, $V_{GEN}$ = –10 V, $R_G$ = 6 Ω | | 15 | 25 | ns |
| Rise Time | $t_r$ | | | 14 | 25 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 40 | 65 | |
| Fall Time | $t_f$ | | | 15 | 25 | |
| Source-Drain Reverse Recovery Time | $t_{rr}$ | $I_F$ = –1.25 A, di/dt = 100 A/µs | | 50 | 80 | |

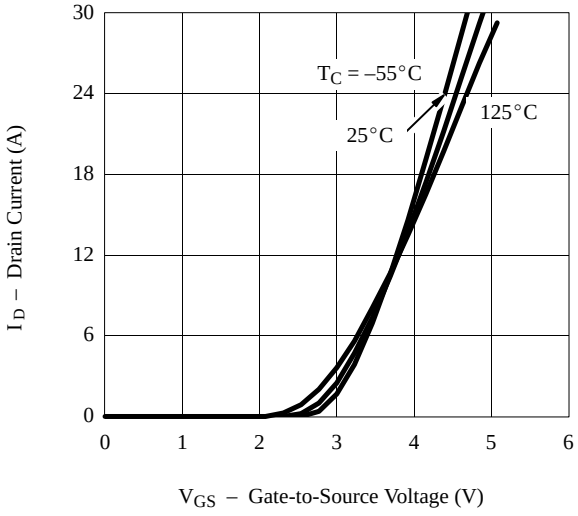
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

## Typical Characteristics (25°C Unless Noted)

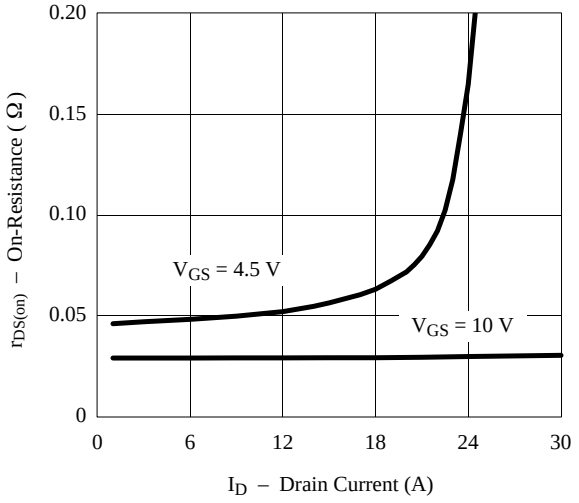
**Output Characteristics**



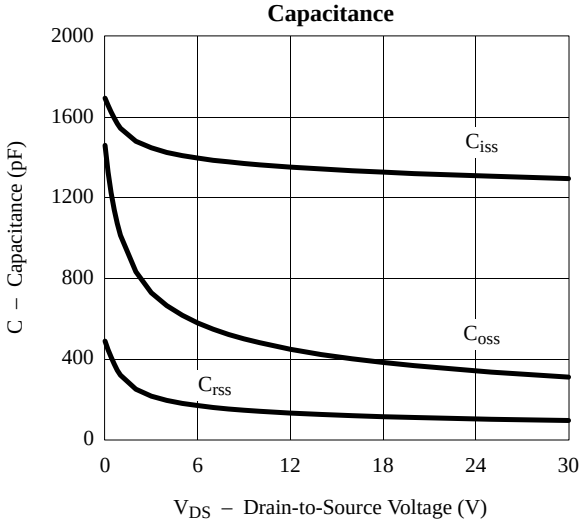

**Transfer Characteristics**



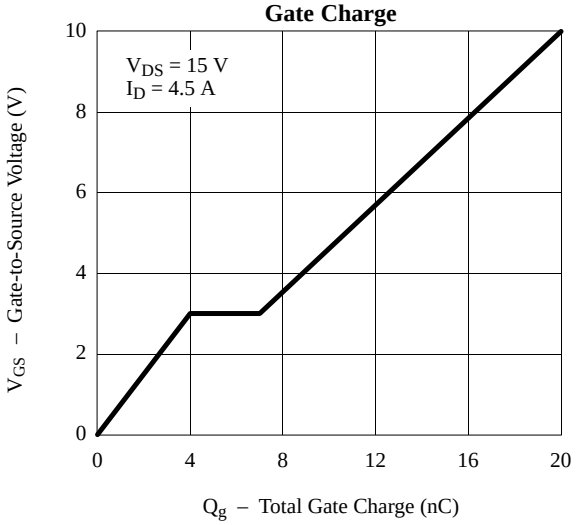

**On-Resistance vs. Drain Current**



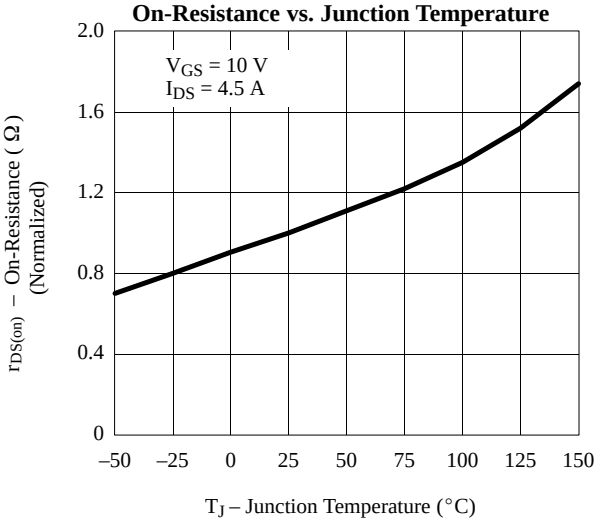

**Capacitance**




**Gate Charge**

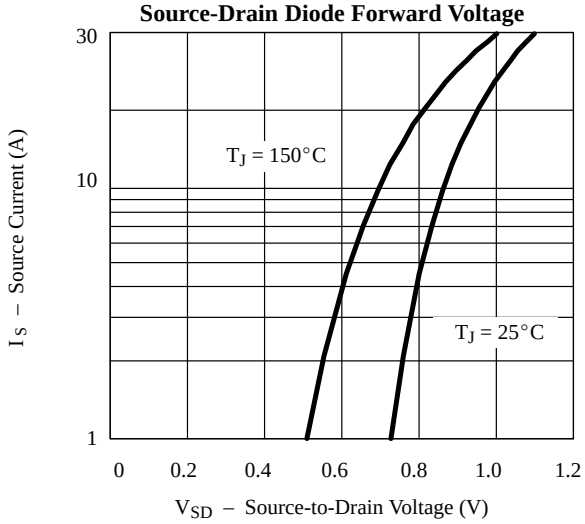



**On-Resistance vs. Junction Temperature**

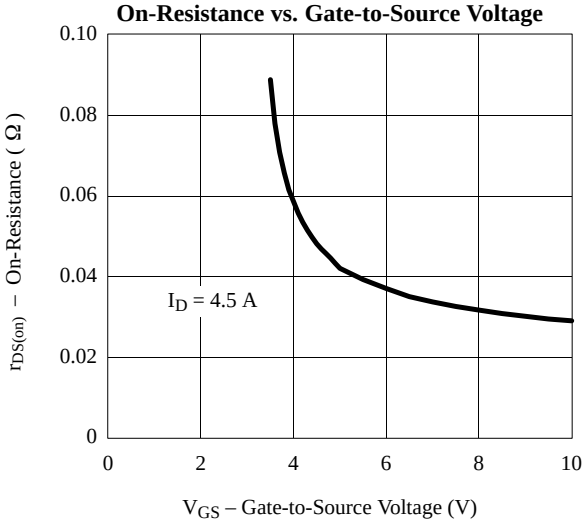


## Typical Characteristics (25°C Unless Noted)

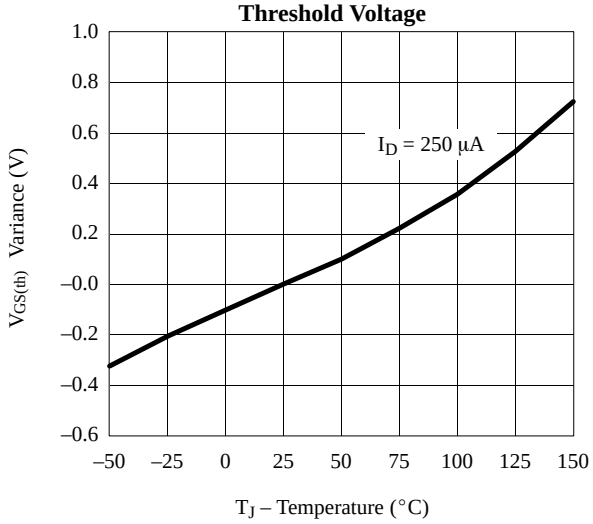
**Source-Drain Diode Forward Voltage**



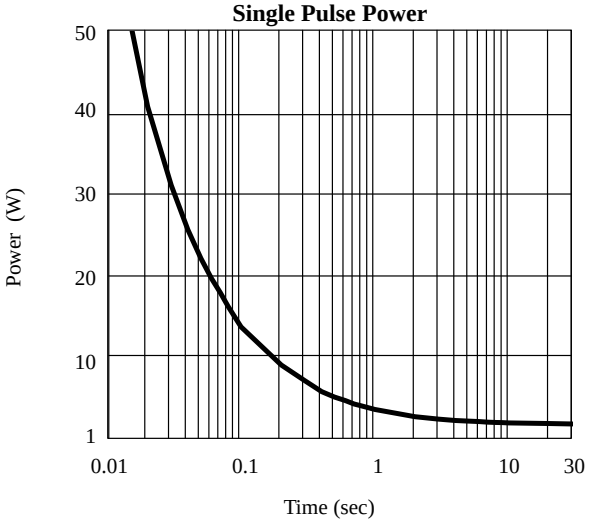

**On-Resistance vs. Gate-to-Source Voltage**




**Threshold Voltage**




**Single Pulse Power**




**Normalized Thermal Transient Impedance, Junction-to-Ambient**