DATA SHEET

SA3600
Low voltage dual-band RF front-end

Preliminary specification

1999 Mar 18

Philips
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Low voltage dual-band RF front-end SA3600

DESCRIPTION

The SA3600 is an integrated dual-band RF front-end that operates at both cellular (AMPS, GSM and TDMA) and PCS/DCS (TDMA and GSM) frequencies, and is designed in a 20 GHz f_T BiCMOS process—QUBiC2. The low-band (LB) is a combined low-noise amplifier (LNA) and mixer. The LNA has a 1.7 dB noise figure (NF) at 881 MHz with 17 dB of gain and an IIP3 of –7 dBm. The wide-dynamic range mixer has a 10 dB NF at 881 MHz with 10 dB of gain and an IIP3 of +6 dBm.

The high-band (HB) is a combined low-noise amplifier (LNA) and mixer, with the low-band and high-band mixers sharing the same mixer output. The LNA has a 2.2 dB NF at 1960 MHz with 16 dB of gain and an IIP3 of –6 dBm. The wide-dynamic range mixer has a 8.5 dB NF at 1960 MHz with 9.5 dB of gain and an IIP3 of +4 dBm.

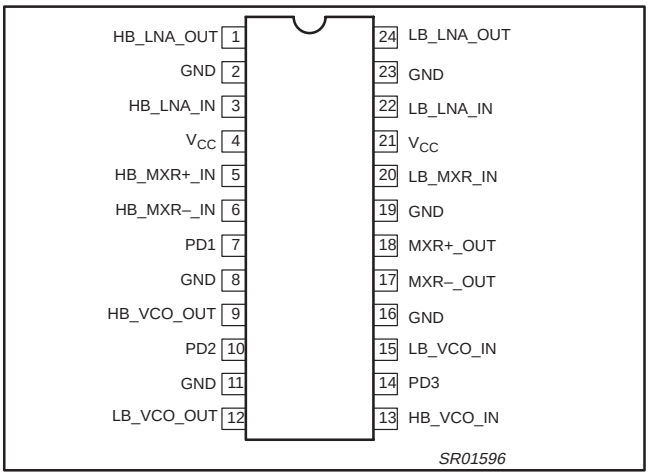
FEATURES

- Low current consumption: LB I_{CC} = 13.5 mA; HB I_{CC} = 15 mA
- Outstanding low- and high-band noise figure
- Excellent gain stability versus temperature and supply
- LO input and output buffers
- Frequency doubler
- On chip logic for network selection and power down
- Very small outline package

APPLICATIONS

- 800 to 1000 MHz analog and digital receivers
- 1800 to 2000 MHz digital receivers
- Portable radios
- Digital mobile communications equipment

PIN CONFIGURATION



ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SA3600	TSSOP24	Plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355–1

PIN DESCRIPTIONS

PIN NO.	PIN NAME	DESCRIPTION	PIN NO.	PIN NAME	DESCRIPTION
1	HB_LNA_OUT	Highband LNA output	13	HB_VCO_IN	Highband VCO input
2	GND	Ground	14	PD3	Power down control 3
3	HB_LNA_IN	Highband LNA input	15	LB_VCO_IN	Lowband VCO input
4	Vcc	Power supply	16	GND	Ground
5	HB_MXR+_IN	Highband mixer positive input	17	MXR–_OUT	Mixer negative output
6	HB_MXR–_IN	Highband mixer negative input	18	MXR+_OUT	Mixer positive output
7	PD1	Power down control 1	19	GND	Ground
8	GND	Ground	20	LB_MXR_IN	Lowband mixer input
9	HB_VCO_OUT	Highband VCO buffered output	21	V_{CC}	Power supply
10	PD2	Power down control 2	22	LB_LNA_IN	Lowband LNA input
11	GND	Ground	23	GND	Ground
12	LB_VCO_OUT	Lowband VCO buffered output	24	LB_LNA_OUT	Lowband LNA output

BLOCK DIAGRAM

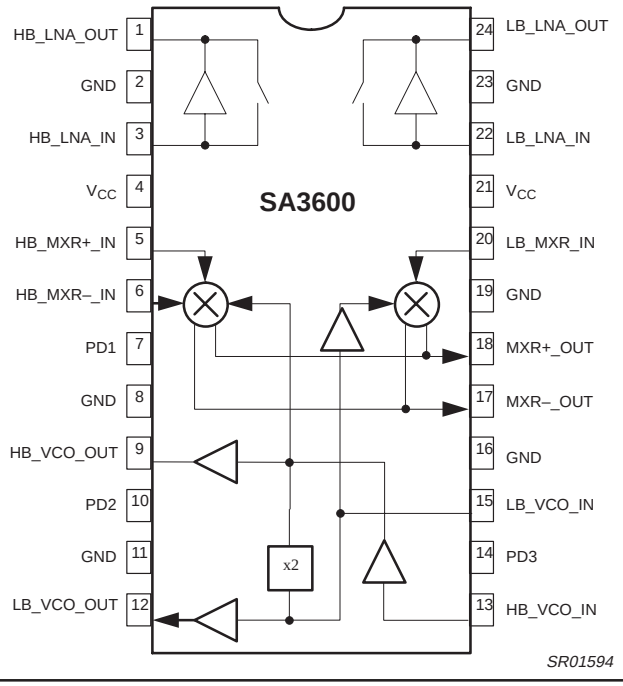


Figure 1. Block Diagram

MODE SELECT LOGIC

PD1	PD2	PD3	OPERATING MODE	Cel LNA	Cel MXR	PCS LNA	PCS MXR	x2 DBL	LB LO O/P	HB LO O/P
0	0	0	Sleep mode	off	off	off	off	off	off	off
0	0	1	Tx mode, LO lowband buffer	off	off	off	off	off	on	off
0	1	0	Rx mode cellular, low gain	off	on	off	off	off	on	off
0	1	1	Rx mode cellular, high gain	on	on	off	off	off	on	off
1	0	0	Rx mode PCS, low gain, x2	off	off	off	on	on	on	off
1	0	1	Rx mode PCS, high gain, x2	off	off	on	on	on	on	off
1	1	0	Rx mode PCS, low gain, no x2	off	off	off	on	off	off	on
1	1	1	Rx mode PCS, high gain, no x2	off	off	on	on	off	off	on

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	LIMITS		UNITS
		MIN.	MAX.	
V_{CC}	Supply voltage	–0.3	+6	V
V_{IN}	Voltage applied to any other pin	–0.3	V_{CC}+0.3	V
P_N	Power dissipation, T_A = +25 °C (still air)		TBD	mW
$T_{J\ MAX}$	Maximum junction temperature		TBD	°C
P_{MAX}	Power input/output		TBD	mW
I_{MAX}	DC current into any I/O pin	–10	+10	mA
T_{STG}	Storage temperature range	–65	+150	°C
T_O	Operating temperature	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all Input/Output ports are single–ended.

DC PARAMETERS

V_{CC} = +3.0V, T_A = +25°C unless otherwise noted

SYMBOL	PARAMETER	TEST CONDITIONS			LIMITS			UNIT
		PD1	PD2	PD3	MIN	TYP	MAX	
I_{CC}	Sleep mode	0	0	0		1		µA
	Tx mode, LO lowband buffer	0	0	1		3.1		mA
	Rx mode cellular, low gain	0	1	0		9.1		mA
	Rx mode cellular, high gain	0	1	1		13		mA
	Rx mode PCS, low gain, x2	1	0	0		16.2		mA
	Rx mode PCS, high gain, x2	1	0	1		21		mA
	Rx mode PCS, low gain, no x2	1	1	0		14.6		mA
	Rx mode PCS, high gain, no x2	1	1	1		19.5		mA
V_{IH}	Input HIGH voltage				0.5xV_{CC}		V_{CC}+0.3	V
V_{IL}	Input LOW voltage				–0.3		0.2xV_{CC}	V
I_{BIAS}	Input bias current	Logic 1 or logic 0			–5		+5	µA

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.0V, f_{RF} = 881 MHz, f_{LO} = 963 MHz, T_A = +25°C, over specified frequency range, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Lowband LNA Section						
f_{RF}	RF input frequency range		869		960	MHz
G_{ENA}	Small signal gain ENABLED			17		dB
NF_{ENA}	Noise figure ENABLED			1.7	2.0	dB
$IIP3_{ENA}$	Input 3rd order Intercept Point			–7		dBm
$P1dB_{ENA}$	Input 1dB Compression Point			–17		dBm
G_{BYP}	Small signal gain BYPASSED			–15		dB
NF_{BYP}	Noise figure BYPASSED			15		dB
$IIP3_{BYP}$	Input 3rd order Intercept Point			10		dBm
Z_{IN}	Input return loss	50Ω system		10		dB
Z_{OUT}	Output return loss	50Ω system		10		dB
T_{SW}	ENABLE/DISABLE speed				20	µs
Lowband Mixer Section						
f_{RF}	RF input frequency range		869		960	MHz
f_{IF}	IF output frequency range		70		200	MHz
f_{LO}	LO input range		939		1160	MHz
G_{MXR}	Small signal gain	P_{LO} = –5 dBm	9	10	11	dB
NF_{MXR}	Noise figure	P_{LO} = –5 dBm		9.5	10	dB
$IIP3_{MXR}$	Input 3rd order Intercept Point	P_{LO} = –5 dBm	4	6		dBm
$P1dB_{MXR}$	Input 1dB Compression Point	P_{LO} = –5 dBm		–16		dBm
P_{LO}	LO input power range		–7	–5	–3	dBm
Z_{IN}	Input return loss	50Ω system		10		dB
Z_{OUT}	Output return loss	50Ω system		10		dB
2–Tone	Two–tone spurious rejection: $2(f_{RF}–f_{Tx})$, $f_{RF}–f_{Tx}=f_{IF}/2$ $3(f_{RF}–f_{Tx})$, $f_{RF}–f_{Tx}=f_{IF}/3$	PLO = –5 dBm f_{RF}=890.0MHz @–36dBm f_{Tx}=848.9MHz @–20dBm f_{RF}=876.3MHz @–36dBm f_{Tx}=848.9MHz @–20dBm		TBD	 –97	 dBm dBm
RF–LO	RF to LO isolation			TBD		dB
LO–RF	LO to RF isolation			27		dB
T_{SW}	ENABLE/DISABLE speed				20	µs
Lowband LO Buffer Section						
P_{LO}	LO Input frequency range		939		1160	MHz
P_{IN}	LO Input power	50Ω matched LB_VCO_IN	–7	–5	–3	dBm
P_{OUT}	LO Output power	50Ω matched LB_VCO_OUT	–9	–7	–5	dBm
Z_{IN}	Input return loss	50Ω system		10		dB
Z_{OUT}	Output return loss	50Ω system		10		dB
	Harmonic content	P_{LO} = –5 dBm		–20		dBc
T_{SW}	ENABLE/DISABLE speed				20	µs

AC ELECTRICAL CHARACTERISTICS (Continued)

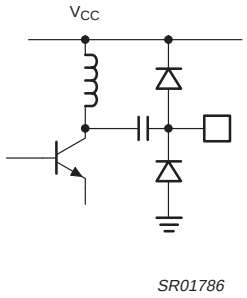
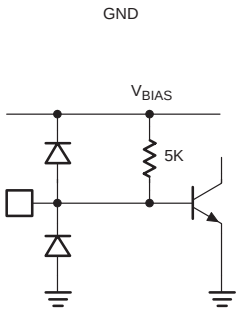
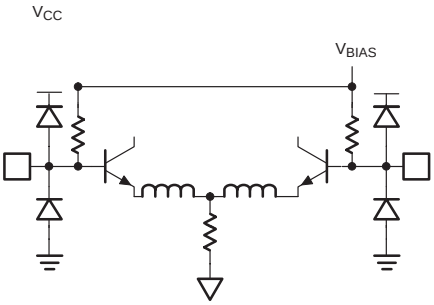
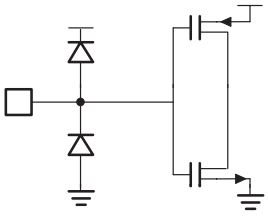
V_{CC} = +3.0V, f_{RF} = 1960 MHz, f_{LO} = 2042 MHz, T_A = +25°C, over specified frequency range, unless otherwise specified

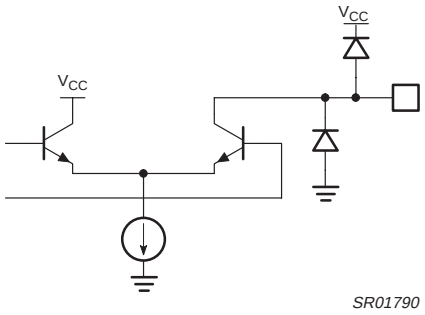
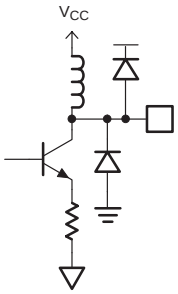
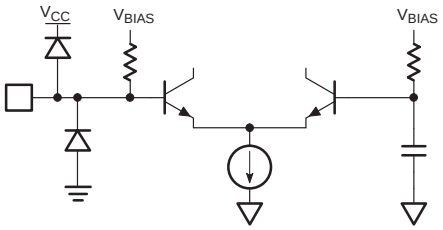
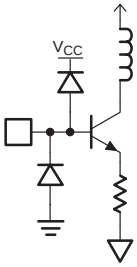
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Highband LNA Section						
f_{RF}	RF input frequency range		1805		1990	MHz
G_{ENA}	Small signal gain ENABLED		15	16	17	dB
NF_{ENA}	Noise figure ENABLED			2.2	2.5	dB
$IIP3_{ENA}$	Input 3rd order Intercept Point			–5		dBm
$P1dB_{ENA}$	Input 1dB Compression Point			–15		dBm
$IIP2_{ENA}$	Input 2nd order Intercept Point			20		dBm
G_{BYP}	Small signal gain BYPASSED			–15		dB
NF_{BYP}	Noise figure BYPASSED			15		dB
$IIP3_{BYP}$	Input 3rd order Intercept Point			10		dBm
Z_{IN}	Input return loss	50Ω system, ENA and BYP		10		dB
Z_{OUT}	Output return loss	50Ω system, ENA and BYP		10		dB
T_{SW}	ENABLE/DISABLE speed				20	µs
Highband Mixer Section						
f_{RF}	RF input frequency range		1805		1990	MHz
f_{IF}	IF output frequency range		70		200	MHz
f_{LO}	LO input range		1735		2190	MHz
G_{MXR}	Small signal gain	P_{LO} = –5 dBm	7.5	9	11	dB
NF_{MXR}	Noise figure	P_{LO} = –5 dBm		8.5		dB
	Noise figure, doubler on	P_{LO} = –5 dBm		9		dB
$IIP3_{MXR}$	Input 3rd order Intercept Point	P_{LO} = –5 dBm	2	5		dBm
	Input 3rd order Intercept Point, doubler on	P_{LO} = –5 dBm	2	4		dBm
$P1dB_{MXR}$	Input 1dB Compression Point	P_{LO} = –5 dBm		–16		dBm
IF/2 rej.	Half–IF spurious rejection $2(f_{RF}–f_{LO})$, $f_{RF}–f_{LO}=f_{IF}/2$	f_{RF}=1972.0MHz @–36dBm f_{LO}=2013.1MHz @–5dBm		26		dBm
IF/3 rej.	Third–IF spurious rejection $3(f_{RF}–f_{LO})$, $f_{RF}–f_{LO}=f_{IF}/3$	f_{RF}=1985.7MHz @–36dBm f_{Tx}=2013.1MHz @–5dBm			–97	dBm
2–Tone	Two–tone spurious rejection:	P_{LO} = –5 dBm,				
	$f_{RF}–fTx$, $fRF–fTx=fIF$	f_{RF}=1933.0MHz @–36dBm f_{Tx}=1850.8MHz @–20dBm		TBD		dBm
	$2(f_{RF}–fTx)$, $f_{RF}–fTx=f_{IF}/2$	f_{RF}=1951.0MHz @–36dBm f_{Tx}=1909.9MHz @–20dBm			–97	dBm
	$3(f_{RF}–fTx)$, $f_{RF}–fTx=f_{IF}/3$	f_{RF}=1937.3MHz @–36dBm f_{Tx}=1909.9MHz @–20dBm			–97	dBm
P_{LO}	LO input power range		–7	–5	–3	dBm
Z_{IN}	Input return loss	50Ω system		10		dB
Z_{OUT}	Output return loss	50Ω system		10		dB
RF–LO	RF to LO isolation	to LB VCO Output		TBD		dB
LO–RF	LO to RF isolation			27		dB
T_{SW}	ENABLE/DISABLE speed				20	µs

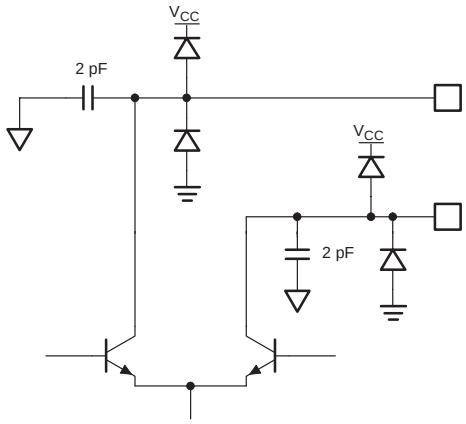
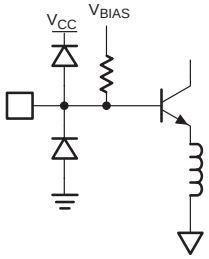
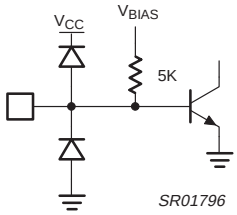
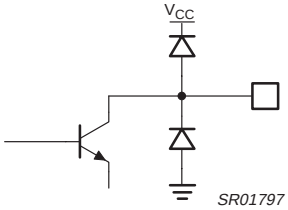
AC ELECTRICAL CHARACTERISTICS (Continued)

T_A = +25°C, V_{CC} = +3.0V, over specified frequency range, unless otherwise specified

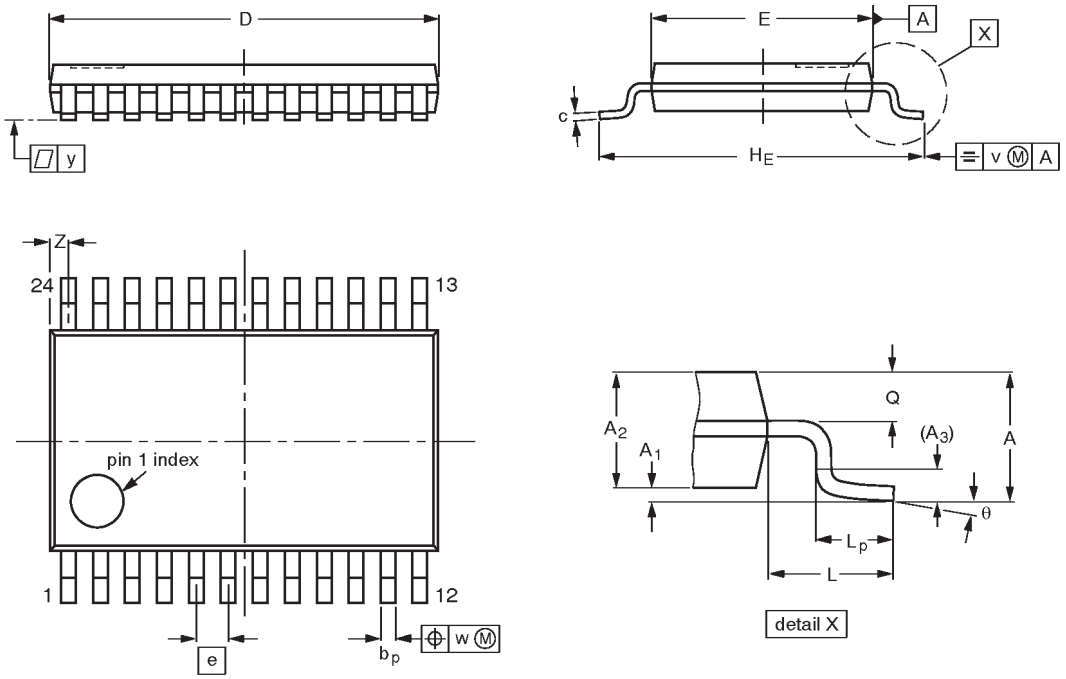
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Highband LO Buffer Section						
P_{LO}	LO Input frequency range		1735		2190	MHz
P_{IN}	LO Input power	50Ω matched HB_VCO_IN	–7	–5	–3	dBm
P_{OUT}	LO Output power	50Ω matched HB_VCO_OUT		–10		dBm
Z_{IN}	Input return loss	50Ω system		10		dB
Z_{OUT}	Output return loss	50Ω system		10		dB
	Harmonic content	P_{LO} = –5 dBm		–20		dBc
T_{SW}	ENABLE/DISABLE speed				20	µs
x2 LO Doubler Section						
f_{LO}	LO Input frequency		867.5		1095	MHz
P_{IN}	LO Input power	50Ω matched LB_VCO_IN	–7	–5	–3	dBm
Z_{IN}	Input return loss	50Ω system		10		dB
Z_{OUT}	Output return loss	50Ω system		10		dB
T_{SW}	ENABLE/DISABLE speed				20	µs

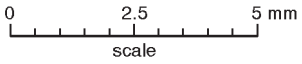
PIN NO	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
1	HB LNA OUT		 SR01786
2	GND		 SR01787
3	HB LNA IN	0.8	
4	V_{CC}		 SR01788
5	HB MXR+ IN	1.2	
6	HB MXR– IN	1.2	
7	PD1	Apply externally	 SR01789
10	PD2		
14	PD3		

PIN NO	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
9	HB VCO OUT	Pull-up externally to V_{CC}	 SR01790
12	LB VCO OUT	V_{CC} – 0.2 V	 SR01791
13	HB VCO IN	1.9	 SR01792
15	LB VCO IN	1.0	 SR01793

PIN NO	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
17	MXR– OUT	Pull-up externally to V_{CC}	 SR01794
18	MXR+ OUT		
20	LB MXR IN	1.2	 SR01795
22	LB LNA IN	0.8	 SR01796
24	LB LNA OUT	Pull-up externally to V_{CC}	 SR01797

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153AD				~~93-06-16~~ 95-02-04

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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