SGS-THOMSON MICROELECTRONICS

QN110 QUALITY NOTE

HIGH RELIABILITY OTP MEMORY PROGRAMMING

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OTP Memory is a type of EPROM (Electrically Programmable Read Only Memory) packaged in plastic packages. This allows them to be made in surface mount as well as through hole, Dual-in-Line style, packages. Unlike UV EPROM which has a quartz window in the package above the chip to allow erasure by UV light, OTP Memory can not be erased once it has been programmed.

The use of OTP Memory products is growing because of their distinct advantages:

– surface mounting packages, like PLCC and TSOP;
– lower cost compared to FLASH Memory, which they can replace directly in many mature applications;
– higher densities which can replace mask ROMs, offering more flexibility for programming;
– ability to be programmed in the application.

Recent developments and innovations in OTP Memory have greatly enhanced the product performance in two key areas: the reliability of programming and the ability to program the memory after mounting on the application board, known as "On Board Programming".

Figure 1. Quality Results for OTP Memory Programming

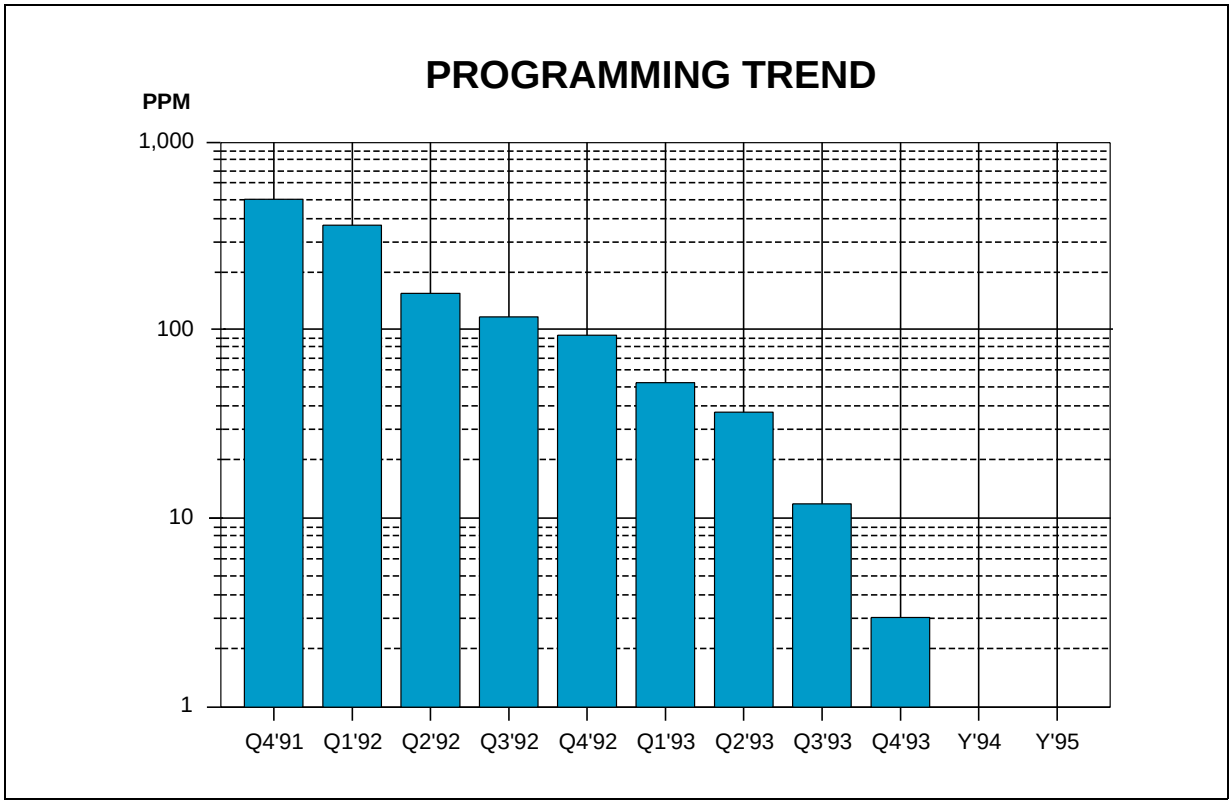


Figure 2. Previous OTP Memory cell programming conditions

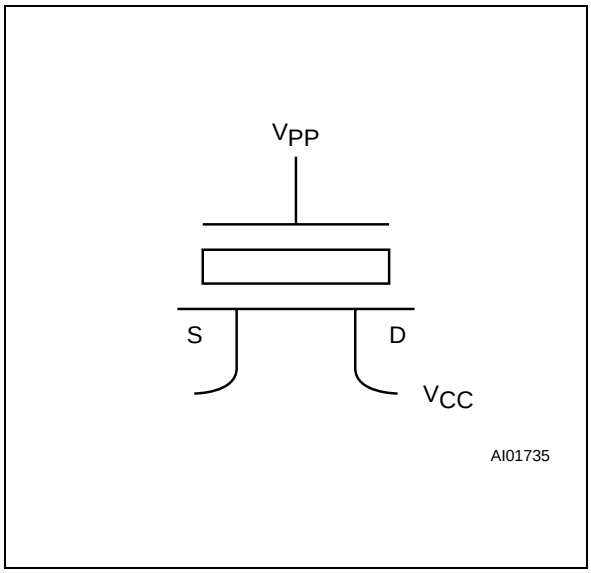
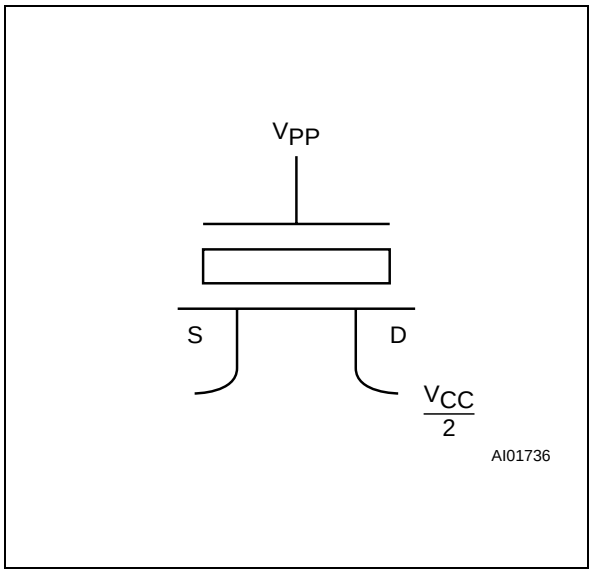


Figure 3. Innovative OTP Memory cell programming conditions



Reliable Programming

Unlike UV EPROM which can be completely programmed during product testing and subsequently erased before shipment to customers, OTP Memory can be programmed only once, by the customer, for the application. To overcome this limitation and allow the OTP Memory to be tested both for programming and for access time selection, extra spare memory cells are included in the design of the memory. These rows and columns of cells are accessible only by the testing programs in a special test mode.

Every production lot of OTP Memory passes a Quality Control Gate which verifies the matrix programming on these extra spare cells. The test flow is as follows:

– Programming using a chess board pattern of zeros and ones. This pattern is one of the most severe as it is able to reveal any interference or short circuits between adjacent bits. It is also the best for testing the access time of the memory since there is an alternating change in the output data read as the addresses are scanned.
– Pattern verification, AC and DC measurements, at 25°C and 70°C.

Reliability Results

Following improvements in the product processing and die and finished product testing procedures, the programming results obtained over the last year has been zero rejects for 133,000 pieces tested. This is equivalent to a statistical failure rate of 6.8 ppm with a 60% confidence level or 17 ppm at 90% confidence.

The long term trend of quality improvement since the beginning of 1991 is shown in Figure 1.

OTP Memory Design for Programming

One of the most important innovations in the design of OTP Memory has been that the programming is independent of the V_{CC} supply voltage.

Previous OTP Memory designs, see Figure 2, used the V_{PP} programming voltage applied to the gate of the cell, and an increased V_{CC} (from the normal operating level of 5V to a value of 6.25V in the programming mode). These voltages generate a cloud of hot electrons in the MOS transistor channel, with enough energy to jump over the oxide potential barrier and land on the floating gate. The accumulated charge on the floating gate programs the cell contents.

The innovative OTP Memory design replaces the V_{CC} supply to the cell during programming with a voltage derived from the V_{PP} programming supply, divided by two. The programming is dependent only on the V_{PP} programming voltage and is independent of the V_{CC} supply voltage.

This innovation means that OTP Memory can be programmed in the application board where a V_{CC} supply of only 5V is available. It also opens up applications, such as automotive engine control systems, which must update the memory contents, storing new values for system tables, during the operation of the equipment.

For reasons of compatibility this ability to be programmed independent of the V_{CC} supply is not reported on the data sheets of the product: this avoids possible conflict and uncertainty about the need for updating of existing commercial programer software and setup. The OTP Memory can, of course, be programmed at the data sheet conditions with V_{CC} at 6.25V.