# Quality Flows

## Digital ICs Products

This document presents the flows used in manufacturing and screening of TEMIC Digital ICs (Microcontrollers, Memories, ASICs and ASSPs).

## Process Control

As shown in the following tables, each device is constructed by manufacturing processes which are under the surveillance of the TEMIC Quality organization. Control of these processes is maintained by the use of statistical techniques such as capability studies and SPC. Results are computerized in accordance with standards, internal specifications, and procedures.

Audits and "self-audits" are used extensively to continuously improve quality by implementing corresponding corrective actions.

TEMIC prepares and maintains suitable documentation covering all phases of conception and manufacturing. The customer may verify that suitable documentation exists and is being applied. Information designated as "Proprietary" will be made available to the customer or its representative only with the written permission of TEMIC.

Process control is recognized as a vital part of the concept of "built-in quality". In addition to formal inspections, TEMIC implements various monitoring systems such as scanning electron microscope (SEM) and glassivation layer integrity.

## Wafer Fabrication: Quality Control Flow Chart

| Process Step | Typical Item | Frequency | Sampling |
|---|---|---|---|
| Incoming Inspection of Silicon Wafers | Resistivity, Bow, TTV, Flatness Oxygen Content, Thickness, Particles | Monthly Monitoring of Each Supplier | 22 Wafers/Lot |
| Incoming Inspection of Masks and Reticules | Defects + Conformity | Every Mask and Reticule | |
| | Dimensions + Registration | Weekly Monitoring of Each Supplier | |
| Oxidation | Thickness | Every Run | 3 Wafers/Run<br>3 Parts/Wafer |
| | C(V) | Monitoring | |
| Ion Implant | Therma-Wave (+ Resistivity) | Every Lot | 2 Wafers/Lot |
| Diffusion | Thickness | Every Run | 3 Wafers/Run<br>3 Parts/Wafer |
| Si-Nitride Deposition and Etching | Thickness | Every Run | 3 Wafers/Run<br>5 Parts per Wafer |
| | Critical Dimensions | Every Lot | 3 Wafers/Run<br>5 Parts per Wafer |
| Gate-Oxidation | Thickness<br>Vfb + Delta Vfb | Every Run | 3 Wafers/Run<br>3 Parts per Wafer |
| | C(V) | Every Run | 1 Wafers/Run<br>1 Parts per Wafer |
| Polysilicon Deposition and Etching | Thickness | Every Run | 3 Wafers/Run<br>3 Parts per Wafer |
| | Critical Dimensions | Every Lot | 3 Wafers/Run<br>5 Parts per Wafer |
| | SEM Inspection | Monitoring / 100% | |

# Quality Flows

## Wafer Fabrication: Quality Control Flow Chart

| Process Step | Typical Item | Frequency | Sampling |
|---|---|---|---|
| Metal Deposition and Etching | Resistivity | Every Week | 1 Wafer |
| | Reflectivity | Every Shift | |
| | Thickness | Every Lot | 1 Wafer/Lot<br>5 Parts/Wafer |
| | Critical Dimensions | Every Lot | 3 Wafers/Lot<br>5 Parts on the 3 Wafers |
| | SEM Inspection | Monitoring /100% | |
| Glassivation Deposition and Etching | Thickness | Every Run | 1 Wafer/Run<br>3 Parts/Wafer |
| | Stress | Every Run | 1 Wafer/Run |
| | SEM Inspection | Monitoring/100% | |
| Test Site | Electrical Parameters | Every Lot/visual inspenction all lots | 100% Wafers<br>3 or 5 Site/Wafer |
| Wafer-Sort | Functional Test | Every Lot | 100% Wafers<br>100% Dice |
| QC Visual Inspection | Visual Defects | Monitoring/100% | 5 Wafers/Lot |
| Lot Acceptance | | SPC results/Gate all lots | 5 Wafers/Lot |

Note: QA representatives may audit operations at any time.

## Assembly: Quality Control Flow Chart

Various assembly process flows are used :

- L0: MIL-STD-883 Class B Compliant Hermetic Assembly
- L1, L2: MIL–STD–883 Class S / ESA SCC 9000 Space Hermetic Assembly
- L3: TEMIC/MHS Military Hermetic Assembly
- L4: Commercial/Industrial/Automotive Plastic Assembly
- L6: Prototype Hermetic Assembly
- L7: Commercial/Industrial/Automotive Hermetic Assembly

Note: QA representatives may audit operations at any time.

## Hermetic Assembly: Quality Control Flow Chart

| Process Step | Typical Item | Frequency per Process | | | | Method |
|---|---|---|---|---|---|---|
| | | L1 / L2 | L0 | L3 | L7 | |
| Incoming Inspection | Base/Frame/ Caps/Bonding- Materials/Wires | Every Raw Material Lot | | | | TEMIC/MHS Spec SCC9000 |
| First Optical | Visual | Every Lot/100% Wafers | | | | TEMIC/MHS Spec |
| 2nd Optical Inspection QA | Visual | 100% Cond. A[1] | 100% Cond. B[1] | AQL = 0.4% | | [1]MIL-2010 TEMIC/MHS Spec |
| SEM Inspection | | Every Lot* | – | | | MIL-2018 SCC21400 |
| QC Inspection AQL = 0.4% | Visual | Every Lot Cond. A[1] | Every Lot Cond. B[1] | Monitoring | NA | [1]MIL-2010 TEMIC/MHS Spec |
| Die-Bonding | Visual | Same As Second Optical | | | | MIL-2010 |
| | Die-Shear | 4# per Lot | | | | MIL-2019 |
| | Stud-Pull | 7# per Lot | | | | MIL-2027 |
| | X-Ray | 100% | 10# per Lot | | NA | MIL-2012 |
| QC Inspection AQL = 0.4% | Visual | Every Lot Cond. A[1] | Every Lot Cond. B[1] | Monitoring | NA | [1]MIL-2010 TEMIC/MHS Spec |
| Wire-Bonding | Visual | 100% Cond. A[1] | 100% Cond. B[1] | 100% | 100% | [1]MIL-2010/ TEMIC/MHS Spec |
| | Bond-Pull | 4#/40 Wires/Every Lot | | | | MIL-2011 |
| | Loop-Height | 5#/Every Lot | | | | TEMIC/MHS Spec |
| QC Inspection AQL = 0.4% | Visual | Every Lot Cond. A[1] | Every Lot Cond. B[1] | Monitoring | NA | [1]MIL-2010 TEMIC/MHS Spec |
| Third Optical | Visual (die) | 100% Cond. A[1] | 100% Cond. B[1] | AQL= 0.4% | NA | [1]MIL-2010 TEMIC/MHS Spec |
| QC Inspection AQL = 0.4% | Visual | Every Lot Cond. A[1] | Monitoring Cond. B[1] | Monitoring | NA | [1]MIL-2010 TEMIC/MHS Spec |
| Prestab Bake Sealing Stabilization Bake | Visual (L2 only) | 100% on Every Lot | | | | TEMIC/MHS Spec |
| Thermal Cycling | | Every Lot | | | | MIL-1010 Cond. C (x5 cycles for L7) |
| Constant Acceleration | Visual | 22# on Every Lot | | | NA | MIL-2001 Cond. E |
| Trimming/Forming | Visual and Dimensional | 1% on Every Lot | | | | MIL-2009 + SCC20500 |
| Solder-Dip | Visual Thickness | 100% on Every Lot 5# per Lot | | | | MIL-2009 |
| PIND Test | | 100% on Every Lot* | Monitoring | | NA | MIL-2020 |
| Fine/Gross Leak | | 100% on Every Lot | | | LTPD 1% | MIL-1014 |
| Marking (back-side) | Visual | 100% on Every Lot | | | | TEMIC/MHS Spec |
| Final Inspection | Visual | 100% on Every Lot | Every Lot LTPD = 2 | AQL = 0.4% | LTPD 7% | MIL-2009 + SCC 20500 |
| QC Inspection AQL = 0.4% | Visual | Every Lot | Monitoring | | NA | MIL-2009 + SCC 20500 |

* : L2 process only.

## Plastic Assembly: Quality Control Flow Chart

| Process Step | Typical Item | Frequency | Sampling |
|---|---|---|---|
| Incoming Inspection | Frame/Resin/Bonding-Materials/ Wires<br>...Thickness, Particles | Every Raw Material Lot | |
| 1st Optical Inspection<br>QA | Visual | Every Lot/Sampling | TEMIC/MHS Spec<br>AQL 0.65% or Lower |
| Dicing | DI Water<br>Kerf Width<br>Visual | SPC | |
| 2nd Optical Inspection<br>QA | Visual | Every Lot/Sampling | TEMIC/MHS Spec<br>AQL 0.65% or Lower |
| Die Bonding | Visual<br>Die-Shear<br>Cure Temperature | SPC | |
| Wire Bonding | Visual<br>Bond-Pull<br>Ball-Shear<br>Bond Crater | SPC | |
| 3rd Optical Inspection<br>QA | Visual | Every Lot/Sampling | TEMIC/MHS Spec<br>AQL 0.65% or Lower |
| Molding | X-Ray<br>Step Temperature and Time | SPC | |
| Marking (top side)<br>Optional | Visual<br>Cure-Temperature<br>Permanency | SPC | |
| Solder Plating | Composition<br>Thickness<br>Solderability | SPC | |
| Marking (back-side) | Visual | SPC | |
| Trimming/Forming | Visual<br>Dimensional incl. Coplanarity | SPC | |
| Final Inspection<br>QA | Visual<br>Coplanarity | Every Lot/Sampling | TEMIC/MHS Spec<br>AQL 0.1% |
| Electrical Test | Open/Shorts | Monitoring | TEMIC/MHS Spec |

Note: QA representatives may audit operations at any time.

## Die Form: Quality Control Flow Chart

All products are available in die form (sawn or unsawn) upon request.
They are screened either using TEMIC standards or MIL and SPACE standards (DB, PS flows).

### All flows except DB and PS

Several screening levels are defined leading to guarantee the performance of the products over the whole temperature range from 90 to 95% for 1st level up to 100% for KGD level.
In addition to that, the KGD level assures to keep under control the early failure rate level with the appropriate screening.

| Process Step | Typical Item | Frequency | Sampling |
|---|---|---|---|
| Wafer Fab<br>Test Site | See Fab Control Flow Chart<br>Electrical Characterization | 100% Wafers/5 PCM | |
| Probe | 1st level<br>2nd level<br>KGD level | 100% dice<br>1 or 2 probes<br>EFR screening | |
| Dicing (Die Form)<br>(Sawn Wafer) | Visual | 100% Wafers | MIL-2010 Cond. B |
| Optical Inspection<br>QA | Visual | Every Lot/Sampling<br>AQL 0.4% | MIL-2010 Cond. B |
| Lot Acceptance<br>Sample Assembly | | Optional | Flow L6 |
| Lot Acceptance Test | | Optional | TEMIC/MHS Spec |

### DB Flow (compliant MIL–Std 883 level B)

| Process Step | Typical Item | Frequency | Sampling |
|---|---|---|---|
| Wafer Fab<br>Test Site | See Fab Control Flow Chart<br>Electrical Characterization | 100% Wafers/5 PCM | |
| Die Sorting | Static/Dynamic Functional Tests<br>Visual | 100% Wafers<br>10% Wafers | TEMIC/MHS Spec<br>TEMIC/MHS Spec |
| Dicing | Visual | 100% Dice | MIL-2010 Cond. B |
| Optical Inspection<br>QA | Visual | Every Lot/Sampling | MIL-2010 Cond. B<br>AQL = 0.4% |
| Lot Acceptance<br>Sample Assembly | | | Flow L0 |
| Mechanical Conformance | Bond Pull<br>Die Shear | 5 Parts - 10 Wires<br>3 Parts | MIL-2011<br>MIL-2019 |
| Electrical Conformance | Acc. to Specification | LTPD 10 – C = 1 | @ 25, 125, –55°C |

## PS Flow (compliant MIL–Std 883 class S or ESA/PSS01608)

| Process Step | Typical Item | Frequency | Sampling |
|---|---|---|---|
| Wafer Fab<br>Test Site | See Fab Control Flow Chart<br>Electrical Characterization | 100% Wafers/5 PCM | |
| Die Sorting | Static/Dynamic Functional Tests<br>Visual | 100% Wafers<br>10% Wafers | TEMIC/MHS Spec<br>TEMIC/MHS Spec |
| Dicing | Visual | 100% Dice | MIL-2010 Cond. A |
| Optical Inspection<br>QA | Visual | Every Lot/Sampling | MIL-2010 Cond. B<br>AQL = 0.4% |
| Lot Acceptance<br>Sample Assembly | | | Flow L2 |
| Mechanical Conformance | Bond Pull<br>Die Shear | 5 Parts - 10 Wires<br>3 Parts | MIL-2011<br>MIL-2019 |
| Electrical Conformance | Acc. to Specification | Acc. See QON level B or<br>MIL 883 class S | |

## Product Flows

TEMIC offers a broad range of screening flows, such as commercial, industrial, automotive, military and space. Methods associated with each step are covered by TEMIC procedures or procedures defined in standards (MIL-STD-883) depending on the flow. The following tables describe these flows.

## Commercial/Industrial/Automotive

| | Commercial 0 to 70°C | | Industrial −40 to 85°C | | Automotive −40 to 125°C | |
|---|---|---|---|---|---|---|
| | | with Burn In | | with Burn In | | with Burn In |
| **Flows per Family** | | | | | | |
| ASICs | –5 | –Q | –9 | –N | –A | |
| Memories | –5 | –Q | –9 | –N | –A | |
| New Memories | CMx—— | CMX——D | IMx—— | IMx——D | AMx—— | AMx——D |
| Microcontrollers | _xxxxx | Qx—— | Ix——— | Lx——— | Ax——— | |
| **Process Steps** | | | | | | |
| QA Wafer Inspection | Monitoring | Monitoring | Monitoring | Monitoring | Monitoring | Monitoring |
| Assembly Flow | L4/L7 | L4/L7 | L4/L7 | L4/L7 | L4/L7 | L4/L7 |
| Marking | Test Date Code | Test Date Code | Test Date Code | Test Date Code | Test Date Code | Test Date Code |
| Serialization | — | — | — | — | — | — |
| Pre Burn-In Test | — | — | — | — | — | — |
| Dynamic Burn-In | — | 100% 24h/140°C or Equivalent | — | 100% 24h/140°C or Equivalent | — | 100% 24h/140°C or Equivalent |
| Electrical Test | | | | | | |
| • Room Temperature | — | — | — | — | — | — |
| • High Temperature | 100% | 100% | 100% | 100% | 100% | 100% |
| • Low Temperature | — | — | — | — | — | — |
| • Drift | — | — | — | — | — | — |
| • Electrical PDA | — | 5% | — | 5% | — | 5% |
| • QA Electrical Gate | AQL 0.065% | AQL 0.065% | AQL 0.065% | AQL 0.065% | AQL 0.065% | AQL 0.065% |
| Gross and Fine Leaks | — | — | — | — | — | — |
| X-Ray Inspection | — | — | — | — | — | — |
| External Visual | 100% | 100% | 100% | 100% | 100% | 100% |
| Global PDA | — | — | — | — | — | — |
| Electrical Conformation | Monitoring | Monitoring | Monitoring | Monitoring | Monitoring | Monitoring |
| Mechanical Conformation | Monitoring | Monitoring | Monitoring | Monitoring | Monitoring | Monitoring |
| Reliability Conformation | Monitoring | Monitoring | Monitoring | Monitoring | Monitoring | Monitoring |
| Customer Source Inspection | — | — | — | — | — | — |
| Certification of Compliance | — | — | — | — | — | — |
| Data Package | — | — | — | — | — | — |
| Shipping Inspection | All Deliveries | All Deliveries | All Deliveries | All Deliveries | All Deliveries | All Deliveries |

## Military and Space

| | Military –55 to 125°C | | Space –55 to 125°C | | |
|---|---|---|---|---|---|
| | TEMIC/MHS Mil Flow | SMD & MIL-883 Compliant | SCC 9000 Level C | SCC 9000 Level B | MIL-883 Class S |
| **Flows per Family** | | | | | |
| ASICs | –2 | .../883* | –SC | –SB | –MS |
| Memories | –2 | .../883* | –SC | –SB | –MS |
| New Memories | MMx—– | MMx—–/883* | SMx—–SC** | SMx—–SB** | SMx—–MS |
| Microcontrollers | Mx——– | Mx——–/883* | Mx—–SC** | Mx—–SB** | Mx—–MS |
| **Process Steps** | | | | | |
| Wafer fab. flow | Standard | Standard | HiRel | HiRel | HiRel |
| Assembly Flow | L3 | L0 | L1 | L2 | L2 |
| Marking | Test Date Code | Sealing Date Code | Sealing Date Code | Sealing Date Code | Sealing Date Code |
| Serialization | — | — | — | Yes | Yes |
| Pre Burn-In Test | — | 100% | 100% | 100% + Record | 100% + Record |
| Dynamic Burn-In | — | 100% 168h/125°C or Equivalent | 100% 168h/125°C | 100% 240h/125°C | 100% 240h/125°C or Equivalent |
| Electrical Test | | | | | |
| • Room Temperature | — | 100% | 100% | 100% + Record | 100% + Record |
| • High Temperature | 100% | 100% | 100% | 100% + Record | 100% + Record |
| • Low Temperature | 100% | 100% | 100% | 100% + Record | 100% + Record |
| • Drift | — | — | — | Yes | If Specified |
| • Electrical PDA | — | 5% @ Room Temp. | See Global PDA | See Global PDA | 5% @ Room Temp. (3% Functionnal) |
| • QA Electrical Gate | AQL 0.065% | NA | NA | NA | NA |
| Gross and Fine Leaks | — | — | 100% | 100% | 100% |
| X-Ray Inspection | — | — | — | 100% | 100% |
| External Visual | 100% | 100% | 100% | 100% | 100% |
| Global PDA | — | — | 5% | 5% | — |
| Electrical Conformation | Monitoring | Group A | LAT 3 | LAT 3 | Group A |
| Mechanical Conformation | Monitoring | Group B | LAT 3 | LAT 3 | Group B |
| Reliability Conformation | Monitoring | Group C/D | LAT 1 + 2 | LAT 1 + 2 | Group C/D |
| Customer Source Inspection | — | — | All Deliveries | All Deliveries | All Deliveries |
| Certification of Compliance | — | All Deliveries | All Deliveries | All Deliveries | All Deliveries |
| Data Package | — | All Deliveries | All Deliveries | All Deliveries | All Deliveries |
| Shipping Inspection | All Deliveries | All Deliveries | All Deliveries | All Deliveries | All Deliveries |

*Existing products in "–MB" flow keep their current name. Product under SMD reference use SMD drawing.
**Product under ESA SCC detail spec. reference use ESA SCC detail spec.