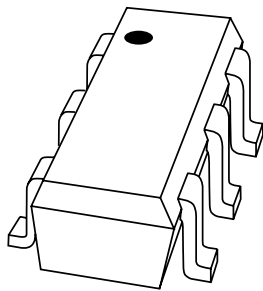


# DATA SHEET



## **PUMD9** NPN/PNP resistor-equipped transistors

Product specification  
Supersedes data of 1999 Jan 07

1999 May 20

# NPN/PNP resistor-equipped transistors

# PUMD9

### FEATURES

- Transistors with different polarity and built-in bias resistors R1 and R2 (typ. 10 kΩ and 47 kΩ respectively)
- No mutual interference between the transistors
- Simplification of circuit design
- Reduces number of components and board space.

### APPLICATIONS

- Especially suitable for space reduction in portable equipment
- Inverter circuit configurations without use of external resistors.

### DESCRIPTION

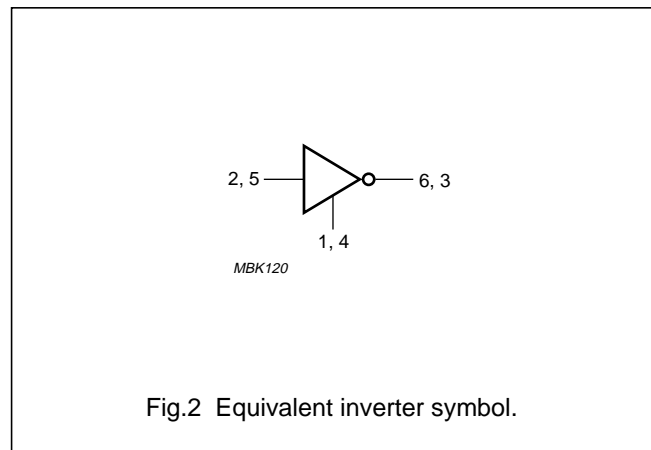
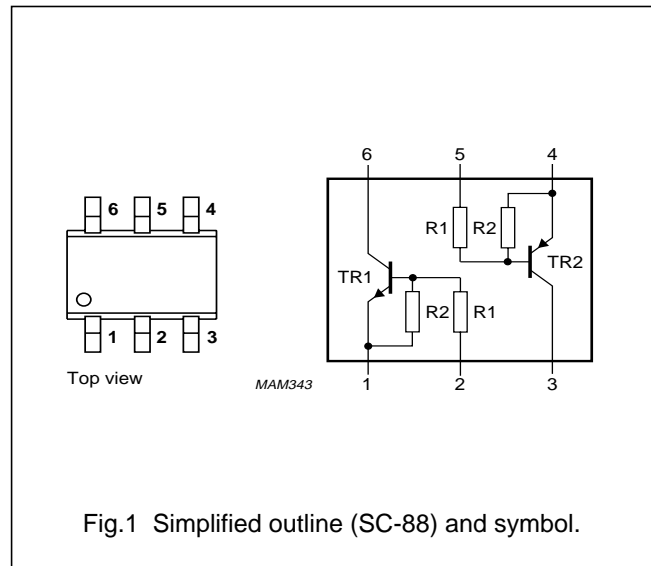
NPN/PNP resistor-equipped transistors in an SC-88 (SOT363) plastic package.

### PINNING

PIN	DESCRIPTION
1, 4	emitter TR1; TR2
2, 5	base TR1; TR2
6, 3	collector TR1; TR2

### MARKING

TYPE NUMBER	MARKING CODE
PUMD9	Dt9



## NPN/PNP resistor-equipped transistors

## PUMD9

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
<b>Per transistor; for the PNP transistor with negative polarity</b>					
V <sub>CBO</sub>	collector-base voltage	open emitter	–	50	V
V <sub>CEO</sub>	collector-emitter voltage	open base	–	50	V
V <sub>EBO</sub>	emitter-base voltage	open collector	–	10	V
V <sub>I</sub>	input voltage positive negative		–	+40	V
			–	–6	V
I <sub>O</sub>	output current (DC)		–	100	mA
I <sub>CM</sub>	peak collector current		–	100	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C; note 1	–	200	mW
T <sub>stg</sub>	storage temperature		–65	+150	°C
T <sub>j</sub>	junction temperature		–	150	°C
T <sub>amb</sub>	operating ambient temperature		–65	+150	°C
<b>Per device</b>					
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C; note 1	–	300	mW

**Note**

1. Refer to SC-88 standard mounting conditions.

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R <sub>th j-a</sub>	thermal resistance from junction to ambient	note 1	416	K/W

**Note**

1. Refer to SC-88 standard mounting conditions.

## NPN/PNP resistor-equipped transistors

## PUMD9

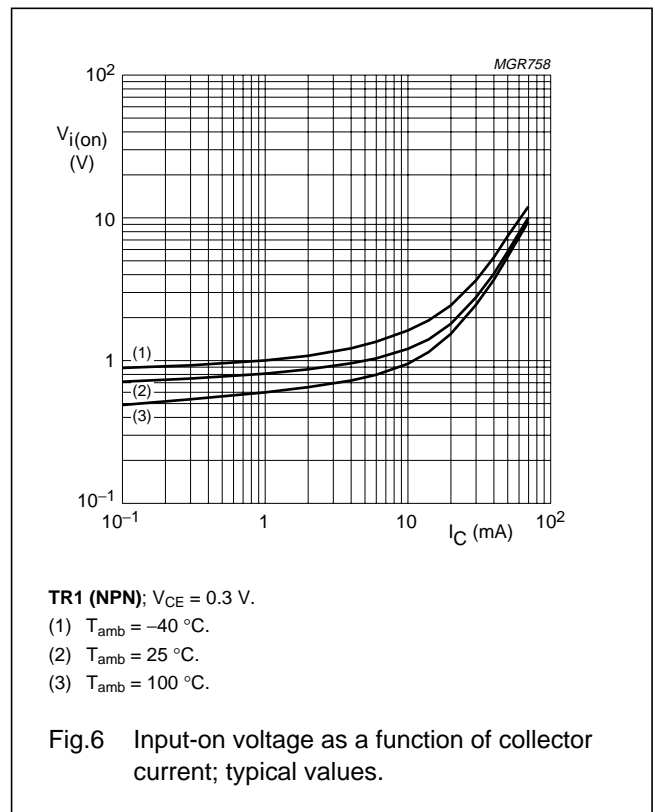
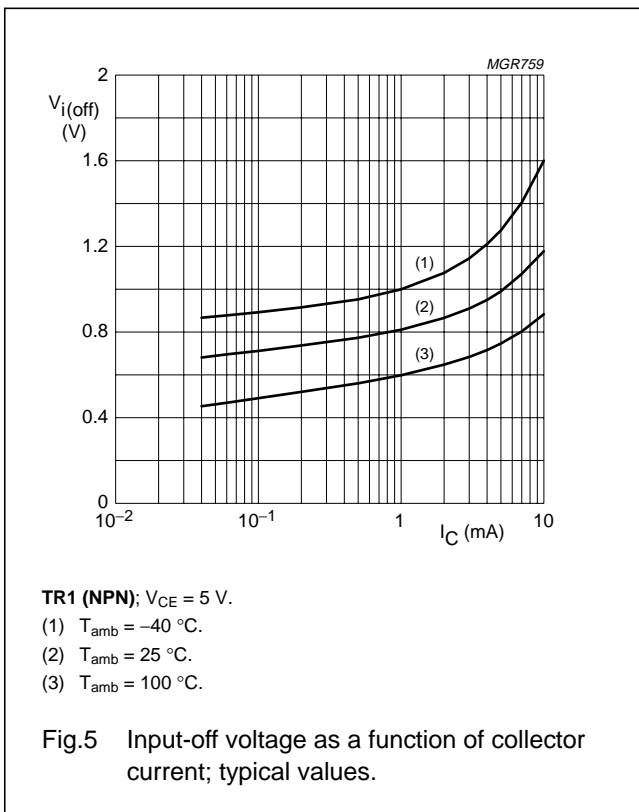
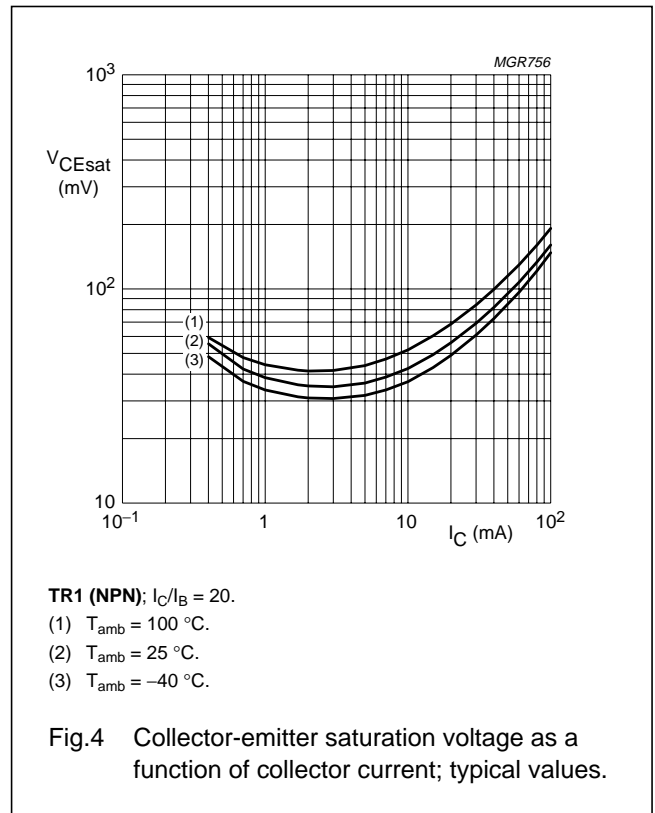
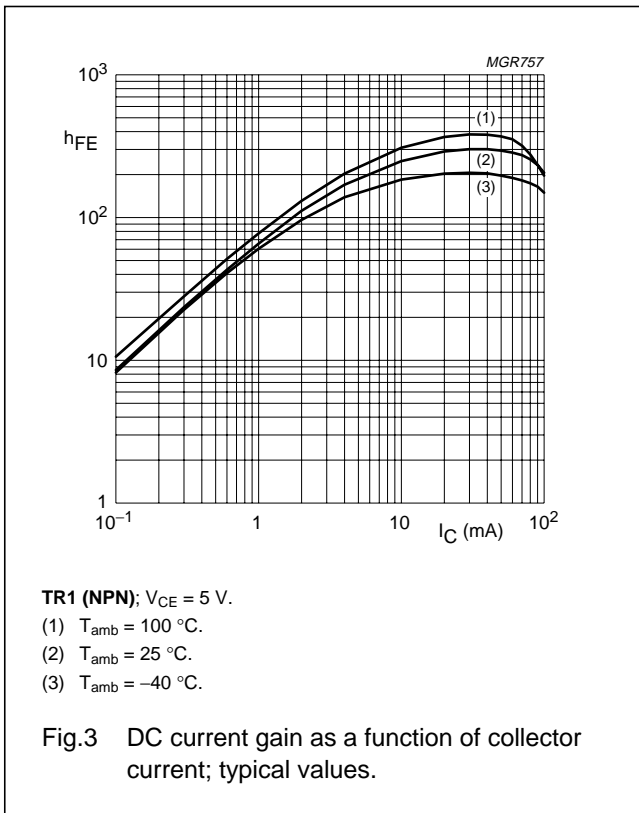
**CHARACTERISTICS**

$T_{amb} = 25\text{ °C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Per transistor; for the PNP transistor with negative polarity</b>						
$I_{CBO}$	collector cut-off current	$I_C = 0; V_{CB} = 50\text{ V}$	–	–	100	nA
$I_{CEO}$	collector cut-off current	$I_B = 0; V_{CE} = 30\text{ V}$	–	–	1	$\mu\text{A}$
		$I_B = 0; V_{CE} = 30\text{ V}; T_j = 150\text{ °C}$	–	–	50	$\mu\text{A}$
$I_{EBO}$	emitter cut-off current	$I_C = 0; V_{EB} = 5\text{ V}$	–	–	150	$\mu\text{A}$
$h_{FE}$	DC current gain	$I_C = 5\text{ mA}; V_{CE} = 5\text{ V}$	100	–	–	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = 5\text{ mA}; I_B = 0.25\text{ mA}$	–	–	100	mV
$V_{i(off)}$	input-off voltage	$I_C = 100\text{ }\mu\text{A}; V_{CE} = 5\text{ V}$	–	0.7	0.5	V
$V_{i(on)}$	input-on voltage	$I_C = 1\text{ mA}; V_{CE} = 0.3\text{ V}$	1.4	0.8	–	V
R1	input resistor		7	10	13	k $\Omega$
$\frac{R2}{R1}$	resistor ratio		3.7	4.7	5.7	
$C_c$	collector capacitance	$I_E = i_e = 0; V_{CB} = 10\text{ V}; f = 1\text{ MHz}$	–	–	2.5	pF
	TR1 (NPN)				3	
	TR2 (PNP)					

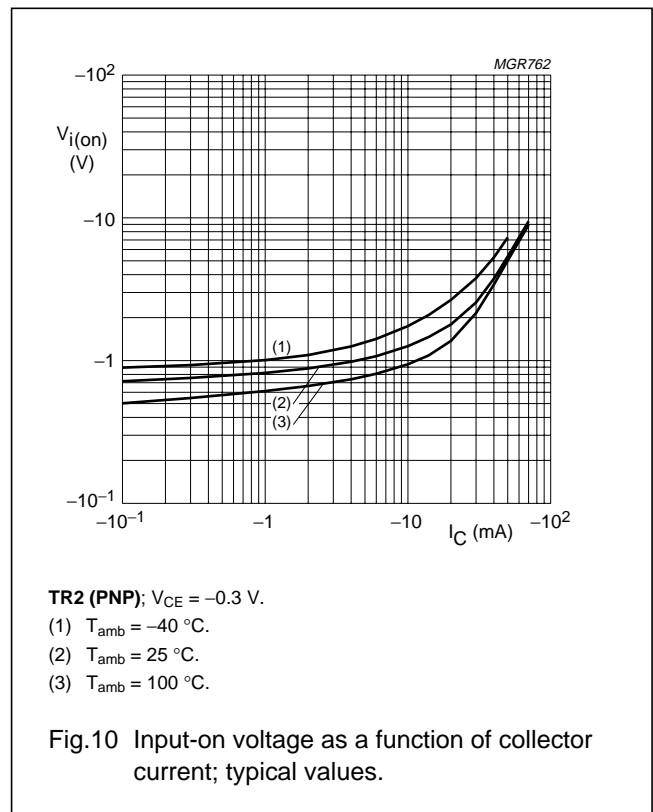
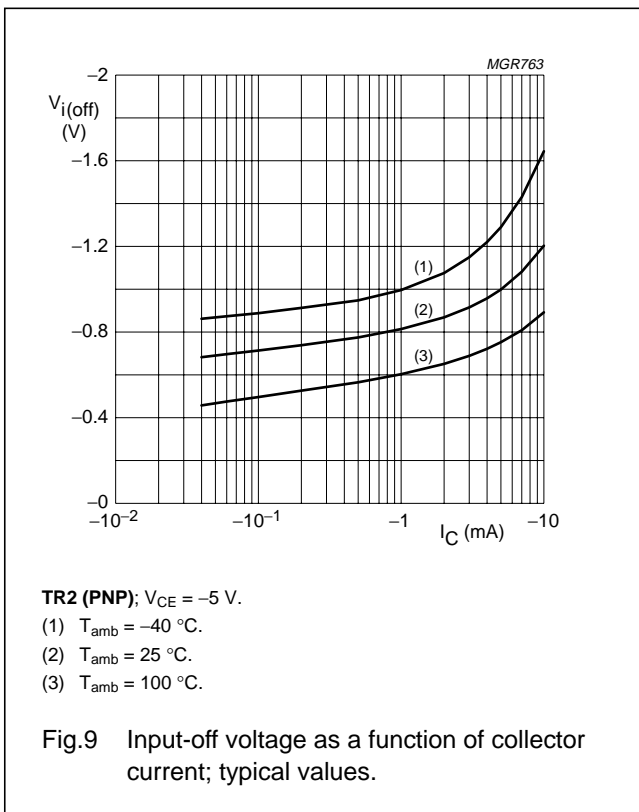
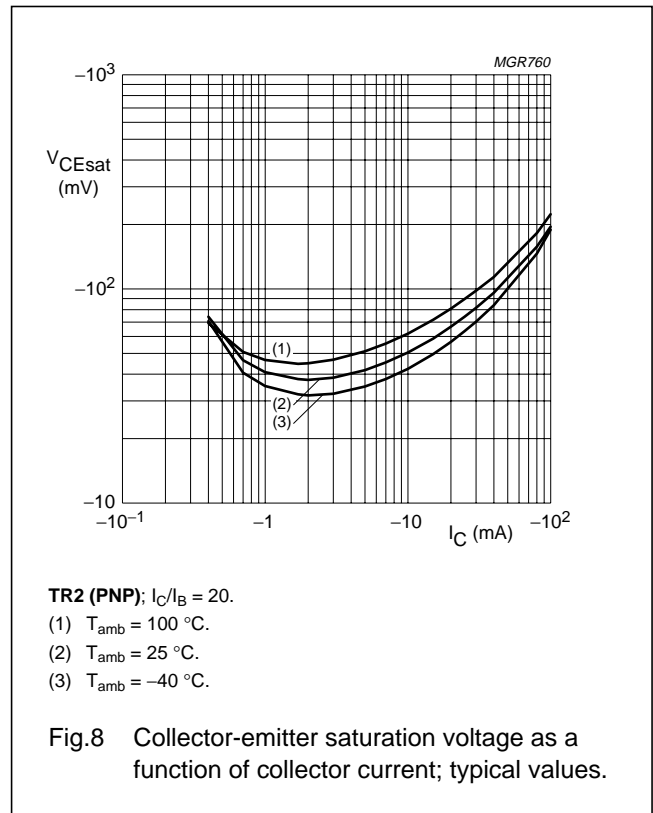
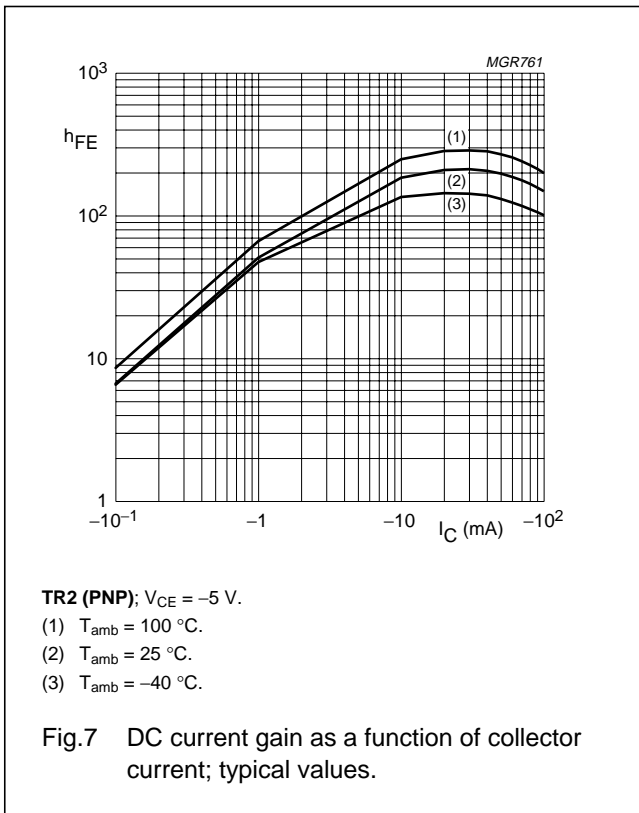
NPN/PNP resistor-equipped transistors

PUMD9



NPN/PNP resistor-equipped transistors

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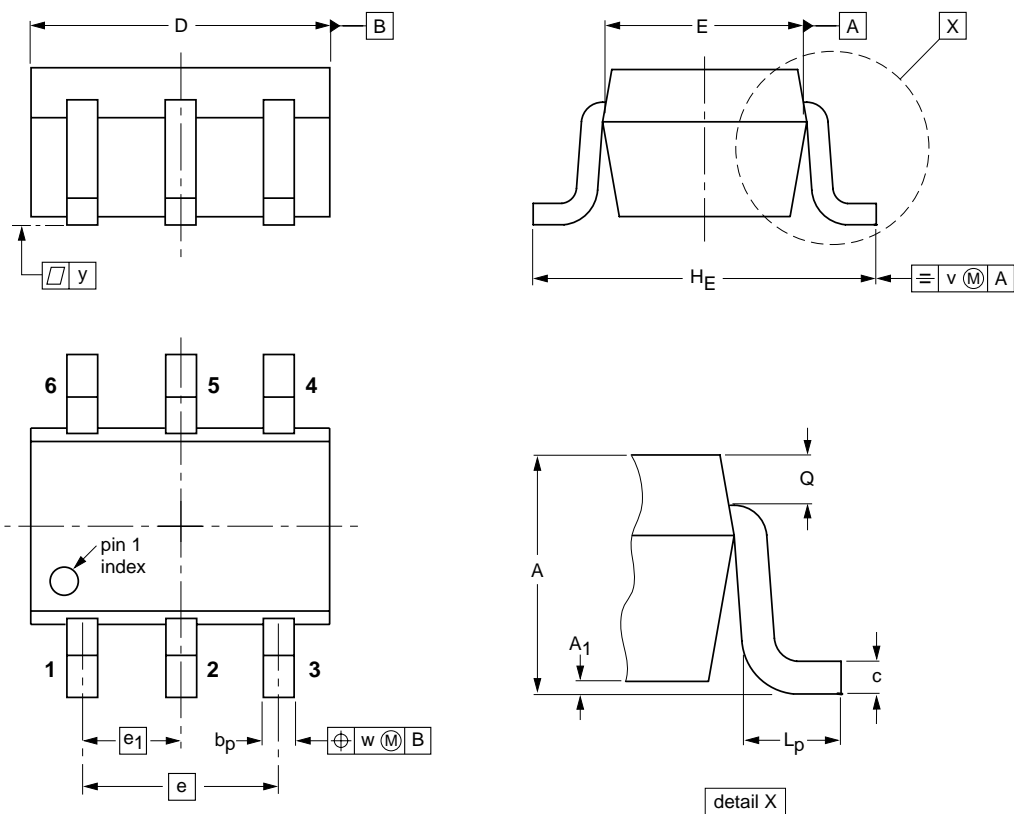
NPN/PNP resistor-equipped transistors

PUMD9

PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT363



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT363			SC-88			97-02-28

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**NPN/PNP resistor-equipped transistors****PUMD9**

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**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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**NPN/PNP resistor-equipped transistors**

**PUMD9**

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**NOTES**

**NPN/PNP resistor-equipped transistors**

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**NOTES**

**NPN/PNP resistor-equipped transistors**

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**NOTES**

# Philips Semiconductors – a worldwide company

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**Australia:** 34 Waterloo Road, NORTH RYDE, NSW 2113,  
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**Austria:** Computerstr. 6, A-1101 WIEN, P.O. Box 213,  
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

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**China/Hong Kong:** 501 Hong Kong Industrial Technology Centre,  
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**Czech Republic:** see Austria

**Denmark:** Sydhavnsgade 23, 1780 COPENHAGEN V,  
Tel. +45 33 29 3333, Fax. +45 33 29 3905

**Finland:** Sinikalliontie 3, FIN-02630 ESPOO,  
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**France:** 51 Rue Carnot, BP317, 92156 SURESNES Cedex,  
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**India:** Philips INDIA Ltd, Band Box Building, 2nd floor,  
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Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

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**Italy:** PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,  
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**Middle East:** see Italy

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**Norway:** Box 1, Manglerud 0612, OSLO,  
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**South America:** Al. Vicente Pinzon, 173, 6th floor,  
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ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

**Ukraine:** PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,  
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

**United Kingdom:** Philips Semiconductors Ltd., 276 Bath Road, Hayes,  
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

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