INTEGRATED CIRCUITS

DATA SHEET

PCF8579
LCD column driver for dot matrix graphic displays

Product specification
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Philips Semiconductors

PHILIPS

LCD column driver for dot matrix graphic displays

PCF8579

FEATURES

- LCD column driver
- Used in conjunction with the PCF8578, this device forms part of a chip set capable of driving up to 40960 dots
- 40 column outputs
- Selectable multiplex rates; 1 : 8, 1 : 16, 1 : 24 or 1 : 32
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications (up to 32 devices)
- 1280-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8578)
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8578)
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology.

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation.

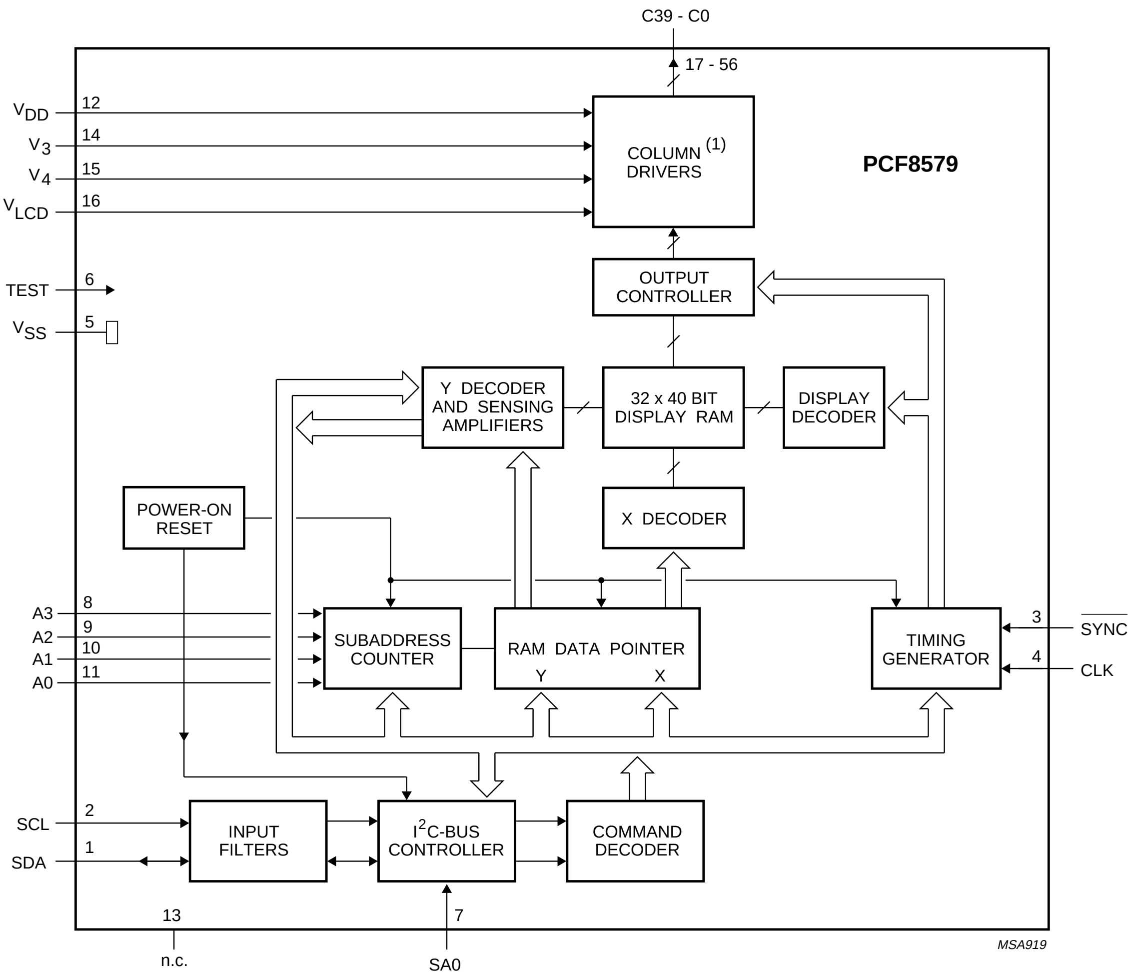
GENERAL DESCRIPTION

The PCF8579 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1 : 8, 1 : 16, 1 : 24 or 1 : 32. The device has 40 outputs and can drive 32 × 40 dots in a 32 row multiplexed LCD. Up to 16 PCF8579s can be cascaded and up to 32 devices may be used on the same I^2C-bus (using the two slave addresses). The device is optimized for use with the PCF8578 LCD row/column driver. Together these two devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40960 dots. The PCF8579 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8579T	56	VSO56	plastic	SOT190
PCF8579U7	–	chip with bumps on-tape	–	–

BLOCK DIAGRAM



(1) LCD voltage levels, all other blocks operate at logic levels.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	I^2C-bus serial data line
SCL	2	I^2C-bus serial clock line
$\overline{SYNC}$	3	cascade synchronization input
CLK	4	external clock input
V_{SS}	5	ground (logic)
TEST	6	test pin (connect to V_{SS})
SA0	7	I^2C-bus slave address input (bit 0)
A3 to A0	8 to 11	I^2C-bus subaddress inputs
V_{DD}	12	supply voltage
n.c.	13[1]	not connected
V_3, V_4	14, 15	LCD bias voltage inputs
V_{LCD}	16	LCD supply voltage
C39 to C0	17 to 56	LCD column driver outputs

Note

1. Do not connect, this pin is reserved.

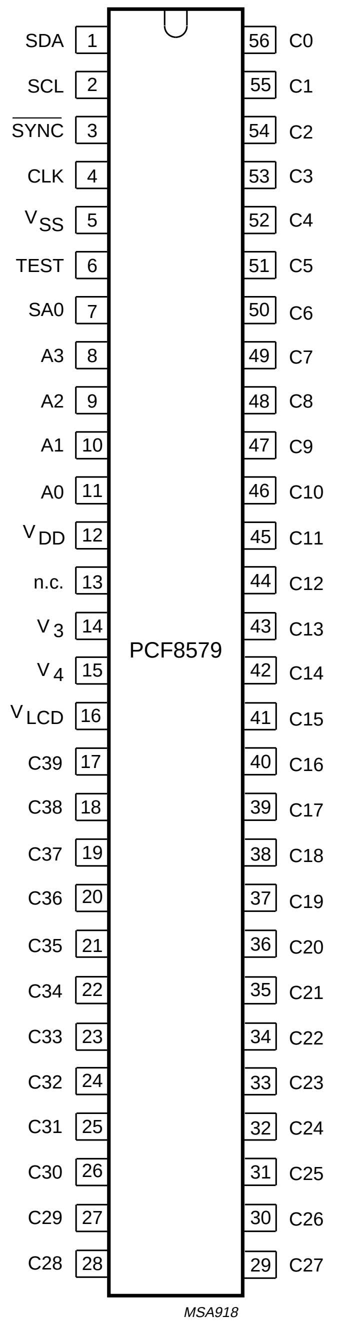


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The PCF8579 column driver is designed for use with the PCF8578. Together they form a general purpose LCD dot matrix chip set.

Typically up to 16 PCF8579s may be used with one PCF8578. Each of the PCF8579s is identified by a unique 4-bit hardware subaddress, set by pins A0 to A3. The PCF8578 can operate with up to 32 PCF8579s when using two I^2C-bus slave addresses. The two slave addresses are set by the logic level on input SA0.

Multiplexed LCD bias generation

The bias levels required to produce maximum contrast depend on the multiplex rate and the LCD threshold voltage (V_{th}). V_{th} is typically defined as the RMS voltage at which the LCD exhibits 10% contrast. Table 1 shows the optimum voltage bias levels for the PCF8578/PCF8579 chip set as functions of V_{op} ($V_{op} = V_{DD} - V_{LCD}$), together with the discrimination ratios (D) for the different multiplex rates. A practical value for V_{op} is obtained by equating $V_{off(rms)}$ with V_{th}.

Table 1 Optimum LCD bias voltages.

PARAMETER	MULTIPLEX RATE			
	1 : 8	**1 : 16**	**1 : 24**	**1 : 32**
$\frac{V_2}{V_{op}}$	0.739	0.800	0.830	0.850
$\frac{V_3}{V_{op}}$	0.522	0.600	0.661	0.700
$\frac{V_4}{V_{op}}$	0.478	0.400	0.339	0.300
$\frac{V_5}{V_{op}}$	0.261	0.200	0.170	0.150
$\frac{V_{off(rms)}}{V_{op}}$	0.297	0.245	0.214	0.193
$\frac{V_{on(rms)}}{V_{op}}$	0.430	0.316	0.263	0.230
$D = \frac{V_{on(rms)}}{V_{off(rms)}}$	1.447	1.291	1.230	1.196
$\frac{V_{op}}{V_{th}}$	3.370	4.080	4.680	5.190

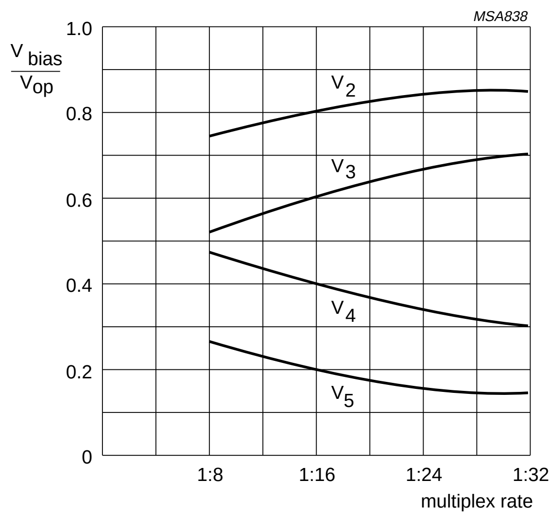


Fig.3 LCD bias voltages as a function of the multiplex rate.

Power-on reset

At power-on the PCF8579 resets to a defined starting condition as follows:

1. Display blank (in conjunction with PCF8578).
2. 1 : 32 multiplex rate.
3. Start bank, 0 selected.
4. Data pointer is set to X, Y address 0, 0.
5. Character mode.
6. Subaddress counter is set to 0.
7. I^2C-bus is initialized.

Data transfers on the I^2C-bus should be avoided for 1 ms following power-on, to allow completion of the reset action.

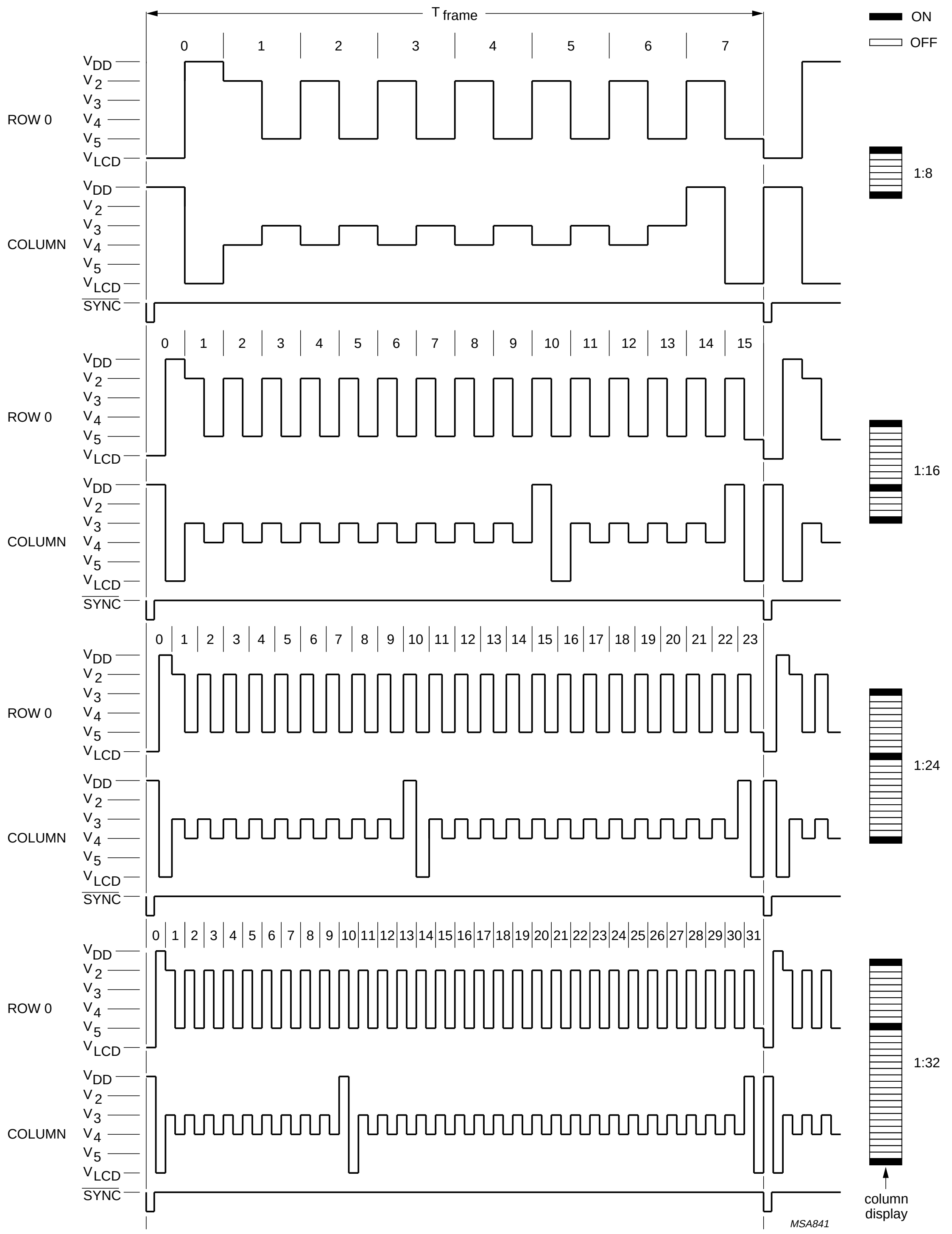
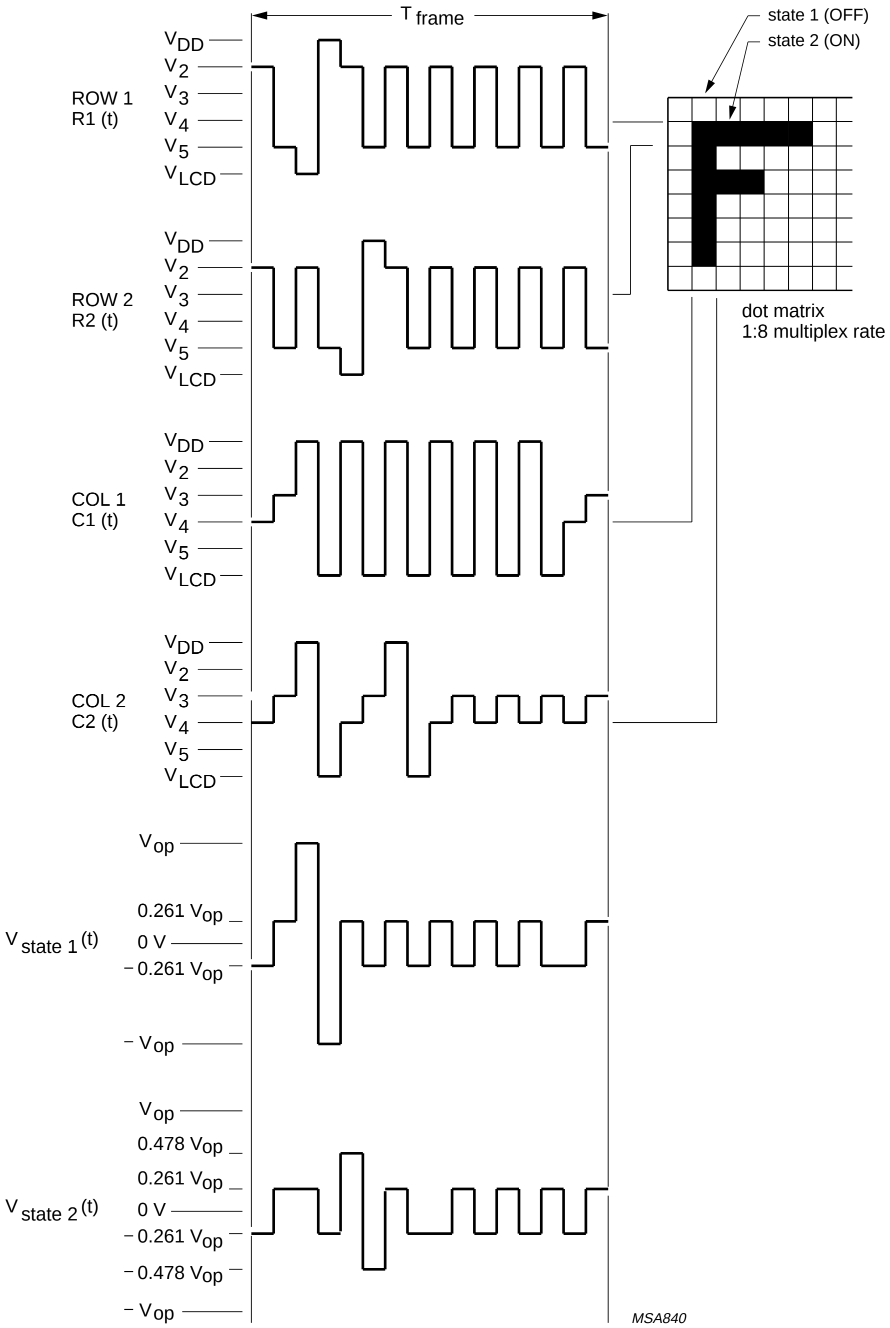


Fig.4 LCD row/column waveforms.



$V_{state\ 1}(t) = C1(t) - R1(t)$:

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{8} + \frac{\sqrt{8} - 1}{8\,(\sqrt{8} + 1)}} = 0.430$$

$V_{state\ 2}(t) = C2(t) - R2(t)$:

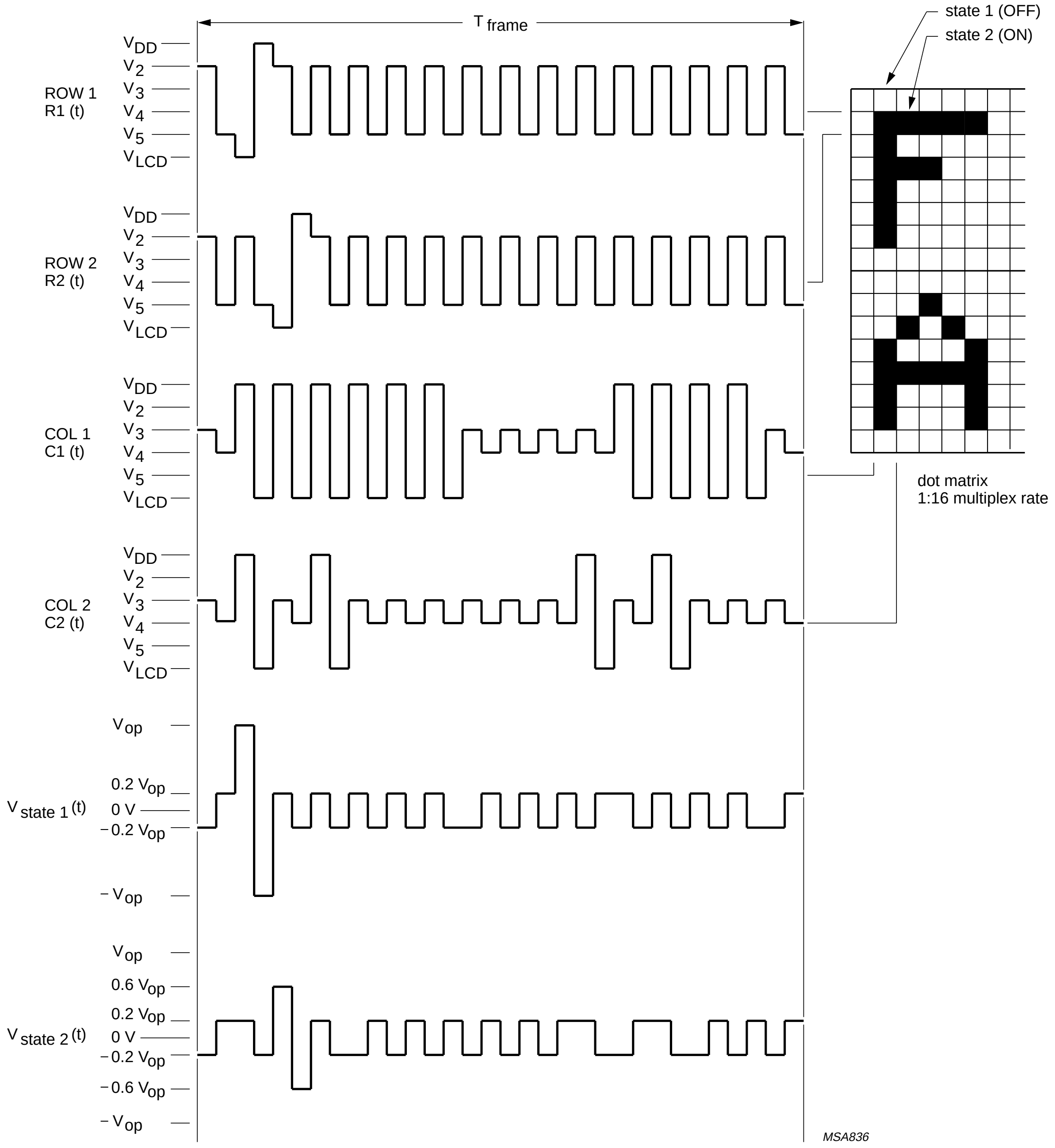
$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2\,(\sqrt{8} - 1)}{\sqrt{8}\,(\sqrt{8} + 1)^2}} = 0.297$$

general relationship (n = multiplex rate)

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n} - 1}{n\,(\sqrt{n} + 1)}}$$

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2\,(\sqrt{n} - 1)}{\sqrt{n}\,(\sqrt{n} + 1)^2}}$$

Fig.5 LCD drive mode waveforms for 1 : 8 multiplex rate.



$V_{state\,1}(t) = C1(t) - R1(t)$:

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{16} + \frac{\sqrt{16} - 1}{16\,(\sqrt{16} + 1)}} = 0.316$$

$V_{state\,2}(t) = C2(t) - R2(t)$:

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2\,(\sqrt{16} - 1)}{\sqrt{16}\,(\sqrt{16} + 1)^2}} = 0.254$$

general relationship (n = multiplex rate)

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n} - 1}{n\,(\sqrt{n} + 1)}}$$

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2\,(\sqrt{n} - 1)}{\sqrt{n}\,(\sqrt{n} + 1)^2}}$$

Fig.6 LCD drive mode waveforms for 1 : 16 multiplex rate.

Timing generator

The timing generator of the PCF8579 organizes the internal data flow from the RAM to the display drivers. An external synchronization pulse $\overline{SYNC}$ is received from the PCF8578. This signal maintains the correct timing relationship between cascaded devices.

Column drivers

Outputs C0 to C39 are column drivers which must be connected to the LCD. Unused outputs should be left open-circuit.

Display RAM

The PCF8579 contains a 32 × 40 bit static RAM which stores the display data. The RAM is divided into 4 banks of 40 bytes (4 × 8 × 40 bits). During RAM access, data is transferred to/from the RAM via the I^2C-bus.

Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows an individual data byte or a series of data bytes to be written into, or read from, the display RAM, controlled by commands sent on the I^2C-bus.

Subaddress counter

The storage and retrieval of display data is dependent on the content of the subaddress counter. Storage and retrieval take place only when the contents of the subaddress counter agree with the hardware subaddress at pins A0, A1, A2 and A3.

I^2C-bus controller

The I^2C-bus controller detects the I^2C-bus protocol, slave address, commands and display data bytes. It performs the conversion of the data input (serial-to-parallel) and the data output (parallel-to-serial). The PCF8579 acts as an I^2C-bus slave transmitter/receiver. Device selection depends on the I^2C-bus slave address, the hardware subaddress and the commands transmitted.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

RAM access

There are three RAM ACCESS modes:

- Character
- Half-graphic
- Full-graphic.

These modes are specified by bits G1 and G0 of the RAM ACCESS command. The RAM ACCESS command controls the order in which data is written to or read from the RAM (see Fig.7).

To store RAM data, the user specifies the location into which the first byte will be loaded (see Fig.8):

- Device subaddress (specified by the DEVICE SELECT command)
- RAM X-address (specified by the LOAD X-ADDRESS command)
- RAM bank (specified by bits Y1 and Y0 of the RAM ACCESS command).

Subsequent data bytes will be written or read according to the chosen RAM access mode. Device subaddresses are automatically incremented between devices until the last device is reached. If the last device has subaddress 15, further display data transfers will lead to a wrap-around of the subaddress to 0.

Display control

The display is generated by continuously shifting rows of RAM data to the dot matrix LCD via the column outputs. The number of rows scanned depends on the multiplex rate set by bits M1 and M0 of the SET MODE command.

The display status (all dots on/off and normal/inverse video) is set by bits E1 and E0 of the SET MODE command. For bank switching, the RAM bank corresponding to the top of the display is set by bits B1 and B0 of the SET START BANK command. This is shown in Fig.9 This feature is useful when scrolling in alphanumeric applications.

TEST pin

The TEST pin must be connected to V_{SS}.

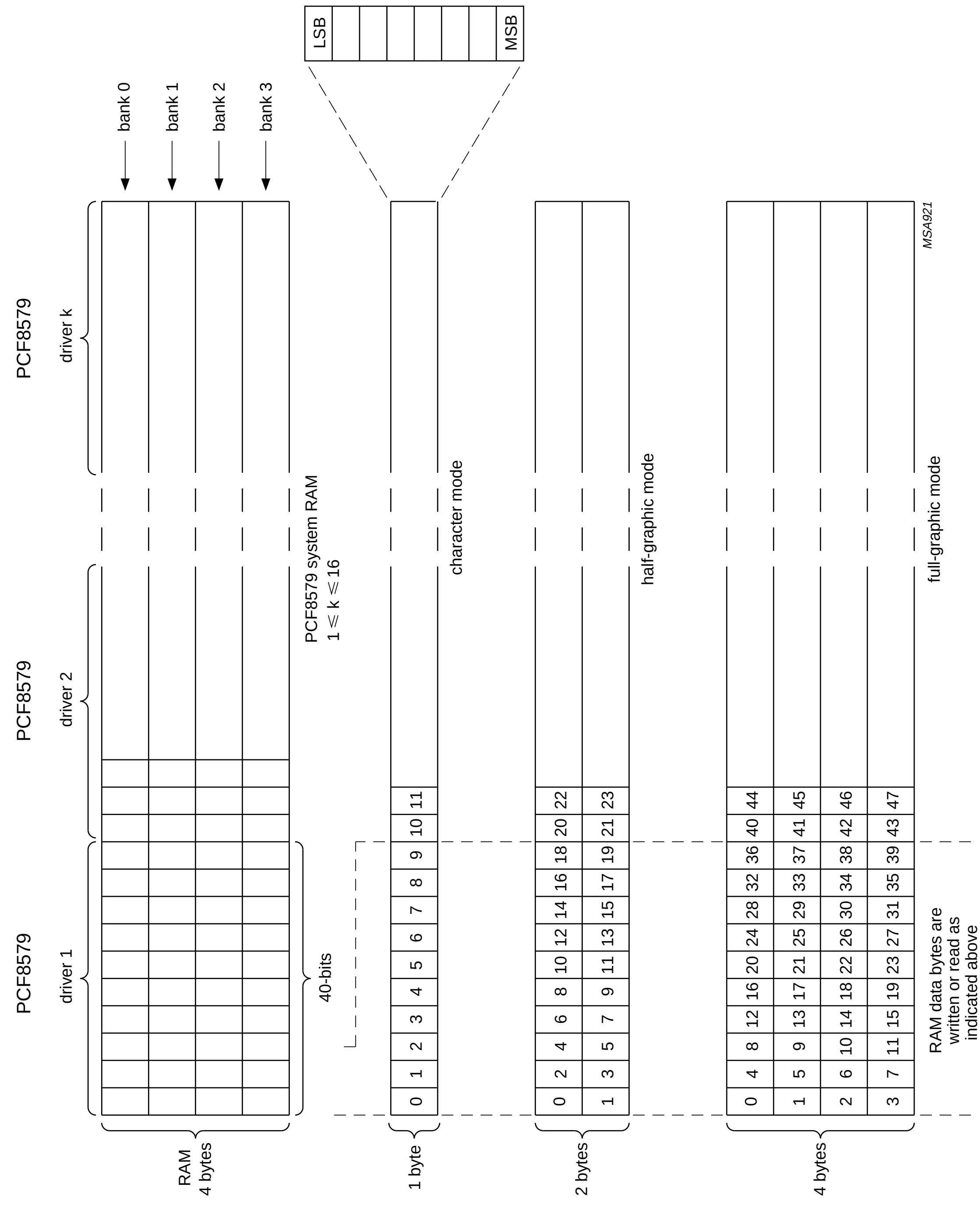


Fig.7 RAM access mode.

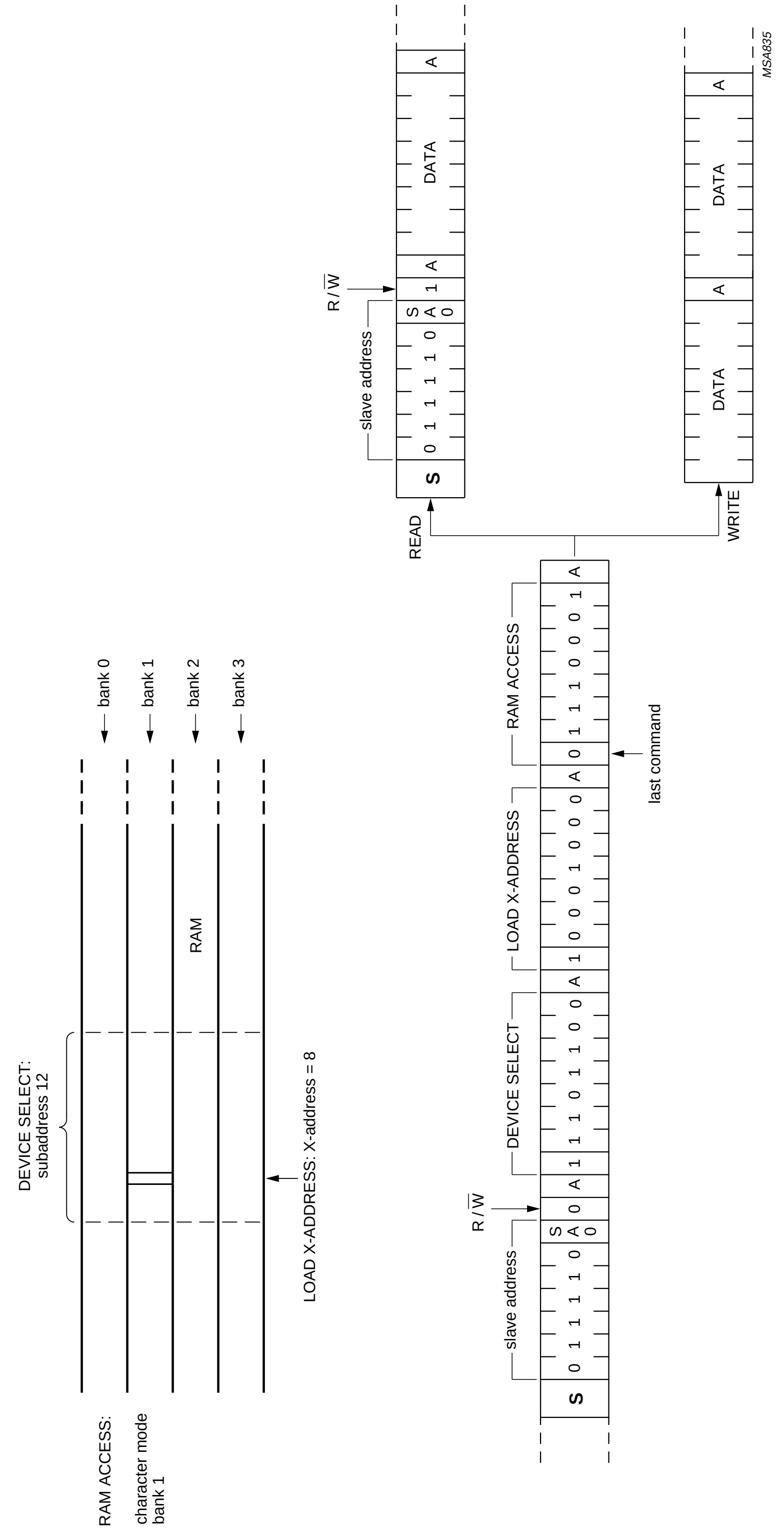


Fig.8 Example of commands specifying initial data byte RAM locations.

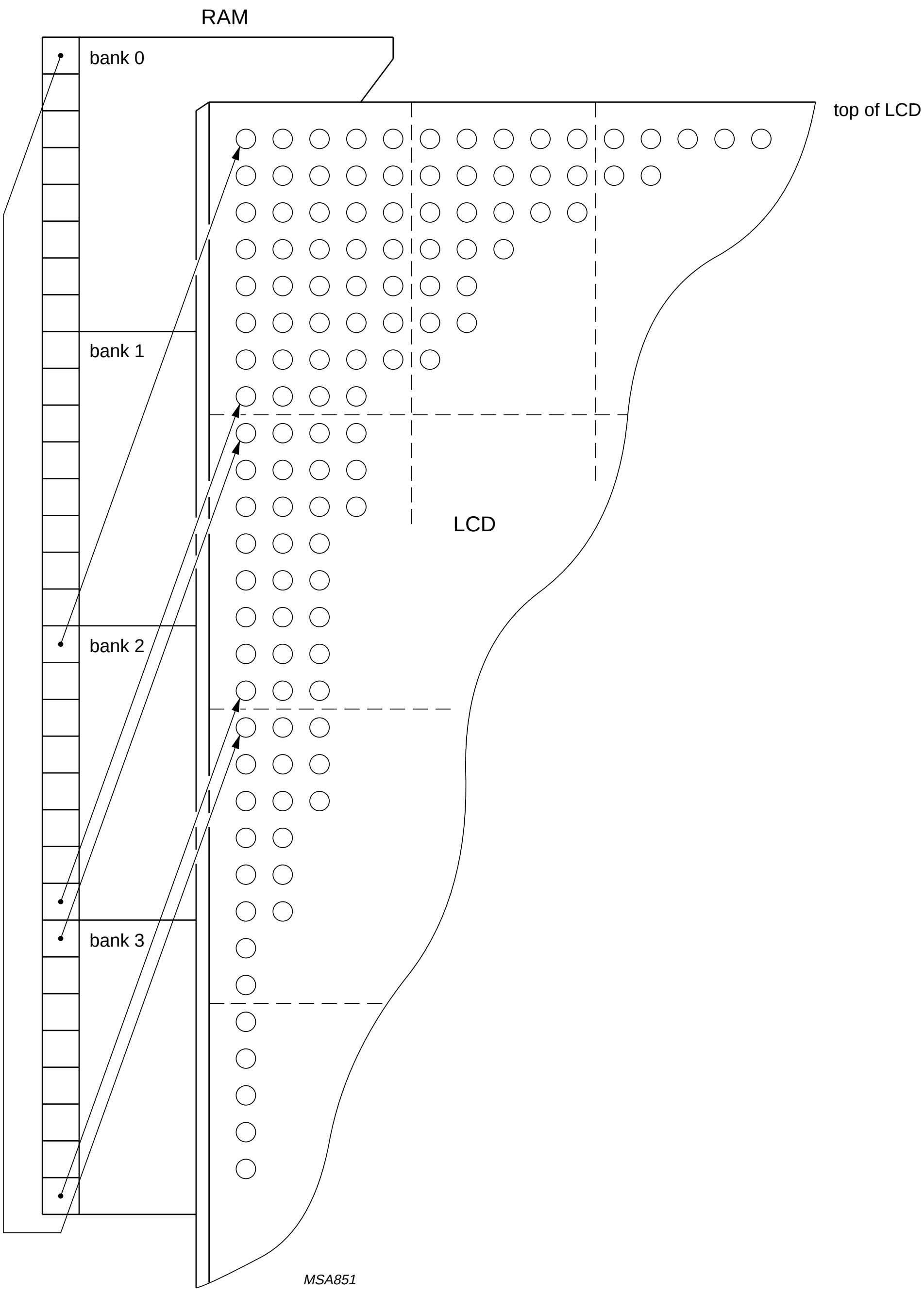


Fig.9 Relationship between display and SET START BANK; 1 : 32 multiplex rate and start bank = 2.

I^2C-BUS PROTOCOL

Two 7-bit slave addresses (0111100 and 0111101) are reserved for both the PCF8578 and PCF8579. The least-significant bit of the slave address is set by connecting input SA0 to either 0 (V_{SS}) or 1 (V_{DD}). Therefore, two types of PCF8578 or PCF8579 can be distinguished on the same I^2C-bus which allows:

1. One PCF8578 to operate with up to 32 PCF8579s on the same I^2C-bus for very large applications.
2. The use of two types of LCD multiplex schemes on the same I^2C-bus.

In most applications the PCF8578 will have the same slave address as the PCF8579.

The I^2C-bus protocol is shown in Fig.10. All communications are initiated with a start condition (S) from the I^2C-bus master, which is followed by the desired slave address and read/write bit. All devices with this slave address acknowledge in parallel. All other devices ignore the bus transfer.

In WRITE mode (indicated by setting the read/write bit LOW) one or more commands follow the slave address acknowledgement. The commands are also acknowledged by all addressed devices on the bus. The last command must clear the continuation bit C. After the last command a series of data bytes may follow. The acknowledgement after each byte is made only by the (A0, A1, A2 and A3) addressed PCF8579 or PCF8578 with its implicit subaddress 0. After the last data byte has been acknowledged, the I^2C-bus master issues a stop condition (P).

In READ mode, indicated by setting the read/write bit HIGH, data bytes may be read from the RAM following the slave address acknowledgement. After this acknowledgement the master transmitter becomes a master receiver and the PCF8579 becomes a slave transmitter. The master receiver must acknowledge the reception of each byte in turn. The master receiver must signal an end of data to the slave transmitter, by **not** generating an acknowledge on the last byte clocked out of the slave. The slave transmitter then leaves the data line HIGH, enabling the master to generate a stop condition (P).

Display bytes are written into, or read from, the RAM at the address specified by the data pointer and subaddress counter. Both the data pointer and subaddress counter are automatically incremented, enabling a stream of data to be transferred either to, or from, the intended devices.

In multiple device applications, the hardware subaddress pins of the PCF8579s (A0 to A3) are connected to V_{SS} or V_{DD} to represent the desired hardware subaddress code. If two or more devices share the same slave address, then each device **must** be allocated a unique hardware subaddress.

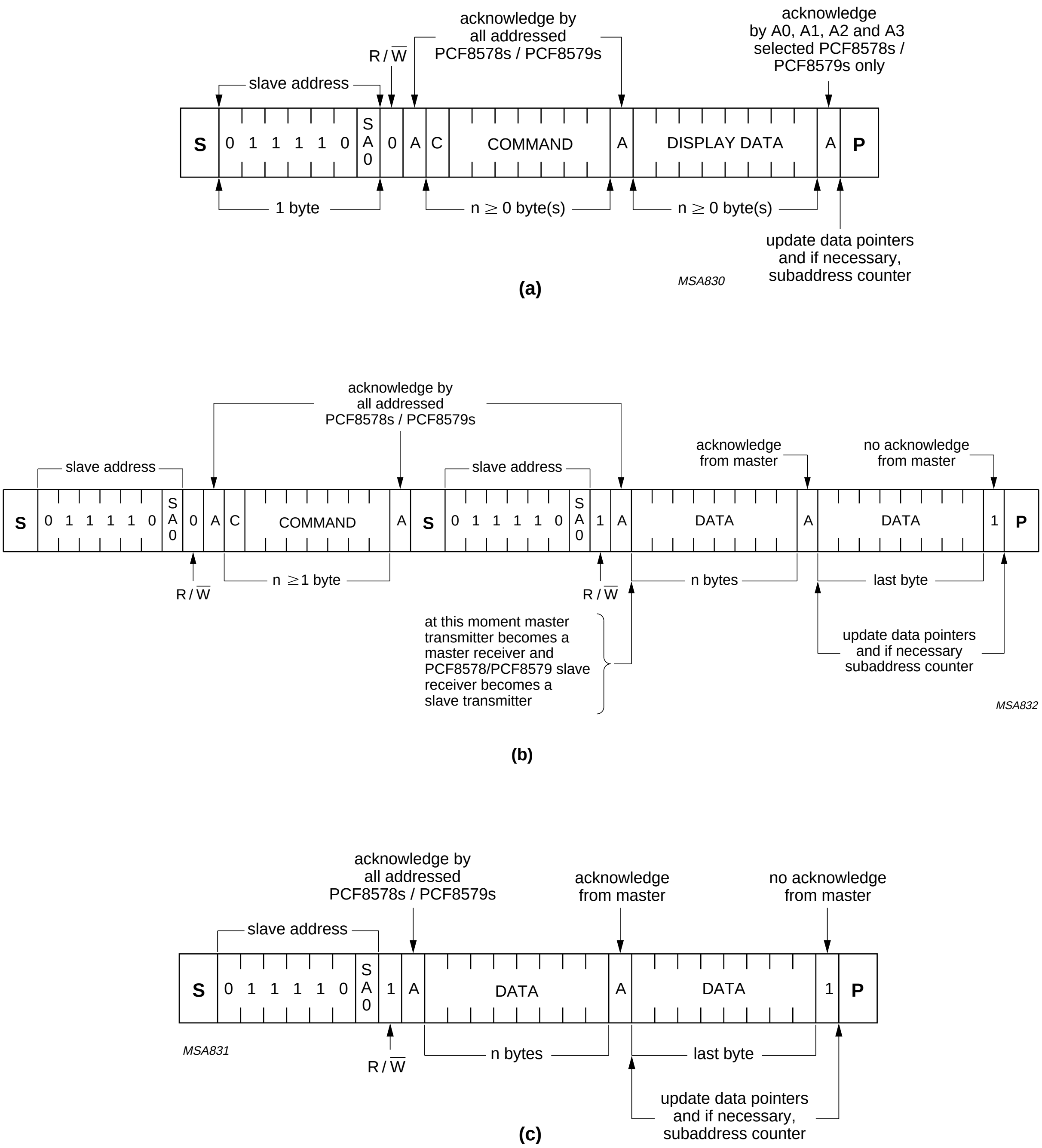
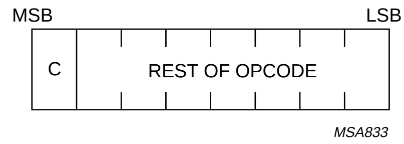


Fig.10 (a) Master transmits to slave receiver (WRITE mode); (b) Master reads after sending command string (WRITE commands; READ data); (c) Master reads slave immediately after sending slave address (READ mode).

Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus. The most-significant bit of a command is the continuation bit C (see Fig.11). When this bit is set, it indicates that the next byte to be transferred will also be a command. If the bit is reset, it indicates the conclusion of the command transfer. Further bytes will be regarded as display data. Commands are transferred in WRITE mode only.

The five commands available to the PCF8579 are defined in Tables 2 and 3.



C = 0; last command.
C = 1; commands continue.

Fig.11 General format of command byte.

Table 2 Summary of commands.

COMMAND	OPCODE[1]	DESCRIPTION
SET MODE	C 1 0 D D D D D	multiplex rate, display status, system type
SET START BANK	C 1 1 1 1 1 D D	defines bank at top of LCD
DEVICE SELECT	C 1 1 0 D D D D	defines device subaddress
RAM ACCESS	C 1 1 1 D D D D	graphic mode, bank select (D D D D ≥ 12 is not allowed; see SET START BANK opcode)
LOAD X-ADDRESS	C 0 D D D D D D	0 to 39

Note

1. C = command continuation bit.
   D = may be a logic 1 or 0.

Table 3 Definition of PCF8578/PCF8579 commands.

COMMAND	OPCODE								OPTIONS	DESCRIPTION
SET MODE	C	1	0	T	E1	E0	M1	M0	see Table 4	defines LCD drive mode
									see Table 5	defines display status
									see Table 6	defines system type
SET START BANK	C	1	1	1	1	1	B1	B0	see Table 7	defines pointer to RAM bank corresponding to the top of the LCD; useful for scrolling, pseudo-motion and background preparation of new display
DEVICE SELECT	C	1	1	0	A3	A2	A1	A0	see Table 8	four bits of immediate data, bits A0 to A3, are transferred to the subaddress counter to define one of sixteen hardware subaddresses
RAM ACCESS	C	1	1	1	G1	G0	Y1	Y0	see Table 9	defines the auto-increment behaviour of the address for RAM access
									see Table 10	two bits of immediate data, bits Y0 to Y1, are transferred to the X-address pointer to define one of forty display RAM columns
LOAD X-ADDRESS	C	0	X5	X4	X3	X2	X1	X0	see Table 11	six bits of immediate data, bits X0 to X5, are transferred to the X-address pointer to define one of forty display RAM columns

Table 4 Set mode option 1.

LCD DRIVE MODE		BITS	
		M1	**M0**
1 : 8	MUX (8 rows)	0	1
1 : 16	MUX (16 rows)	1	0
1 : 24	MUX (24 rows)	1	1
1 : 32	MUX (32 rows)	0	0

Table 5 Set mode option 2.

DISPLAY STATUS	BITS	
	E1	**E0**
Blank	0	0
Normal	0	1
All segments on	1	0
Inverse video	1	1

Table 6 Set mode option 3.

SYSTEM TYPE	BIT T
PCF8578 row only	0
PCF8578 mixed mode	1

Table 7 Set start bank option 1.

START BANK POINTER	BITS	
	B1	**B0**
Bank 0	0	0
Bank 1	0	1
Bank 2	1	0
Bank 3	1	1

Table 8 Device select option 1.

DESCRIPTION	BITS			
Decimal value of 0 to 15	A3	A2	A1	A0

Table 9 RAM access option 1.

RAM ACCESS MODE	BITS	
	G1	**G0**
Character	0	0
Half-graphic	0	1
Full-graphic	1	0
Not allowed (note 1)	1	1

Note

1. See opcode for SET START BANK in Table 3.

Table 10 RAM access option 2.

DESCRIPTION	BITS	
Decimal value of 0 to 3	Y1	Y0

Table 11 Load X-address option 1.

DESCRIPTION	BITS					
Decimal value of 0 to 39	X5	X4	X3	X2	X1	X0

CHARACTERISTICS OF THE I^{2}C-BUS

The I^{2}C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL) which must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this moment will be interpreted as control signals.

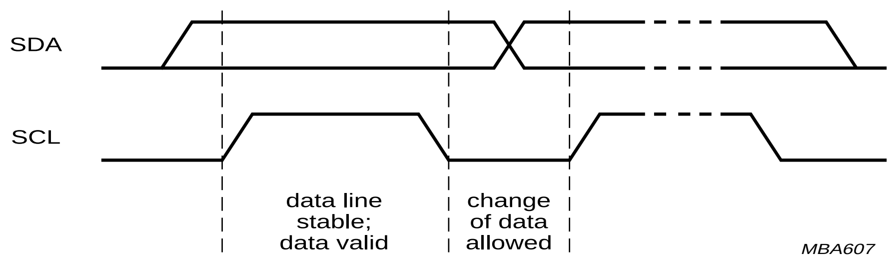


Fig.12 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

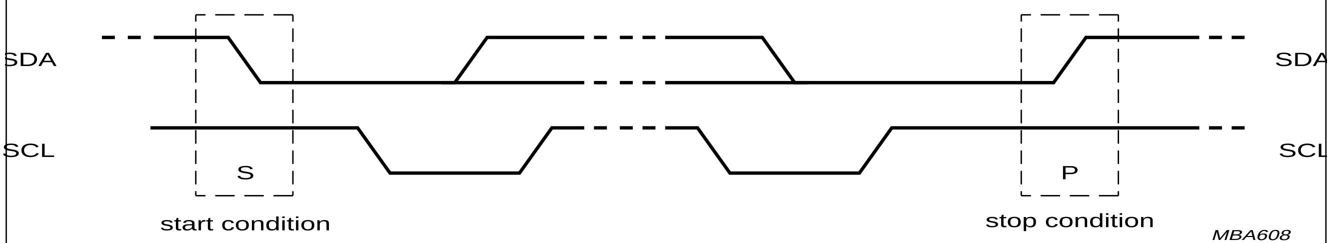


Fig.13 Definition of start and stop condition.

System configuration

A device transmitting a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message flow is the 'master' and the devices which are controlled by the master are the 'slaves'.

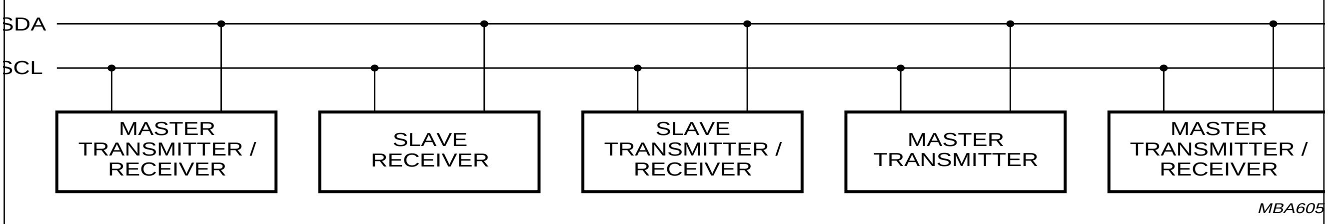
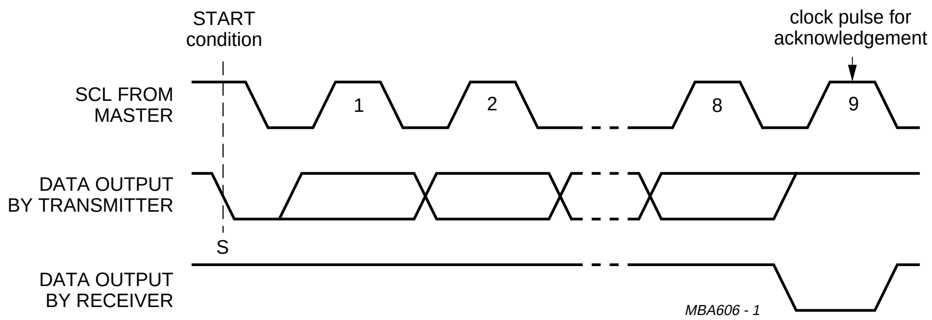


Fig.14 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal the end of a data transmission to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.



The general characteristics and detailed specification of the I^2C-bus are available on request.

Fig.15 Acknowledgment on the I^2C-bus.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+8.0	V
V_{LCD}	LCD supply voltage	V_{DD} – 11	V_{DD}	V
V_{I1}	input voltage SDA, SCL, $\overline{SYNC}$, CLK, TEST, SA0, A0, A1, A2 and A3	V_{SS} – 0.5	V_{DD} + 0.5	V
V_{I2}	input voltage V_3 and V_4	V_{LCD} – 0.5	V_{DD} + 0.5	V
V_{O1}	output voltage SDA	V_{SS} – 0.5	V_{DD} + 0.5	V
V_{O2}	output voltage C0 to C39	V_{LCD} – 0.5	V_{DD} + 0.5	V
I_I	DC input current	–10	+10	mA
I_O	DC output current	–10	+10	mA
I_{DD}, I_{SS}, I_{LCD}	V_{DD}, V_{SS} or V_{LCD} current	–50	+50	mA
P_{tot}	total power dissipation per package	–	400	mW
P_o	power dissipation per output	–	100	mW
T_{stg}	storage temperature	–65	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe it is desirable to take normal precautions appropriate to handling MOS devices.

DC CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} – 3.5 V to V_{DD} – 9 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.5	–	6.0	V
V_{LCD}	LCD supply voltage		V_{DD} – 9	–	V_{DD} – 3.5	V
I_{DD}	supply current	f_{clk} = 2 kHz; note 1	–	9	20	μA
V_{POR}	power-on reset level	note 2	–	1.3	1.8	V
Logic						
V_{IL}	LOW level input voltage		V_{SS}	–	0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7V_{DD}	–	V_{DD}	V
I_{L1}	leakage current at SDA, SCL, $\overline{\text{SYNC}}$, CLK, TEST, SA0, A0, A1, A2 and A3	V_I = V_{DD} or V_{SS}	–1	–	+1	μA
I_{OL}	LOW level output current at SDA	V_{OL} = 0.4 V; V_{DD} = 5 V	3	–	–	mA
C_I	input capacitance	note 3	–	–	5	pF
LCD outputs						
I_{L2}	leakage current at V_3 to V_4	V_I = V_{DD} or V_{LCD}	–2	–	+2	μA
V_{DC}	DC component of LCD drivers C0 to C39		–	±20	–	mV
R_{COL}	output resistance at C0 to C39	note 4	–	3	6	kΩ

Notes

1. Outputs are open; inputs at V_{DD} or V_{SS}; I^2C-bus inactive; clock with 50% duty factor.
2. Resets all logic when $V_{DD} < V_{POR}$.
3. Periodically sampled; not 100% tested.
4. Resistance measured between output terminal (C0 to C39) and bias input (V_3, V_4, V_{DD} and V_{LCD}) when the specified current flows through one output under the following conditions (see Table 1):
   - $V_{op} = V_{DD} - V_{LCD}$ = 9 V;
   - $V_3 - V_{LCD} \geq$ 4.70 V; $V_4 - V_{LCD} \leq$ 4.30 V; I_{LOAD} = 100 μA.

AC CHARACTERISTICS

All timing values are referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} – 3.5 V to V_{DD} – 9 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{clk}	clock frequency	50% duty factor	–	note 1	10	kHz
t_{PLCD}	driver delays	V_{DD} – V_{LCD} = 9 V; with test loads	–	–	100	µs
I²C-bus						
f_{SCL}	SCL clock frequency		–	–	100	kHz
t_{SW}	tolerable spike width on bus		–	–	100	ns
t_{BUF}	bus free time		4.7	–	–	µs
$t_{SU;STA}$	start condition set-up time	repeated start codes only	4.7	–	–	µs
$t_{HD;STA}$	start condition hold time		4.0	–	–	µs
t_{LOW}	SCL LOW time		4.7	–	–	µs
t_{HIGH}	SCL HIGH time		4.0	–	–	µs
t_r	SCL and SDA rise time		–	–	1.0	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{SU;STO}$	stop condition set-up time		4.0	–	–	µs

Note

1. Typically 0.9 to 3.3 kHz.

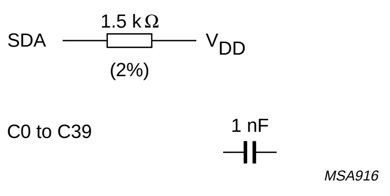


Fig.16 AC test loads.

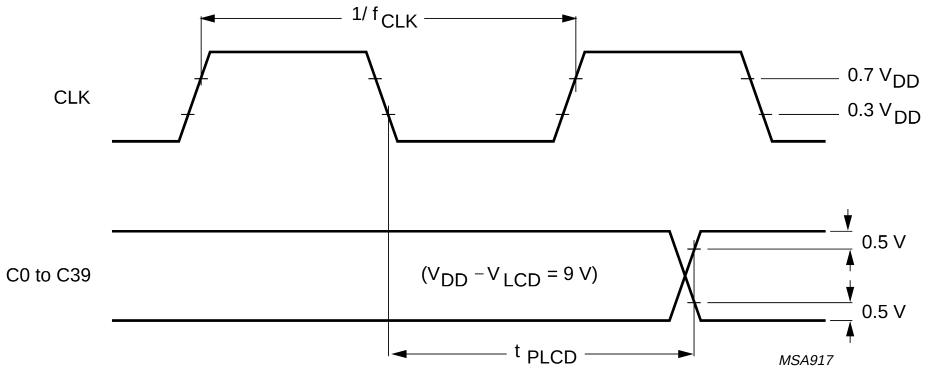


Fig.17 Driver timing waveforms.

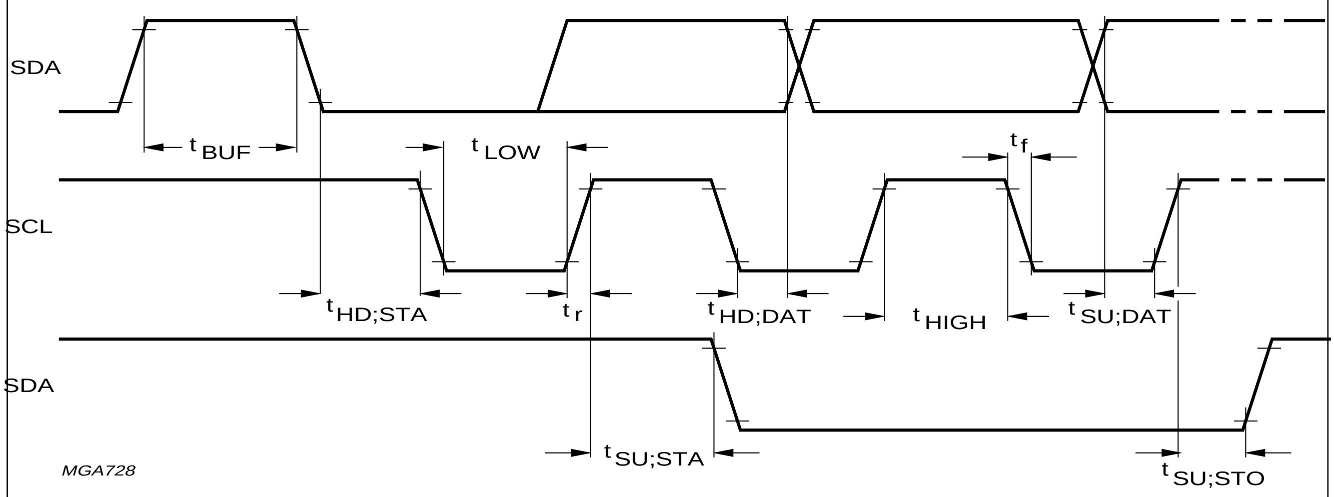


Fig.18 I^2C-bus timing waveforms.

APPLICATION INFORMATION

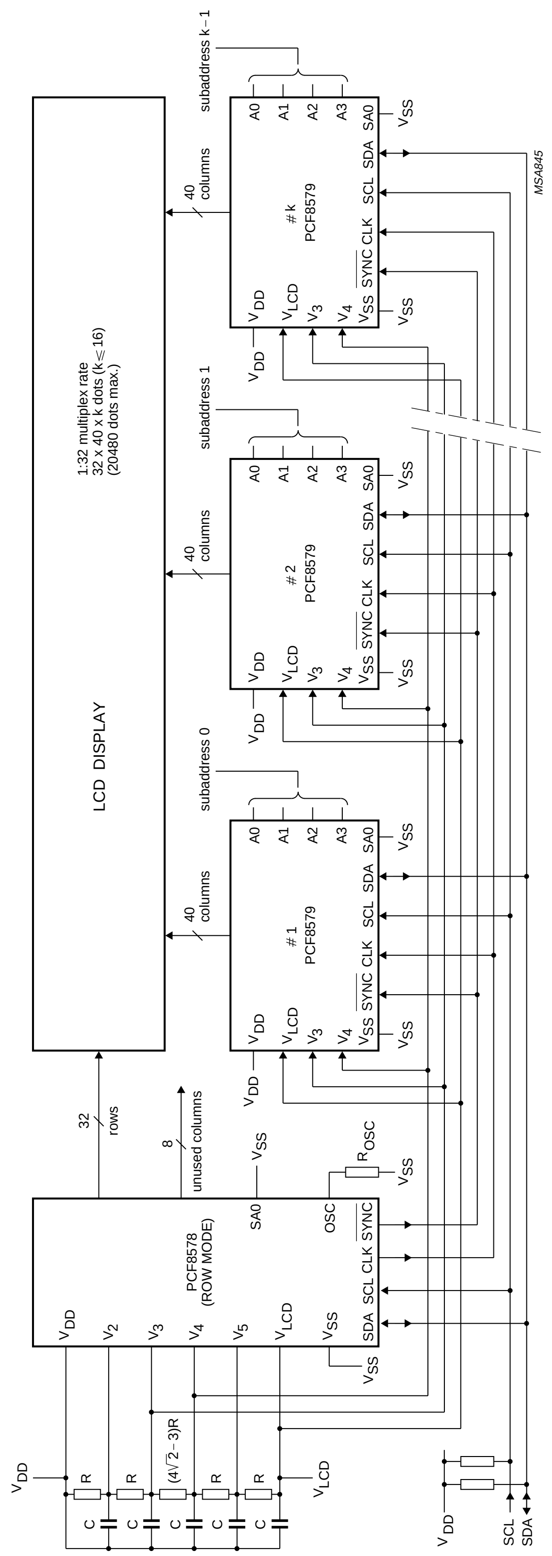


Fig.19 Typical LCD driver system with 1 : 32 multiplex rate.

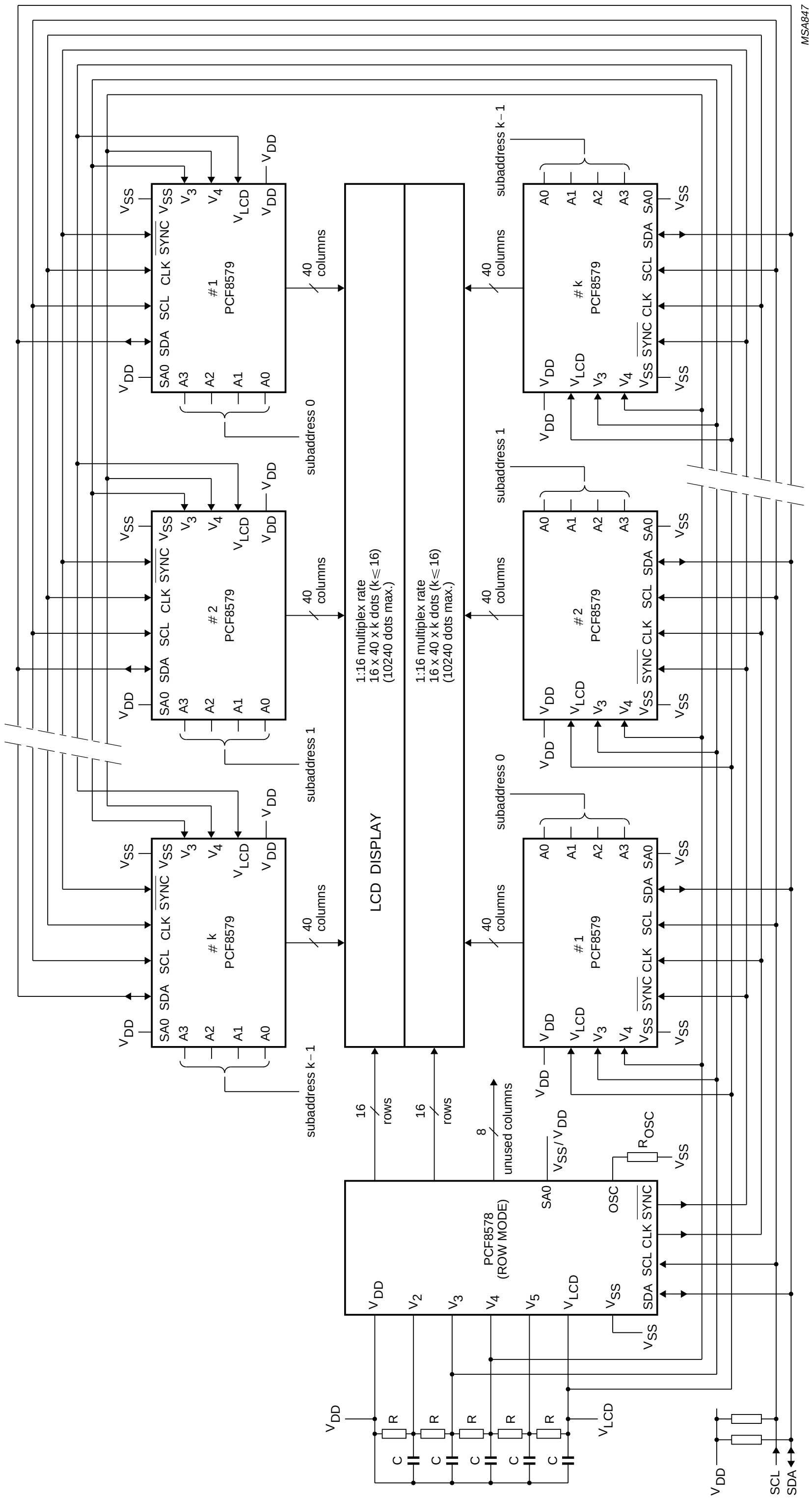


Fig.20 Split screen application with 1 : 16 multiplex rate for improved contrast.

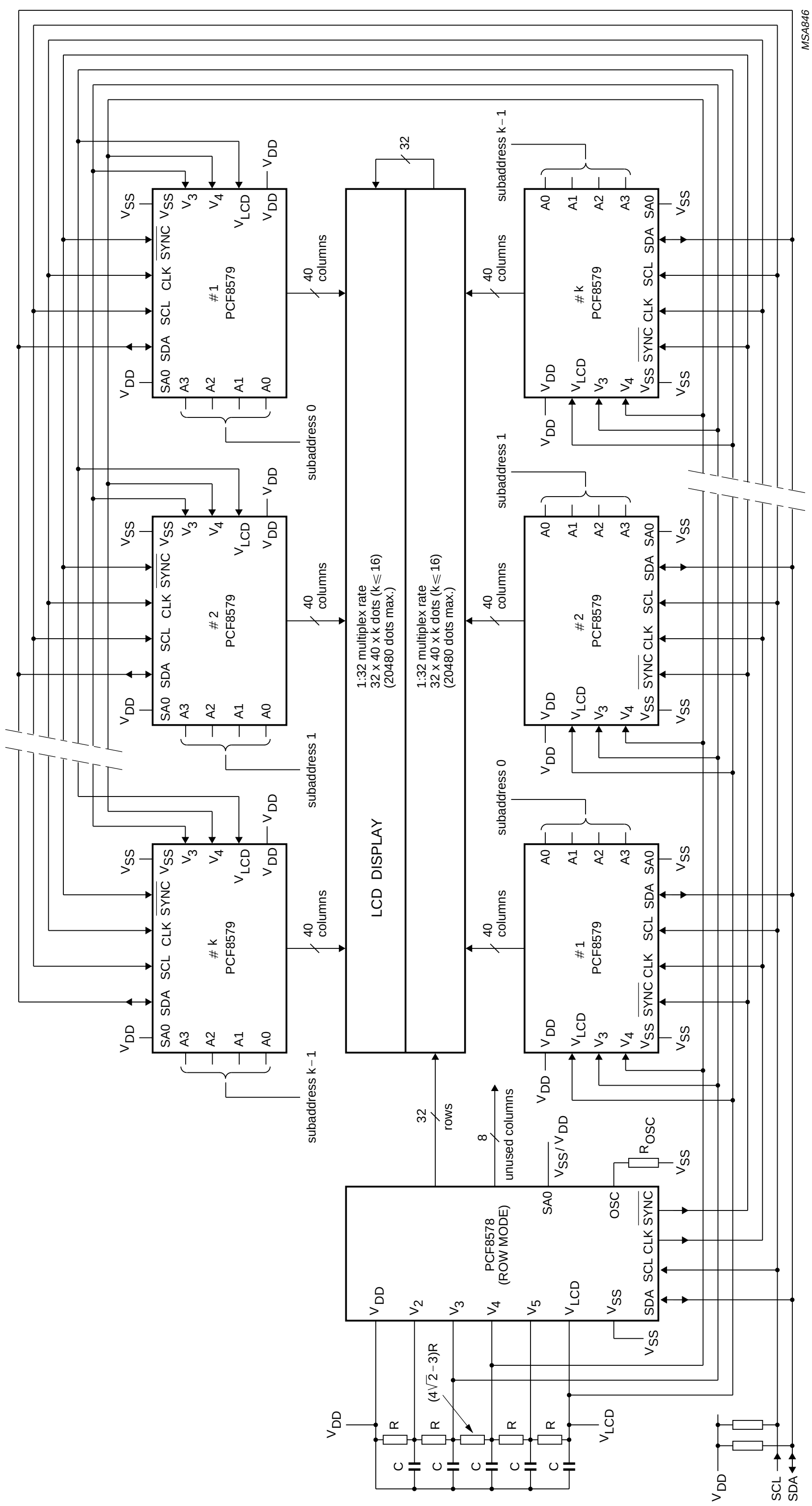


Fig.21 Split screen application with 1 : 32 multiplex rate.

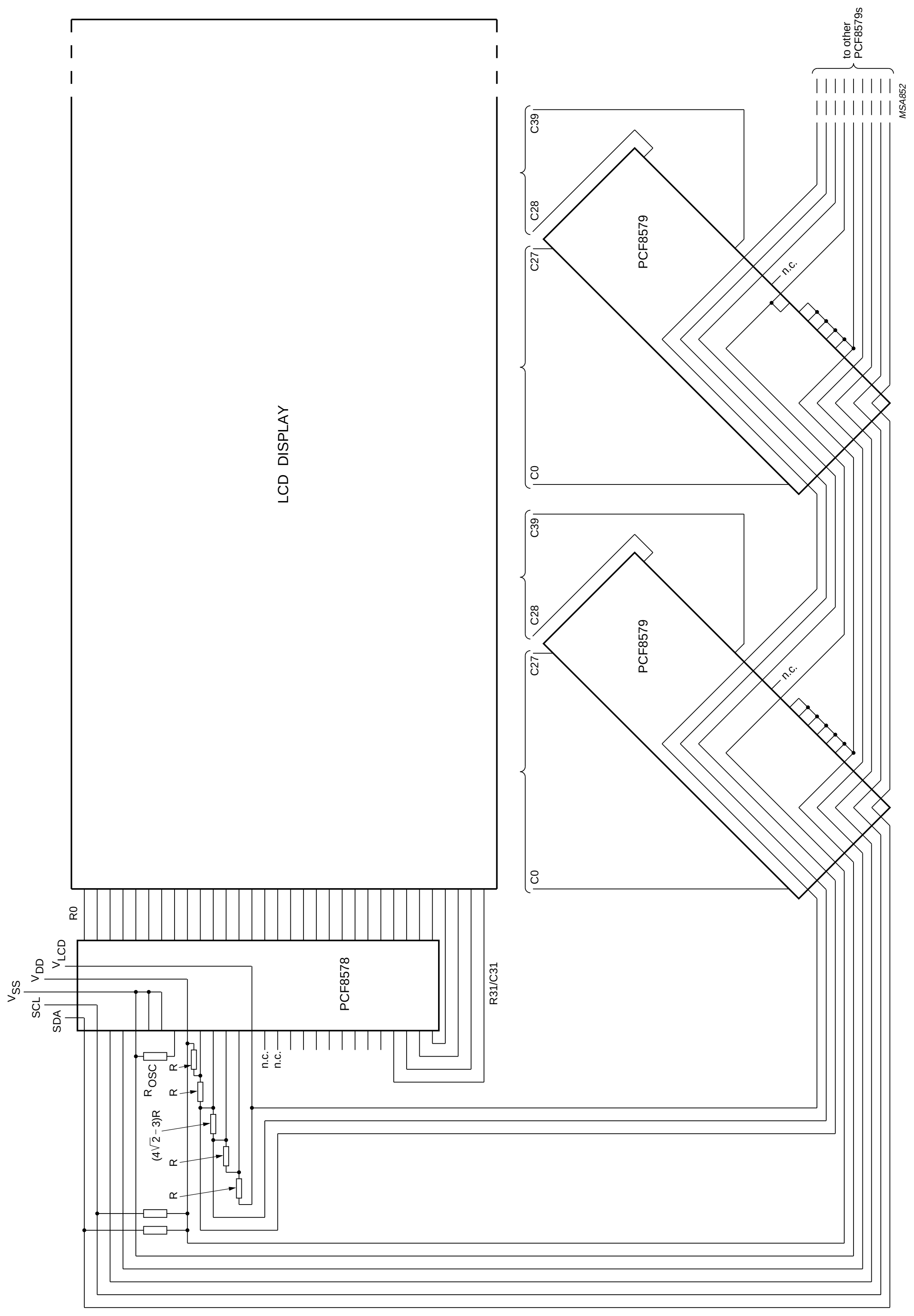
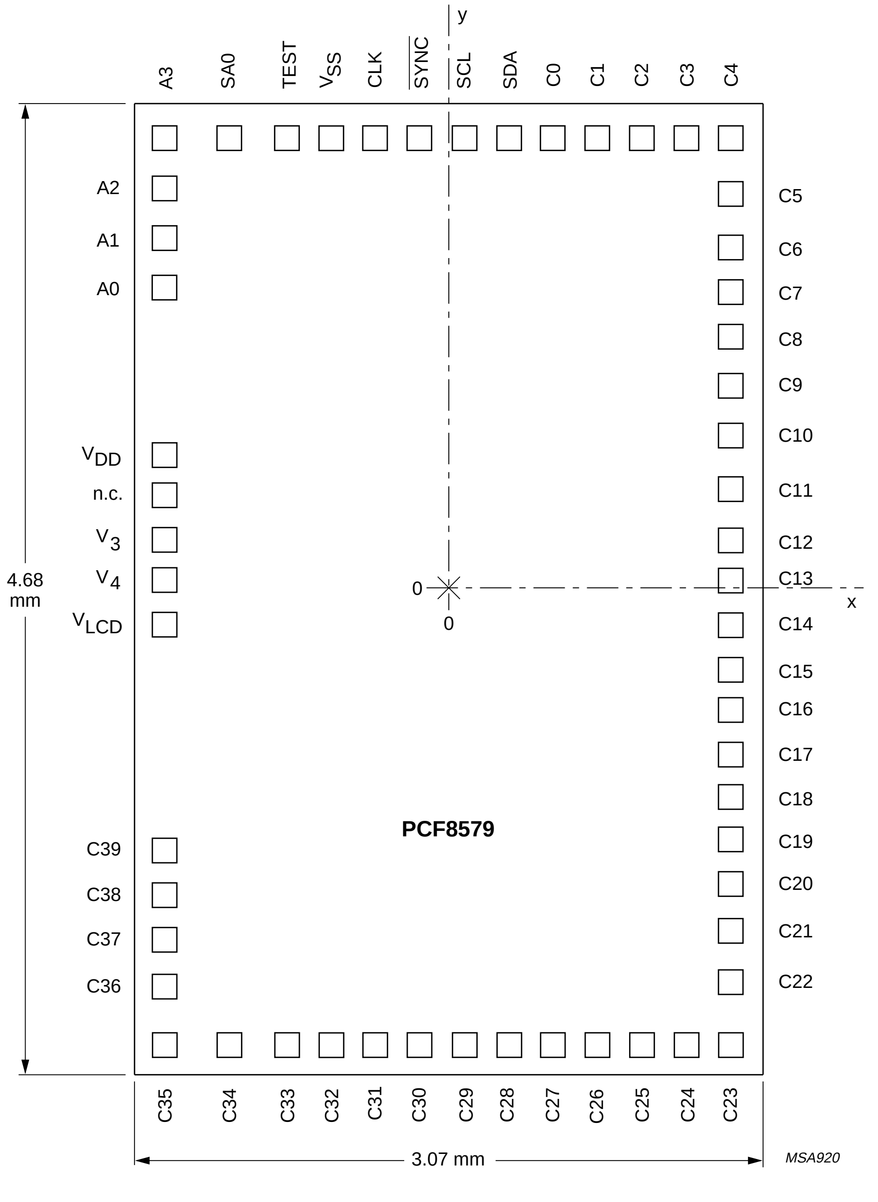


Fig.22 Example of single plane wiring, single screen with 1 : 32 multiplex rate (PCF8578 in row driver mode).

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 14.37 mm^2.

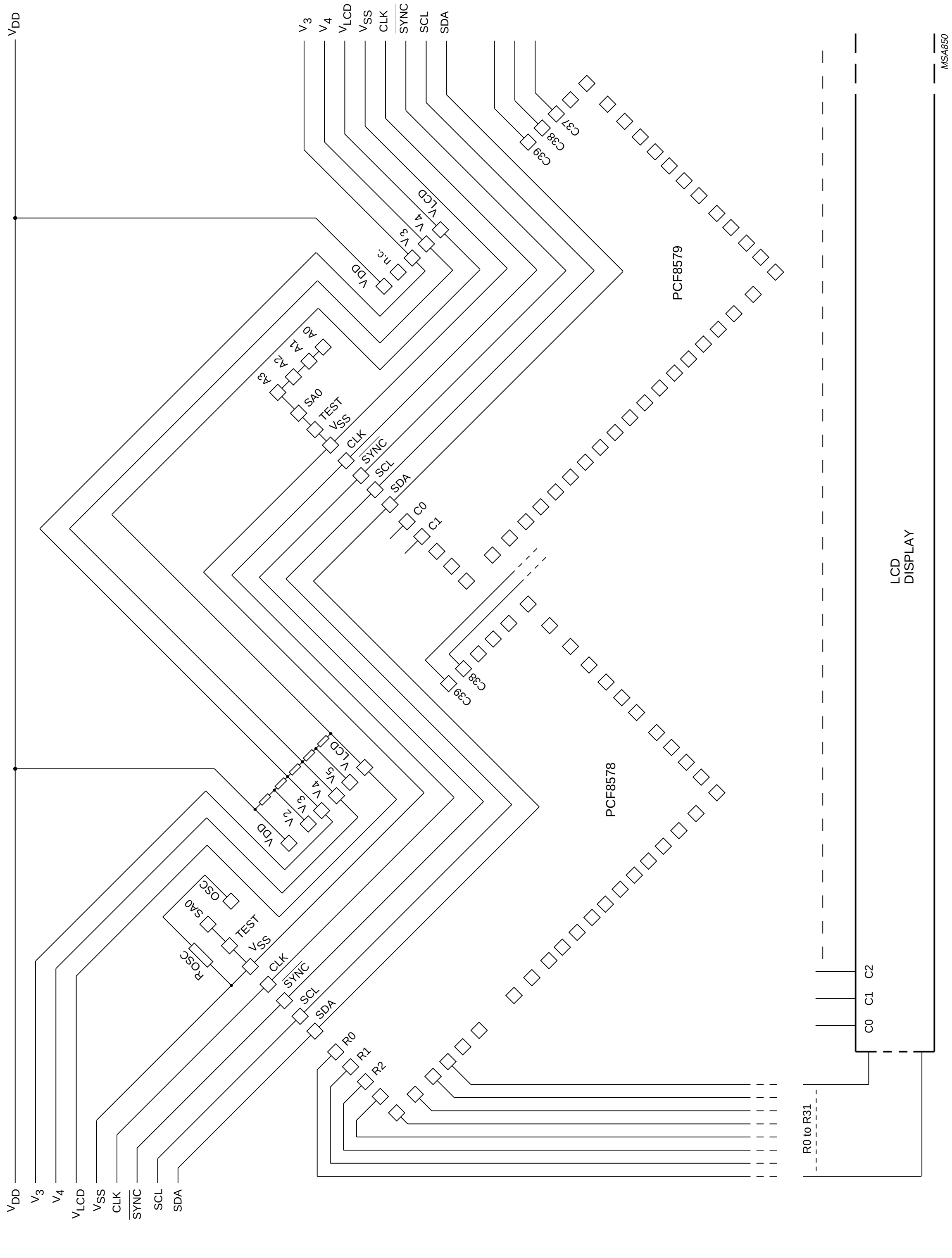
Bonding pad dimensions: 120 µm × 120 µm.

Fig.23 Bonding pad locations.

Table 12 Bonding pad locations (dimensions in μm).
All x/y coordinates are referenced to centre of chip, see Fig.23.

PAD	x	y	PAD	x	y
SDA	252	2142	C27	498	–2142
SCL	48	2142	C26	702	–2142
$\overline{SYNC}$	–156	2142	C25	906	–2142
CLK	–360	2142	C24	1110	–2142
V_{SS}	–564	2142	C23	1314	–2142
TEST	–786	2142	C22	1314	–1830
SA0	–1032	2142	C21	1314	–1570
A3	–1314	2142	C20	1314	–1326
A2	–1314	1920	C19	1314	–1122
A1	–1314	1716	C18	1314	–918
A0	–1314	1512	C17	1314	–714
V_{DD}	–1314	708	C16	1314	–510
n.c.	–1314	504	C15	1314	–306
V_3	–1314	300	C14	1314	–102
V_4	–1314	96	C13	1314	102
V_{LCD}	–1314	–108	C12	1314	306
C39	–1314	–1308	C11	1314	510
C38	–1314	–1512	C10	1314	714
C37	–1314	–1716	C9	1314	918
C36	–1314	–1920	C8	1314	1122
C35	–1314	–2142	C7	1314	1326
C34	–1032	–2142	C6	1314	1566
C33	–786	–2142	C5	1314	1830
C32	–564	–2142	C4	1314	2142
C31	–360	–2142	C3	1110	2142
C30	–156	–2142	C2	906	2142
C29	48	–2142	C1	702	2142
C28	252	–2142	C0	498	2142

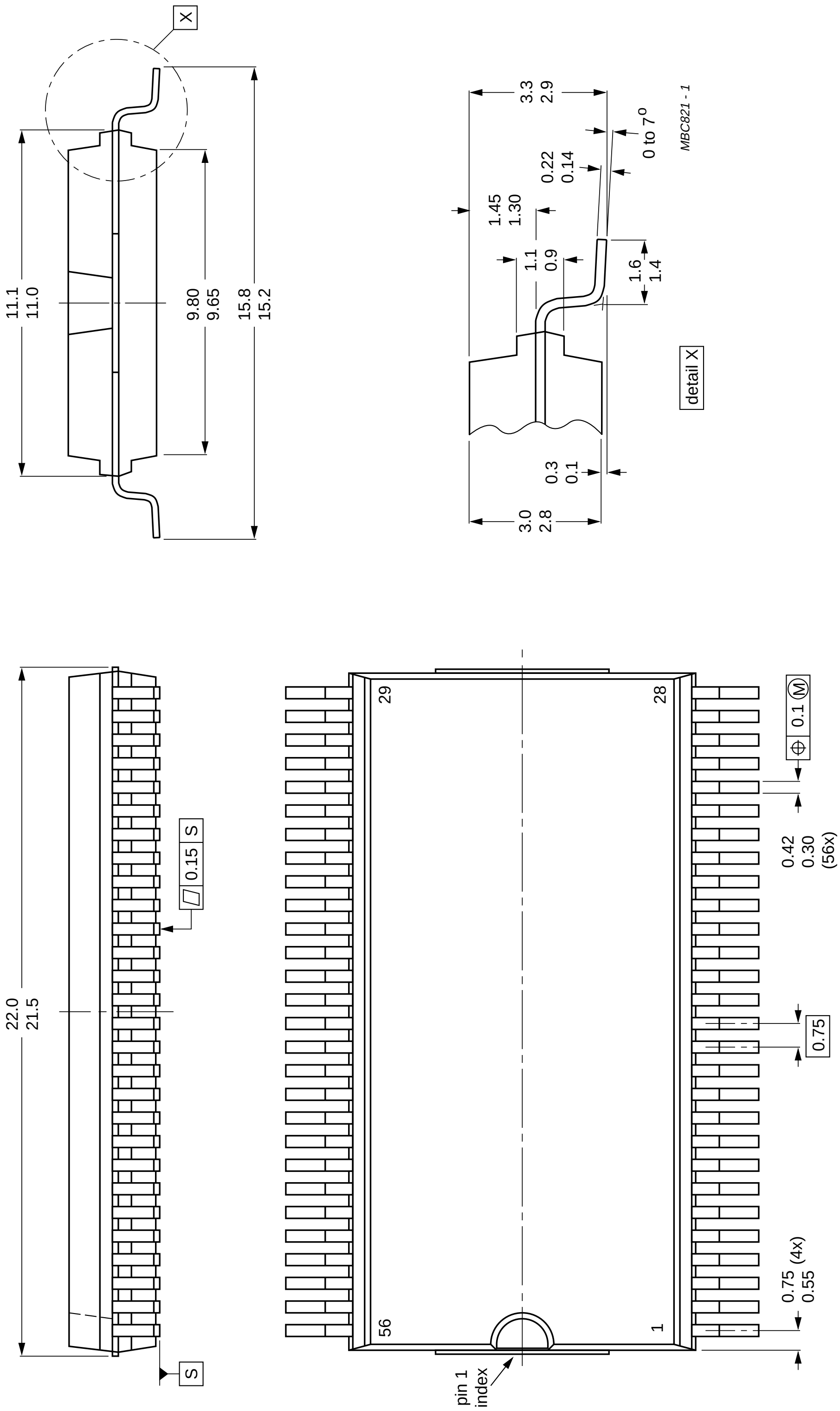
CHIP-ON GLASS INFORMATION



If inputs SA0 and A0 to A3 are left unconnected they are internally pulled-up to V_{DD}.

Fig.24 Typical chip-on glass application (viewed from underside of chip).

PACKAGE OUTLINE



Dimensions in mm.

Fig.25 56-lead mini-pack; plastic (VSO56; SOT190).

SOLDERING

Plastic mini-packs

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which, in a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C°.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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