DATA SHEET

PCD5096
Universal codec

Preliminary specification
File under Integrated Circuits, IC17

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Philips
Semiconductors

PHILIPS

CONTENTS

1 FEATURES

- Applications in digital terminal equipment featuring line interface and/or voice functions
- Digital signal processor performing echo cancellation, codec functions and dial tone detection
- Two independent receive and transmit channels
- Independent programmable gain for all analog inputs and outputs
- Programmable filter correction functions
- Flexible configuration of all functions
- IOM-2 serial data interface (slave mode only)
- Serial data interface to DTAM speech compression ICs
- 400 kHz I^2C-bus slave interface (four I^2C-bus subaddresses)
- Codec compatible with G.714 CCITT specification
- PCM A-Law/u-Law (G.711 CCITT) and 16-bit linear data
- Dual differential inputs and outputs performing the following functions:
  - Line interface connection
  - Loudspeaker, speaker phone (hands-free)
  - Earpiece, microphone (handset)
- Peripheral interface: two I/O pins
- Separate ringer function
- Tone and ringer generator
- Conference call
- QFP44 package
- Low voltage (2.7 to 3.6 V)
- Low power consumption.

2 GENERAL DESCRIPTION

The universal codec combines two high resolution bidirectional analog channels with a DSP in a single chip. Besides the analog interfaces the PCD5096 includes two digital interfaces: an I^2C-bus interface allowing an external microcontroller to program the chip, and a 4-wire serial interface compatible with IOM-2 and with DTAM speech compression ICs. This programmable serial interface offers up to 14 channels and is capable of handling 8-bit (A-law) or 16-bit (linear PCM) data packages, or any combination of them. It opens the scope for a wide application area, for example in combination with the PCD5093H DECT baseband chip for digital cordless business applications.

Several PCD5096s can be connected together for small switching systems (PABX) offering a combination of corded and cordless functionality. Besides the basic functions like echo cancellation for two channels the on-chip DSP provides all necessary functions such as conference call and DTMF.

3 APPLICATIONS

The PCD5096 is designed for the telecommunications market and is targeting small business and residential systems offering a two-line interface or a one-line interface combined with hands-free speaker phone. Specific applications are detailed in Chapter 12.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5096H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body $10 \times 10 \times 1.75$ mm	SOT307-2

5 BLOCK DIAGRAM

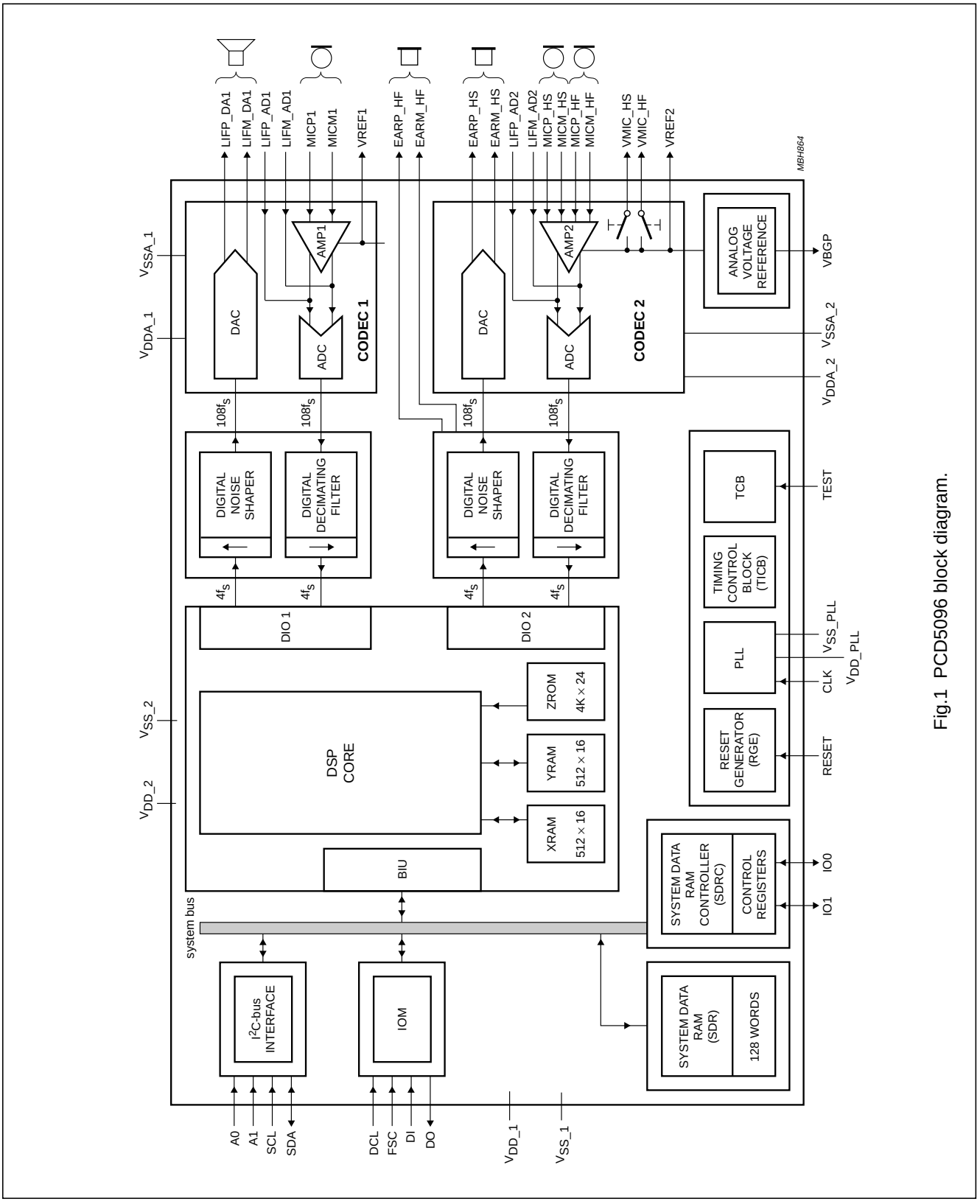


Fig.1 PCD5096 block diagram.

6 PINNING INFORMATION

6.1 Pin description

Table 1 QFP44 package

SYMBOL	PIN	I/O[1]	DESCRIPTION
IO0	1	I/O	programmable I/O pin 0 (Schmitt trigger input, pull-up output)
IO1	2	I/O	programmable I/O pin 1 (Schmitt trigger input, pull-up output)
CLK	3	I	clock input
V_{DD_PLL}	4	P	3 V analog supply for PLL
V_{SS_PLL}	5	P	analog ground supply for PLL
V_{SS_1}	6	P	peripheral ground supply
V_{DD_1}	7	P	3 to 5 V peripheral supply
SCL	8	I	I^2C-bus clock signal input (Schmitt trigger)
SDA	9	I/O	I^2C-bus data signal
A0	10	I	I^2C-bus subaddress
A1	11	I	I^2C-bus subaddress
LIFM_DA1	12	O	negative analog output from Codec 1 to line interface
LIFP_DA1	13	O	positive analog output from Codec 1 to line interface
V_{DDA_1}	14	P	3 V analog supply for Codec 1
LIFM_AD1	15	I	negative analog input to Codec 1 from line interface
LIFP_AD1	16	I	positive analog input to Codec 1 from line interface
V_{SSA_1}	17	P	analog ground supply for Codec 1
MICM1	18	I	negative analog input to Codec 1 from microphone
MICP1	19	I	positive analog input to Codec 1 from microphone
VREF1	20	O	Codec 1 analog reference voltage
VBGP	21	O	bandgap analog output voltage
VREF2	22	O	Codec 2 analog reference voltage
VMIC_HS	23	O	positive analog supply voltage from Codec 2 for handset microphone
MICP_HS	24	I	positive analog input to Codec 2 from handset microphone
MICM_HS	25	I	negative analog input to Codec 2 from handset microphone
VMIC_HF	26	O	positive analog supply voltage from Codec 2 for hands-free microphone
MICP_HF	27	I	positive analog input to Codec 2 from hands-free microphone
MICM_HF	28	I	negative analog input to Codec 2 from hands-free microphone
V_{SSA_2}	29	P	analog ground supply for Codec 2
LIFP_AD2	30	I	positive analog input to Codec 2 from line interface
LIFM_AD2	31	I	negative analog input to Codec 2 from line interface
V_{DDA_2}	32	P	3 V analog supply for Codec 2
EARP_HS	33	O	positive analog output from Codec 2 to handset earpiece
EARM_HS	34	O	negative analog output from Codec 2 to handset earpiece
EARP_HF	35	O	positive output to hands-free earpiece
EARM_HF	36	O	negative output to hands-free earpiece
TEST	37	I	test input; pull-down

SYMBOL	PIN	I/O(1)	DESCRIPTION
RESET	38	I	reset input (Schmitt trigger)
V_{SS_2}	39	P	digital core ground supply
V_{DD_2}	40	P	3 V digital core supply
DI	41	I	IOM-2 interface serial data input
DO	42	O	IOM-2 interface serial data output (open-drain)
FSC	43	I/O	IOM-2 interface 8 kHz frame synchronization clock (Schmitt trigger input); note 2
DCL	44	I/O	IOM-2 interface data clock (Schmitt trigger input); note 2

Note

1. ‘P’ denotes power line.
2. FSC and DCL are outputs only in test modes.

6.2 Pinning

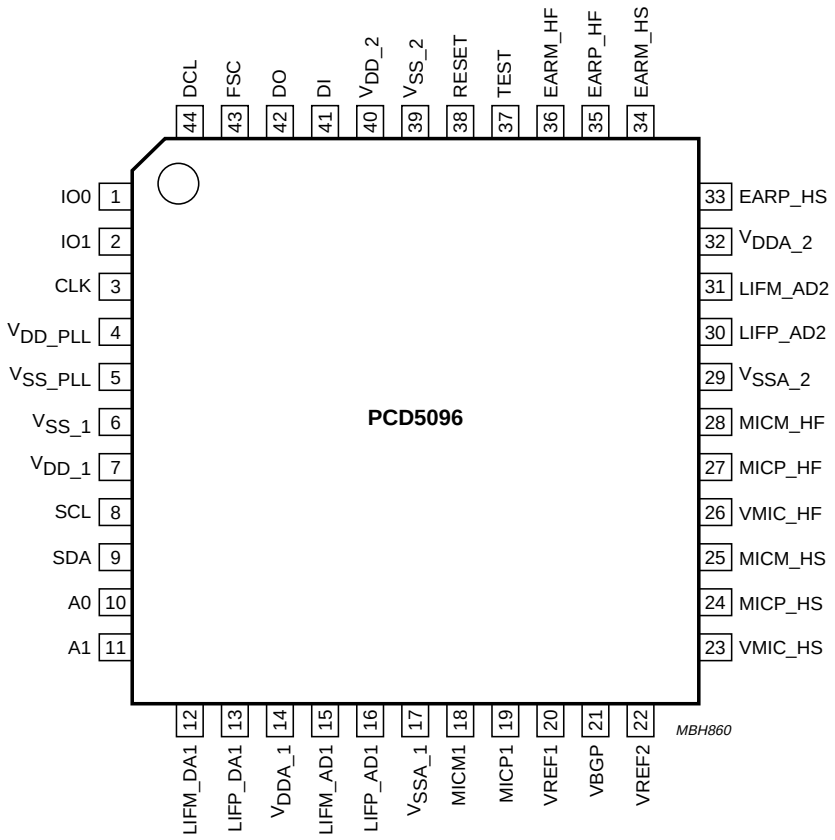


Fig.2 Pin configuration.

6.3 Supply concept

The universal codec is designed for 3 V systems with a voltage range of 2.7 to 3.6 V. To allow connection to 5 V systems the digital I/Os include level shifters. The core must run on 3.3 V and the peripheral supply on 5 V.

The five power supplies are listed in Table 2. Codec 1 and Codec 2 have their own power supplies: V_{DDA_1} and V_{DDA_2} respectively. V_{DD_PLL} is the power supply dedicated to the PLL. The digital core and the memories are powered by V_{DD_2} and the digital peripherals by V_{DD_1}. All digital pins (EARP_HF, EARM_HF, TEST, RESET, DI, DO, FSC, DCL, IO0, IO1, CLK, SCL, SDA, A0 and A1) have internal level shifters, allowing the chip to be used in a 3 to 5 V environment.

Table 2 PCD5096 power supply

SUPPLY PAIR	ASSOCIATED DEVICE
V_{DD_1} and V_{SS_1}	3 to 5 V peripheral supply
V_{DD_2} and V_{SS_2}	3 V digital core supply
V_{DD_PLL} and V_{SS_PLL}	3 V PLL supply
V_{DDA_1} and V_{SSA_1}	3 V Codec 1 supply
V_{DDA_2} and V_{SSA_2}	3 V Codec 2 supply

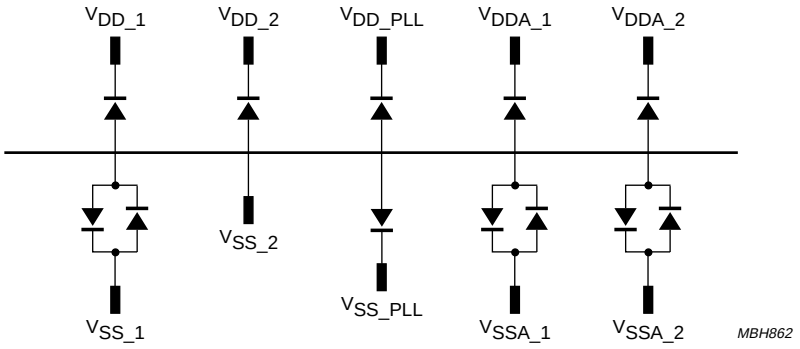


Fig.3 PCx5096 supply rails with protection diodes.

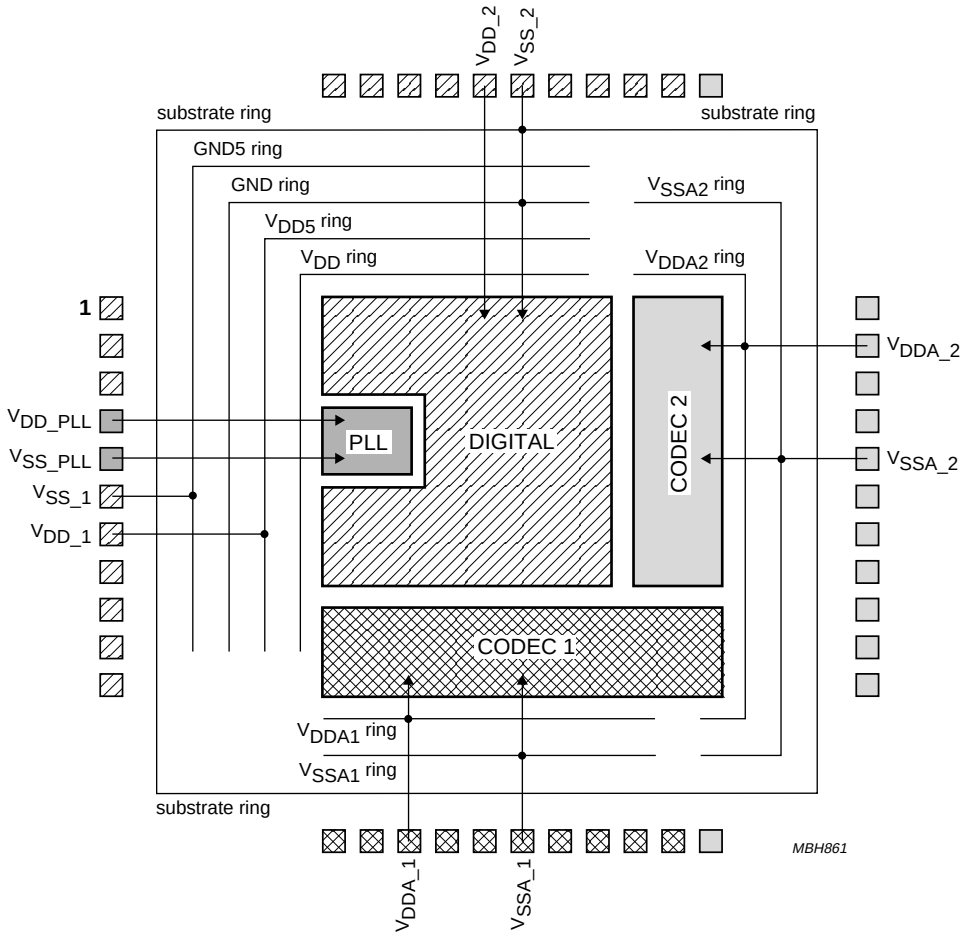


Fig.4 PCD5096 power supply.

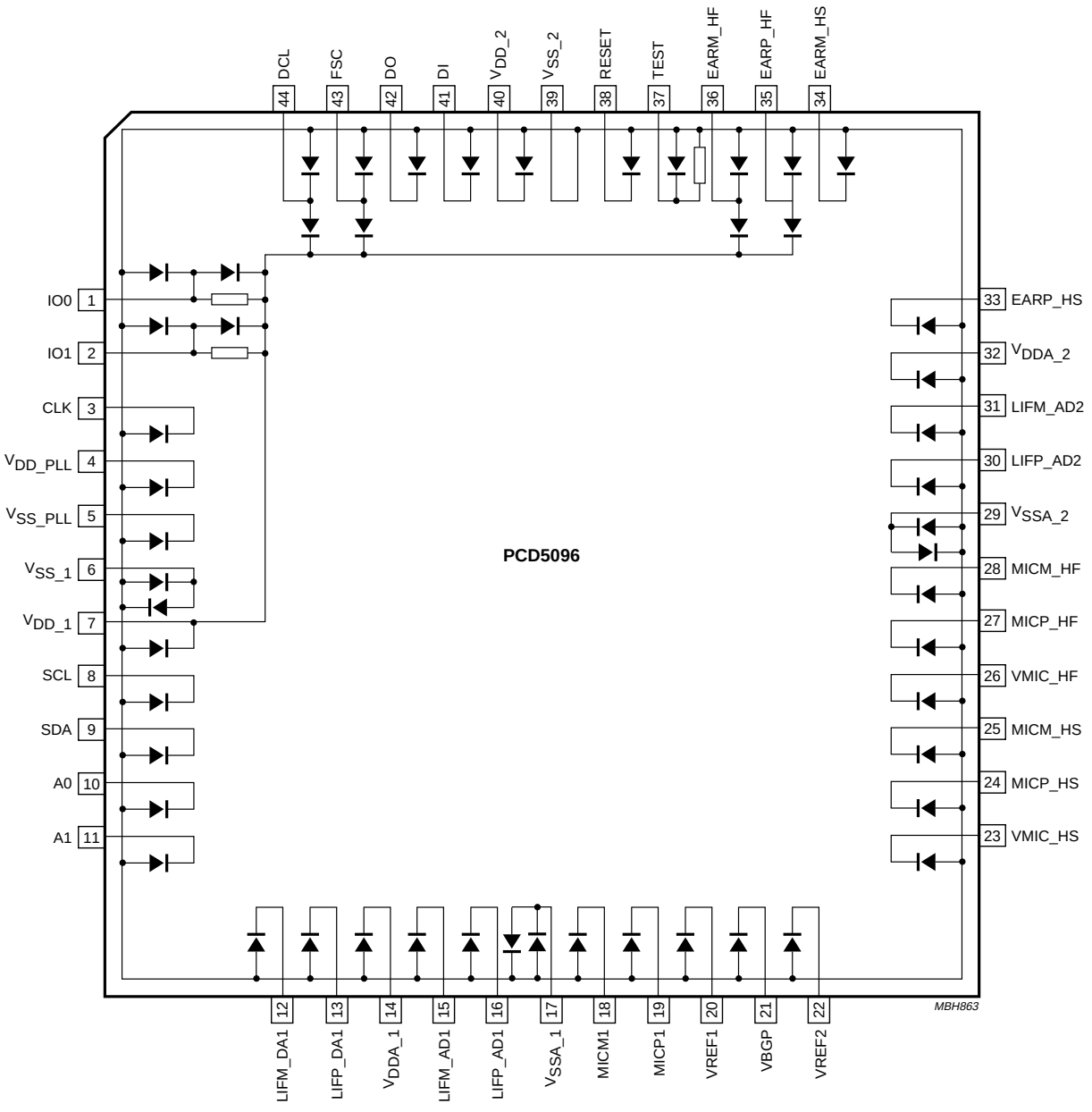


Fig.5 Open/short diagram.

7 FUNCTIONAL DESCRIPTION

7.1 General

The PCD5096 is a universal codec designed for use in digital terminal equipment. It connects two PSTN lines to a digital interface (IOM-2), thus covering a wide application area. Echo cancellation is performed on both PSTN lines by an on-chip DSP. Hands-free speaker phone functionality is also provided by sacrificing one PSTN line connection. The chip is controlled by an external microcontroller via a high bit rate I^2C-bus interface.

Figure 1 shows the block diagram of the PCD5096. The different functional blocks operate more or less autonomously and communicate with each other via the System Data RAM (SDR). Each block has access to the SDR via an internal system bus. Access to this bus is controlled by the System Data RAM Controller (SDRC).

The IOM block connects to a $n \times 256$ kbits/s digital interface (IOM-2 interface) and also supports interfacing to DTAM speech compression ICs. The IOM block stores and fetches speech data into/from the SDR using internal addressing logic.

The DSP block is the link between the data in the SDR stored/fetched by the IOM block on one hand, and the analog front-end on the other hand. The basic functions of the DSP are data filtering, local echo cancelling, network echo suppressing, A-law coding and decoding according to the G.711 CCITT recommendations, dial tone detection and generation, DTMF generation, side-tone, automatic volume control, automatic gain control, double talk detection and conference call.

Data processed by the DSP goes to and comes from two independent codecs interfacing to the PSTN lines. The codecs comply with the G.714 specifications and handle the PCM coding and decoding of speech signals. They perform the analog and high speed digital speech processing functions: analog bitstream A/D and D/A conversion, analog filtering and amplification, digital decimation filtering and noise shaping. Both codecs should be connected to a local line or to a PSTN line, but one codec also supports a corded handset and hands-free speaker and microphone.

The control of the entire chip is done via the I^2C-bus block by writing to the SDR or to special control registers. In this way the DSP and the IOM operation modes can be set, as well as some analog parameters in the two codecs.

The PCD5096 has two general purpose programmable I/O pins controlled by two special registers (direction and state). These two special registers are accessible via the I^2C-bus interface or by the on-chip DSP. A typical application is the generation of interrupts by the DSP, indicating that DTMF tones were detected.

The timing for the whole chip is generated in the Timing Control Block (TICB). The system clock (20.736 MHz) is delivered by a PLL which triples the input clock frequency.

7.2 Clocking

The universal codec is designed to operate in a digital cordless telephone system, for example together with a PCD5093 baseband controller. To save the expense of having to provide each universal codec with a separate crystal, a common clock is provided by the master controller. In the current generation of the Philips DECT baseband controllers this clock is GP_CLK7, a 6.912 MHz clock output derived from the 13.824 MHz crystal oscillator. GP_CLK7 must therefore be used as the input clock for the universal codec. GP_CLK7 is enabled during a reset of the PCD5093 and when either the Burst Mode Logic or codec are turned on (see PCD5093 data sheet).

In order to meet the DSP processing requirements for the various applications an on-chip PLL is used to generate a system clock which is triple the input clock frequency (20.736 MHz).

7.3 Reset and power-down strategy

The universal codec must be reset at power-up. The RESET input must remain HIGH until the CLK input is active (toggling) and stable. After releasing the RESET input, an additional 1024 CLK periods (≈150 μs at 6.912 MHz) must elapse before starting to program the chip via the I^2C-bus interface. This must be done after every RESET pulse. The minimum duration of a RESET pulse is one CLK period. During reset, the I^2C-bus and the IOM-2 interface are inactive.

Entering the Power-down mode is achieved by resetting the chip and holding the RESET input HIGH. This resets the on-chip PLL and stops the system clock. The user must ensure that the IOM-2 interface is deactivated and the I^2C-bus idle before resetting the chip in order not to interrupt any transaction on these two interfaces. Note that stopping the CLK input is only allowed while the RESET input is HIGH. To exit the Power-down mode the RESET input is set LOW and after 1024 CLK periods (≈150 μs at 6.912 MHz) have elapsed normal operation can be resumed.

After reset, all the flip-flops are in a defined state, and the IOM, DSP and codecs are in inactive mode. In typical applications the universal codec is used with the PCD5093, which provides a clock (GP_CLK7) and a reset signal to the universal codec. The reset signal must be generated by a microcontroller port bit. The RESET_OUT pin of the PCD5093 cannot be used for this purpose, because GP_CLK7 is stopped while RESET_OUT is LOW after a Power-on-reset.

8 MEMORY AND CONTROL REGISTERS

8.1 DSP memories

The DSP in the PCD5096 has access to a 4k $\times$ 24-bit DSP program ROM, a 512 $\times$ 16-bit XRAM and a 512 $\times$ 16-bit YRAM.

8.2 Data memory and control register map

The PCD5096 contains a 128 word (128 $\times$ 16-bit) System Data RAM (SDR) and a group of 7 control registers mapped onto the upper addresses of the SDR.
The registers and the SDR are byte and word accessible externally, via the I^2C-bus interface and internally via the internal system bus.

The memory map is shown in Fig.6. The lower 32 words contain the DSP parameter table. The next 32 words are reserved for the IOM control table, which is used to control the activity on the IOM-2 interface (maximum 32 slots per 8 kHz speech frame). The rest of the SDR addressable space (40H to 77H) is free RAM and can be used to store up to 14 IOM data buffer pairs. In cases where not all 14 IOM buffer pairs are needed this memory space can be used for other applications via the I^2C-bus. The same holds for the unused part of the IOM control table.

The upper addresses of the SDR (78H to 7EH) are mapped onto 7 control registers (CR0 to CR6) that control the entire chip (DSP mode, data rate on the IOM-2 interface, control of the two codecs).

Note that the uppermost address of the SDR (7FH) is not mapped to any hardware register and is addressable as a normal RAM word.

The contents of the IOM control table and the IOM data buffers are described in Chapter 9. For further details about the DSP parameter table, see the *"PCD5096 DSP user manual"*.

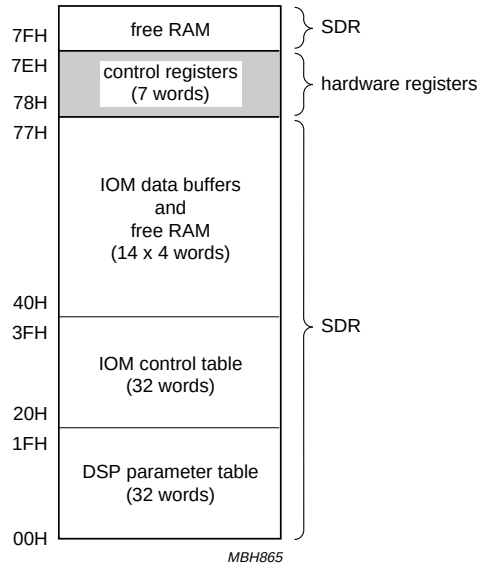


Fig.6 PCD5096 Memory map.

8.3 Control registers organization

8.3.1 CONTROL REGISTER ASSIGNMENT

The control register address assignment in the PCD5096 is shown in Table 3.

Table 3 Control register map

REGISTER	REGISTER MNEMONIC	SIZE (BITS)	ADDRESS (HEX)	RESET STATE (HEX)	FUNCTION
Control Register 0	CR0	16	78	0000	control signals for codecs, codec test modes, Power-down control and disable phase correction
Control Register 1	CR1	3	79	00	IOM control
Control Register 2	CR2	16	7A	0000	gain setting of analog-to-digital (A/D) and digital-to-analog (D/A) paths
Control Register 3	CR3	16	7B	A0A0	reference voltage setting of Codec 1 and Codec 2
Control Register 4	CR4	16	7C	0000	selection of the DSP modes
Control Register 5	CR5	2	7D	02	control of I/O pin IO0
Control Register 6	CR6	2	7E	02	control of I/O pin IO1

8.3.2 Control Register 0 (CR0)

Table 4 Control Register 0 (address 78H)

15	14	13	12	11	10	9	8
–	DISPC	CDC2TM2	CDC2TM1	CDC2TM0	CDC1TM2	CDC1TM1	CDC1TM0

Table 5 Control Register 0 (continued)

7	6	5	4	3	2	1	0
HFMICON	HSMICON	LHFEN	EHSEN	CDC2ON	ADD_DC	LIF1_EN	CDC1ON

Table 6 Description of CR0 bits

BIT	SYMBOL	DESCRIPTION
15	–	reserved, not used
14	DISPC	**Disable Phase Correction.** If DISPC = 1, phase correction is disabled.
13	CDC2TM2	**Functional test modes of Codec 2.** These 3 bits select the functional test modes of Codec 2; see Table 7.
12	CDC2TM1	
11	CDC2TM0	
10	CDC1TM2	**Functional test modes of Codec 1.** These 3 bits select the functional test modes of Codec 1; see Table 7.
9	CDC1TM1	
8	CDC1TM0	
7	HFMICON	**Hands-free Microphone ON in Codec 2.** When this bit is set the internal microphone reference voltage VREFMIC is connected to pad VMIC_HF (supply pad for the external hands-free microphone).
6	HSMICON	**Handset Microphone ON in Codec 2.** When this bit is set the internal microphone reference voltage VREFMIC is connected to pad VMIC_HS (supply pad for the external handset microphone).
5	LHFEN	**Loudspeaker Enable for hands-free.** This bit enables the Noise Shaper data in Codec 2 to the hands-free pads EARP_HF and EARM_HF.
4	EHSEN	**Earpiece Enable for Handset.** This bit enables the Noise Shaper data to the DAC in Codec 2.
3	CDC2ON	**Codec 2 ON.** When CDC2ON = 1, Codec 2 is ON.
2	ADD_DAC	**Add a DC offset in the microphone amplifier of Codec 1.**
1	LIF1_EN	**Line Interface Enable for Codec 1.** This bit enables the Noise Shaper data to the DAC in Codec 1.
0	CDC1ON	**Codec 1 ON.** When CDC1ON = 1, Codec 1 is ON.

Table 7 Selection of functional test modes for Codec 1 and Codec 2

CDC2TM2	CDC2TM1	CDC2TM0	FUNCTIONAL TEST MODE
CDC1TM2	CDC1TM1	CDC1TM0	
0	0	0	normal operation
0	0	1	1 bit analog
0	1	0	1 bit digital
0	1	1	1 bit closed loop
1	0	0	$4f_s$ codec
1	0	1	$4f_s$ DSP
1	1	0	$4f_s$ closed loop
1	1	1	PCM probe

8.3.3 CONTROL REGISTER 1 (CR1)

Table 8 Control Register 1 (address 79H)

2	1	0
IOM2	IOM1	IOM0

Table 9 Description of CR1 bits

BIT	SYMBOL	DESCRIPTION
2	IOM2	These 3 bits select the IOM mode; see Table 10.
1	IOM1	
0	IOM0	

Table 10 Selection of IOM mode

IOM2	IOM1	IOM0	IOM MODE
0	0	0	inactive
0	0	1	not used
0	1	0	IOM slave 256 kbits/s in 4 speech-slots/speech-frame
0	1	1	IOM slave 512 kbits/s in 8 speech-slots/speech-frame
1	0	0	IOM slave 768 kbits/s in 12 speech-slots/speech-frame
1	0	1	IOM slave 1024 kbits/s in 16 speech-slots/speech-frame
1	1	0	SpeechPro slave 2048 kbits/s in 32 speech-slots/speech-frame; note 1
1	1	1	IOM slave 2048 kbits/s in 32 speech-slots/speech-frame

Note

1. The SpeechPro mode is similar to the IOM slave 32 slots mode, but with a non-doubled data clock DCL.

8.3.4 CONTROL REGISTER 2 (CR2)

CR2 contains the gain setting values of the analog Codec 1 and Codec 2 section. The state of CR2 after reset is 0000H. This sets the A/D path and the D/A path gain to their minimum values of +9 dB and –13 dB respectively.

The D/A path gain is defined as the relationship between the level of the analog output signal, differentially seen at EARP_HS - EARM_HS or LIFP_DA1 - LIFM_DA1, expressed in dBm (0 dBm0 is 1 mW in 600 Ω), and the level of the digital input signal at the PCM interface, expressed in dBm0 according to CCITT Recommendation G.711. This D/A path gain definition assumes that the volume control in the DSP is set to the default value of 0 dB.

The A/D path gain is defined as the relationship between the level of the digital output signal at the PCM interface, expressed in dBm0, and the level of the analog input signal at the LIF interface, differentially seen at LIFP_AD2 - LIFM_AD2 or LIFP_AD1 - LIFM_AD1, expressed in dBm.

Table 11 Control Register 2 (address 7AH)

15	14	13	12	11	10	9	8
DA2.3	DA2.2	DA2.1	DA2.0	AD2.3	AD2.2	AD2.1	AD2.0

Table 12 Control Register 2 (continued)

7	6	5	4	3	2	1	0
DA1.3	DA1.2	DA1.1	DA1.0	AD1.3	AD1.2	AD1.1	AD1.0

Table 13 Description of CR2 bits

BIT	SYMBOL	DESCRIPTION
15	DA2.3	These 4 bits select the D/A path gain for Codec 2; see Table 14.
14	DA2.2	
13	DA2.1	
12	DA2.0	
11	AD2.3	These 4 bits select the A/D path gain for Codec 2; see Table 15.
10	AD2.2	
9	AD2.1	
8	AD2.0	
7	DA1.3	These 4 bits select the D/A path gain for Codec 1; see Table 14.
6	DA1.2	
5	DA1.1	
4	DA1.0	
3	AD1.3	These 4 bits select the A/D path gain for Codec 1; see Table 15.
2	AD1.2	
1	AD1.1	
0	AD1.0	

Table 14 Selection of D/A path gain for Codec 1 and Codec 2

DA1.3	DA1.2	DA1.1	DA1.0	D/A PATH GAIN (dB)
DA2.3	DA2.2	DA2.1	DA2.0	
0	0	0	0	–13
0	0	0	1	–12
0	0	1	0	–11
0	0	1	1	–10
0	1	0	0	–9
0	1	0	1	–8
0	1	1	0	–7
0	1	1	1	–6
1	0	0	0	–5
1	0	0	1	–4
1	0	1	0	–3
1	0	1	1	–2
1	1	0	0	–1
1	1	0	1	0
1	1	1	0	+1
1	1	1	1	+2

Table 15 Selection of A/D path gain for Codec 1 and Codec 2

AD1.3	AD1.2	AD1.1	AD1.0	A/D PATH GAIN (FROM LIF TO PCM) (dB)
AD2.3	AD2.2	AD2.1	AD2.0	
0	0	0	0	+9
0	0	0	1	+10
0	0	1	0	+11
0	0	1	1	+12
0	1	0	0	+13
0	1	0	1	+14
0	1	1	0	+15
0	1	1	1	+16
1	0	0	0	+17
1	0	0	1	+18
1	0	1	0	+19
1	0	1	1	+20
1	1	0	0	+21
1	1	0	1	+22
1	1	1	0	+23
1	1	1	1	+24

8.3.5 CONTROL REGISTER 3 (CR3)

This 16-bit register is used to adjust the reference voltage of Codec 1 and Codec 2 to 2000 mV. An accuracy of 12 mV is guaranteed. The equation for determining the reference voltage (VREFn) for each codec is given below:

$$VREFn = \frac{256 \times VBGP}{RVnREF}$$

Where 'n' is the codec number and can take a value of '1' or '2'. The default value for VBGP is 1.25 V but this may vary due to process spread (see Chapter 16). Note that increasing RVnREF reduces VREFn.

For correct function of the analog blocks, care must be taken to have sensible values in CR3. For example, bits (15:14), as well as (7:6) must be '10'. The state of this register after reset is A0A0H.

Table 16 Control Register 3 (address 78H)

15	14	13	12	11	10	9	8
1	0	RV2REF5	RV2REF4	RV2REF3	RV2REF2	RV2REF1	RV2REF0

Table 17 Control Register 3 (continued)

7	6	5	4	3	2	1	0
1	0	RV1REF5	RV1REF4	RV1REF3	RV1REF2	RV1REF1	RV1REF0

Table 18 Description of CR2 bits

BIT	SYMBOL	DESCRIPTION
15	–	This bit must be set to a logic 1.
14	–	This bit must be set to a logic 0.
13	RV2REF5	These 5 bits are used to select the reference voltage of Codec 2.
12	RV2REF4	
11	RV2REF3	
10	RV2REF2	
9	RV2REF1	
8	RV2REF0	
7	–	This bit must be set to a logic 1.
6	–	This bit must be set to a logic 0.
5	RV1REF5	These 5 bits are used to select the reference voltage of Codec 1.
4	RV1REF4	
3	RV1REF3	
2	RV1REF2	
1	RV1REF1	
0	RV1REF0	

8.3.6 CONTROL REGISTER 4 (CR4)

CR4 is used to select the DSP modes. For further information see the *"PCD5096 DSP user manual*". Its state after reset is 0000H.

Table 19 Control Register 4 (address 7CH)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	–	LLb2	LLb1	LLb0	LLa2	LLa1	LLa0	OPM1	OPM0

Table 20 Description of CR4 bits

BIT	SYMBOL	DESCRIPTION
15 to 8	–	These 8 bits are not used.
7	LLb2	These 3 bits select the connection mode for channel LLb; see Table 21.
6	LLb1	
5	LLb0	
4	LLa2	These 3 bits select the connection mode for channel LLa; see Table 21.
3	LLa1	
2	LLa0	
1	OPM1	These 2 bits select the operation mode, see Table 22.
0	OPM0	

Table 21 Selection of the connection mode for channels LLb and LLa

LLb2	LLb1	LLb0	CONNECTION MODES
LLa2	LLa1	LLa0	
0	0	0	Idle mode with reset of LEC coefficients
0	0	1	Idle mode without reset of LEC coefficients
0	1	0	speech and tone
0	1	1	tone generation
1	0	0	dial tone detection
1	0	1	not allowed
1	1	0	not allowed
1	1	1	not allowed

Table 22 Selection of the operation mode

OPM1	OPM0	OPERATION MODE
0	0	connection mode
0	1	read/write RAM mode
1	0	software reset
1	1	not allowed

8.3.7 Control Register 5 (CR5)

CR5 controls the general purpose I/O pin IO0.

Table 23 Control Register 5 (address 7DH)

1	0
IODIR0	IO0

Table 24 Description of CR5 bits

BIT	SYMBOL	DESCRIPTION
1	IODIR0	Direction control for IO0. If IODIR0 = 1, then IO0 is an input. If IODIR0 = 0, then IO0 is an output. Input during and after reset; see note 1.
0	IO0	State of IO0

Note

1. Depending on the DSP program, the contents of CR5 might be overwritten by the DSP as soon as the reset is inactive.

8.3.8 Control Register 6 (CR6)

CR6 controls the general purpose I/O pin IO1.

Table 25 Control Register 6 (address 7EH)

1	0
IODIR1	IO1

Table 26 Description of CR6 bits

BIT	SYMBOL	DESCRIPTION
1	IODIR1	Direction control for IO1. If IODIR1 = 1, then IO1 is an input. If IODIR1 = 0, then IO1 is an output. Input during and after reset; see note 1.
0	IO1	State of IO1

Note

1. Depending on the DSP program, the contents CR6 might be overwritten by the DSP as soon as the reset is inactive.

9 IOM

9.1 Features

The IOM block in the PCD5096 is a 4-wire serial interface performing the following functions:

- Digital interface with up to fourteen 64 kbits/s channels at a bit rate of n × 256 kbits/s (n = 1, 2, 3, 4 or 8), complying with the IOM-2 specifications (IOM-2 is a registered trademark of Siemens AG)
- Digital interface with 32 slots/frame and non-doubled data clock, compatible with the digital interface of some DTAM speech compression ICs
- Autonomous storing/fetching of data to/from the system data memory (SDR) using internal addressing logic
- Byte or word (16 bits) transfer
- 14 data buffers (byte or word)
- Muting of speech data
- Local call.

9.2 Pin description

The following pins are used by the IOM-2 interface:

- **DI**: serial data input with a bit rate of n × 256 kbits/s (n = 1, 2, 3, 4 or 8)
- **DO**: serial data output with a bit rate of n × 256 kbits/s (n = 1, 2, 3, 4 or 8). DO is an open-drain pin, as many devices must be able to write on the same data line in a time-multiplexed mode. Therefore, DO must be externally pulled-up.
- **FSC**: 8 kHz frame synchronization input
- **DCL**: data clock input. Twice the data transmission frequency on DI and DO, except in the non-doubled data clock mode (see Section 9.3).

9.3 Functional description

The digital interface of the PCD5096 can work at several bit rates; these are specified Table 27. The bit rate is selected by writing the appropriate 3 bit code, given in Table 27, into Control Register 1 (address 79H).

The PCD5096 is always a slave on the IOM interface, which means that both FSC and DCL are inputs. This is valid for both the IOM modes and the Speech mode.

FSC is an 8 kHz framing signal for synchronizing data transmission on DI and DO. The rising edge of FSC gives the time reference for the first bit transmitted in the first slot of a speech frame. The number of slots per speech frame depends on the selected data rate. Each slot contains 8 data bits.

DCL is a data clock. Its frequency is twice the selected data rate in IOM mode. In Speech mode, the DCL frequency is equal to the data rate (2048 kHz for 2048 kbits/s).

DI is the serial data input. Data coming on DI in packets of 8 bits (A-law PCM encoded data) or 16 bits (linear PCM data) is stored temporarily in an IOM data buffer, from where it is processed by the on-chip DSP. On the other hand, data written into the IOM data buffers by the DSP is shifted out on pin DO.

There are 14 IOM data buffers, allowing the use of 14 different channels. One channel is 64 kbits/s for A-law PCM encoded data and 128 kbits/s if linear PCM data is transferred, in which case two consecutive slots are used.

The Speech mode was implemented to support the codec interface of some speech compression ICs. This mode is very similar to the IOM 32 slots mode, the main difference being the non-doubled data clock. See Section 9.4 for timing information.

Table 27 IOM modes

IOM2	IOM1	IOM0	MODE
0	0	0	These codes deactivate the IOM-2 interface and stop all the transactions on the IOM bus. This is the default state after reset.
0	0	1	
0	1	0	IOM slave mode, 256 kbits/s in 4 slots/speech-frame
0	1	1	IOM slave mode, 512 kbits/s in 8 slots/speech-frame
1	0	0	IOM slave mode, 768 kbits/s in 12 slots/speech-frame
1	0	1	IOM slave mode, 1024 kbits/s in 16 slots/speech-frame
1	1	0	Speech mode, 2048 kbits/s in 32 slots/speech-frame. The Speech mode is similar to the IOM slave 32 slots mode, but with a non-doubled data clock DCL.
1	1	1	IOM slave mode, 2048 kbits/s in 32 slots/speech-frame

9.4 Timing

The timing on the 4-wire interface for the IOM mode is shown in Fig.7 and specified in Table 28. The timing for the Speech mode is shown Fig.8 and specified in Table 29.

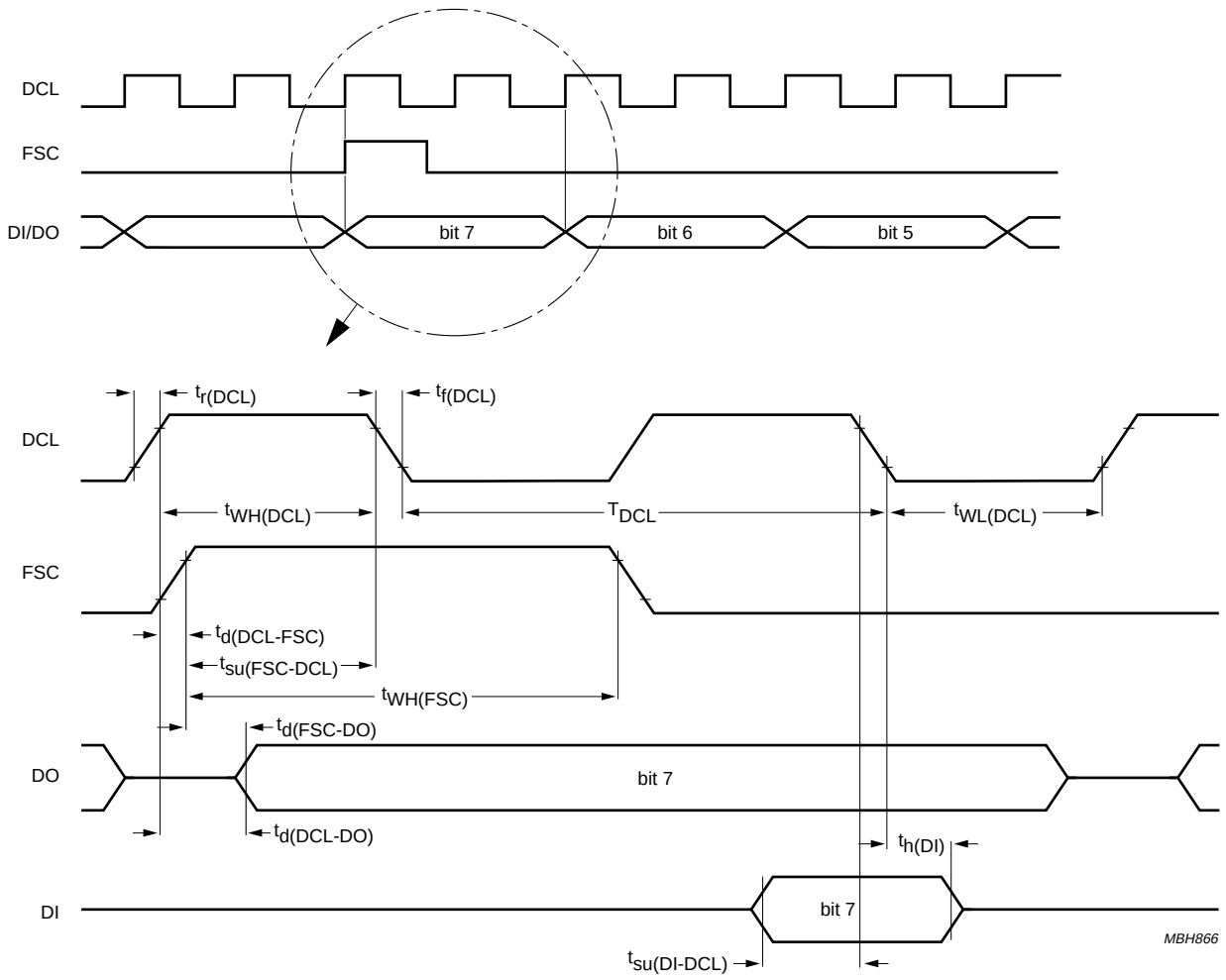


Fig.7 4-wire interface timing in IOM mode.

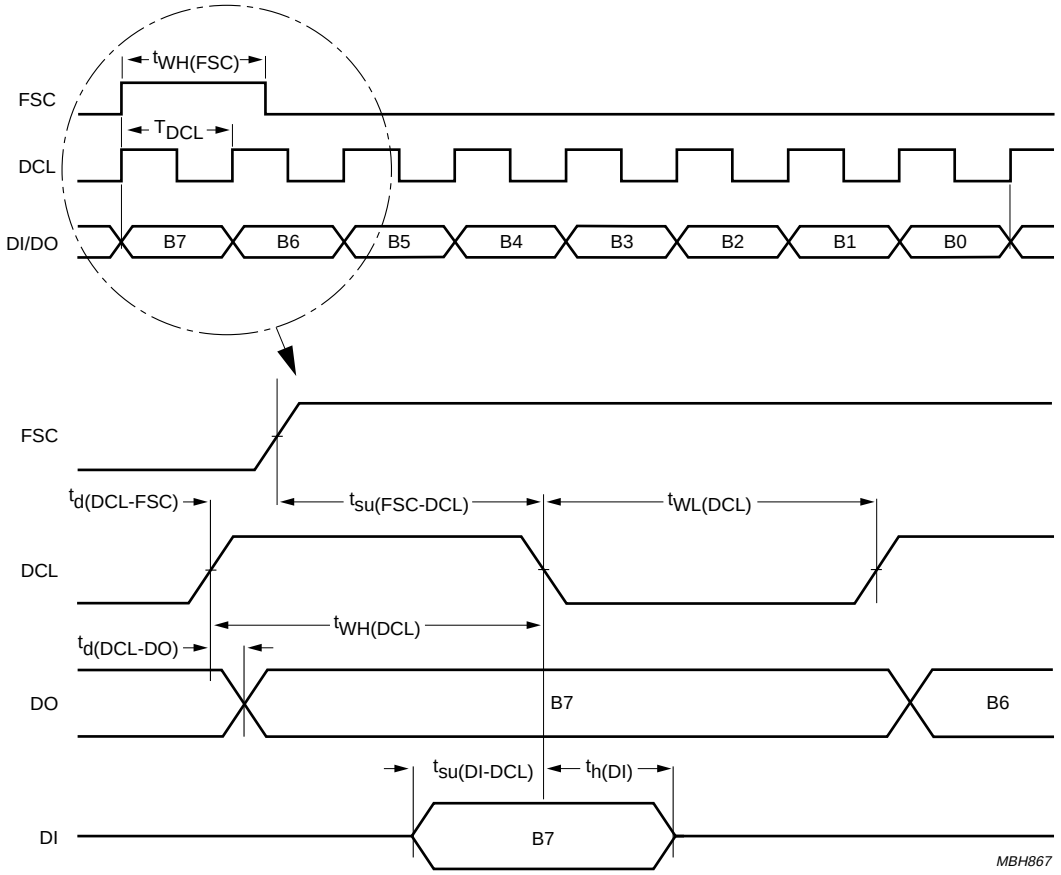


Fig.8 4-wire interface timing in Speech mode.

Table 28 Timing parameters in IOM mode; see Fig.7

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$t_{r(DCL)}$	data clock rise time	–	60	ns
$t_{f(DCL)}$	data clock fall time	–	60	ns
T_{DCL}	data clock period	220[1]	–	ns
$t_{WH(DCL)}$	data clock pulse width HIGH	80	–	ns
$t_{WL(DCL)}$	data clock pulse width LOW	80	–	ns
$t_{r(FSC)}$	frame sync rise time	–	60	ns
$t_{f(FSC)}$	frame sync fall time	–	60	ns
$t_{d(DCL-FSC)}$	frame delay DCL to FSC	$-t_{WL(DCL)}$	60	ns
$t_{su(FSC-DCL)}$	frame set-up time FSC to DCL	60	–	ns
$t_{WH(FSC)}$	frame width HIGH	130	–	ns
$t_{d(DLC-DO)}$	data delay from data clock	–	100[2]	ns
$t_{d(FSC-DO)}$	data delay from frame	–	150[2]	ns
$t_{su(DI-DCL)}$	set-up time DI to DCL	$t_{WH(DCL)}$	–	ns
$t_{h(DI)}$	data hold time	50	–	ns

Notes

1. Corresponds to the highest DCL frequency allowed (4.096 MHz) with a 10% margin.
2. C_L = 150 pF.

Table 29 Timing parameters in Speech mode; see Fig.8

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$t_{d(DCL-FSC)}$	frame delay time DCL to FSC	$-t_{WL(DCL)}$	100	ns
$t_{su(FSC-DCL)}$	frame set-up time FSC to DCL	60	–	ns
$t_{WH(FSC)}$	frame width HIGH	130	–	ns
T_{DCL}	data clock period	440[1]	–	ns
$t_{WL(DCL)}$	data clock pulse width LOW	150	–	ns
$t_{WH(DCL)}$	data clock pulse width HIGH	150	–	ns
$t_{d(DCL-DO)}$	data delay from clock	–	100[2]	ns
$t_{su(DI-DCL))}$	set-up time DI to DCL	60	–	ns
$t_{h(DI)}$	data hold time	60	–	ns

Notes

1. Corresponds to the DCL frequency (2.048 MHz) with a 10% margin.
2. C_L = 150 pF.

9.5 IOM control table

The selection of active slots in the IOM-2 interface and the logic connection between an IOM slot and an IOM data buffer is defined in the IOM control table located at addresses 20H to 3FH of the SDR. The IOM control table is ‘n’ words long. The number ‘n’ is the number of slots resulting from the IOM mode selection in Control Register 1. Speech slot 0 is defined by word 0 (address 20H) in the IOM control table, and speech slot ‘n’ by word ‘n’ (address 20H + n). The IOM interface block reads all words in the IOM control table once every speech frame (125 μs). In every IOM slot in a speech frame the IOM-2 interface block reads the corresponding word in the IOM control table. The function of the bits within each word is shown in Table 30. Depending on the IOM mode selected, only part of the IOM control table address space is used. The unused space is free for extra IOM data buffers or for other applications.

Table 30 Word definition in the IOM control table

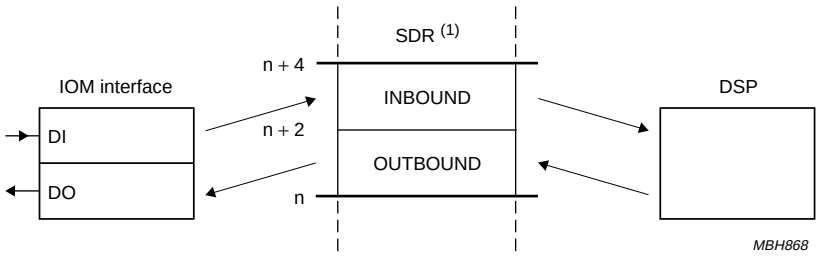
BIT	FUNCTION
B15 to B10	not used
B9	**Mute.** If B9 = 1, data on the DO output is forced to zero regardless of the contents of the IOM data buffer. The input data on DI is not affected. If B9 = 0, then normal operation is selected.
B8	**Local.** If B8 = 1, swap in/out buffers. If B8 = 0, then normal operation is selected. See Section 9.7.
B7	**Select byte.** When byte transfer is selected (B6 = 1); B7 = 1, selects the high byte and B7 = 0 selects the low byte.
B6	**Byte/word transfer.** If B6 = 1, then byte transfer is selected. If B6 = 0, then word transfer is selected and two consecutive slots are activated.
B5	**Active slot.** If B5 = 1, the slot is active. If B5 = 0, the slot is idle.
B4 to B0	**IOM data buffer assigned to the slot.** These 4 bits select the locations in SDR where the IOM data buffer will reside. The allowed values are 10000 to 11101; see Table 31.

Table 31 IOM data buffers location in SDR

IOM BUFFER CODE					ADDRESS IN SDR (HEX)
B4	B3	B2	B1	B0	
1	0	0	0	0	40 to 43
1	0	0	0	1	44 to 47
1	0	0	1	0	48 to 4B
1	0	0	1	1	4C to 4F
1	0	1	0	0	50 to 53
1	0	1	0	1	54 to 57
1	0	1	1	0	58 to 5B
1	0	1	1	1	5C to 5F
1	1	0	0	0	60 to 63
1	1	0	0	1	64 to 67
1	1	0	1	0	68 to 6B
1	1	0	1	1	6C to 6F
1	1	1	0	0	70 to 73
1	1	1	0	1	74 to 77

9.6 IOM data buffers

The address space 40H to 77H in the SDR is reserved for up to 14 IOM data buffers. These buffers are used to exchange data between the IOM-2 interface and the on-chip DSP. Each IOM data buffer consists of four 16-bit words: two words for storing inbound data and two words for outbound data; this is shown in Fig.9



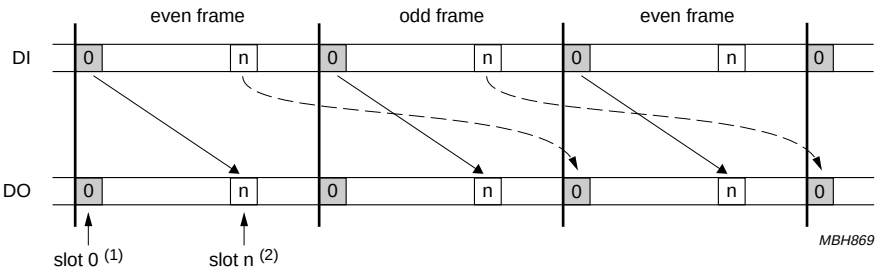
(1) IOM data buffers location is SDR: n = S × 4 with S = B4 to B0 of the corresponding word in the IOM control table.

Fig.9 Data flow between the IOM-2 interface and the DSP.

9.7 Local loop

A local call is implemented in order to loop-back data from one codec to another codec and vice-versa, as illustrated in Fig.10. The inbound and outbound buffer are simply swapped. This is done by setting bit 8 in the correct IOM control table word (see Section 9.5).

A local call is created by assigning one IOM data buffer to 2 codecs, whereby in one IOM control word bit 8 is set, and in the other IOM control word bit 8 is reset.



(1) Bit 8 is set in slot 0 control word.
(2) Bit 8 is reset in slot n control word.

Fig.10 Local call switching on the IOM interface.

10 I²C-BUS INTERFACE

The PCD5096 is programmed by writing to the control registers (CR0 to CR6) and loading the SDR using the I²C-bus interface. The master on the I²C-bus is either a PCD509x DECT processor or an external microcontroller.

The memory map of the PCD5096 is given in Chapter 8. It consists of 128 words (16 bits wide) of system data IOM buffers, IOM control data and DSP parameters) and 7 words (16 bits wide) of control registers mapped at addresses 78H to 7EH.

The I²C-bus interface uses word and byte access to the RAM and to the control registers. For byte access the address is not incremented automatically. For word access the address is incremented after two data bytes (low, high byte) in order to be able to fill the memory without a full I²C-bus protocol (start, slave address, stop bits).

The protocol is shown in Figs 12 to 15. I2C_BYTE = 1, for byte access and I2C_BYTE = 0, for word access. I2C_BSEL = 1 for selecting the high byte and I2C_BSEL = 0 for selecting the low byte. For control registers with less than 8 bits, there is no difference between word access, high byte access and low byte access.

The PCD5096 has two pins (A1 and A0) for programming the slave address. This means that a maximum of four devices can be located on a board without glue logic. The I²C-bus slave address allocated for the PCD5096 is shown in Fig.11.

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
0	0	1	1	0	A1	A0	

MBH870

Fig.11 PCD5096 I²C-bus slave address.

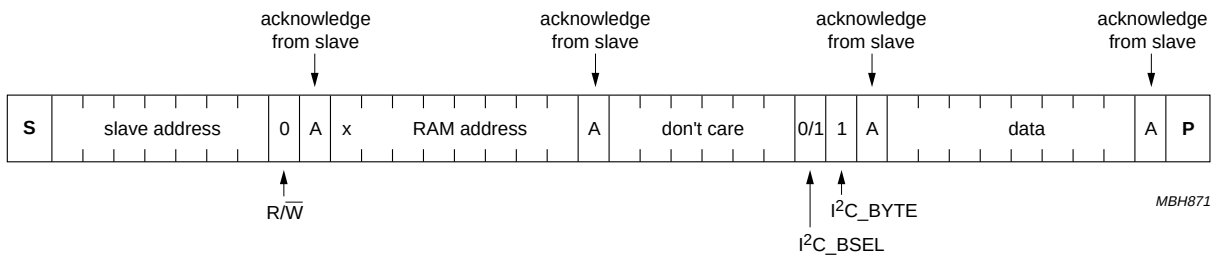


Fig.12 I^2C-bus write byte.

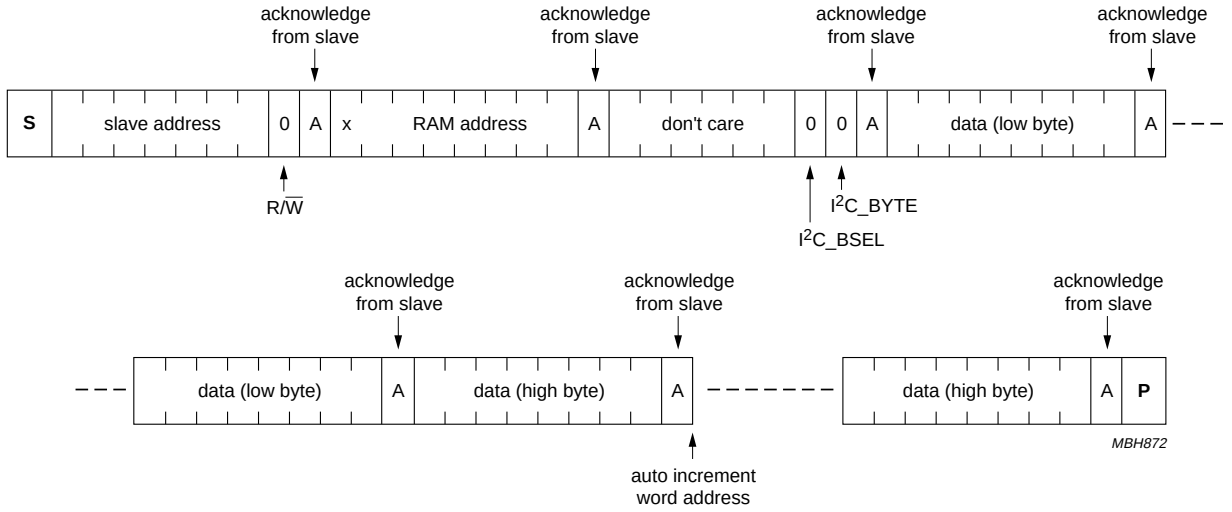


Fig.13 I^2C-bus write word.

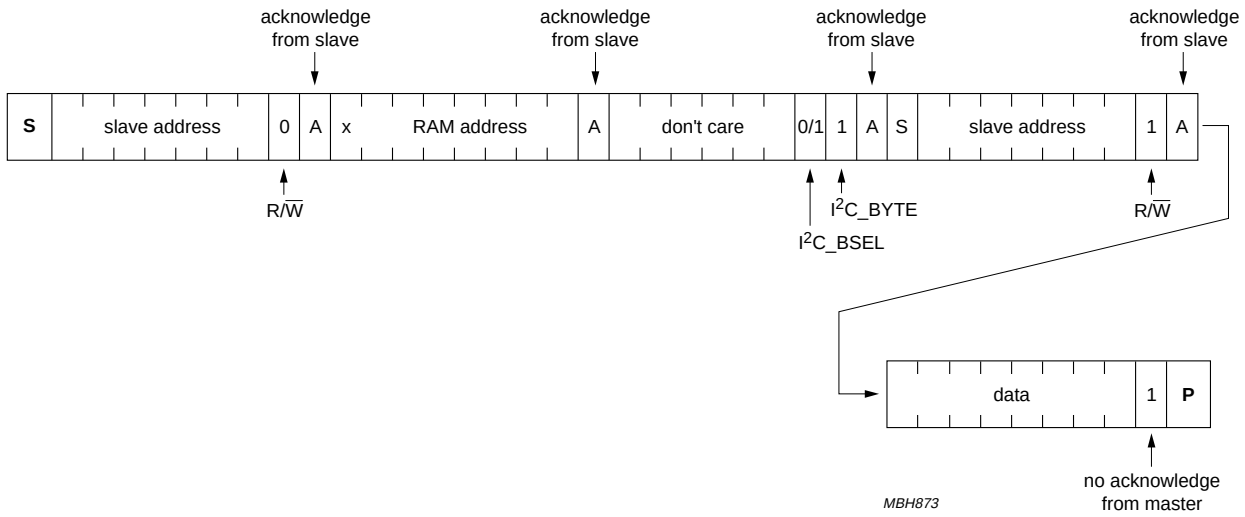


Fig.14 I^2C-bus read byte.

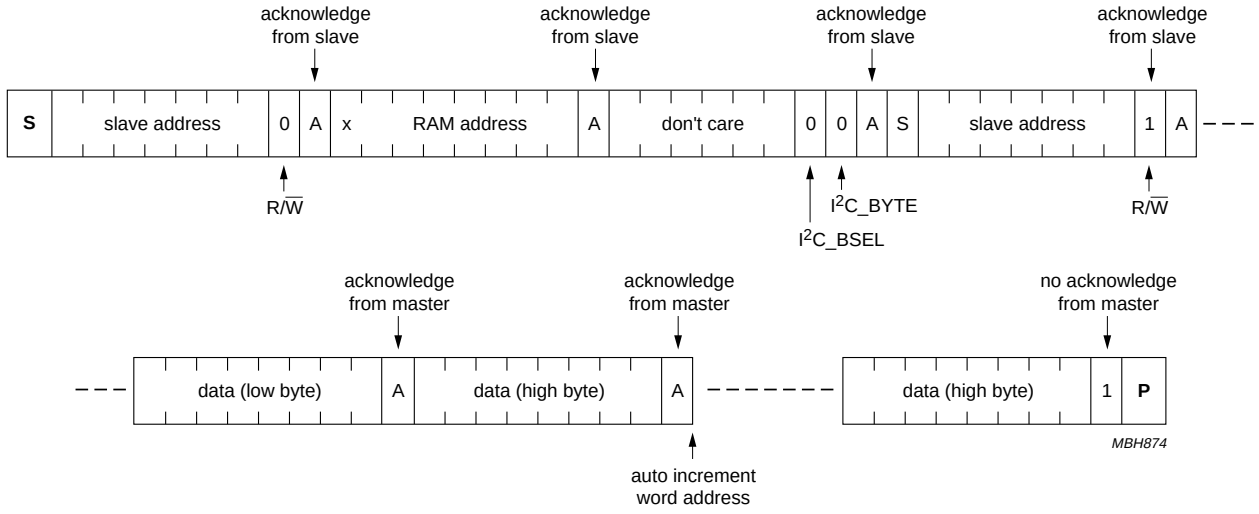


Fig.15 I^2C-bus read word.

11 CODEC TEST LOOPS

11.1 Test modes definition

For debug and evaluation purposes some test loops are implemented in the speech codecs. These test loops are activated by setting bits 13 to 8 in Control Register 0; see Table 32. The signal flow in the test loops is shown in Fig.16 and is described as follows:

- **Normal operation**: the codec is not in any of its test loop modes; used for a normal application.
- **1 bit analog**: this loop is intended for a separate evaluation of the analog parts of the codec. A bitstream interface ($108f_s$) is available. Via TEST_INPUT bitstream data is fed to the DAC and bitstream data from the ADC is present on TEST_OUTPUT.
- **1 bit digital**: this loop allows the evaluation of DDF and DNS at the $108f_s$ interface. Bitstream data from TEST_INPUT is led to DDF and bitstream data from DNS is available on TEST_OUTPUT.
- **1 bit closed loop**: a connection between the bitstream output of the ADC and the bitstream input of the DAC is made. The bitstream data is also made available on TEST_OUTPUT.
- **$4f_s$ codec**: the $4f_s$ codec loop gives access to the $4f_s$ interface for evaluation of DDF and DNS. 16-bit input data is serially shifted in (two's complement, MSB first) on TEST_INPUT and the 14 MSBs are used by DNS. On the other side 16 bits DDF output data is serially shifted out on TEST_OUTPUT.
- **$4f_s$ DSP**: this loop allows evaluation of the DSP software. On TEST_INPUT and TEST_OUTPUT, data can be exchanged with the DSP (16 bits serially, 2's complement, MSB first).
- **$4f_s$ closed loop**: a connection between the parallel output of DDF and the input of DNS is made. The loop data at $4f_s$ can be monitored by shifting out bits serially via TEST_OUTPUT.
- **PCM probe**: this special test loop allows the evaluation of DSP software. The DSP software however, must include a test mode in which any 16-bit data at a sample rate of f_s or 8 kHz (normally only present as numbers within the DSP algorithm) is written to the output line that is connected to DNS. While normally the data on this line has a $4f_s$ (32 kHz) sample rate, up to four (interleaved) PCM signals can be monitored via TEST_OUTPUT.

Next to these hardware codec test loops there also may be software DSP test loops, depending on the DSP software version. For more information about the DSP software the DSP manuals must be consulted.

In all codec test loop modes (except the normal operation mode) the signals lines TEST_INPUT_x and TEST_OUTPUT_x (x = 1 for Codec 1, x = 2 for Codec 2) are mapped onto pins that normally have a different function. Next to these data signals some timing signals (FS4 and CLK3) are presented on pins. Table 33 shows which pins are used in the codec test loop modes.

Table 32 Selection of functional test modes for Codec 1 and Codec 2

CDC1TM2	CDC1TM1	CDC1TM0	FUNCTIONAL TEST MODE
CDC2TM2	CDC2TM1	CDC2TM0	
0	0	0	normal operation
0	0	1	1 bit analog
0	1	0	1 bit digital
0	1	1	1 bit closed loop
1	0	0	$4f_s$ codec
1	0	1	$4f_s$ DSP
1	1	0	$4f_s$ closed loop
1	1	1	PCM probe

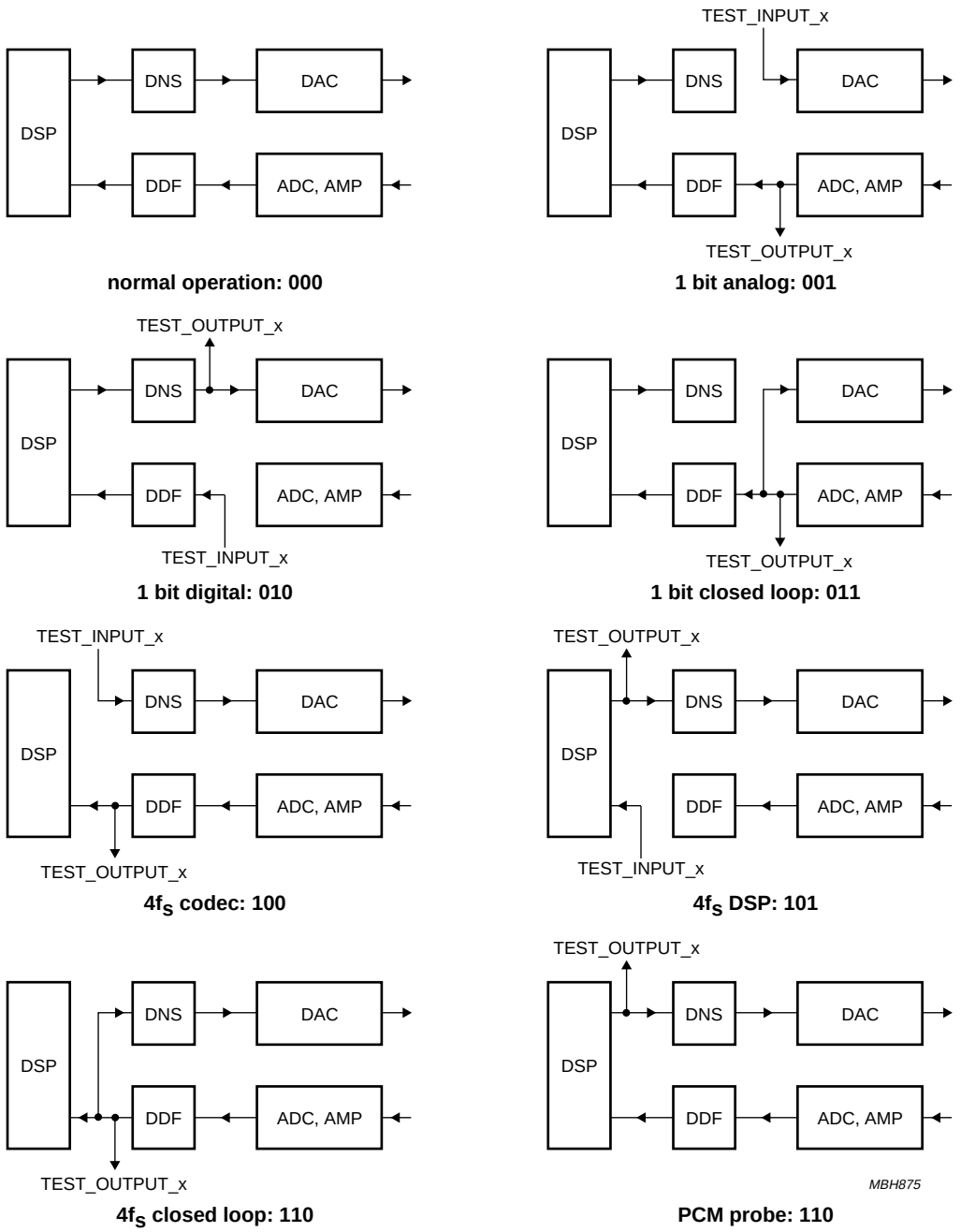


Fig.16 Speech codec test loops.

Table 33 Pin redefinition in Codec test loop mode

NORMAL MODE	CODEC TEST LOOP MODE		
PIN NAME	**SIGNAL NAME**	**I/O**	**DESCRIPTION**
DI	TEST_INPUT_1	I	$108f_s$ bitstream or $4f_s$ serial data input to Codec 1
DO	TEST_OUTPUT_1	O	$108f_s$ bitstream or $4f_s$ serial data output from Codec 1
A1	TEST_INPUT_2	I	$108f_s$ bitstream or $4f_s$ serial data input to Codec 2
IO1	TEST_OUTPUT_2	O	$108f_s$ bitstream or $4f_s$ serial data output from Codec 2
DCL	CLK3	O	3456 kHz bit clock signal ($4 \times 108f_s$) with 50% duty cycle
IO0	FS4	O	32 kHz word synchronization signal ($4f_s$), duty cycle = 12/108

11.2 Codec test loop signal timing

The TEST_OUTPUT_x signal changes at the falling edge of CLK3, and the signal presented on TEST_INPUT_x is sampled just before the falling edge of CLK3. Note that the $4f_s$ serial PCM data shifted in via TEST_INPUT_x is only used during the next FS4 HIGH period.

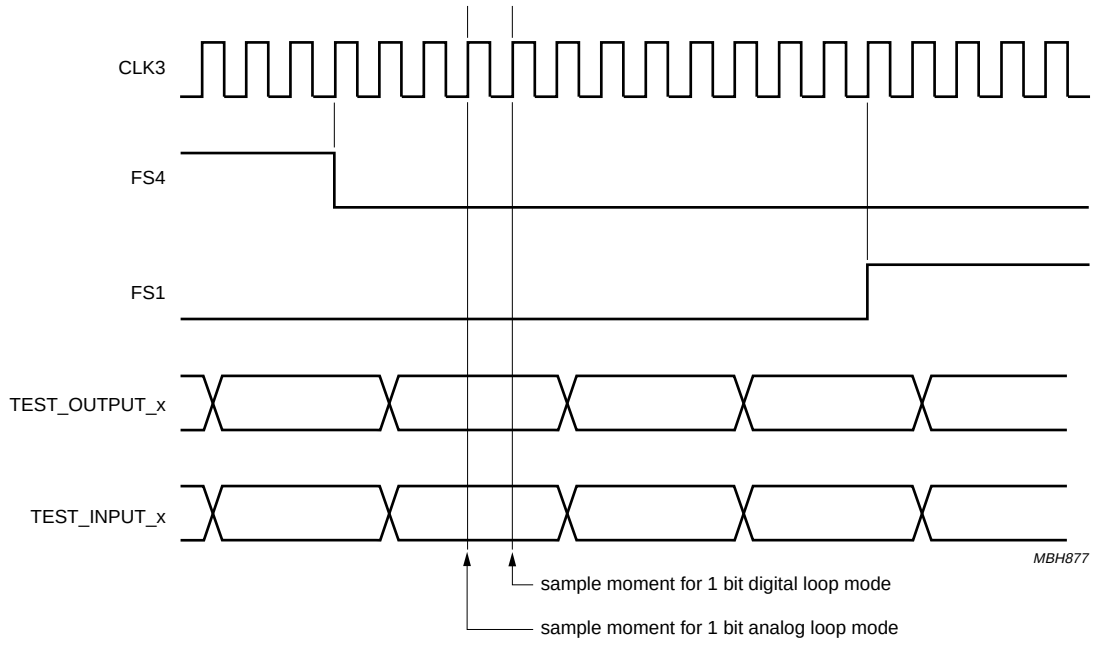


Fig.17 Codec test loop signal timing for $108f_s$ 1-bit bitstream signals.

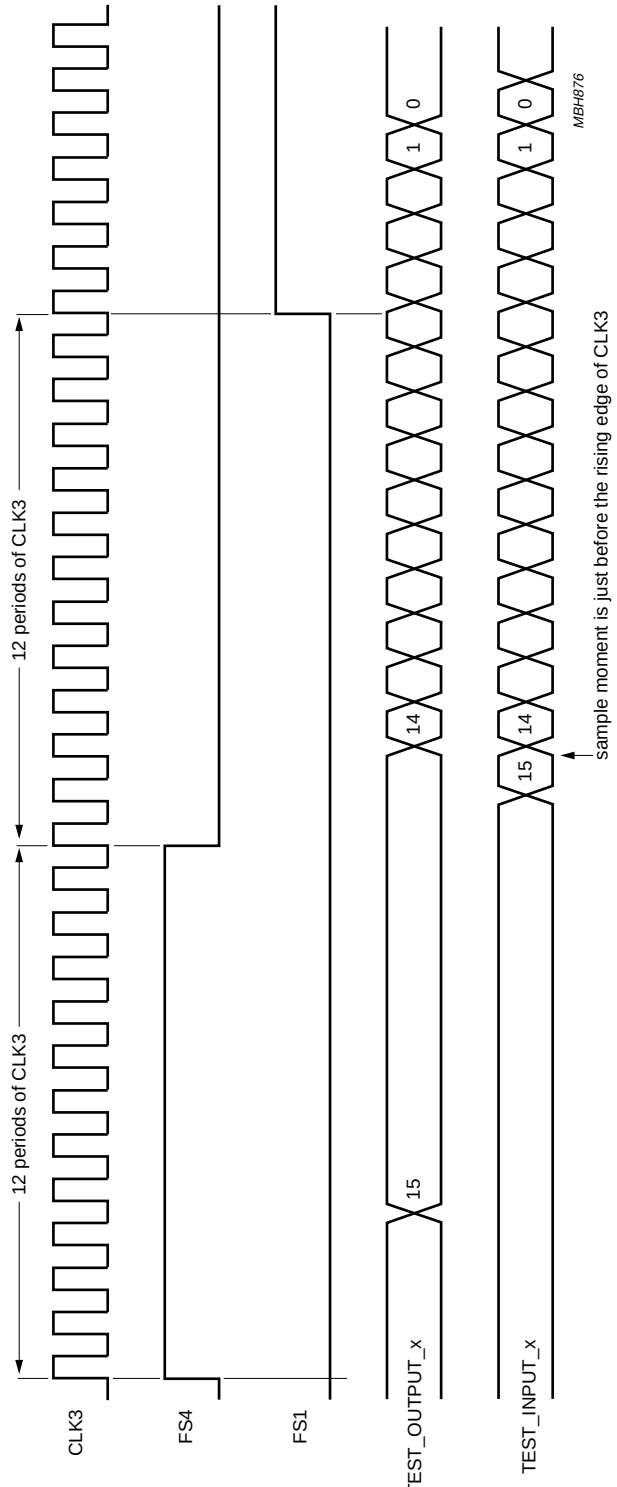


Fig.18 Codec test loop signal timing for $4f_s$ 16-bit serial signals.

12 APPLICATION INFORMATION

12.1 Small business systems

The PCD5096 is designed for business and residential phone systems. In combination with a processor like the PCD5093, two simultaneous calls on 2 PSTN lines (Ba, Bb) can be processed. To realize single line systems with hands-free functionality one analog interface port can be connected to a speaker phone and the other to the line interface. A typical small business system consists of a PCD5093 DECT processor with radio interface and a single universal codec (see Fig.19).

The possible configurations for speech connections in the universal codec are listed in Table 34.

A real hands-free solution can also be implemented by using one PSTN line port and connecting a corded handset, a hands-free microphone and a loudspeaker to the second analog interface port of the universal codec.

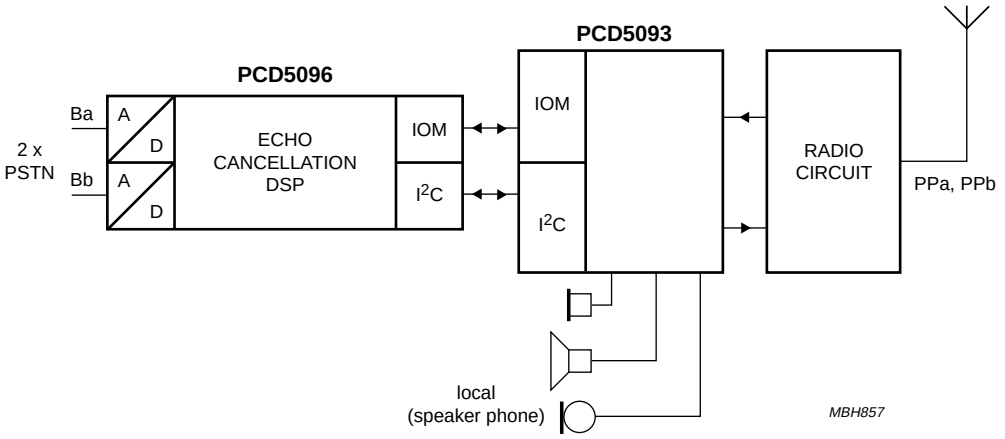


Fig.19 Small business system.

Table 34 Possible speech connections in a small business system

SINGLE CONNECTIONS	DUAL CONNECTIONS	
LOCAL ↔ Ba	(LOCAL ↔ Ba) + (Bb ↔ PPa)	(LOCAL ↔ Ba) + (Bb ↔ PPb)
LOCAL ↔ Bb	(LOCAL ↔ Bb) + (Ba ↔ PPa)	(LOCAL ↔ Bb) + (Ba ↔ PPb)
LOCAL ↔ PPa	(LOCAL ↔ PPa) + (Ba ↔ PPb)	(LOCAL ↔ PPa) + (Bb ↔ PPb)
LOCAL ↔ PPb	(LOCAL ↔ PPb) + (Ba ↔ PPa)	(LOCAL ↔ PPb) + (Bb ↔ PPa)
Ba ↔ PPa	(Ba ↔ PPa) + (Bb ↔ PPb)	–
Ba ↔ PPb	(Ba ↔ PPb) + (Bb ↔ PPa)	–
Bb ↔ PPa	–	–
Bb ↔ PPb	–	–

12.2 Large business systems

For large business systems, local loop and public access systems, several PCD5096 codecs can be connected together utilizing the serial bus system. A digital cordless base station for large business systems typically consists of a baseband processor, radio interface and a number of universal codecs interfacing to local lines, PSTN lines and to the local corded handset/hands-free interface. A diagram of this configuration is shown in Fig.20.

The universal codec can connect to different applications in a typical large business system. They are as follows:

1. PSTN Line Interface
2. Speaker phone with hands-free feature
3. Local Line Interface.

In these applications the additional processing required for conference calling is performed either in the host baseband processor, or in the universal codecs.

For further details about these three applications consult the *"PCD5096 DSP user manual"*.

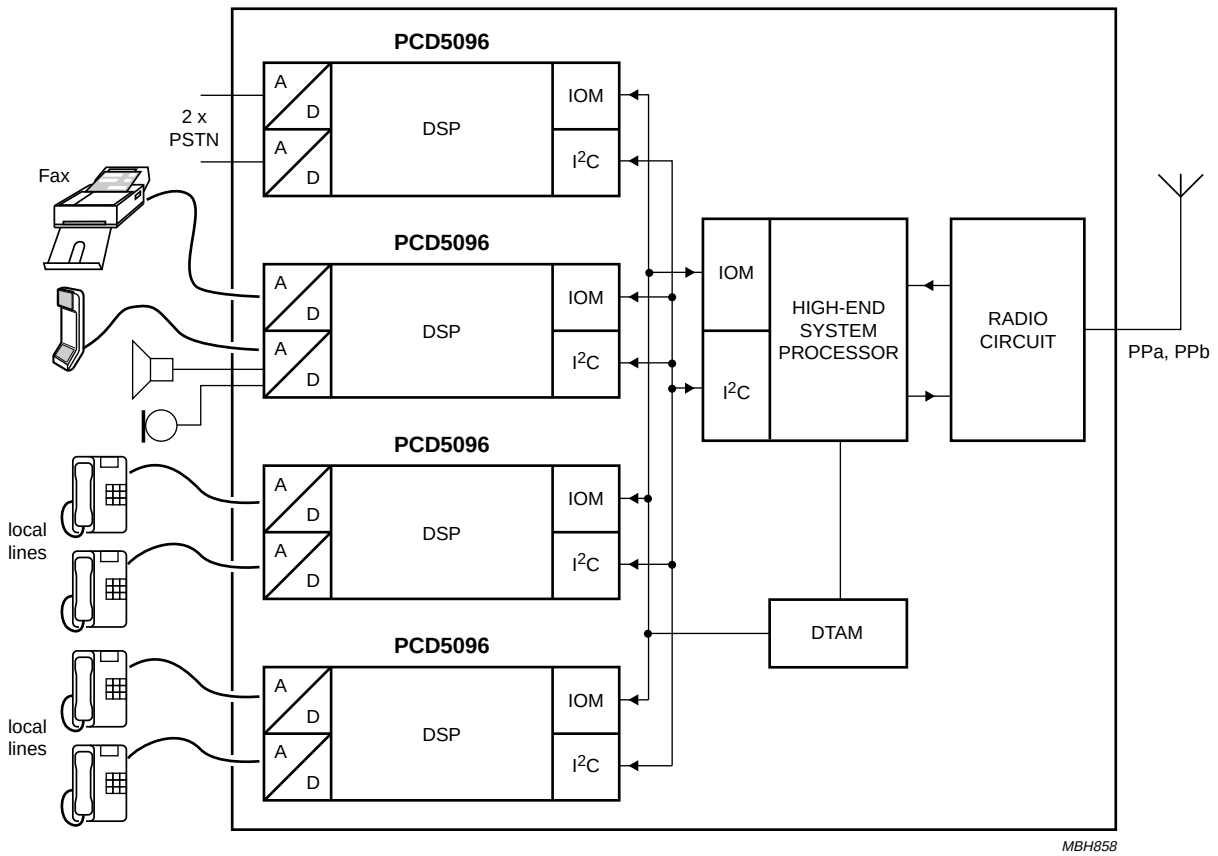


Fig.20 Large business system.

12.3 DECT and ISDN

The PCD5096 is perfectly suited to extend an ISDN-based DECT base station with analog extension lines. The IOM-2 interface communicates with the S0 interface chip. The host controller can connect via IOM-2 or I^2C-bus to the PCD5096. The two analog interfaces of the PCD5096 can either be used to connect to analog phones/Fax machines, or combine hands-free and one analog extension.

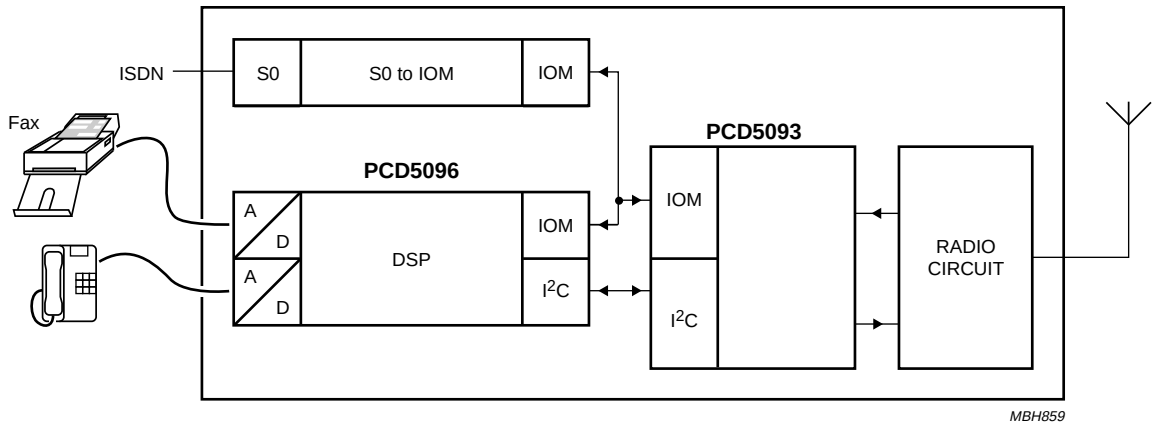


Fig.21 DECT and ISDN.

13 APPLICATION EXAMPLES

In this chapter some application examples are given to assist users with the programming of the PCD5096 (DSP parameter settings, control register settings and IOM-2 interface programming). Three examples are considered: a two channel application, a conference call application between one PSTN line and two IOM buffers, and a conference call application between two PSTN lines and one IOM buffer.

13.1 PCD5096 with two active channels

A typical application for the PCD5096 is depicted in Fig.22. Two handsets (PPa and PPb) are connected through a PCD5093 and a PCD5096 to two PSTN lines. Tables 35, 36 and 37 show possible settings for the DSP parameters, the IOM control table and the control registers in the PCD5096.

Note that the chosen values for the IOM pointers, the volume parameters and the frequency parameters depend on the application. This means that they can differ from the values that are given in this example.

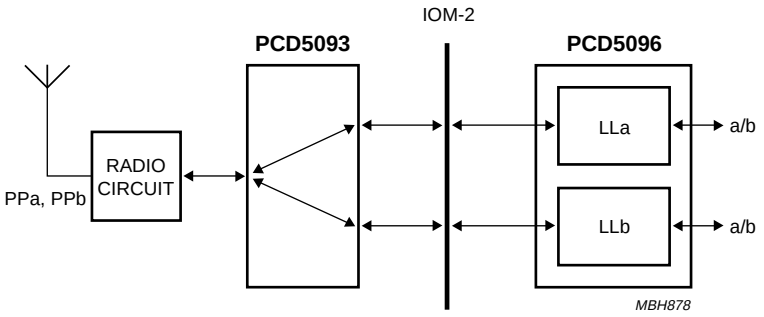


Fig.22 Typical PCD5096 application with two channels.

Table 35 DSP parameters for two active channels

SDR ADDRESS (HEX)	PARAMETER NAME		VALUE (HEX)	FUNCTION
00	LLa_IOM1	LLb_IOM1	484C	not used
01	LLa_LSW	LLb_LSW	FFFF	2 × analog line interface (LLx_IOM1 not used)
02	LLa_LEC	LLb_LEC	FFFF	2 × Local Echo Canceller ON
03	LLa_NES	LLb_NES	2D2D	2 × Network Echo Suppressor (9 dB attenuation)
04	LLa_AGC	LLb_AGC	FFFF	2 × Automatic Gain Control ON
05	LLa_TXV	LLb_TXV	2020	2 × Transmit Volume set to 0 dB
06	LLa_ISW	LLb_ISW	0000	2 × 8-bit A-law PCM data
07	LLa_IOM2	LLb_IOM2	4044	Codec 1 uses IOM buffer at address 40H
				Codec 2 uses IOM buffer at address 44H
08	LLa_SMU2	LLb_SMU2	0000	2 × Soft Mute OFF
09	LLa_AVR	LLb_AVR	0000	2 × Automatic Volume Control OFF
0A	LLa_RXV	LLb_RXV	2020	2 × Receive Volume set to 0 dB
0B	LLa_PST	LLb_PST	0000	2 × Site Tone OFF
0C	LLa_TST	LLb_TST	0000	2 × Tone Site Tone OFF (LLx_TOGx and LLx_TOVx not used)
0D	LLa_TOV1	LLb_TOV1	4040	2 × Tone Volume for Tone 1 set to 0 dB
0E	LLa_TOV2	LLb_TOV2	4040	2 × Tone Volume for Tone 2 set to 0 dB
0F	LLa_TOG1		7ECE	Tone 1 to Codec 1
10	LLa_TOG2		7E8A	Tone 2 to Codec 1
11	LLb_TOG1		7E37	Tone 1 to Codec 2
12	LLb_TOG2		7DD2	Tone 2 to Codec 2
13	CCa_CNC	reserved	0000	no conference call (CCa_IOMx not used)
14	CCa_IOM3	CCa_IOM4	5054	not used
15	CCa_SMU3	CCa_SMU4	0000	not used

Table 36 IOM control table for two active channels

SDR ADDRESS (HEX)	PARAMETER NAME	VALUE (HEX)	FUNCTION
20	slot 0 control	0070	IOM slot 0 uses buffer at address 40H
21	slot 1 control	0071	IOM slot 1 uses buffer at address 44H
22 to 3F	slot 2-slot 32	0000	slots 2 to 32 inactive

Table 37 Control registers for two active channels

SDR ADDRESS (HEX)	PARAMETER NAME	VALUE (HEX)	FUNCTION
78	codec control	005B	Codec 1 ON, Codec 2 ON
79	IOM control	0004	IOM slave mode, 768 kbits/s
7A	gain settings A/D and D/A paths	D0D0	A/D gain = +9 dB, D/A gain = 0 dB for both channels
7B	VREF1, VREF2 settings	A0A0	default setting for VREF1 and VREF2
7C	DSP modes	0048	both channels run in speech and tone mode

13.2 Conference call between one PSTN line and two IOM buffers

The PCD5096 is able to perform a 3 party conference call. Figure 23 shows a typical configuration, with two handsets in conference call with an PSTN line. Tables 38, 39 and 40 show possible settings for the DSP parameters, the IOM control table and the control registers in the PCD5096.

Note that the LLb block of the PCD5096 could be used in parallel to connect a second PSTN line to another IOM buffer. This is not covered in this example.

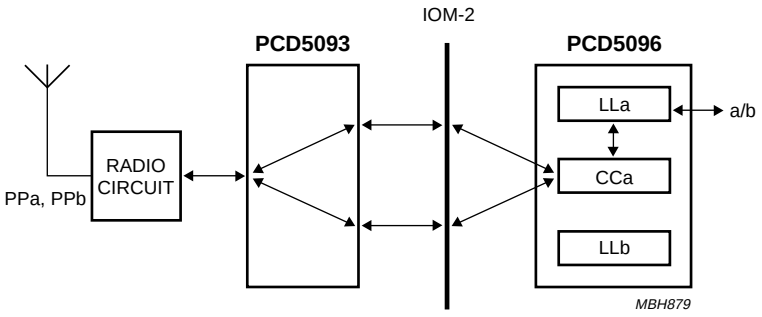


Fig.23 Conference call between one PSTN line and two IOM buffers.

Table 38 DSP parameters for conference call between one PSTN line and two IOM buffers

SDR ADDRESS (HEX)	PARAMETER NAME		VALUE (HEX)	FUNCTION
00	LLa_IOM1	LLb_IOM1	5054	not used
01	LLa_LSW	LLb_LSW	FF00	LLa analog line interface (LLx_IOM1 not used)
02	LLa_LEC	LLb_LEC	FF00	Local Echo Canceller ON in Codec 1
03	LLa_NES	LLb_NES	2D00	Network Echo Suppressor (9 dB attenuation) in Codec 1
04	LLa_AGC	LLb_AGC	FF00	Automatic Gain Control ON in Codec 1
05	LLa_TXV	LLb_TXV	2000	Transmit Volume set to 0 dB in Codec 1
06	LLa_ISW	LLb_ISW	0000	8-bit A-law PCM data
07	LLa_IOM2	LLb_IOM2	484C	not used
08	LLa_SMU2	LLb_SMU2	0000	Soft Mute OFF
09	LLa_AVR	LLb_AVR	0000	Automatic Volume Control OFF
0A	LLa_RXV	LLb_RXV	2000	Receive Volume set to 0 dB in Codec 1
0B	LLa_PST	LLb_PST	0000	Site Tone OFF
0C	LLa_TST	LLb_TST	0000	Tone Site Tone OFF (LLx_TOGx and LLx_TOVx not used)
0D	LLa_TOV1	LLb_TOV1	4040	Tone Volume for Tone 1 set to 0 dB
0E	LLa_TOV2	LLb_TOV2	4040	Tone Volume for Tone 2 set to 0 dB
0F	LLa_TOG1		7ECE	Tone 1 to Codec 1
10	LLa_TOG2		7E8A	Tone 2 to Codec 1
11	LLb_TOG1		7E37	Tone 1 to Codec 2
12	LLb_TOG2		7DD2	Tone 2 to Codec 2
13	CCa_CNC	reserved	0900	conference call between Codec 1 and Codec 2 IOM buffers (8 bit A-law PCM data)
14	CCa_IOM3	CCa_IOM4	4044	conference call IOM buffer 1 at address 40H
				conference call IOM buffer 2 at address 44H
15	CCa_SMU3	CCa_SMU4	0000	soft mute off

Table 39 IOM control table for conference call between one PSTN line and two IOM buffers

SDR ADDRESS (HEX)	PARAMETER NAME	VALUE (HEX)	FUNCTION
20	slot 0 control	0070	IOM slot 0 uses buffer at address 40H
21	slot 1 control	0071	IOM slot 1 uses buffer at address 44H
22 to 3F	slot 2 to slot 32	0000	slots 2 to 32 inactive

Table 40 Control registers for conference call between one PSTN line and two IOM buffers

SDR ADDRESS (HEX)	PARAMETER NAME	VALUE (HEX)	FUNCTION
78	codec control	0003	Codec 1 ON, Codec 2 OFF
79	IOM control	0004	IOM slave mode, 768 kbits/s
7A	gain settings A/D and D/A paths	00D0	A/D gain = +9 dB, D/A gain = 0 dB in Codec 1
7B	VREF1, VREF2 settings	A0A0	default setting for VREF1 and VREF2
7C	DSP modes	0008	channel a in speech and tone mode

13.3 Conference call between two PSTN lines and one IOM buffer

Another configuration for conference call is between two PSTN lines and one IOM buffer, as shown in Fig.24. Tables 41, 42 and 43 show possible settings for the DSP parameters, the IOM control table and the control registers in the PCD5096.

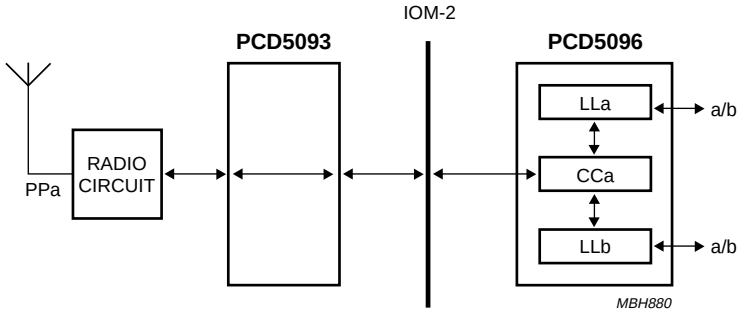


Fig.24 Conference call between two PSTN lines and one IOM buffer.

Table 41 DSP parameters for conference call between one IOM buffer and two PSTN lines

SDR ADDRESS (HEX)	PARAMETER NAME		VALUE (HEX)	FUNCTION
00	LLa_IOM1	LLb_IOM1	5054	not used
01	LLa_LSW	LLb_LSW	FFFF	2 × analog line interface (LLx_IOM1 not used)
02	LLa_LEC	LLb_LEC	FFFF	2 × Local Echo Canceller ON
03	LLa_NES	LLb_NES	2D2D	2 × Network Echo Suppressor (9 dB attenuation)
04	LLa_AGC	LLb_AGC	FFFF	2 × Automatic Gain Control ON
05	LLa_TXV	LLb_TXV	2020	2 × Transmit Volume set to 0 dB
06	LLa_ISW	LLb_ISW	0000	2 × 8-bit A-law PCM data
07	LLa_IOM2	LLb_IOM2	484C	not used
08	LLa_SMU2	LLb_SMU2	0000	2 × Soft Mute OFF
09	LLa_AVR	LLb_AVR	0000	2 × Automatic Volume Control OFF
0A	LLa_RXV	LLb_RXV	2020	2 × Receive Volume set to 0 dB
0B	LLa_PST	LLb_PST	0000	2 × Site Tone OFF
0C	LLa_TST	LLb_TST	0000	2 × Tone Site Tone OFF (LLx_TOGx and LLx_TOVx not used)
0D	LLa_TOV1	LLb_TOV1	4040	2 × Tone Volume for Tone 1 set to 0 dB
0E	LLa_TOV2	LLb_TOV2	4040	2 × Tone Volume for Tone 2 set to 0 dB
0F	LLa_TOG1		7ECE	Tone 1 to Codec 1
10	LLa_TOG2		7E8A	Tone 2 to Codec 1
11	LLb_TOG1		7E37	Tone 1 to Codec 2
12	LLb_TOG2		7DD2	Tone 2 to Codec 2
13	CCa_CNC	reserved	0100	conference call between Codec 1, Codec 2 and one IOM buffer (8 bit A-law PCM data)
14	CCa_IOM3	CCa_IOM4	4044	conference call with IOM buffer at address 40H CCa_IOM4 not used
15	CCa_SMU3	CCa_SMU4	0000	soft mute off

Table 42 IOM control table for conference call between one IOM buffer and two PSTN lines

SDR ADDRESS (HEX)	PARAMETER NAME	VALUE (HEX)	FUNCTION
20	slot 0 control	0070	IOM slot 0 uses buffer at address 40H
21 to 3F	slot 1 to slot 32	0000	slots 1 to 32 inactive

Table 43 Control registers for conference call between one IOM buffer and two PSTN lines

SDR ADDRESS (HEX)	PARAMETER NAME	VALUE (HEX)	FUNCTION
78	codec control	00FB	Codec 1 ON, Codec 2 ON with hands-free
79	IOM control	0004	IOM slave mode, 768 kbits/s
7A	gain settings A/D and D/A paths	D0D0	A/D gain = +9 dB, D/A gain = 0 dB for both channels
7B	VREF1, VREF2 settings	A0A0	default setting for VREF1 and VREF2
7C	DSP modes	0048	both channels run in speech and tone mode

14 LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD_1}	supply voltage V_{DD_1} with respect to V_{SS_1}	–0.5	+6.0	V
V_{DD_2}	supply voltage V_{DD_2} with respect to V_{SS_2}	–0.5	+5.0	V
V_{DDA_1}	analog supply voltage V_{DDA_1} with respect to V_{SSA_1}	–0.5	+5.0	V
V_{DDA_2}	analog supply voltage V_{DDA_2} with respect to V_{SSA_2}	–0.5	+5.0	V
V_{DD_PLL}	supply voltage V_{DD_PLL} with respect to V_{SS_PLL}	–0.5	+5.0	V
I_{DC}	DC current through pins			
	supply pins	–	150	mA
	other pins	–	10	mA
P_{tot}	total power dissipation	–	500	mW
T_{amb}	operating ambient temperature	–25	+70	°C
T_{stg}	storage temperature	–65	+150	°C

15 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. ESD protection according to Human Body Model is guaranteed up to 2 kV. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

16 ELECTRICAL SPECIFICATIONS

Table 44 General parameters

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{clk}	clock frequency		–	6.912	–	MHz
T_{amb}	ambient temperature		–25	+25	+70	°C
V_{DD_1}	supply voltage	note 1	2.7	3.3	5.5	V
$I_{DD\_1(act)}$	active supply current	note 2	–	–	–	mA
$I_{DD\_1(off)}$	power off supply current	note 3	–	0.1	–	µA
V_{DD_2}	supply voltage	note 4	2.7	3.3	3.6	V
$I_{DD\_2(act)}$	active supply current	note 5	–	18	28	mA
$I_{DD\_2(off)}$	power off supply current	note 3	–	4	–	µA
V_{DDA_1}	analog supply voltage	note 4	2.7	3.3	3.6	V
$I_{DDA\_1(act)}$	active analog supply current	no load; notes 5 and 6	–	1.5	3	mA
$I_{DDA\_1(off)}$	power off supply current	note 3	–	33	–	µA
V_{DDA_2}	analog supply voltage	note 4	2.7	3.3	3.6	V
$I_{DDA\_2(act)}$	active analog supply current	no load; notes 5 and 6	–	1.5	3	mA
$I_{DDA\_2(off)}$	power off supply current	note 3	–	2	–	µA
V_{DD_PLL}	supply voltage	note 4	2.7	3.3	3.6	V
$I_{DD\_PLL(act)}$	active supply current	note 5	–	0.1	1	mA
$I_{DD\_PLL(off)}$	power off supply current	note 3	–	1	–	µA
$I_{DD(tot)(off)}$	total power off supply current	note 3	–	40	70	µA

Notes

1. V_{DD_1} supplies all digital I/Os to ensure 5 V interfacing. V_{DD_1} may vary over its range independent of the value of V_{DD_2}, V_{DDA_1}, V_{DDA_2} and V_{DD_PLL}. If V_{DD_1} is 5.5 V, V_{DD_2} cannot be lower than 3.0 V.
2. $I_{DD\_1(act)}$ is application dependent.
3. Power off at 25 °C and 3.3 V, RESET pin HIGH, clock not running. The pins IO0 and IO1 are then inputs and must be kept HIGH (internal pull-ups).
4. V_{DD_2}, V_{DDA_1}, V_{DDA_2} and V_{DD_PLL} will have the same value. Internally they are NOT connected.
5. Active mode at 25 °C and 3.3 V, clock running. DSP parameter table, IOM control table and control registers set according to Section 13.1 (application example with two active channels). A sine wave signal (1031.25 Hz) at a level of –25 dBm is applied to the microphone input of both codecs. DI is tied to DO to simulate activity on the IOM-2 interface.
6. No load on LIFM_DA1, LIFP_DA1, EARM_HS, EARP_HS, VBGP, VREF1, VREF2, VMIC_HS and VMIC_HF.

Table 45 Digital I/Os

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{LI}	leakage current input pins		–	–	1	μA
V_{IH}	HIGH-level input voltage		$0.7V_{DD\_1}$	–	–	V
V_{IL}	LOW-level input voltage		–	–	$0.3V_{DD\_1}$	V
V_{OH}	HIGH-level output voltage	note 1	$0.8V_{DD\_1}$	–	–	V
V_{OL}	LOW-level output voltage	notes 2 and 4	–	–	0.4	V
R_{pd}	equivalent pull-down resistor	note 3	–	50	–	kΩ
R_{pu}	equivalent pull-up resistor	note 3	–	100	–	kΩ
$t_{o(f)}$	SDA output fall time	notes 4 and 5	–	–	250	ns

Notes

1. I_{OH} = –8 mA for pins EARM_HF and EARP_HF. I_{OH} = –2 mA for pins IO0 and IO1.
2. I_{OL} = 8 mA for pins EARM_HF, EARP_HF and DO. I_{OL} = 2 mA for pins IO0 and IO1.
3. Pull-down resistor present at pin TEST. Pull-up resistor present at pins IO0 and IO1.
4. For SDA pin, I_{OL} = 3 mA at 5 V, 1 mA at 3.3 V and 0.7 mA at 2.7 V.
5. Output fall time of SDA measured from $V_{IH(min)}$ to $V_{IL(max)}$.

Table 46 Analog supplies

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{bgp}	bandgap voltage	note 1	1	1.2	1.5	V
V_{ref}	reference voltage	notes 2 and 3	1.975	2.000	2.025	V
R_{vmic}	microphone supply output resistance	note 4	–	75	150	Ω

Notes

1. VBGP output current is zero. Decoupling capacitance between pins VBGP and V_{SSA_1} is 100 nF at 25 °C. The bandgap has a temperature coefficient between –0.2 and +0.2 mV/°C.
2. V_{ref} stands for VREF1 or VREF2. V_{ref} output current is zero. Decoupling capacitance between VREF1 and V_{SSA_1}, or between VREF2 and V_{SSA_2} is between 1 μF and 100 μF, with a 100 nF capacitance in parallel. The voltage is programmed by setting the appropriate value (80H to BFH) for each codec, in Control Register 3. VMIC_HS and VMIC_HF output current is zero (e.g. by setting bits 6 and 7 in Control Register 3 to a logic 0. The output can only source current (i.e. not sink).
3. Pins VMIC_HS and VMIC_HF (called VMIC below) are internally connected to VREF2 via two switches. The VMIC_HS switch is closed by setting the HSMICON bit in Control Register 0 to a logic 1. The VMIC_HF switch is closed by setting the HFMICON bit in Control Register 0 to a logic 1. The VMIC DC output current is 400 μA maximum, and VREF2 must be programmed to its typical value. Use a low pass filter (resistor + capacitor) between VMIC and V_{SSA_2} of 100 Ω + 10 μF, with a 100 nF capacitance in parallel. VMIC adjustment can only be done by adjusting VREF2.
4. Valid for both VMIC_HS and VMIC_HF pins.

Table 47 Speech codec

V_{ref1} and V_{ref2} are tuned to 2.0 V. Typical values for the A/D and D/A filter characteristics conform to the G.712 specification.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{i(MIC1)}$	MIC input level (Codec 1)	note 1	–	–	–22	dBm
$V_{i(MIC\_HS)}$	handset MIC input level (Codec 2)	note 1	–	–	–22	dBm
$V_{i(MIC\_HF)}$	hands-free MIC input level (Codec 2)	note 1	–	–	–22	dBm
$R_{i(MIC1)(dm)}$	MIC input resistance differential mode seen across MICP1 and MICM1		–	200	–	kΩ
$R_{i(MIC\_HS)(dm)}$	handset MIC input resistance differential mode seen across MICP_HS and MICM_HS		–	200	–	kΩ
$R_{i(MIC\_HF)(dm)}$	hands-free MIC input resistance differential mode seen across MICP_HF and MICM_HF		–	200	–	kΩ
$R_{i(MIC1)(cm)}$	MIC input resistance common mode seen between MICP1 (or MICM1) and V_{SSA_1}		–	500	–	kΩ
$R_{i(MIC\_HS)(cm)}$	handset MIC input resistance common mode seen between MICP_HS (or MICM_HS) and V_{SSA_2}		–	500	–	kΩ
$R_{i(MIC\text{-}HF)(cm)}$	hands-free MIC input resistance common mode seen between MICP_HF (or MICM_HF) and V_{SSA_2}		–	500	–	kΩ
$V_{i(LIF\_AD1)}$	LIF input level (Codec 1)	note 2	–	–	–6	dBm
$V_{i(LIF\_AD2)}$	LIF input level (Codec 2)	note 2	–	–	–6	dBm
$R_{i(LIF\_AD1)(dm)}$	LIF input resistance differential mode seen across LIFP_AD1 and LIFM_AD1		–	30	–	kΩ
$R_{i(LIF\_AD2)(dm)}$	LIF input resistance differential mode seen across LIFP_AD2 and LIFM_AD2		–	30	–	kΩ
$R_{i(LIF\_AD1)(cm)}$	LIF input resistance common mode seen between LIFP_AD1 (or LIFM_AD1) and V_{SSA_1}		–	15	–	kΩ
$R_{i(LIF\_AD2)(cm)}$	input resistance common mode seen between LIFP_AD2 (or LIFM_AD2) and V_{SSA_2}		–	15	–	kΩ

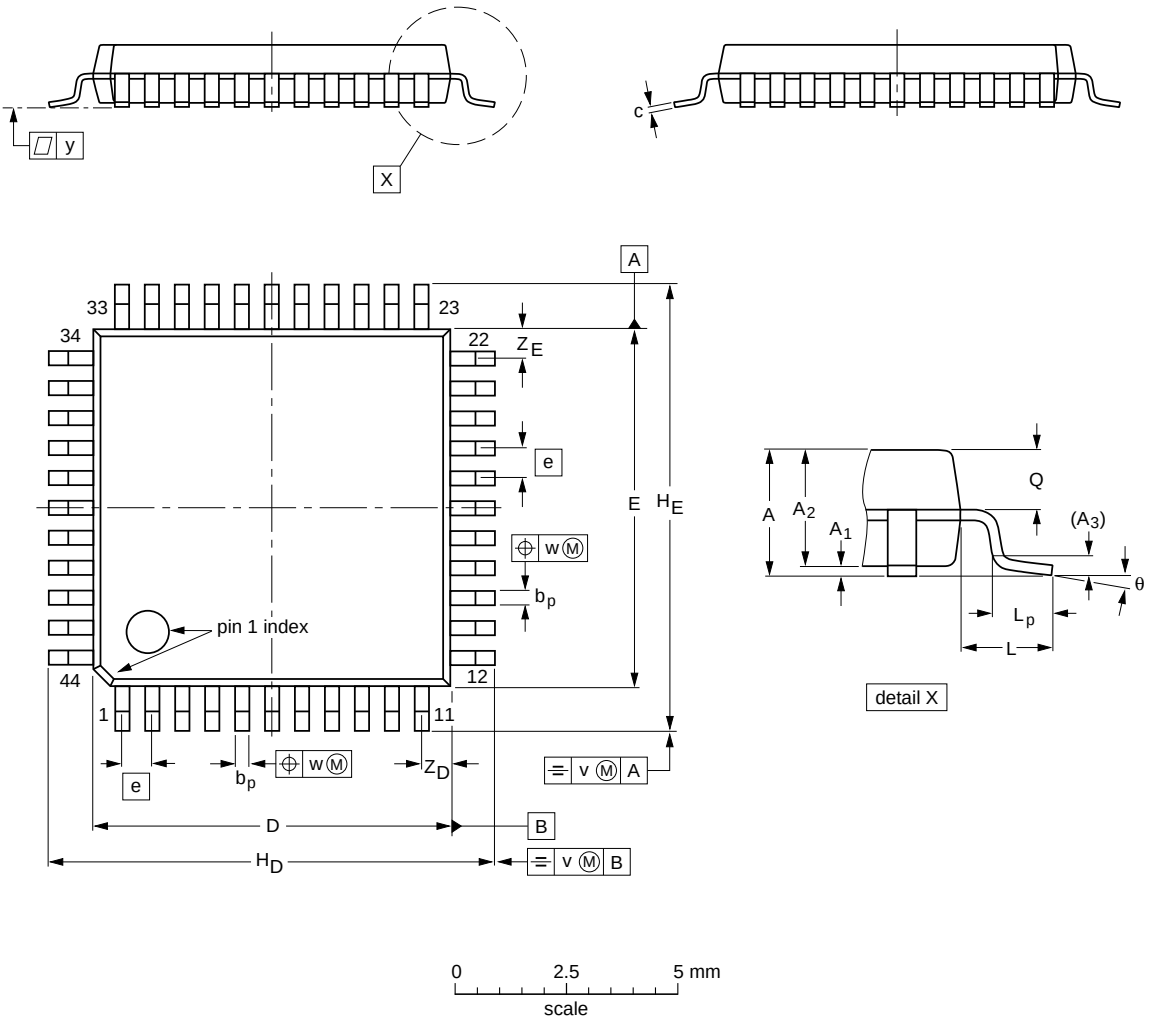
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$F_{(A/D)(idle)}$	A/D idle channel noise	note 3	–	–85	–72	dBm0p
$S/(N + THD)_{(A/D)(65)}$	A/D signal-to-noise plus total harmonic distortion ratio (–65 dBm input level)	note 4	32	40	–	dBp
$S/(N + THD)_{(A/D)(25)}$	A/D signal-to-noise plus total harmonic distortion ratio (–25 dBm input level)	note 4	40	60	–	dBp
$t_{d(g)(A/D)}$	A/D path group delay		–	500	–	µs
$G_{(MIC1)}$	Codec 1 MIC gain from MICP1 - MICM1 to LIFP_AD1 - LIFM_AD1		12	15	18	dB
$G_{(MIC\_HS)}$	Codec 2 handset MIC gain from MICP_HS - MICM_HS to LIFP_AD2 - LIFM_AD2		12	15	18	dB
$G_{(MIC\_HF)}$	Codec 2 hands-free MIC gain from MICP_HF - MICM_HF to LIFP_AD2 - LIFM_AD2		12	15	18	dB
$G_{(A/D)}$	gain A/D path from LIF to PCM	note 5	$G_{AD} – 1.5$	G_{AD}	$G_{AD} + 1.5$	dB
$G_{step(A/D)}$	gain difference between adjacent steps (A/D path)	note 6	+0.1	+1.0	+1.9	dB
$G_{(D/A)}$	gain D/A path from PCM to LIF	note 7	$G_{DA} – 1$	G_{DA}	$G_{DA} + 1$	dB
$G_{step(D/A)}$	gain difference between adjacent steps (D/A path)	note 6	+0.5	+1.0	+1.5	dB
$V_{o(D/A)}$	D/A path output level	note 8	–	1350	–	mV
$R_{o(D/A\_1)}$	D/A path output resistance seen between LIFP_DA1 and LIFM_DA1		–	10	20	Ω
$R_{o(D/A\_2)}$	D/A path output resistance seen between EARP_HS and EARM_HS		–	10	20	Ω
$F_{(D/A)(idle)}$	D/A idle channel noise	note 9	–	–85	–72	dBmp
$S/(N + THD)_{(D/A)(40)}$	D/A signal-to-noise plus total harmonic distortion ratio (–40 dBm0 input level)	note 10	32	40	–	dBp
$S/(N + THD)_{(D/A)(0)}$	D/A signal-to-noise plus total harmonic distortion ratio (0 dBm0 input level)	notes 10 and 11	40	70	–	dBp
$t_{d(g)(D/A)}$	D/A-path group delay		–	500	–	µs

Notes

1. A sine wave rms level applied differentially between the microphone pins. The A/D path gain in Control Register 2 is set to +9 dB. For larger input levels the output signal will saturate.
2. A sine wave rms level applied differentially between pins LIFP_ADn and LIFM_ADn (n = 1 for Codec 1; n = 2 for Codec 2). The A/D path gain is set to +9 dB using Control Register 2. For larger input levels the output signal will saturate.
3. Valid for Codec 1 and Codec 2. Control Register 0 = 0003H (Codec 1) or 0018H (Codec 2) and the A/D path gain in Control Register 2 is set to +9 dB. The microphone pins are shorted together. The value is psophometrically weighted.
4. Valid for Codec 1 and Codec 2. Control Register 0 = 0003H (Codec 1) or 0018H (Codec 2) and the A/D path gain in Control Register 2 is set to +9 dB. A sine wave of 1030 Hz is applied between the microphone input pins. The value is psophometrically weighted and includes harmonic distortion.
5. Valid for Codec 1 and Codec 2. G_{AD} is the A/D gain value selected in Control Register 2. The gain is measured at 1030 Hz from the LIF interface (pins LIFP_ADn and LIFM_ADn, where n = 1 for Codec 1 and n = 2 for Codec 2) to the PCM interface.
6. The difference between two adjacent gain settings as specified in Control Register 2. Valid for Codec 1 and Codec 2.
7. Valid for Codec 1 and Codec 2. G_{DA} is the D/A gain value selected in Control Register 2. The gain is measured at 970 Hz, from the PCM interface to the LIF interface (pins LIFP_DA1 and LIFM_DA1, for Codec 1 and pins EARP_HS and EARM_HS for Codec 2).
8. Valid for Codec 1 and Codec 2. Sine wave rms level differentially seen between pins LIFP_DA1 and LIFM_DA1 (Codec 1) or EARP_HS and EARM_HS (Codec 2), with an input signal of 970 Hz and a level of +3.14 dBm0 at the PCM interface. Load resistance is larger than 120 Ω. The D/A path gain in Control Register 2 is set to +2 dB.
9. Valid for Codec 1 and Codec 2. Control Register 0 = 0003H (Codec 1) or 0018H (Codec 2). The D/A path gain in Control Register 2 is set to 0 dB and the DSP is set to idle mode. The value is psophometrically weighted.
10. Valid for Codec 1 and Codec 2. Control Register 0 = 0003H (Codec 1) or 0018H (Codec 2).The D/A path gain in Control Register 2 is set to 0 dB. A sine wave of 970 Hz is applied. The value is psophometrically weighted and includes harmonic distortion.
11. The D/A path is loaded with (150 Ω + 800 μF)//100 pF.

17 PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm **SOT307-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.85 0.75	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						~~92-11-17~~ 95-02-04

18 SOLDERING

18.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

18.2 Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

18.3 Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

18.4 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

19 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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