

MEMORY

5V-ONLY FLASH MEMORY CARD

MB98A81063-15/MB98A81183-15/MB98A81273-15/
MB98A81373-15/MB98A81473-15/MB98A81573-15

1M/2M/4M/8M/16M/32M-BYTE 5V-ONLY FLASH ERASABLE AND PROGRAMMABLE MEMORY CARD

■ DESCRIPTION

The Fujitsu 5V-Only Flash memory cards are electrically erasable and programmable memory cards capable of storing and retrieving large amounts of data. The memory circuits are housed in a credit-card sized 68-pin package. Internal circuit is protected by two metal panels, one at the top and the other at the bottom of the card, that help to reduce chip damage from electrostatic discharge.

A unique feature of the Fujitsu memory cards allows the user to organize the card into either an 8-bit or a 16-bit bus configuration. All cards are portable and operate on low power at high speed.

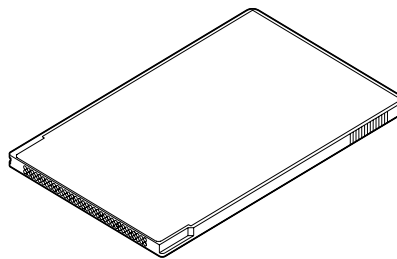
In accordance with the Personal Computer Memory Card International Association (PCMCIA) and Japan Electrical Industry Development Association (JEIDA) industry standard specifications, Flash memory cards offer additional EEPROM memory that is used to store attribute data. The attribute memory is a Flash memory card option. (See page 3 for description of the three available options.)

■ PRODUCT LINE & FEATURES

- Meet PCMCIA and JEIDA industry standards for 68-pin memory card
Type I : 85.6 mm × 54.0 mm × 3.3 mm
- +5 V \pm 5% power supply program and erase
- Command control for Automated Program / Automated Erase operation
- Erase Suspend Read / Program Capability (Only Erase Suspend Read is possible for MB98A81063)
- 128 KB Sector Erase (at $\times 16$ mode)
- Any Combination of Sectors Erase and Full Chip Erase
- Detection of completion of program/erase operation with $\overline{\text{Data}}$ Polling or Toggle bit.
- Ready/Busy Output with R/B (Except for MB98A81063)
- Reset Function with RESET pin (Except for MB98A81063)
- Write protect function with WP switch
- Low V_{cc} Write Inhibit

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■ PACKAGE



CRD-68P-M17

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■ DESCRIPTIONS

DESCRIPTION TABLE

| Part Number | Common Memory | | | Attribute Memory | | |
|-------------|---------------------------|---------------------------|----------------|-----------------------|---------------------------|----------------|
| | Memory Device | Organization (W × bit) | Access Time | Memory Device | Organization (W × bit) | Access Time |
| MB98A81063 | 4M bit Flash Memory × 2 | 1M × 8/512K × 16 | 150 ns max. | 16K bit EEPROM × 1 | 2K × 8 | 250 ns max. |
| MB98A81183 | 8M bit Flash Memory × 2 | 2M × 8/1M × 16 | | | | |
| MB98A81273 | 16M bit Flash Memory × 2 | 4M × 8/2M × 16 | | | | |
| MB98A81373 | 16M bit Flash Memory × 4 | 8M × 8/4M × 16 | | | | |
| MB98A81473 | 16M bit Flash Memory × 8 | 16M × 8/8M × 16 | | | | |
| MB98A81573 | 16M bit Flash Memory × 16 | 32M × 8/16M × 16 | | | | |

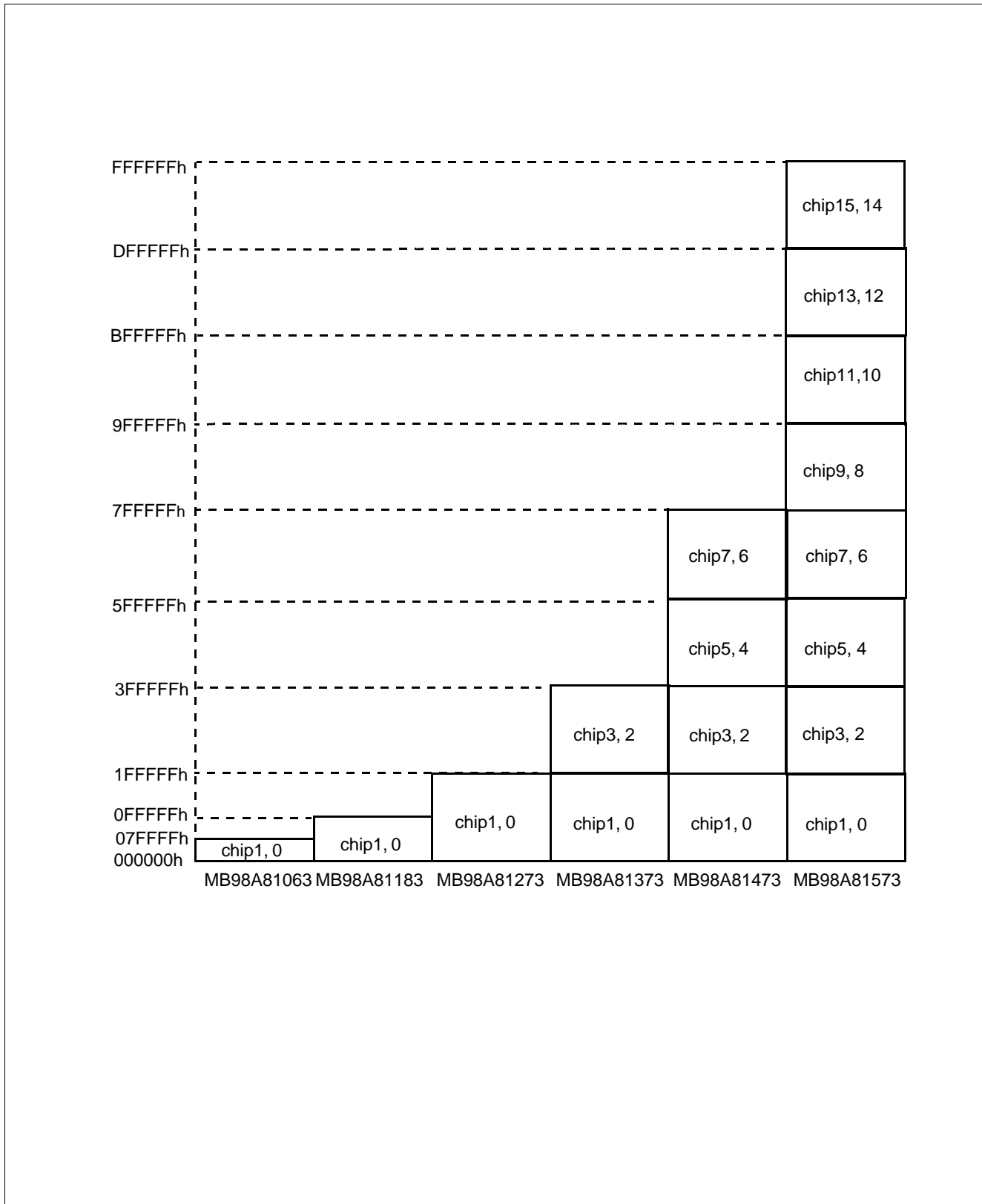
DIFFERENCES

| | MB98A81063 | MB98A81183 | MB98A81273 | MB98A81373 | MB98A81473 | MB98A81573 |
|-----------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|
| Density | 1MB | 2MB | 4MB | 8MB | 16MB | 32MB |
| Memory Device | 4M bit | 8M bit | 16M bit | ← | ← | ← |
| Quantity | 2 | 2 | 2 | 4 | 8 | 16 |
| Read | 1 B unit | ← | ← | ← | ← | ← |
| Program | 1 B unit | ← | ← | ← | ← | ← |
| Chip Erase | 512 KB unit | 1 MB unit | 2 MB unit | ← | ← | ← |
| Sector Erase | 64 KB unit | ← | ← | ← | ← | ← |
| Number of Sectors | 16 | 32 | 64 | 128 | 256 | 512 |
| Erase Suspend Read | Yes | Yes | Yes | Yes | Yes | Yes |
| Erase Suspend Program | No | Yes | Yes | Yes | Yes | Yes |
| Address | A ₀ to A ₁₉ | A ₀ to A ₂₀ | A ₀ to A ₂₁ | A ₀ to A ₂₂ | A ₀ to A ₂₃ | A ₀ to A ₂₄ |
| RESET | No | Yes | Yes | Yes | Yes | Yes |
| R/Ī | No | Yes | Yes | Yes | Yes | Yes |

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■ DESCRIPTIONS (Continued)

ADDRESS MAP (for × 16 mode, not contained A₀)



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■ PIN ASSIGNMENTS

| Pin No. | Symbol | Pin No. | Symbol | Pin No. | Symbol | Pin No. | Symbol |
|---------|------------------|---------|-----------------|---------|------------------------|---------|------------------------|
| 1 | GND | 18 | N.C. | 35 | GND | 52 | N.C. |
| 2 | D ₃ | 19 | A ₁₆ | 36 | $\overline{CD1}$ | 53 | A ₂₂ /N.C.* |
| 3 | D ₄ | 20 | A ₁₅ | 37 | D ₁₁ | 54 | A ₂₃ /N.C.* |
| 4 | D ₅ | 21 | A ₁₂ | 38 | D ₁₂ | 55 | A ₂₄ /N.C.* |
| 5 | D ₆ | 22 | A ₇ | 39 | D ₁₃ | 56 | N.C. |
| 6 | D ₇ | 23 | A ₆ | 40 | D ₁₄ | 57 | N.C. |
| 7 | $\overline{CE1}$ | 24 | A ₅ | 41 | D ₁₅ | 58 | RESET/N.C. |
| 8 | A ₁₀ | 25 | A ₄ | 42 | $\overline{CE2}$ | 59 | N.C. |
| 9 | \overline{OE} | 26 | A ₃ | 43 | N.C. | 60 | N.C. |
| 10 | A ₁₁ | 27 | A ₂ | 44 | N.C. | 61 | REG |
| 11 | A ₉ | 28 | A ₁ | 45 | N.C. | 62 | BVD2 |
| 12 | A ₈ | 29 | A ₀ | 46 | A ₁₇ | 63 | BVD1 |
| 13 | A ₁₃ | 30 | D ₀ | 47 | A ₁₈ | 64 | D ₈ |
| 14 | A ₁₄ | 31 | D ₁ | 48 | A ₁₉ | 65 | D ₉ |
| 15 | \overline{WE} | 32 | D ₂ | 49 | A ₂₀ /N.C.* | 66 | D ₁₀ |
| 16 | R/B/N.C.* | 33 | WP | 50 | A ₂₁ /N.C.* | 67 | $\overline{CD2}$ |
| 17 | V _{CC} | 34 | GND | 51 | V _{CC} | 68 | GND |

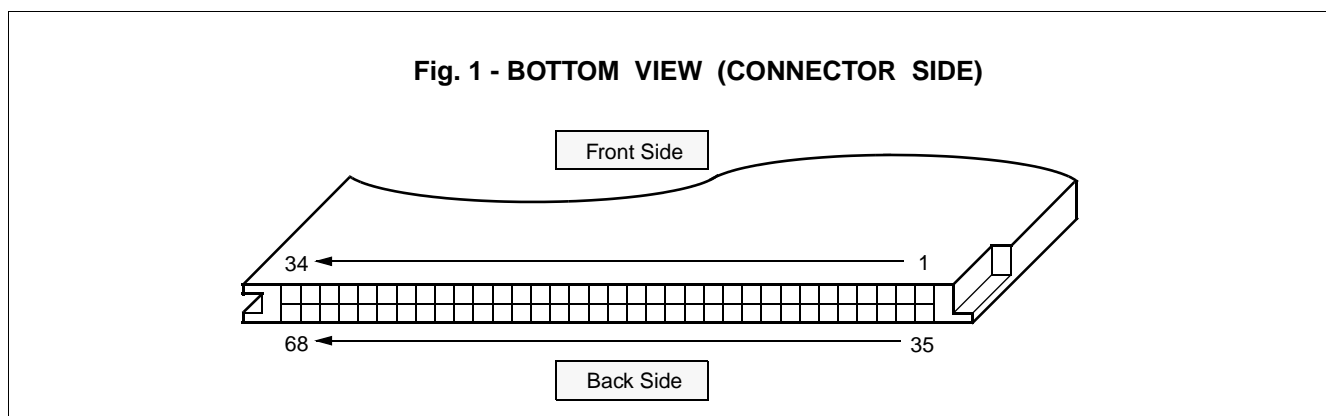
* : See "DESCRIPTIONS".

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■ PIN DESCRIPTIONS

| Symbol | Pin Name | Input/Output | Function |
|-------------------------------------|----------------------------|--------------|---|
| A ₀ to A ₂₄ | Address Input | Input | Address Inputs, A ₀ to A ₂₄ . |
| D ₀ to D ₁₅ | Data Input/Output | Input/Output | Data Inputs/Outputs. This data bus size (8-bit or 16-bit) is selected with CE1 and CE2. |
| $\overline{CE1}$ | Card Enable for Lower Byte | Input | Active Low. -Lower byte (D ₀ to D ₇) is selected for read/write/erase function of flash memory cards. |
| $\overline{CE2}$ | Card Enable for Upper Byte | Input | Active Low. -Upper byte (D ₈ to D ₁₅) is selected for read/write / erase function of flash memory cards. |
| \overline{REG} | Attribute Memory Select | Input | Active Low. -Attribute memory is selected for read/write function of identification data of flash memory cards. (N.C. or "FF" data or attribute data.) |
| \overline{OE} | Output Enable | Input | Active Low. -Output enable for flash memory cards. |
| \overline{WE} | Write Enable | Input | Active Low. -Write enable for flash memory cards. |
| $\overline{CD1}$, $\overline{CD2}$ | Card Detect | Output | These pins detect if the card has been correctly inserted. Both pins are tied to GND internally. |
| WP | Write Protect | Output | Write controller for flash memory cards. This pin outputs the Protect/Non Protect status of "WP Switch". |
| BVD1, BVD2 | Battery Voltage Detect | Output | Both pins are tied to V _{CC} internally. |
| RESET | Hardware Reset | Input | The card may be reset by driving the RESET pin to V _{IH} . |
| R/ \overline{B} | Ready/Busy | Output | System can be detect the completion of program or erase operation. |
| V _{CC} | Power Supply | — | Power Supply Voltage. (+5.0 V \pm 5%) |
| GND | Ground | — | System Ground. |
| N.C. | Non Connection | — | |

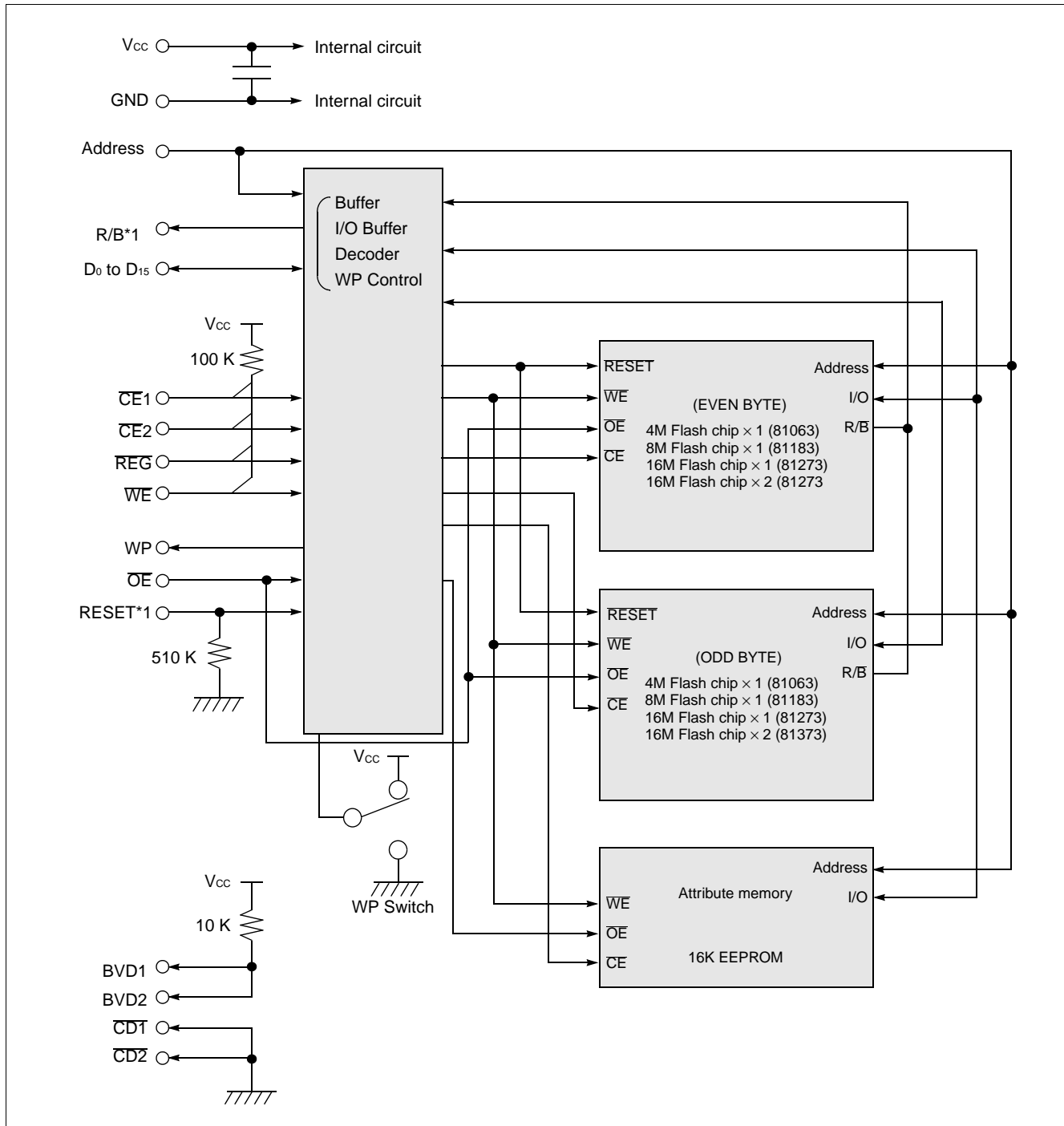
■ PIN LOCATIONS



MB98A81063-15/81183-15/81273-15/81373-15/81473-15/81573-15

■ BLOCK DIAGRAM

MB98A81063, MB98A81183, MB98A81273 and MB98A81373



*1: Not available for MB98A81063.

Fig. 2.1 - Block Diagram

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■ BLOCK DIAGRAM (Continued)

MB98A81473 and MB98A81573

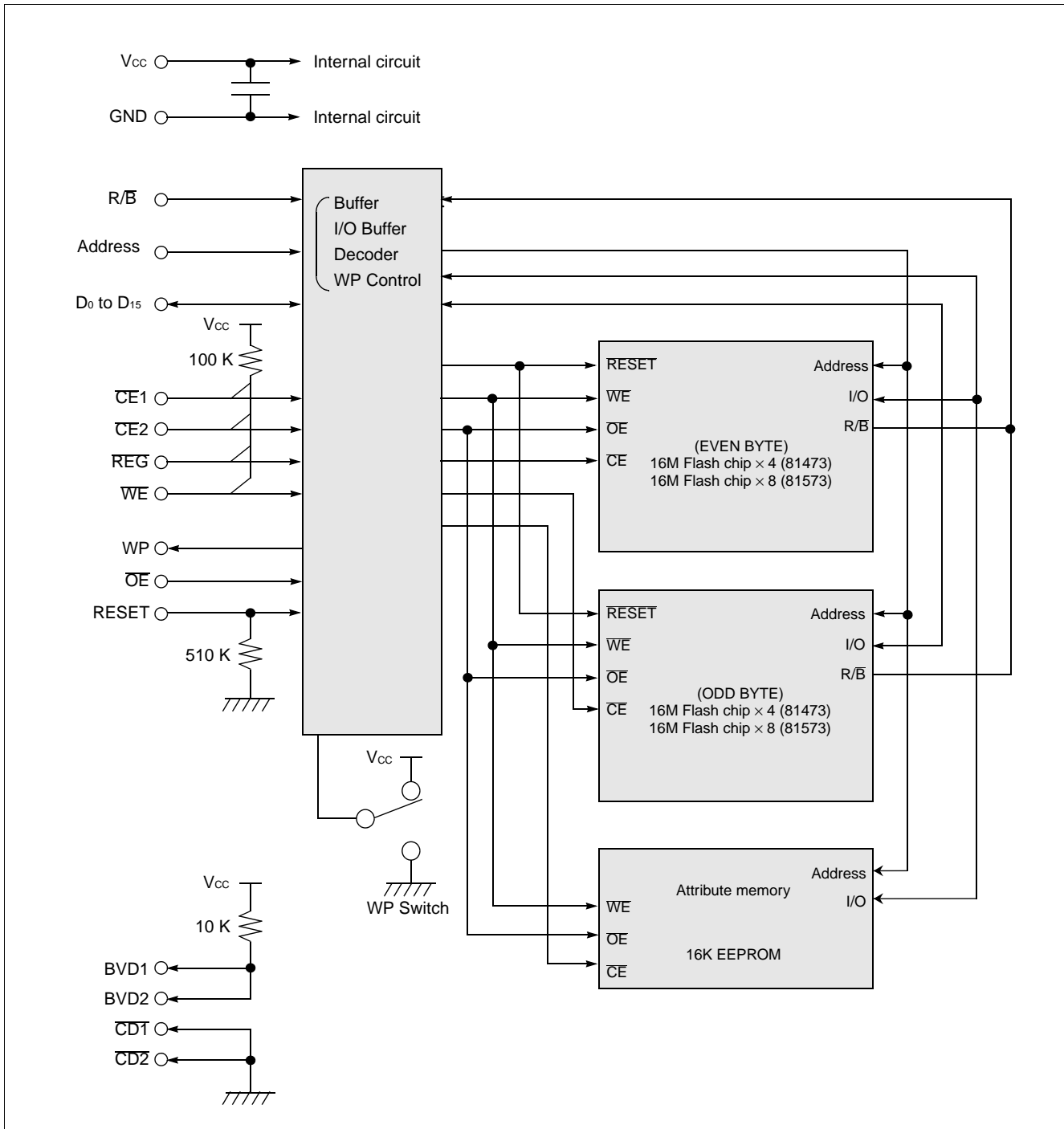


Fig. 2.2 - Block Diagram

MB98A81063-15/81183-15/81273-15/81373-15/81473-15/81573-15

■ CHIP AND SECTOR DECODING

- Chip can be selected with;
 - A₀, A₂₂, A₂₃ and A₂₄ for × 8-bit mode No.1.
 - A₂₂, A₂₃ and A₂₄ for × 8-bit mode No.2 and × 16-bit mode.
- Sector per each chip can be selected with A₁₇, A₁₈, A₁₉, A₂₀ and A₂₁.

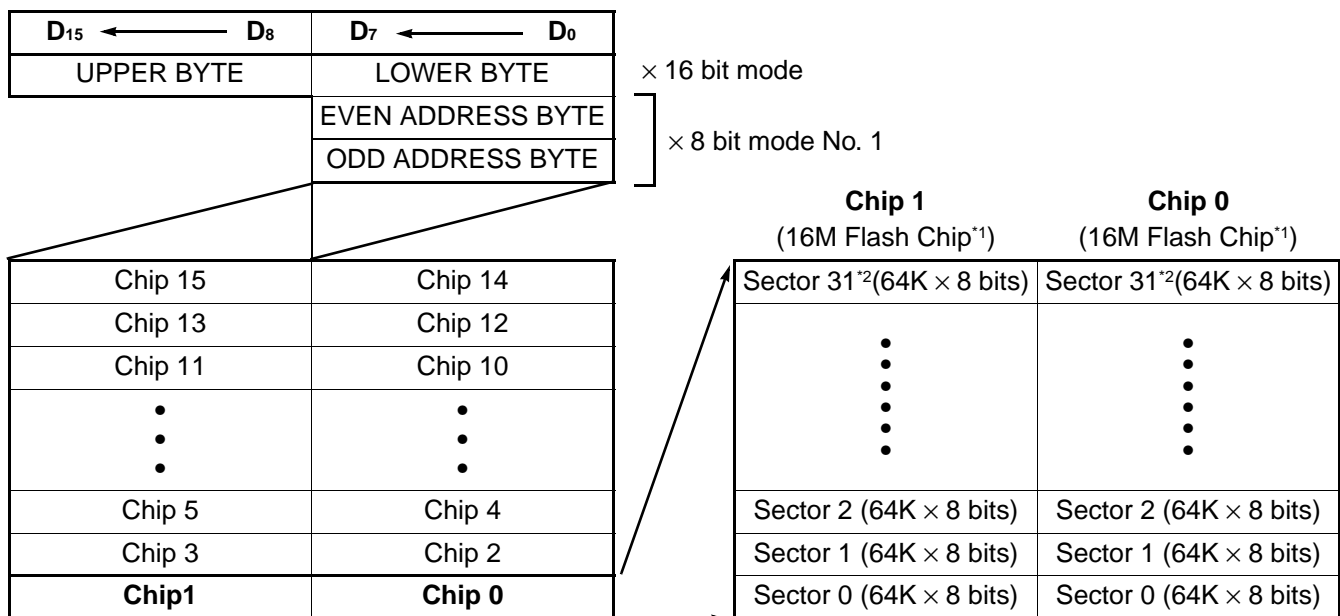
ERASE SECTOR DECODING TABLE

| | Sector Address (SA) | | | | |
|---------------------------------|---------------------|--------------------|-----------------|-----------------|-----------------|
| | A ₂₁ *2 | A ₂₀ *1 | A ₁₉ | A ₁₈ | A ₁₇ |
| Sector 31 | 1 | 1 | 1 | 1 | 1 |
| Sector 30 | 1 | 1 | 1 | 1 | 0 |
| Sector 29 | 1 | 1 | 1 | 0 | 1 |
| • | • | • | • | • | • |
| • | • | • | • | • | • |
| • | • | • | • | • | • |
| • | • | • | • | • | • |
| • | • | • | • | • | • |
| • | • | • | • | • | • |
| Total 32 sectors*1*2 per 1 chip | | | | | |
| Sector 2 | 0 | 0 | 0 | 1 | 0 |
| Sector 1 | 0 | 0 | 0 | 0 | 1 |
| Sector 0 | 0 | 0 | 0 | 0 | 0 |

*1: A₂₀ is not available for MB98A81063. MB98A81063 has 8 sectors.

*2: A₂₁ is not available for MB98A81063 and MB98A81183. MB98A81063 has 8 sectors and MB98A81183 has 16 sectors.

CARD CHIP / SECTOR CONFIGURATION



Card Chip Configuration for 32MB Card

Sector Configuration for 2 Chips

*1: 4M Flash Chip for MB98A81063. 8M Flash chip for MB98A81183.

*2: Sector 7 for MB98A81063. Sector 15 for MB98A81183.

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■ FUNCTION DESCRIPTIONS

1. Read Mode

The data in the common and attribute memory can be read with " $\overline{OE}=V_{IL}$ " and " $\overline{WE}=V_{IH}$ ". The address is selected with A_0 to A_{24} . And $\overline{CE1}$ and $\overline{CE2}$ select output mode ($\times 8/\times 16$ output mode, See "FUNCTION TRUTH TABLES"). The following 1) and 2) are the descriptions for Common Memory Read and Attribute Memory Read mode.

- (1) Common Memory Read
 - Two modes of Common Memory Read, reading the data in memory array and Intelligent ID are available. The card enter each Read mode by writing "Read Memory/Reset Command" or "Intelligent ID Read Command". The card automatically resets to the condition of Common Memory Read mode upon initial power-up.
- (2) Attribute Memory Read
 - The data on the attribute memory can be read with " $\overline{REG}=V_{IL}$ ", " $\overline{OE}=V_{IL}$ " and " $\overline{WE}=V_{IH}$ ".
 - An address on attribute memory can be selected with A_0 to A_{11} pin. And $\overline{CE1}$ and $\overline{CE2}$ select output mode.

2. Standby Mode

- $\overline{CE1}$ and $\overline{CE2}$ at " V_{IH} " place the card in Standby mode. D_0 to D_{15} are placed in a high-Z state independent of the status " \overline{OE} ", " \overline{WE} " and " \overline{REG} ".

3. Output Disable Mode

- The outputs are disabled with \overline{OE} and \overline{WE} at " V_{IH} ". D_0 to D_{15} are placed in high-Z state.

4. Write Mode

- (1) Common Memory Write
 - The card is in Write mode with " $\overline{OE}=V_{IH}$ " and " \overline{WE} and $\overline{CE}=V_{IL}$ ".
 - Commands can be written at the Write mode. See "5.Command Definitions".
 - Two types of the Write mode, " \overline{WE} control" and " \overline{CE} control" are available.
- (2) Attribute Memory Write
 - \overline{REG} at L-level selects Attribute memory and " $\overline{OE}=V_{IH}$ ", " \overline{WE} and $\overline{CE}=V_{IL}$ " place it in write mode. Two types of the write mode, " \overline{WE} control" and " \overline{CE} control" are available.
 - Attribute memory is not controlled by writing Commands. And attribute memory has the \overline{Data} polling function, which can detect whether the attribute memory status is in programming operation. When the read operation is executed at programming cycle, the opposite data is output from D_7 ($\overline{17}$), and the same data (O_7) as the written data is output from D_7 pin at the completion of programming operation.

5. Command Definitions

- User can select the card operation by writing the specific address and data sequences into the command register. If incollect address and data are written or improper sequence is done, the card is reseted to read mode. See "COMMAND DEFINISION TABLE".

6. Automated Program Capability

- Programming operation can switch the data from "1" to "0".
- The data is programmed on a byte-by-byte or word-by-word basis.
- The card will automatically provide adequate internally generated programming pulses and verify the programmed cell margine by writing four bus cycle operation. The card returns to Common Memory Read mode automatically after the programming is completed.
- Addresses are latched at falling edge of \overline{WE} or \overline{CE} and data is latched at rising edge of \overline{WE} or \overline{CE} . The fourth rising edge of \overline{WE} or \overline{CE} on the command write cycle begins programming operation.
- We can check whether a byte (word) programming operation is completed successfully by sequence flug with R/\overline{B} (Except for MB98A81063), \overline{Data} Polling or Toggle Bit function. See "WRITE OPERATION STATUS".
- Any commands written to the chip during programming operation will be ignored.

7. Automated Chip Erase Capability

- We can execute chip erase operation by 6 bus cycle operation. Chip erase does not require the user to pre-program prior to erase. Upon executing the Erase command sequence the chip automatically will program and verify the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timing during these operations.
- The card returns to Common Memory Read mode automatically after the chip erasing is completed.

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■ FUNCTION DESCRIPTIONS (Continued)

- Whether or not chip erase operation is completed successfully can be checked by sequence flug with R/ \overline{B} (Except for MB98A81063), \overline{Data} Polling or Toggle Bit function. See "WRITE OPERATION STATUS".
- Any commands written to the chip during programming operation will be ignored.

8. Automated Sector Erase Capability

- We can execute the erase operation on any sectors by 6 bus cycle operation.
- A time-out of 50 μ s (typ.) from the rising edge of the last Sector Erase command will initiate the Sector Erase command(s) for other sector than the sector that sector erase command have been valid.
- Multiple sectors in a chip can be erased concurrently. This sequence is followed with writes of 30H to addresses in other sectors desired to be concurrently erased. The time between writes 30H must be less than 50 μ s, otherwise that command will not be accepted. Any command other than Sector Erase or Erase Suspend during this time-out period will reset the chip to Read mode. The automated sector erase begins after the 50 μ s (typ.) time out from the rising edge of \overline{WE} pulse for the last Sector Erase command pulse. Whether the sector erase window is still open can be monitored with D_3 and D_{11} .
- Sector Erase does not require the user to pre-program prior to erase. The chip automatically programs "0" to all memory locations in the sector(s) prior to electrical erase. The system is not required to provide any controls or timing during these operations.
- The card returns to Common Memory Read mode automatically after the sector erasing is completed.
- Whether or not sector erase operation is completed successfully can be checked by sequence flug with R/ \overline{B} , \overline{Data} Polling or Toggle Bit function. The sequence flug must be read from the address of the sector involved in erase operation. See "WRITE OPERATION STATUS".

9. Erase Suspend

- Erase Suspend command allows the user to interrupt the sector erase operation and then do data reads or program from or to a non-busy sector in the chip which has the sector(s) suspended erase (only data read is possible for MB98A81063). This command is applicable only during the sector erase operation (including the sector erase time-out period after the sector erase commands 30H) and will be ignored if written during the chip erase or programming operation. Writing this command during the time-out will result in immediate termination of the time-out period. The addresses are "don't cares" in writing the Erase Suspend or Resume commands in the chip.
- When the Erase Suspend command is written during a Sector Erase operation, the chip will enter the Erase Suspend Read mode. User can read the data from other sectors than those in suspension. The read operation from sectors in suspension results D_2/D_{10} toggling for MB98A81183 and MB98A8xx7x. User can program to non-busy sectors by writing program commands for MB98A81183 and MB98A8xx7x.
- A read from a sector being erase suspended may result in invalid data.

10. Intelligent Identifier (ID) Read Mode

- Each common memory can execute an Intelligent Identifier operation, initiated by writing Intelligent ID command (90H). Following the command write, a read cycle from address 00H retrieves the manufacture code, and a read cycle from address 01H returns the device code as follows. To terminate the operation, it is necessary to write Read/Reset command.

| Part Number | Maker Code | Device Code |
|-----------------------------|---------------|---------------|
| MB98A81063 | 04 h / 0404 h | A4 h / A4A4 h |
| MB98A81183 | 04 h / 0404 h | D5 h / D5D5 h |
| MB98A81273/81373/1473/81573 | 04 h / 0404 h | 3D h / 3D3D h |

11. Hardware Reset (not applied for MB98A81063)

- The Card may be reset by driving the RESET pin to V_{IH} . The RESET pin must be kept High (V_{IH}) for at least 500 ns. Any operation in progress will be terminated and the card will be reset to the read mode 20 μ s after the RESET pin is driven High. If a hardware reset occurs during a program operation, the data at that particular location will be indeterminate.
- When the RESET pin is high and the internal reset is complete, the Card goes to standby mode and cannot be accessed. Also, note that all the data output pins are High-Z for the duration of the RESET pulse. Once the RESET pin is taken low, the Card requires 500 ns of wake up time until outputs are valid for read access.
- If hardware reset occurs during a erase operation, there is a possibility that the erasing sector(s) cannot be used after this.

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■ FUNCTION DESCRIPTIONS (Continued)

12. Data Protection

- The card has WP (Write Protect) switch for write lockout.
- To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 3.2 V (typically 3.7 V). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition the device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO} . It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above 3.2 V.
- If V_{CC} would be less than V_{LKO} during program/erase operation, the operation will stop. And after that, the operation will not resume even if V_{CC} returns recommended voltage level. Therefore, program command must be written again because the data on the address interrupted program operation is invalid. And regarding interrupting erase operation, there is possibility that the erasing sector(s) cannot be used.
- Noise pulses of less than 5 ns (typical) on \overline{OE} , \overline{CE} or \overline{WE} will not initiate a write cycle.

■ FUNCTION TRUTH TABLE

MAIN MEMORY FUNCTION*1

| Mode | RESET*3 | REG | CE2 | CE1 | A ₀ | OE | WE | WP*2 | Data Input/Output | | WP SW | | | | | | | | |
|-----------------|---------|-----|-----|-----|--------------------------------|----|----|------|-----------------------------------|----------------------------------|---------|--------------------------------|-------------------------------|--------|---|--------|-------------------------------|-----------------|--------|
| | | | | | | | | | D ₈ to D ₁₅ | D ₀ to D ₇ | | | | | | | | | |
| Hardware Reset | H | X | X | X | X | X | X | X | High-Z | | P or NP | | | | | | | | |
| Standby | | X | H | H | X | X | X | X | High-Z | | | | | | | | | | |
| Read (×8 No.1) | | H | H | L | L | L | H | X | High-Z | D _{OUT} (Even Byte) | | | | | | | | | |
| Read (×8 No.1) | | | | H | D _{OUT} (Odd Byte) | | | | | | | | | | | | | | |
| Read (×8 No.2) | | | L | H | X | H | L | X | High-Z | D _{OUT} (Odd Byte) | | High-Z | | | | | | | |
| Read (×16) | | | | | L | | | | | D _{OUT} | | | | | | | | | |
| Write (×8 No.1) | | | H | H | L | L | H | L | L | High-Z | | D _{IN} (Even Byte) | NP | | | | | | |
| Output Disable | | | | | | | | | | | | L | High-Z | P | | | | | |
| Write (×8 No.1) | | | | | H | H | | | | | | H | L | L | X | High-Z | D _{IN} (Odd Byte) | NP | |
| Output Disable | | | | | | | | | | | | L | | | | | High-Z | P | |
| Write (×8 No.2) | | | | L | H | X | L | H | L | L | | High-Z | D _{IN} (Odd Byte) | NP | | | | | |
| Output Disable | | | | | | | | | | | | | L | High-Z | P | | | | |
| Write (×16) | | | | | L | L | X | | | | | | L | H | L | L | High-Z | D _{IN} | NP |
| Output Disable | | | | | | | | | | | | | | | | | | H | High-Z |
| Output Disable | | | | X | X | X | X | H | H | X | | High-Z | P or NP | | | | | | |

Notes:

*1: H = V_{IH} , L = V_{IL} , X = Either V_{IL} or V_{IH} , WP SW = Write Protect Switch, P = Protect, NP = Non Protect

*2: L-level is output when WPSW = NP. H-level is output when WPSW = P.

*3: Not available for MB98A81063.

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■ FUNCTION TRUTH TABLE (Continued)

ATTRIBUTE MEMORY FUNCTION*1

| Mode | RESET*3 | REG | CE2 | CE1 | A ₀ | OE | WE | WP*2 | Data Input/Output | | WP SW | | | | | | | | | | | | | | | |
|-----------------|---------|-----|-----|-----|----------------|----|----|----------------------------|-----------------------------------|----------------------------------|---------|-----------------|------------------|---|--------|---|---|--------|-----------------|--------|---|----------------------------|----|---|---|----------------------------|
| | | | | | | | | | D ₈ to D ₁₅ | D ₀ to D ₇ | | | | | | | | | | | | | | | | |
| Standby | L | X | H | H | X | X | X | X | High-Z | | P or NP | | | | | | | | | | | | | | | |
| Read (×8 No.1) | | L | L | H | L | L | H | X | High-Z | D _{OUT} | | P or NP | | | | | | | | | | | | | | |
| Read (×8 No.1) | | | | | | | | | | H | | | | | | | | | | | | | | | | |
| Read (×8 No.2) | | | | | | | | | L | H | | | X | H | High-Z | | | | | | | | | | | |
| Read (×16) | | | | | | | | | | L | | | D _{OUT} | | | | | | | | | | | | | |
| Write (×8 No.1) | | | | | | | | | H | L | | | L | L | H | L | L | High-Z | D _{IN} | NP | | | | | | |
| Output Disable | | | | | | | | | | | | | | | | | | | High-Z | High-Z | P | | | | | |
| Write (×8 No.1) | | | | | | | | | | | | | | | | | | | | H | H | INVALID D _{IN} | NP | | | |
| Output Disable | | | | | | | | | | | | | | | | | | | High-Z | | | | | P | | |
| Write (×8 No.2) | | | | | | | | | | | | | | | | | | L | | H | X | H | L | | L | INVALID D _{IN} |
| Output Disable | | | | | | | | | | | | | | | | | | | High-Z | | | | | P | | |
| Write (×16) | | L | L | X | H | L | L | INVALID D _{IN} | | | | D _{IN} | | | | | | | | | | | | | | NP |
| Output Disable | | | | | | | | | | | | | | | | | | | High-Z | | | | | P | | |
| Output Disable | | X | X | X | X | H | H | X | High-Z | | | P or NP | | | | | | | | | | | | | | |

Notes:

*1: H = V_{IH}, L = V_{IL}, X = Either V_{IL} or V_{IH}, WP SW = Write Protect Switch, P = Protect, NP = Non Protect

*2: L-level is output when WPSW = NP. H-level is output when WPSW = P.

*3: Not available for MB98A81063.

MB98A81063-15/81183-15/81273-15/81373-15/81473-15/81573-15

■ COMMAND DEFINITION TABLE

Command table for 8-bit Mode

| Command | Bus Cycle | 1st Bus Write Cycle | | 2nd Bus Write/Read Cycle | | 3rd Bus Write Cycle | | 4th Bus Write/Read Cycle | | 5th Bus Write Cycle | | 6th Bus Write Cycle | |
|---------------------------|-----------|---------------------|-----|--------------------------|-----|---------------------|-----|--------------------------|-----|---------------------|-----|---------------------|-----|
| Read/Reset 1 | 2 | Write | | Read | | | | | | | | | |
| | | CA | F0H | RA | RD | | | | | | | | |
| Read/Reset 2 | 4 | Write | | Write | | Write | | Read | | | | | |
| | | RCMA1 | AAH | RCMA2 | 55H | RCMA1 | F0H | RA | RD | | | | |
| Read Intelligent ID Codes | 4 | Write | | Write | | Write | | Read | | | | | |
| | | ICMA1 | AAH | ICMA2 | 55H | ICMA1 | 90H | IA | ID | | | | |
| Byte Program | 4 | Write | | Write | | Write | | Write | | | | | |
| | | PCMA1 | AAH | PCMA2 | 55H | PCMA1 | A0H | PA | PD | | | | |
| Sector Erase | 6 | Write | | Write | | Write | | Write | | Write | | Write | |
| | | SCMA1 | AAH | SCMA2 | 55H | SCMA1 | 80H | SCMA1 | AAH | SCMA2 | 55H | SA | 30H |
| Chip Erase | 6 | Write | | Write | | Write | | Write | | Write | | Write | |
| | | CCMA1 | AAH | CCMA2 | 55H | CCMA1 | 80H | CCMA1 | AAH | CCMA2 | 55H | CCMA1 | 10H |
| Sector Erase Suspend | 1 | Write | | | | | | | | | | | |
| | | CA | B0H | | | | | | | | | | |
| Sector Erase Resume | 1 | Write | | | | | | | | | | | |
| | | CA | 30H | | | | | | | | | | |

Notes:

CA: Chip Address. (address in chip selected by A₀, A₂₂, A₂₃ and A₂₄)
 SA: Sector Address (address in 64 KB selected by A₀, A₁₇, A₁₈, A₁₉, A₂₀, A₂₁, A₂₂, A₂₃ and A₂₄)
 PA: Program Address (address to be programmed)
 RA: Read Address (address to be read)
 IA: Intelligent ID read address (Manufacture Code 0000H, Device Code 0002H)

PD: Programming data
 RD: Read data
 ID: Intelligent Identifier (ID) Code

CCMA1, CCMA2: Command address for chip erase
 SCMA1, SCMA2: Command address for sector erase
 PCMA1, PCMA2: Command address for program
 RCMA1, RCMA2: Command address for Read/Reset
 ICMA1, ICMA2: Command address for intelligent ID read

See "Command Address Table for 8-bit Mode" in page 16.

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Command Table for 16-bit Mode*1

| Command | Bus Cycle | 1st Bus Write Cycle | | 2nd Bus Write/Read Cycle | | 3rd Bus Write Cycle | | 4th Bus Write/Read Cycle | | 5th Bus Write Cycle | | 6th Bus Write Cycle | |
|---------------------------|-----------|---------------------|-------|--------------------------|-------|---------------------|-------|--------------------------|-------|---------------------|-------|---------------------|-------|
| Read/Reset 1 | 2 | Write | | Read | | | | | | | | | |
| | | — | F0F0H | RA | RD | | | | | | | | |
| Read/Reset 2 | 4 | Write | | Write | | Write | | Read | | | | | |
| | | RCMA1 | AAAAH | RCMA2 | 5555H | RCMA1 | F0F0H | RA | RD | | | | |
| Read Intelligent ID Codes | 4 | Write | | Write | | Write | | Read | | | | | |
| | | ICMA1 | AAAAH | ICMA2 | 5555H | ICMA1 | 9090H | IA | ID | | | | |
| Byte Program | 4 | Write | | Write | | Write | | Write | | | | | |
| | | PCMA1 | AAAAH | PCMA2 | 5555H | PCMA1 | A0A0H | PA | PD | | | | |
| Sector Erase | 6 | Write | | Write | | Write | | Write | | Write | | Write | |
| | | SCMA1 | AAAAH | SCMA2 | 5555H | SCMA1 | 8080H | SCMA1 | AAAAH | SCMA2 | 5555H | SA | 3030H |
| Chip Erase | 6 | Write | | Write | | Write | | Write | | Write | | Write | |
| | | CCMA1 | AAAAH | CCMA2 | 5555H | CCMA1 | 8080H | CCMA1 | AAAAH | CCMA2 | 5555H | CCMA1 | 1010H |
| Sector Erase Suspend | 1 | Write | | | | | | | | | | | |
| | | CA | B0B0H | | | | | | | | | | |
| Sector Erase Resume | 1 | Write | | | | | | | | | | | |
| | | CA | 3030H | | | | | | | | | | |

Notes:

CA: Chip Address. (address in chip selected by A₂₂, A₂₃ and A₂₄)
SA: Sector Address (address in 128 KB selected by A₁₇, A₁₈, A₁₉, A₂₀, A₂₁, A₂₂, A₂₃ and A₂₄)
PA: Program Address (address to be programmed)
RA: Read Address (address to be read)
IA: Intelligent ID read address (Manufacture Code 0000H, Device Code 0001H)

PD: Programming data
RD: Read data
ID: Intelligent Identifier (ID) Code

CCMA1, CCMA2: Command address for chip erase
SCMA1, SCMA2: Command address for sector erase
PCMA1, PCMA2: Command address for program
RCMA1, RCMA2: Command address for Read/Reset
ICMA1, ICMA2: Command address for intelligent ID read

See "Command Address Table for 16-bit Mode" in page 16.

*1: Address number is not contained "A₀".

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■ COMMAND DEFINITION TABLE (Continued)

Command Address Table for 8-bit Mode

| Command Address | MB98A81063 | MB98A81183 | MB98A81273, 81373, 81473, 81573 |
|-----------------|---------------------------|--------------------------|---------------------------------|
| CCMA1 | (CA AND 000001h) OR AAAAh | (CA AND 000001h) OR AAAh | CA |
| CCMA2 | (CA AND 000001h) OR 5554h | (CA AND 000001h) OR 554h | CA |
| SCMA1 | (SA AND 000001h) OR AAAAh | (SA AND 000001h) OR AAAh | CA |
| SCMA2 | (SA AND 000001h) OR 5554h | (SA AND 000001h) OR 554h | CA |
| PCMA1 | (PA AND 000001h) OR AAAAh | (PA AND 000001h) OR AAAh | CA |
| PCMA2 | (PA AND 000001h) OR 5554h | (PA AND 000001h) OR 554h | CA |
| RCMA1 | (RA AND 000001h) OR AAAAh | (RA AND 000001h) OR AAAh | CA |
| RCMA2 | (RA AND 000001h) OR 5554h | (RA AND 000001h) OR 554h | CA |
| ICMA1 | (IA AND 000001h) OR AAAAh | (IA AND 000001h) OR AAAh | CA |
| ICMA1 | (IA AND 000001h) OR 5554h | (IA AND 000001h) OR 554h | CA |

Command Address Table for 16-bit Mode

| Command Address | MB98A81063 | MB98A81183 | MB98A81273, 81373, 81473, 81573 |
|-----------------|------------|------------|---------------------------------|
| CCMA1 | 5555h | 555h | CA |
| CCMA2 | 2AAAh | 2AAh | CA |
| SCMA1 | 5555h | 555h | CA |
| SCMA2 | 2AAAh | 2AAh | CA |
| PCMA1 | 5555h | 555h | CA |
| PCMA2 | 2AAAh | 2AAh | CA |
| RCMA1 | 5555h | 555h | CA |
| RCMA2 | 2AAAh | 2AAh | CA |
| ICMA1 | 5555h | 555h | CA |
| ICMA1 | 2AAAh | 2AAh | CA |

MB98A81063-15/81183-15/81273-15/81373-15/81473-15/81573-15

■ WRITE OPERATION STATUS

Hardware Sequence Flag Table

| Status | | D ₇ , D ₁₅ | D ₆ , D ₁₄ | D ₅ , D ₁₃ | D ₃ , D ₁₁ | D ₂ , D ₁₀ *4 | R/B*4 | |
|----------------------|-------------------------|-------------------------------------|----------------------------------|----------------------------------|----------------------------------|-------------------------------------|-------|---|
| In Progress | Programming | $\overline{D}_7, \overline{D}_{15}$ | Toggle | 0 | 0 | 1 | 0 | |
| | Erasing | 0 | Toggle | 0 | 1 | Toggle | 0 | |
| | Erase Suspend Read | (1) | 1 | 1 | 0 | 0 | *1 | 1 |
| | | (2) | Data | Data | Data | Data | Data | 1 |
| | Erase Suspend*4 Program | $\overline{D}_7, \overline{D}_{15}$ | *2 | 0 | 0 | *1, *3 | 0 | |
| Exceeded Time Limits | Programming | $\overline{D}_7, \overline{D}_{15}$ | Toggle | 1 | 0 | 1 | 0 | |
| | Erasing | 0 | Toggle | 1 | 1 | N/A | 0 | |
| | Erase Suspend*4 Program | $\overline{D}_7, \overline{D}_{15}$ | Toggle | 1 | 0 | N/A | 0 | |

Notes:

(1): Erase Suspended Sector (2): Non-Erase Suspended Sector

*1. Performing successive read operations from the erase-suspended sector will cause D₂, D₁₀ to toggle.

*2. Performing successive read operations from any address will cause D₆, D₁₄ to toggle.

*3. Reading the byte address being programmed while in the erase-suspend program mode will indicate logic "1" at the D₂, D₁₀ bit. However, successive reads from the erase-suspended sector will cause D₂, D₁₀ to toggle.

*4. Not applied for MB98A81063.

D₇, D₁₅ ($\overline{\text{Data}}$ Polling)

The card features $\overline{\text{Data}}$ Polling as a method to indicate to the host that the Program/Erase Operation are in progress or completed. During the program operation an attempt to read the program address will produce the compliment of the data last written to D₇/D₁₅. Upon completion of the program operation, an attempt to read the program address will produce the true data last written to D₇/D₁₅. During the erase operation, an attempt to read the erase address will produce a "0" at the D₇/D₁₅ output. Upon completion of the erase operation an attempt to read the device will produce a "1" at the D₇/D₁₅ output.

For Chip Erase, the $\overline{\text{Data}}$ Polling is valid after the rising edge of the sixth $\overline{\text{WE}}$ pulse in the six write pulse sequence. For sector erase, the $\overline{\text{Data}}$ Polling is valid after the last rising edge of the sector erase $\overline{\text{WE}}$ pulse. Even if the device has completed the operation and D₇/D₁₅ has a valid data, the data outputs on D₀ to D₆/D₈ to D₁₄ may be still invalid. The valid data on D₀ to D₇/D₈ to D₁₅ will be read on the successive read attempts.

The $\overline{\text{Data}}$ Polling feature is only active during the programming operation, erase operation, sector erase time-out, Erase Suspend Read mode and Erase Suspend Program mode.

D₆, D₁₄ (Toggle Bit I)

The card also features the "Toggle Bit" as a method to indicate to the host system that the Program/Erase Operation are in progress or completed.

During an Program or Erase cycle, successive attempts to read ($\overline{\text{OE}}$ or $\overline{\text{CE}}$ toggling) data from the card will result in D₆/D₁₄ toggling between one and zero. Once the Program or Erase cycle is completed, D₆/D₁₄ will stop toggling and valid data will be read on the next successive attempts. During programming, the Toggle Bit is valid after the rising edge of the fourth $\overline{\text{WE}}$ pulse in the four write pulse sequence. For chip erase, the Toggle Bit is valid after the rising edge of the sixth $\overline{\text{WE}}$ pulse in the six write pulse sequence. For sector erase, the Toggle Bit is valid after the last rising edge of the sector erase $\overline{\text{WE}}$ pulse. The Toggle Bit is also active during the sector time out.

Either $\overline{\text{CE}}$ or $\overline{\text{OE}}$ toggling will cause the D₆/D₁₄ to toggle.

MB98A81063-15/81183-15/81273-15/81373-15/81473-15/81573-15**D₅, D₁₃ (Exceeded Timing Limits)**

D₅/D₁₃ will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions D₅/D₁₃ will produce a "1". This is a failure condition which indicates that the program or erase cycle was not successfully completed. $\overline{\text{Data}}$ Polling is the only operating function of the card under this condition. If this failure condition occurs during sector erase operation, it specifies that a particular sector is bad and it may not be reused, however, other sectors are still functional and may be used for the program or erase operation. The chip must be reset to use other sectors. Write the Reset command sequence to the chip, and then execute Program or Erase command sequence. This allows the system to continue to use the other active sectors in the chip.

If this failure condition occurs during the chip erase operation, it specifies that the entire chip or combination of sectors are bad.

If this failure condition occurs during the byte programming operation, it specifies that the entire sector containing that byte is bad and this sector may not be reused, (other sectors are still functional and can be reused).

The D₅/D₁₃ failure condition may also appear if a user tries to program a non blank location without erasing. In this case the card locks out and never completes the card operation. Hence, the system never reads a valid data on D₇/D₁₅ bit and D₆/D₁₄ never stops toggling. Once the card has exceeded timing limits, the D₅/D₁₃ bit will indicate a "1". Please note that this is not a device failure condition since the device was incorrectly used.

D₃, D₁₁ (Sector Erase Timer)

After the completion of the initial sector erase command sequence the sector erase time-out will begin. D₃/D₁₁ will remain low until the time-out is complete. $\overline{\text{Data}}$ Polling and Toggle Bit are valid after the initial sector erase command sequence.

If $\overline{\text{Data}}$ Polling or the Toggle Bit indicates the card has been written with a valid erase command, D₃/D₁₁ may be used to determine if the sector erase timer window is still open. If D₃/D₁₁ is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the card will be ignored until the erase operation is completed as indicated by $\overline{\text{Data}}$ Polling or Toggle Bit. If D₃/D₁₁ is low ("0"), the card will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of D₃/D₁₁ prior to and following each subsequent sector erase command. If D₃/D₁₁ were high on the second status check, the command may not have been accepted.

Refer to Table : Hardware Sequence Flags.

D₂, D₁₀ (Toggle Bit II, not applied for MB98A81063)

This Toggle bit, along with D₆, can be used to determine whether the card is in the Erase operation or in Erase Suspend.

Successive reads from the erasing sector will cause D₂ to toggle during the Erase operation. If the card is in the erase-suspended-read mode, successive reads from the erase-suspended sector will cause D₂ to toggle. When the card is in the erase-suspended-program mode, successive reads from the byte address of the non-erase suspended sector will indicate a logic '1' at the D₂ bit.

D₆ is different from D₂ in that D₆ toggles only when the standard Program or Erase, or Erase Suspend Program operation is in progress.

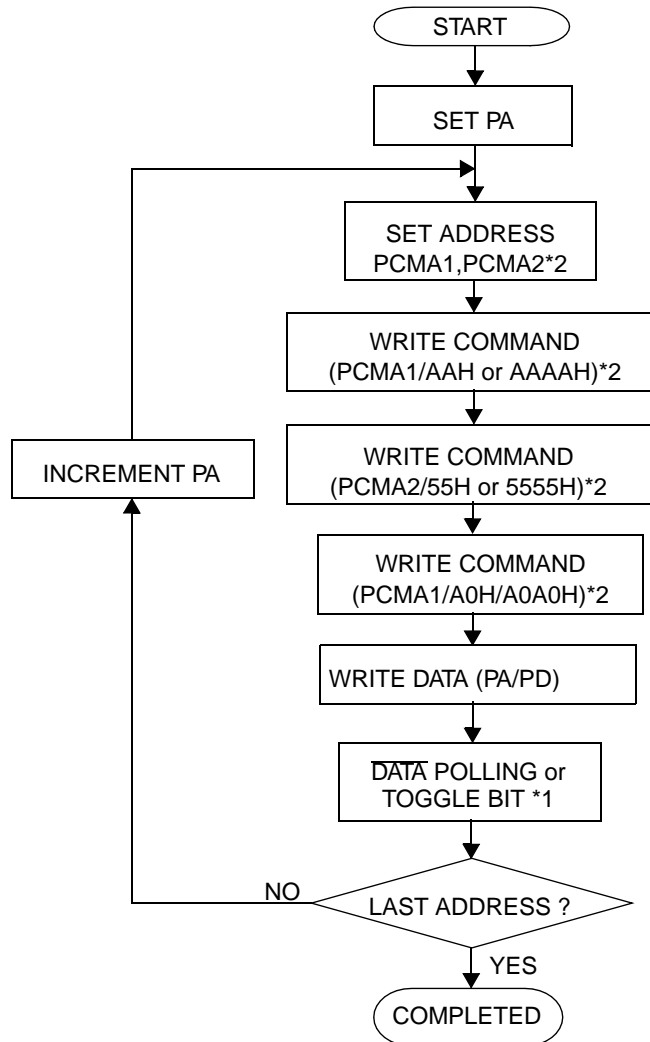
R/ $\overline{\text{B}}$ (Ready/ $\overline{\text{Busy}}$, not applied for MB98A81063)

The card provides a R/ $\overline{\text{B}}$ output pin as a way to indicate to the system that the program or erase operation are either in progress or has been completed. If the output is low, the card is busy with either a program or erase operation. If the card is placed in an Erase Suspend mode, the R/ $\overline{\text{B}}$ output will be high.

During programming, the R/ $\overline{\text{B}}$ pin is driven low after the rising edge of the fourth $\overline{\text{WE}}$ pulse. During an erase operation, the R/ $\overline{\text{B}}$ pin is driven low after the rising edge of the sixth $\overline{\text{WE}}$ pulse. The R/ $\overline{\text{B}}$ pin will indicate a busy condition during the RESET pulse.

PROGRAM / ERASE FLOWCHART

Fig. 3 - PROGRAM FLOWCHART



*1 See Fig. 7, 6, 9, 10.

*2 See "COMMAND DEFINITION TABLE".

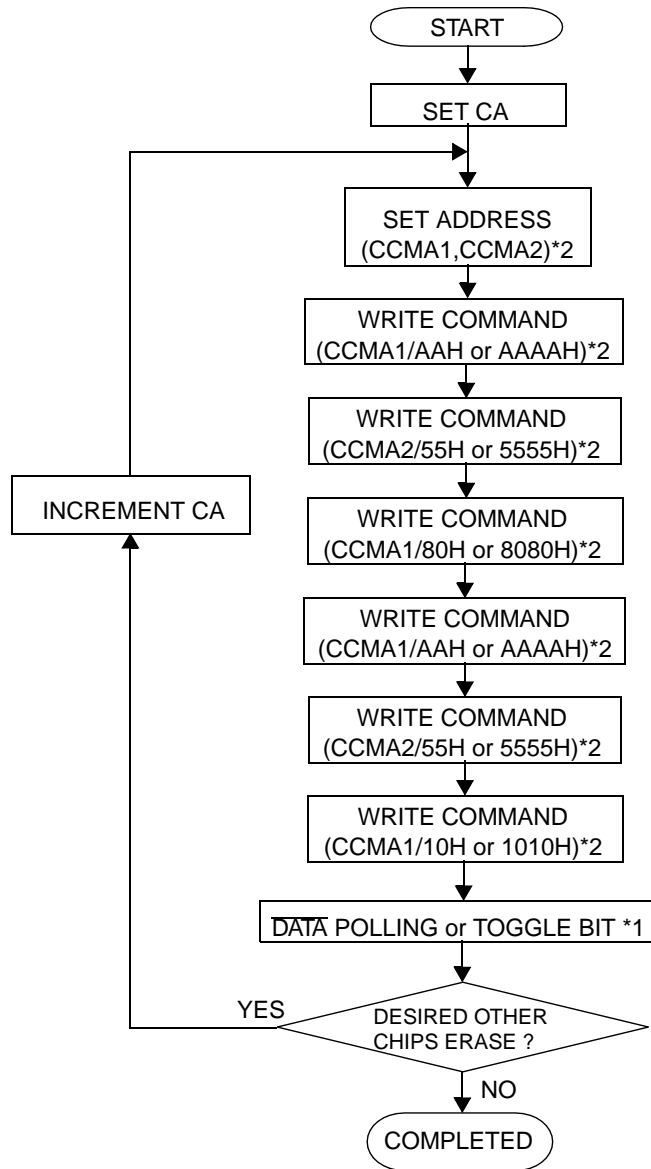
Notes:

PD : PROGRAM DATA

PA : PROGRAM ADDRESS

PROGRAM / ERASE FLOWCHART (Continued)

Fig. 4 - CHIP ERASE FLOWCHART



*1 See Fig. 7, 8, 9, 10.

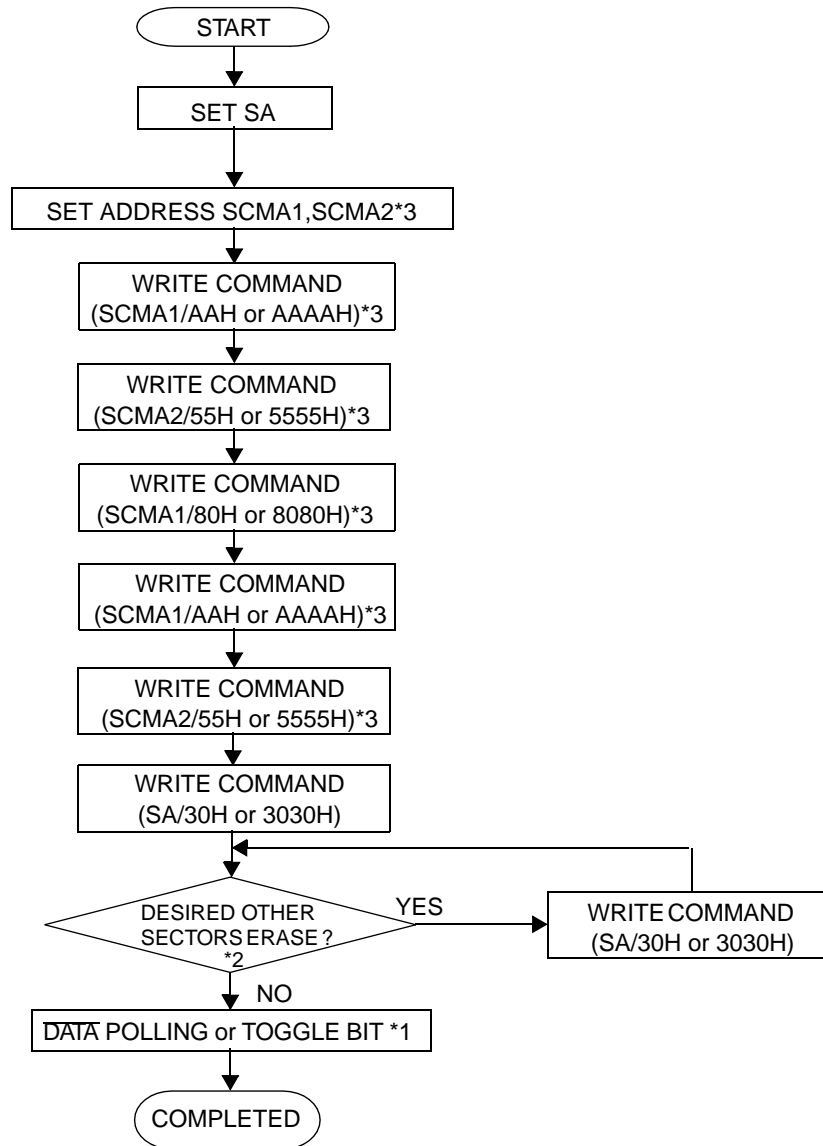
*2 See "COMMAND DEFINITION TABLE".

Note:

CA : CHIP ADDRESS

PROGRAM / ERASE FLOWCHART (Continued)

Fig. 5 - SECTOR ERASE FLOWCHART



*1 See Fig.7, 8, 9, 10.

*2 Possible for the sectors in a chip

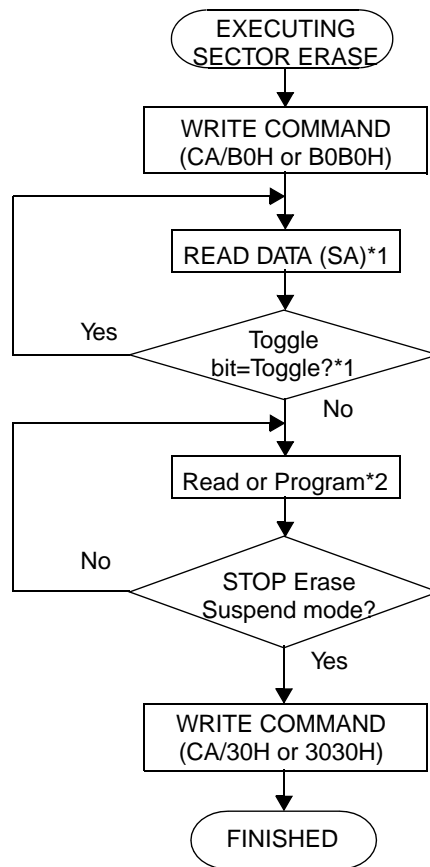
*3 See "COMMAND DEFINITION TABLE".

Note:

SA : SECTOR ADDRESS

PROGRAM / ERASE FLOWCHART (Continued)

Fig. 6 - ERASE SUSPEND FLOWCHART



*1 Detection whether suspend mode is valid can be done by $\overline{\text{Data}}$ Polling and R/ $\overline{\text{B}}$ also. (MB98A81063 does not have R/ $\overline{\text{B}}$).

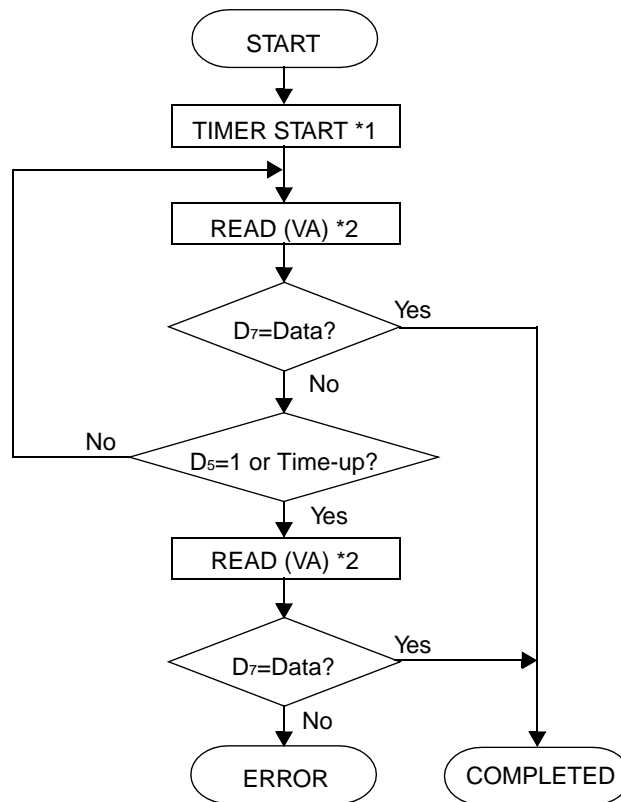
*2 Only Read operation for MB98A81063.

Notes:

CA: CHIP ADDRESS
SA: SECTOR ADDRESS
RA: READ ADDRESS

PROGRAM / ERASE FLOWCHART (Continued)

Fig. 7 - DATA POLLING FLOWCHART: × 8-bit mode No.1

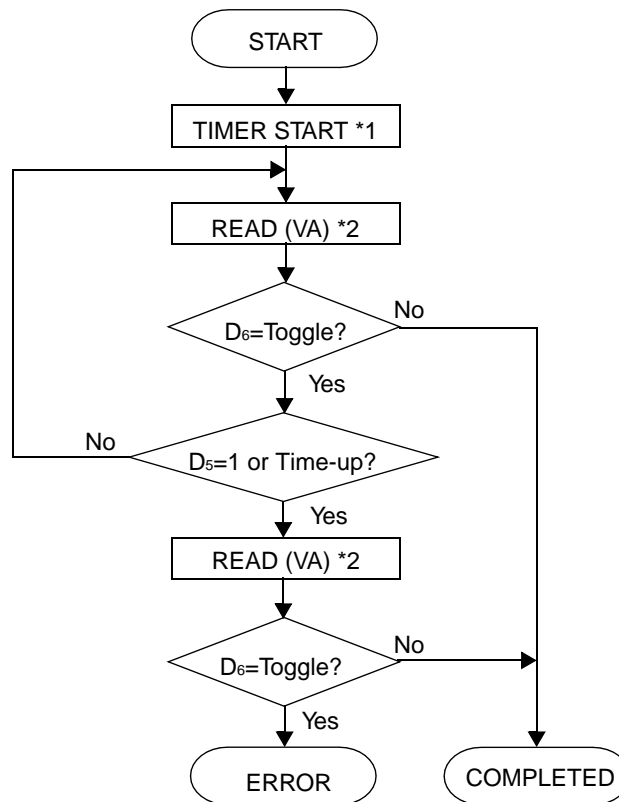


*1 User sets the time period referring to
"PROGRAM AND ERASE PERFORMANCES".

*2 ProgramVA=PA
Chip EraseVA=CA
Sector EraseVA=SA

PROGRAM / ERASE FLOWCHART (Continued)

Fig. 8 - TOGGLE BIT FLOWCHART: × 8-bit mode No.1

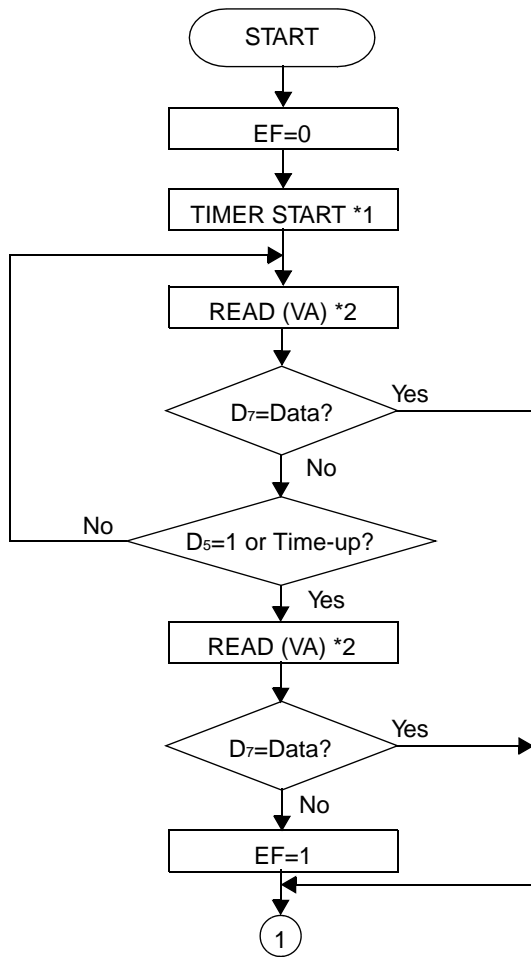


*1 User sets the time period referring to
"PROGRAM AND ERASE PERFORMANCES".

*2 Program VA=PA
Chip Erase VA=CA
Sector Erase VA=SA

PROGRAM / ERASE FLOWCHART (Continued)

Fig. 9 - DATA POLLING FLOWCHART: × 16-bit mode

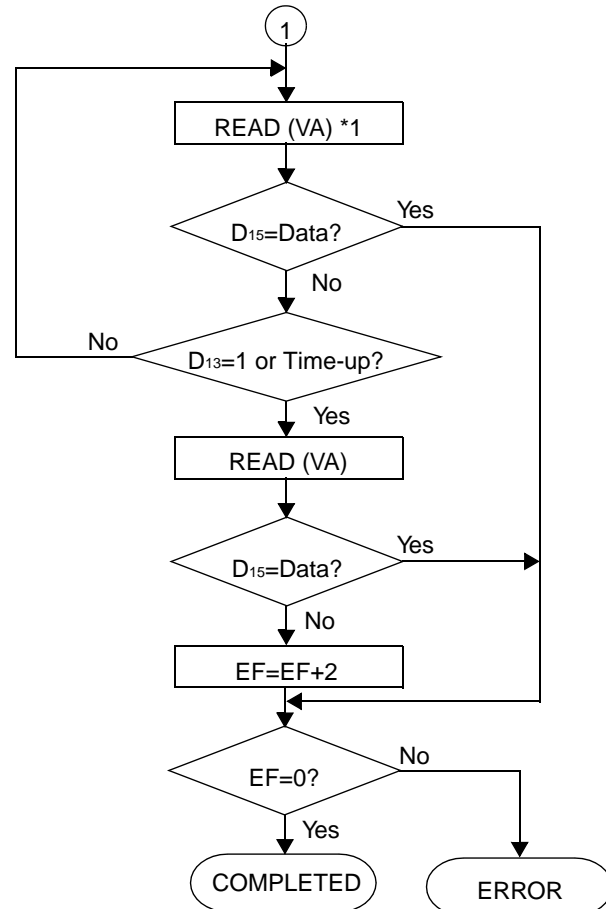


*1 User sets the time period referring to "PROGRAM AND ERASE PERFORMANCES".

*2 Program VA=PA
 Chip Erase VA=CA
 Sector Erase VA=SA

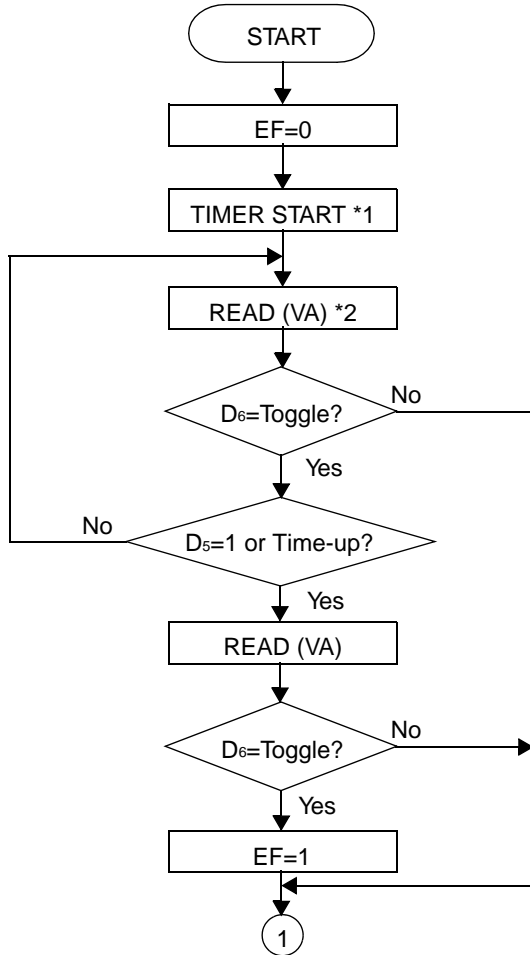
Notes:

EF: Error Flag
 EF=0: Operation Completed
 EF=1: Lower Byte Error
 EF=2: Upper Byte Error
 EF=3: Lower/Upper Byte Error



PROGRAM / ERASE FLOWCHART (Continued)

Fig. 10 - TOGGLE BIT FLOWCHART: × 16-bit mode

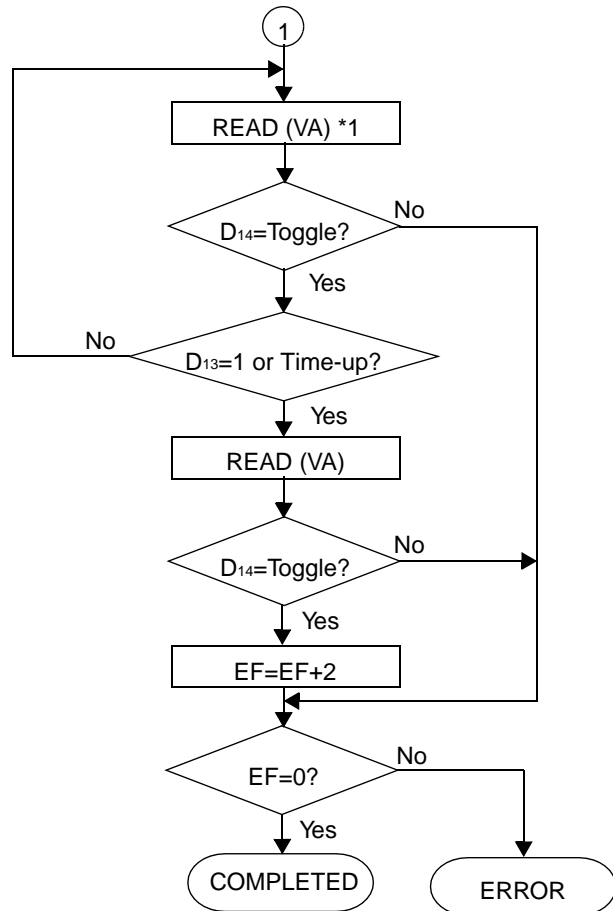


*1 User sets the time period referring to "PROGRAM AND ERASE PERFORMANCES".

*2 Program VA=PA
 Chip Erase VA=CA
 Sector Erase VA=SA

Notes:

EF: Error Flag
 EF=0: Operation Completed
 EF=1: Lower Byte Error
 EF=2: Upper Byte Error
 EF=3: Lower/Upper Byte Error



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■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

| Parameter | Symbol | Value | Unit |
|------------------------|-----------|------------------------|------|
| Supply Voltage | V_{CC} | -0.5 to +6.0 | V |
| Input Voltage | V_{IN} | -0.5 to $V_{CC} + 0.5$ | V |
| Output Voltage | V_{OUT} | -0.5 to $V_{CC} + 0.5$ | V |
| Temperature under Bias | T_A | 0 to +60 | °C |
| Storage Temperature | T_{STG} | -30 to +70 | °C |

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|-------------------------|----------|------|------|------|------|
| V_{CC} Supply Voltage | V_{CC} | 4.75 | 5.0 | 5.25 | V |
| Ground | GND | — | 0 | — | V |
| Ambient Temperature | T_A | 0 | — | 55 | °C |

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating conditions ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ CAPACITANCE

($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{IN} = V_{IO} = \text{GND}$)

| Parameter | Symbol | Min. | Max. | Unit |
|----------------------|----------|------|------|------|
| Input Capacitance *1 | C_{IN} | — | 75 | pF |
| I/O Capacitance *2 | C_{IO} | — | 50 | pF |

Notes:

*1 This value does not apply to $\overline{CE1}$, $\overline{CE2}$, \overline{WE} , \overline{REG} and \overline{RESET} .

*2 This value does not apply to $\overline{CD1}$, $\overline{CD2}$, $\overline{BVD1}$ and $\overline{BVD2}$.

MB98A81063-15/81183-15/81273-15/81373-15/81473-15/81573-15

■ DC CHARACTERISTICS

| Parameter | Test Conditions | Symbol | Value | | | Unit |
|-------------------------------|---|-----------|-------|-----------|----------------|---------------|
| | | | Min. | Typ. | Max. | |
| Input Leakage Current *1 | $V_{CC} = V_{CC \text{ max.}}, V_{IN} = 0 \text{ V or } V_{CC}$ | I_{LI} | — | ± 1.0 | ± 20 | μA |
| Output Leakage Current *2 | $V_{CC} = V_{CC \text{ max.}}, V_{IN} = 0 \text{ V or } V_{CC}$ | I_{LO} | — | ± 1.0 | ± 20 | μA |
| Standby Current | $V_{CC} = V_{CC \text{ max.}}$ $\overline{CE1}, \overline{CE2} = V_{CC}, V_{IN} = 0 \text{ V or } V_{CC}$ | I_{SB1} | — | 0.5 | 1.7 | mA |
| | $V_{CC} = V_{CC \text{ max.}}, \overline{CE1}, \overline{CE2} = V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ | I_{SB2} | — | 4.0 | 8.0 | mA |
| Active Read Current | $V_{CC} = V_{CC \text{ max.}}, \overline{CE1}, \overline{CE2} = V_{IL}$ Cycle = 200 ns, $I_{OUT} = 0 \text{ mA}$ | I_{CC1} | — | 100 | 160 | mA |
| Program Current | Program in progress ($\times 16$ mode) | I_{CC2} | — | — | 120 | mA |
| Erase Current | Erase in progress ($\times 16$ mode) | I_{CC3} | — | — | 120 | mA |
| Input Low Voltage | — | V_{IL} | -0.3 | — | 0.8 | V |
| Input High Voltage | — | V_{IH} | 2.4 | — | $V_{CC} + 0.3$ | V |
| Output Low Voltage | $I_{OL} = 3.2 \text{ mA}, V_{CC} = V_{CC \text{ min.}}$ | V_{OL} | — | — | 0.4 | V |
| Output High Voltage *3 | $I_{OH} = 2.0 \text{ mA}, V_{CC} = V_{CC \text{ min.}}$ | V_{OH} | 3.8 | — | — | V |
| Low V_{CC} Lock-out Voltage | Common Memory | V_{LKO} | 3.2 | 3.7 | 4.2 | V |
| | Attribute Memory | | — | 3.8 | — | V |

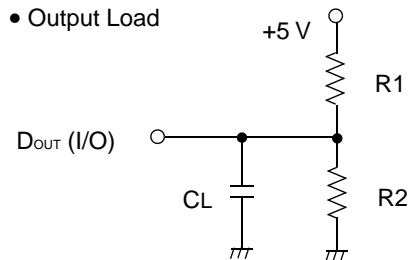
Notes:

- *1 This value does not apply to $\overline{CE1}$, $\overline{CE2}$, \overline{WE} and \overline{REG} .
- *2 This value does not apply to $\overline{BVD1}$, $\overline{BVD2}$, $\overline{CD1}$ and $\overline{CD2}$.
- *3 This value does not apply to $\overline{BVD1}$ and $\overline{BVD2}$.

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■ AC TEST CONDITIONS

Fig. 11 - AC TEST CONDITIONS



- Input Pulse Levels: $V_{IH} = 2.6\text{ V}$, $V_{IL} = 0.6\text{ V}$

- Input Pulse Rise and Fall Times: 5 ns
(Transient between 0.8 V and 2.4 V)

- Timing Reference Levels

Input: $V_{IL} = 0.8\text{ V}$, $V_{IH} = 2.4\text{ V}$ Output: $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$

* Including jig and stray capacitance

| | R1 | R2 | CL | Parameter Measured |
|---------|----------------|--------------|--------|---|
| Load I | 1.8 K Ω | 990 Ω | 100 pF | All parameters except tCLZ, tOLZ, tCHZ, tOHZ, tRCLZ, tROLZ, tRCHZ and tROHZ |
| Load II | 1.8 K Ω | 990 Ω | 5 pF | tCLZ, tOLZ, tCHZ, tOHZ, tRCLZ, tROLZ, tRCHZ and tROHZ |

■ PROGRAM AND ERASE PERFORMANCES

MAIN MEMORY PROGRAM / ERASE PERFORMANCE

(MB98A81063)

| Parameter | Min. | Typ. | Max. | Unit |
|--------------------------|---------|------|------|---------------|
| Byte Program Time *1 | — | 8 | 500 | μs |
| Chip Programming Time *1 | — | 4.2 | 25 | Sec. |
| Sector Erase Time *2 | — | 1 | 15 | Sec. |
| Program/Erase Cycles | 100,000 | — | — | Cycles |

Notes:

*1 Excludes system-level overhead.

*2 Excludes 00H programming prior to erasure.

(MB98A81183)

| Parameter | Min. | Typ. | Max. | Unit |
|--------------------------|---------|------|------|---------------|
| Byte Program Time *1 | — | 8 | 500 | μs |
| Chip Programming Time *1 | — | 8.4 | 50 | Sec. |
| Sector Erase Time *2 | — | 1 | 15 | Sec. |
| Program/Erase Cycles | 100,000 | — | — | Cycles |

Notes:

*1 Excludes system-level overhead.

*2 Excludes 00H programming prior to erasure.

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■ PROGRAM AND ERASE PERFORMANCES (Continued)

(MB98A81273, 81373, 81473, 81573)

| Parameter | Min. | Typ. | Max. | Unit |
|--------------------------|---------|------|------|--------|
| Byte Programming Time *1 | — | 8 | 500 | μs |
| Chip Programming Time *1 | — | 16.8 | 100 | Sec. |
| Sector Erase Time *2 | — | 1 | 15 | Sec. |
| Program/Erase Cycles | 100,000 | — | — | Cycles |

Notes:

*1 Excludes system-level overhead.

*2 Excludes 00H programming prior to erasure.

ATTRIBUTE MEMORY PROGRAM PERFORMANCE

| Parameter | Min. | Typ. | Max. | Unit |
|----------------------------|---------|------|------|-------|
| Byte Program Time | — | — | 1 | ms |
| Number of Program per Byte | 100,000 | — | — | Times |

■ AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

MAIN MEMORY READ CYCLE*1

| Parameter | Symbol | Min. | Max. | Unit |
|--|--------|------|------|------|
| Read Cycle Time | tRC | 150 | — | ns |
| Card Enable Access Time | tCE | — | 150 | ns |
| Address Access Time | tACC | — | 150 | ns |
| Output Enable Access Time | tOE | — | 75 | ns |
| Card Enable to Output in Low-Z*2 | tCLZ | 5 | — | ns |
| Card Disable to Output in High-Z*2 | tCHZ | — | 60 | ns |
| Output Enable to Output in Low-Z*2 | tOLZ | 5 | — | ns |
| Output Disable to Output in High-Z*2 | tOHZ | — | 60 | ns |
| Output Hold from Address, \overline{CE} , or \overline{OE} Change *3 | tOH | 5 | — | ns |
| Ready Time from RESET | tRDY | — | 20 | ms |

Notes:

*1 Rise/Fall time < 5 ns.

*2 Transition is measured at the point of ± 500 mV from steady state voltage. This parameter is specified using Load II in Fig. 11.

*3 This parameter is specified from the rising edge of \overline{OE} , $\overline{CE1}$ or $\overline{CE2}$, whichever occurs first.

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■ AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

MAIN MEMORY PROGRAM / ERASE CYCLE*1 *2

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|--------|------|------|------|---------|
| Write Cycle Time | tWC | 150 | — | — | ns |
| Address Setup Time | tAS | 20 | — | — | ns |
| Address Hold Time | tAH | 20 | — | — | ns |
| Data Setup Time | tDS | 50 | — | — | ns |
| Data Hold Time | tDH | 20 | — | — | ns |
| Read Recovery Time (\overline{WE} control) | tGHWL | 10 | — | — | ns |
| Read Recovery Time (\overline{CE} control) | tGHEL | 10 | — | — | ns |
| Output Enable Hold Time | tOEHL | 10 | — | — | ns |
| Card Enable Setup Time | tCS | 20 | — | — | ns |
| Card Enable Hold Time | tCH | 0 | — | — | ns |
| Write Enable Pulse Width | tWP | 80 | — | — | ns |
| Write Enable Setup Time | tWS | 0 | — | — | ns |
| Write Enable Hold Time | tWH | 0 | — | — | ns |
| Card Enable Pulse Width | tCP | 100 | — | — | ns |
| Duration of Byte Program Operation (\overline{WE} control) | tWHWH1 | — | 8 | — | μ s |
| Duration of Erase Operation *3 (\overline{WE} control) | tWHWH2 | — | 1 | 15 | s |
| Duration of Byte Program Operation (\overline{CE} control) | tEHEH1 | — | 8 | — | μ s |
| Duration of Erase Operation *3 (\overline{CE} control) | tEHEH2 | — | 1 | 15 | s |
| V _{CC} Setup Time *4 | tVCS | 50 | — | — | μ s |
| Reset Pulse Width | tRP | 500 | — | — | ns |
| Busy Delay Time | tBSY | 100 | — | — | ns |

Notes:

- *1 Read timing parameters during Program/Erase operations are the same as those during read only operations. Refer to AC characteristics for Main Memory Read Cycle.
- *2 Rise/Fall time \leq 5 ns.
- *3 These do not include the preprogramming time.
- *4 Not 100% tested.

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■ AC CHARACTERISTICS (Continued)

ATTRIBUTE MEMORY READ CYCLE *1

| Parameter | Symbol | Min. | Max. | Unit |
|-------------------------------------|--------|------|------|------|
| Read Cycle Time | tRRC | 250 | — | ns |
| Address Access Time | tRAA | — | 250 | ns |
| Card Enable Access Time | tRCE | — | 250 | ns |
| Output Enable Access Time | tROE | — | 125 | ns |
| Output Hold from Address Change | tROH | 5 | — | ns |
| Card Enable to Output Low-Z *2 | tRCLZ | 5 | — | ns |
| Output Enable to Output Low-Z *2 | tROLZ | 5 | — | ns |
| Card Enable to Output High-Z *2 | tRCHZ | — | 60 | ns |
| Output Enable to Output High-Z *2*3 | tROHZ | — | 60 | ns |

Notes:

*1 Rise/Fall time < 5 ns.

*2 Transition is measured at the point of ± 500 mV from steady state voltage. This parameter is specified using Load II in Fig. 3.

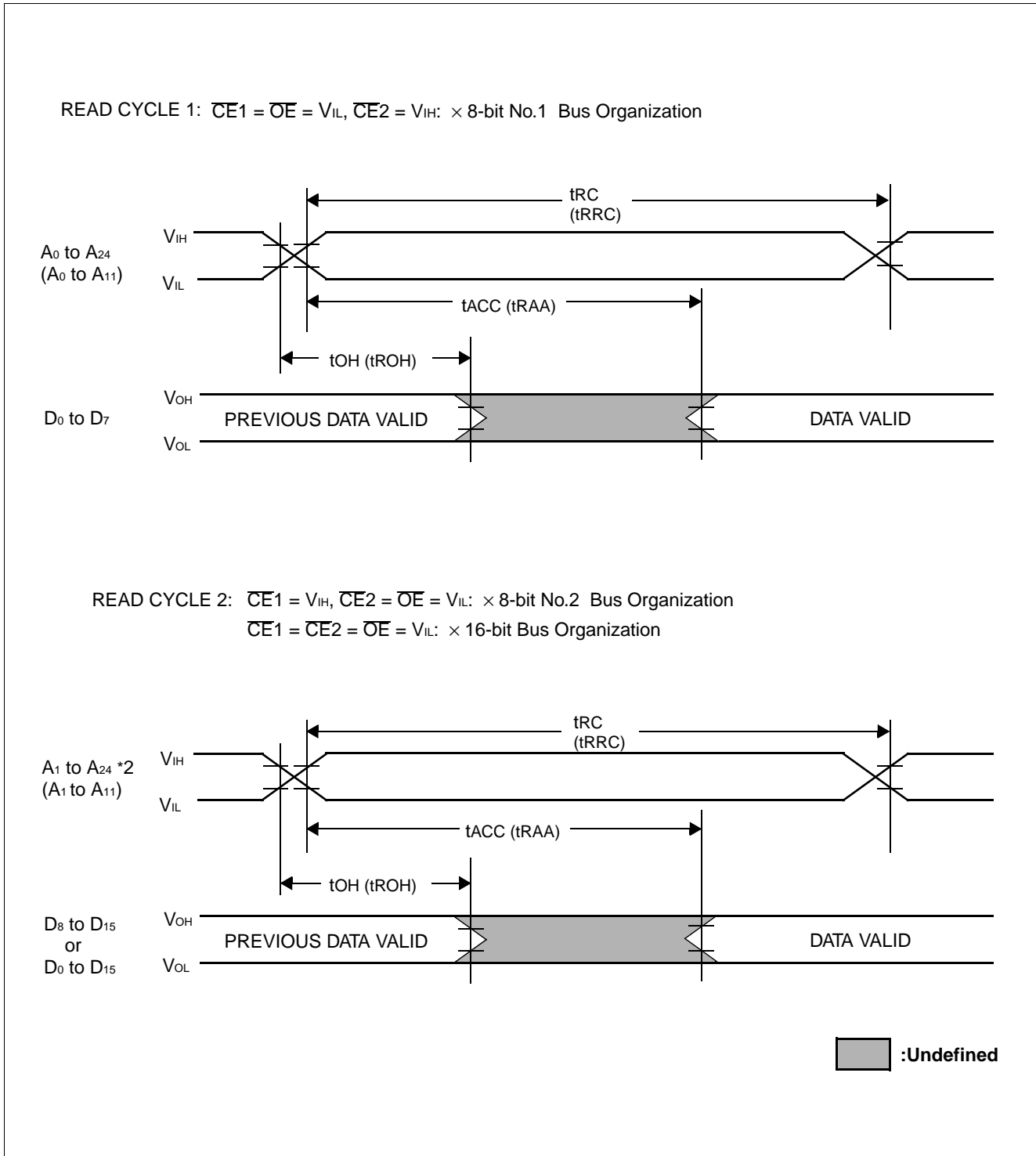
*3 This parameter is specified from the rising edge of \overline{OE} , $\overline{CE1}$ or $\overline{CE2}$, whichever occurs first.

ATTRIBUTE MEMORY PROGRAM CYCLE

| Parameter | Symbol | Min. | Max. | Unit |
|--------------------------|--------|------|------|------|
| Address Setup Time | tRAS | 20 | — | ns |
| Card Enable Setup Time | tRCS | 0 | — | ns |
| Output Enable Setup Time | tOES | 20 | — | ns |
| Write Pulse Width | tRWP | 100 | 1000 | ns |
| Address Hold Time | tRAH | 50 | — | ns |
| Data Setup Time | tRDS | 50 | — | ns |
| Data Hold Time | tRDH | 20 | — | ns |
| Card Enable Hold Time | tRCH | 0 | — | ns |
| Output Enable Hold Time | tROEH | 20 | — | ns |
| Program Time | tRWR | — | 1 | ms |

■ TIMING DIAGRAM

MAIN / ATTRIBUTE MEMORY READ CYCLE TIMING DIAGRAM ($\overline{WE} = V_{IH}, \overline{REG} = V_{IH}$)*1



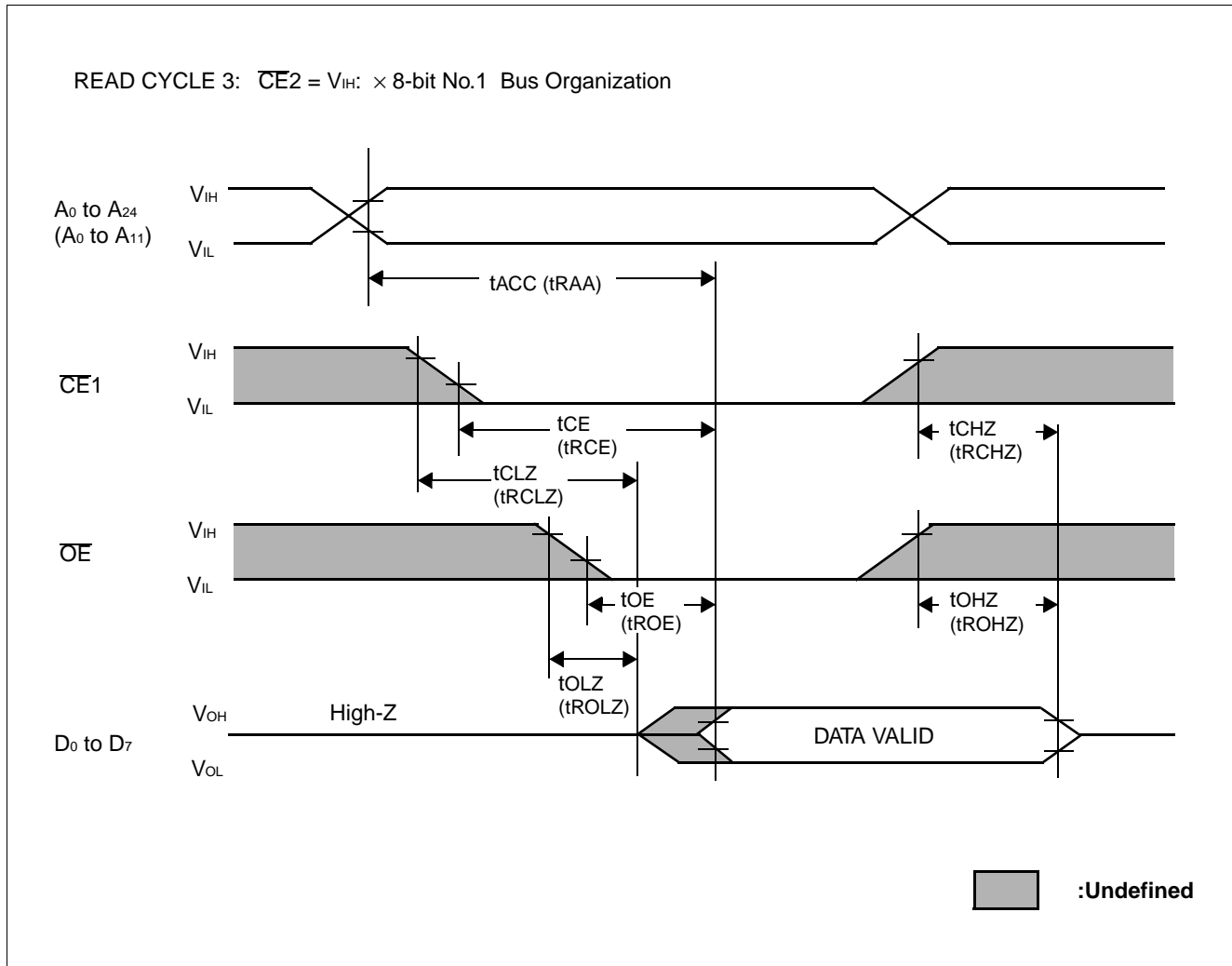
Notes:

*1 The addresses and parameters in () are applied for attribute memory access.

*2 $A_0 =$ Either V_{IH} or V_{IL} .

MB98A81063-15/81183-15/81273-15/81373-15/81473-15/81573-15

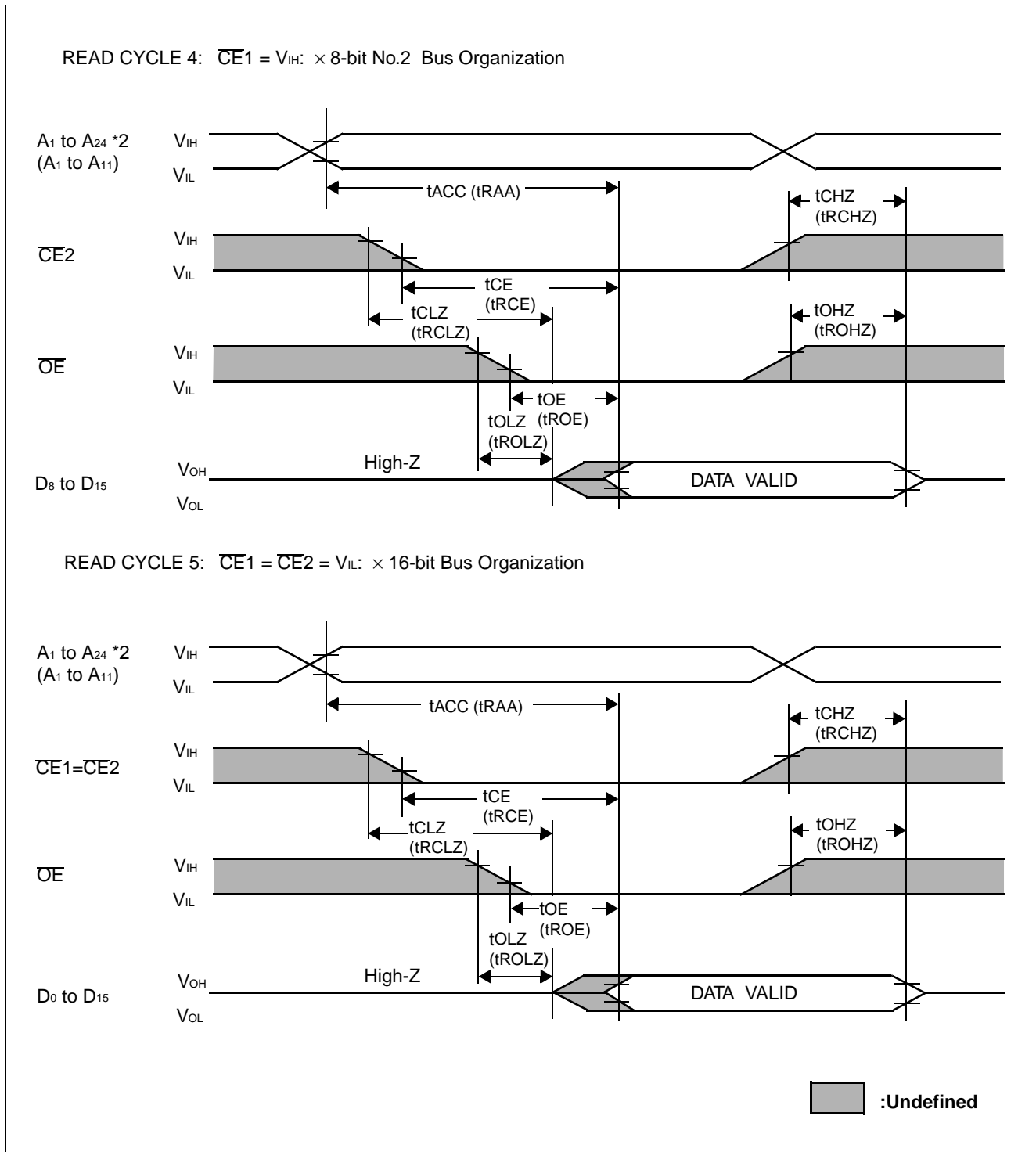
■ TIMING DIAGRAM (Continued)

MAIN / ATTRIBUTE MEMORY READ CYCLE TIMING DIAGRAM (Continued) ($\overline{WE} = V_{IH}$, $\overline{REG} = V_{IH}$)*1**Note:**

*1 The addresses and parameters in () are applied for attribute memory access.

■ TIMING DIAGRAM (Continued)

MAIN / ATTRIBUTE MEMORY READ CYCLE TIMING DIAGRAM(Continued)($\overline{WE} = V_{IH}$, $\overline{REG} = V_{IH}$)*1



Notes:

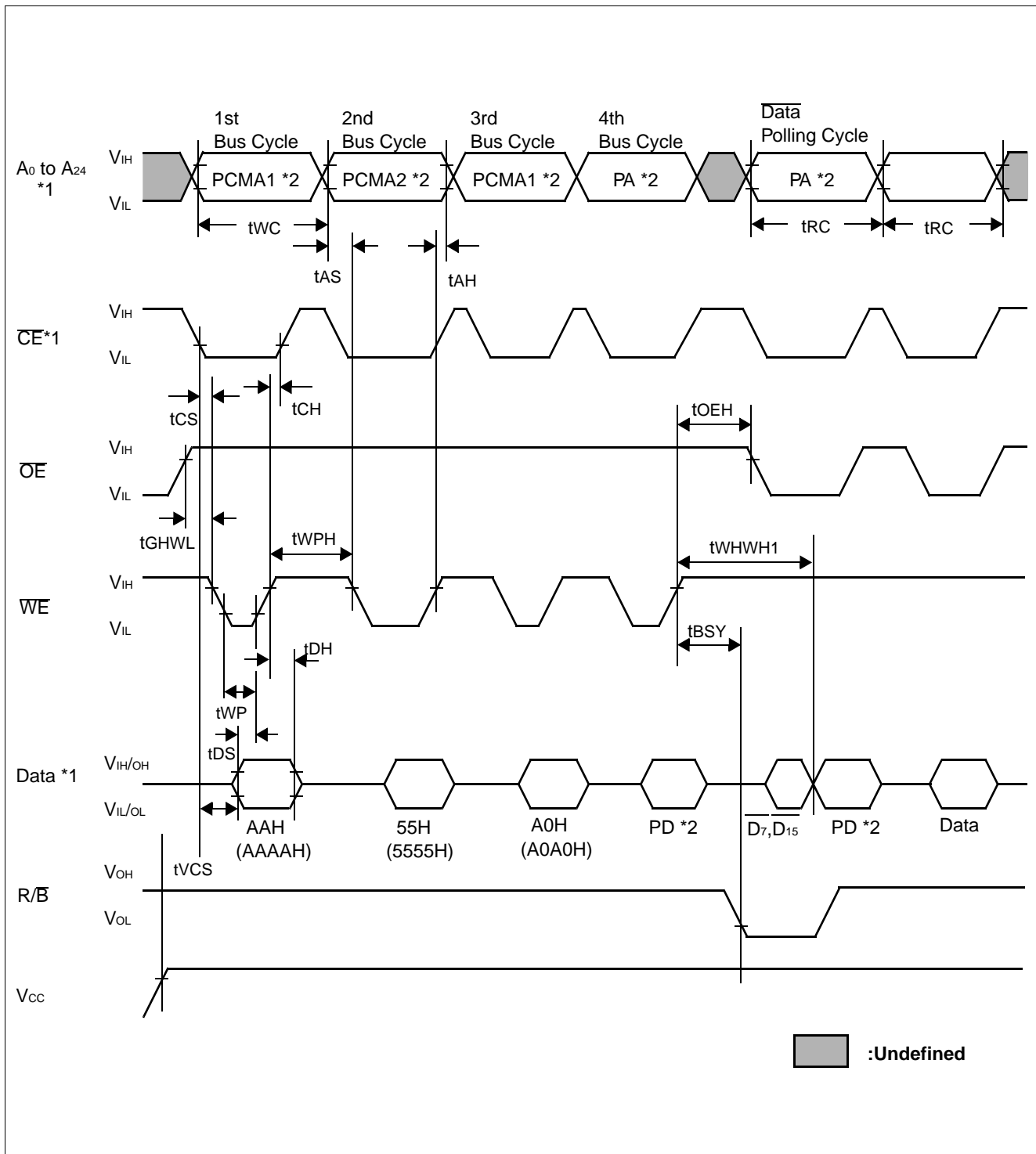
*1 The addresses and parameters in () are applied for attribute memory access.

*2 $A_0 = \text{Either } V_{IH} \text{ or } V_{IL}$.

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■ TIMING DIAGRAM (Continued)

MAIN MEMORY PROGRAM CYCLE TIMING DIAGRAM (\overline{WE} = CONTROLLED, $\overline{REG} = V_{IH}$)



Notes:

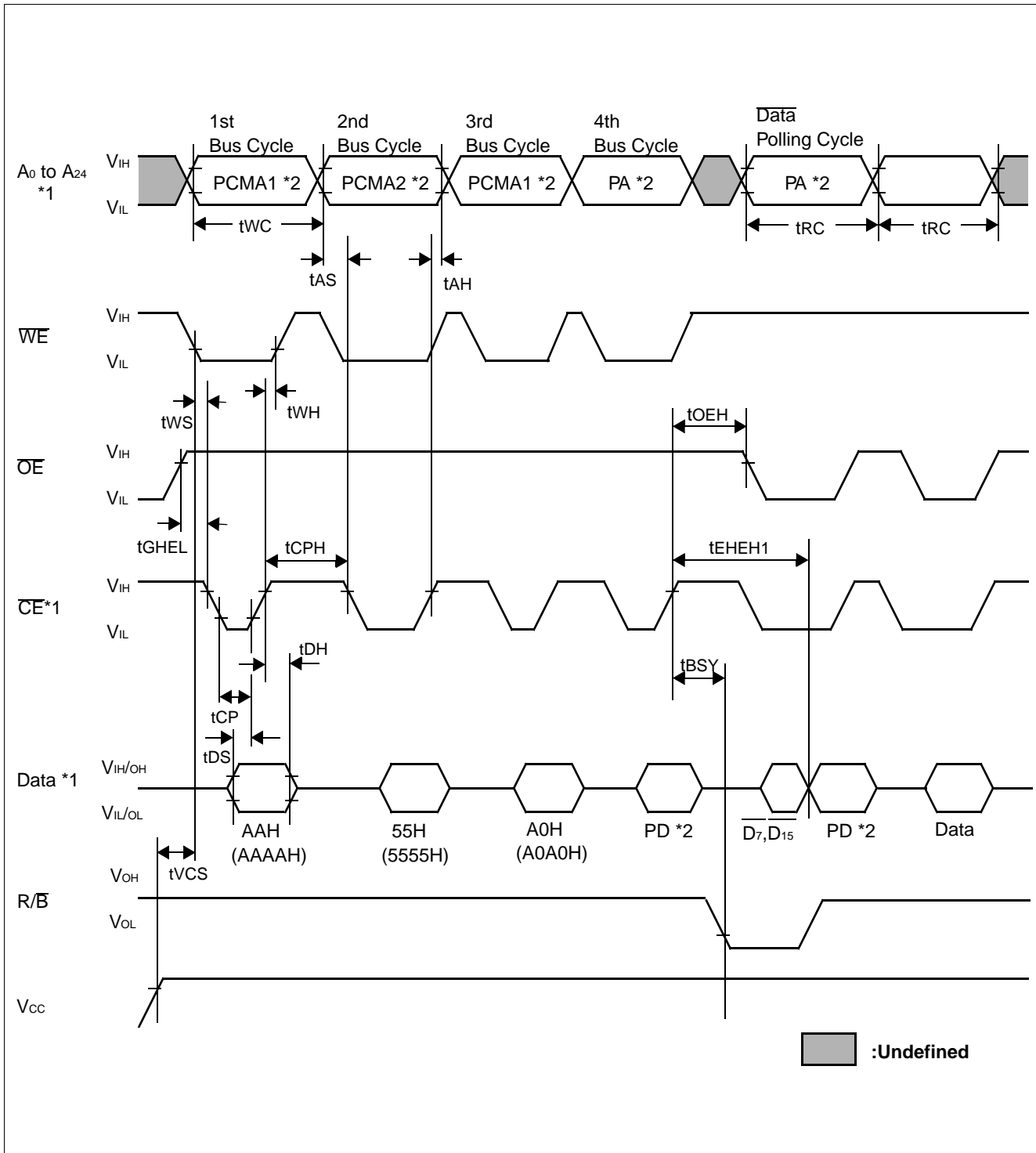
*1 See "FUNCTION TRUTH TABLE".

*2 PCMA1/PCMA2 = Command Address for Program, PA = Program Address, PD = Program Data. See "COMMAND DEFINITION TABLE".

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■ TIMING DIAGRAM (Continued)

MAIN MEMORY PROGRAM CYCLE TIMING DIAGRAM (\overline{CE} = CONTROLLED, $\overline{REG} = V_{IH}$)



Notes:

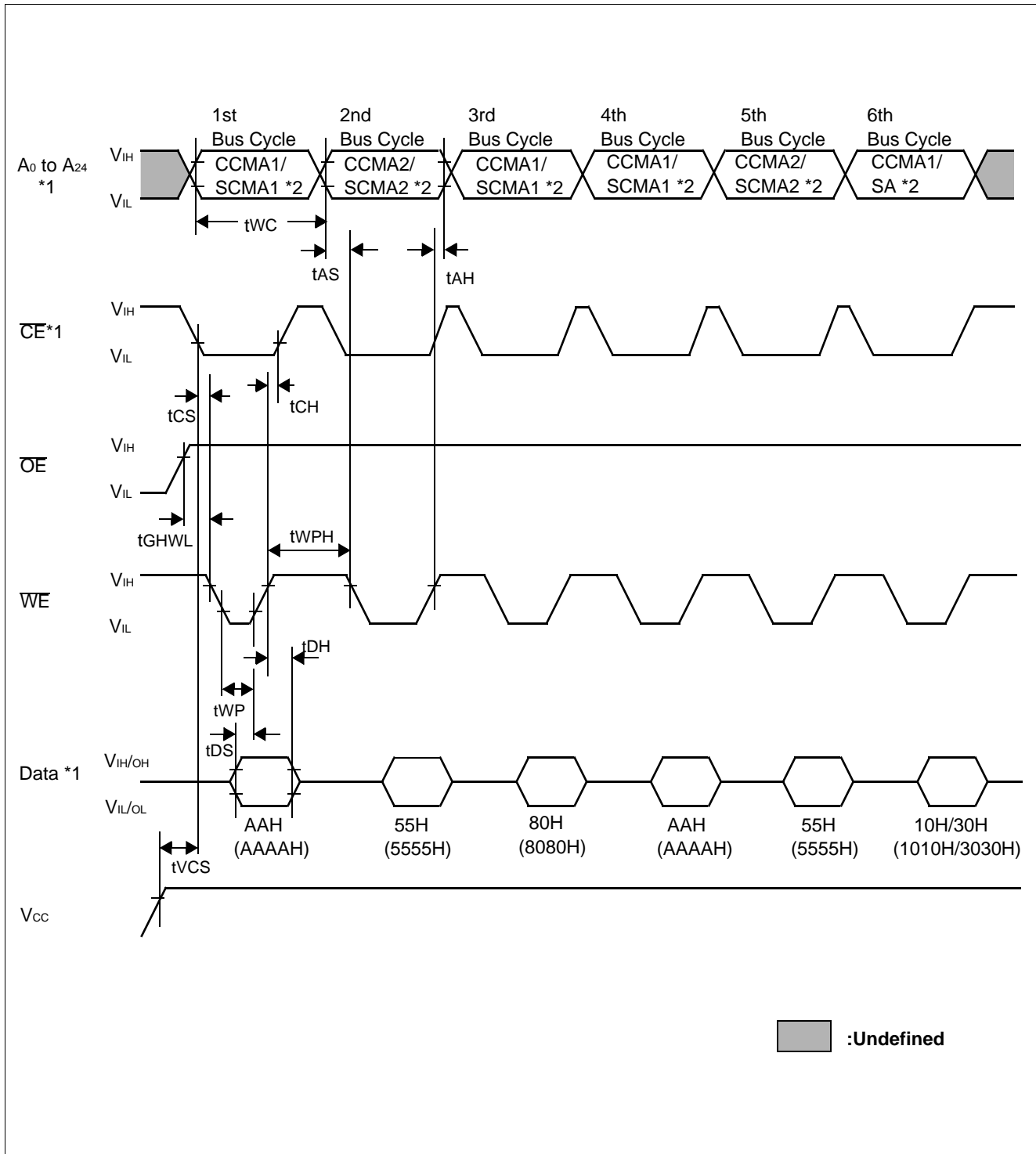
*1 See "FUNCTION TRUTH TABLE".

*2 PCMA1/PCMA2 = Command Address for Program, PA = Program Address, PD = Program Data. See "COMMAND DEFINITION TABLE".

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■ TIMING DIAGRAM (Continued)

MAIN MEMORY ERASE CYCLE TIMING DIAGRAM (\overline{WE} = CONTROLLED, $\overline{REG} = V_{IH}$)



Notes:

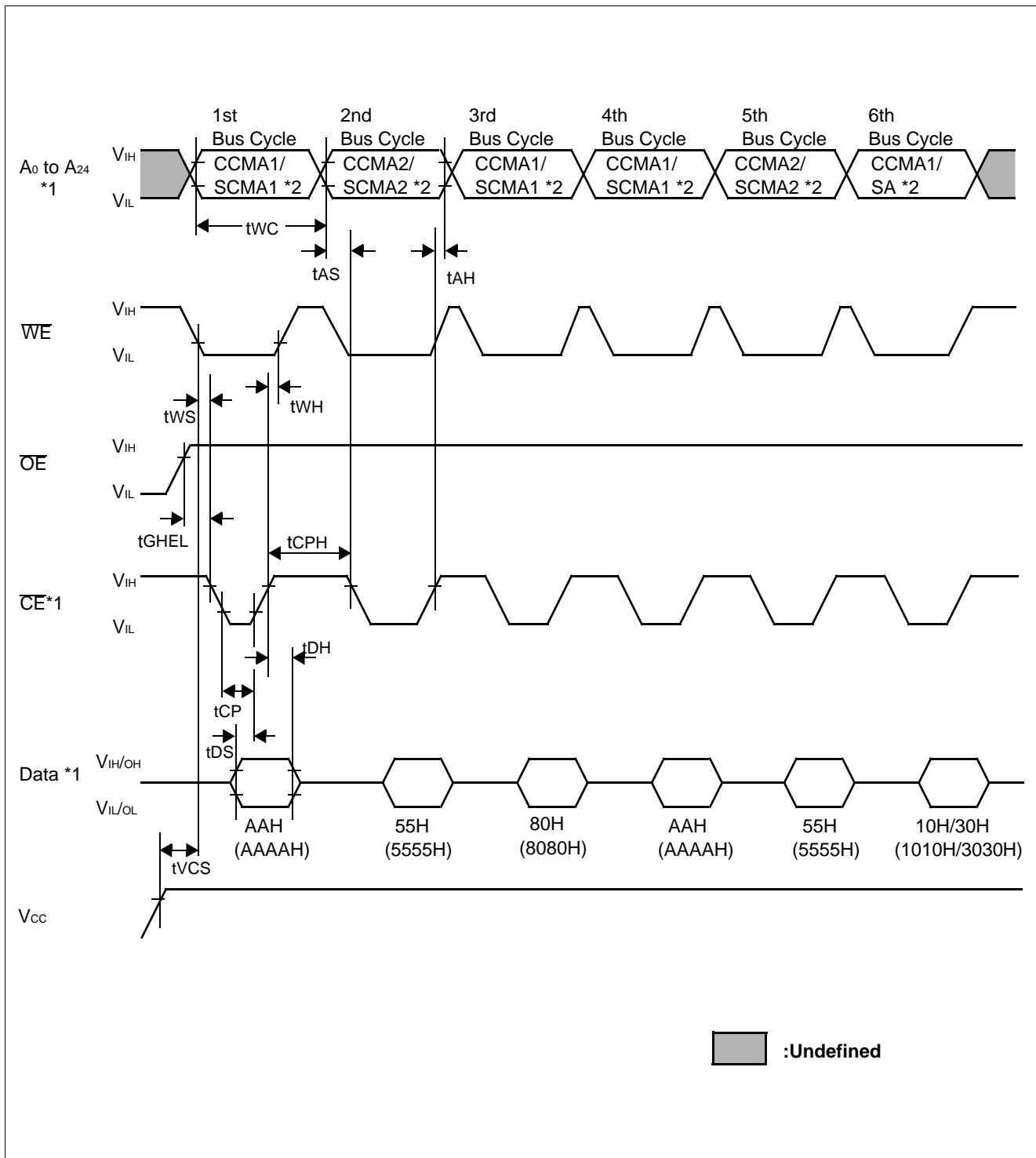
*1 See "FUNCTION TRUTH TABLE".

*2 CCMA1/CCMA2 = Command Address for Chip Erase, SCMA1/SCMA2 = Command Address for Sector Erase, SA = Sector Address. See "COMMAND DEFINITION TABLE".

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■ TIMING DIAGRAM (Continued)

MAIN MEMORY ERASE CYCLE TIMING DIAGRAM (\overline{CE} = CONTROLLED, \overline{REG} = V_{IH})



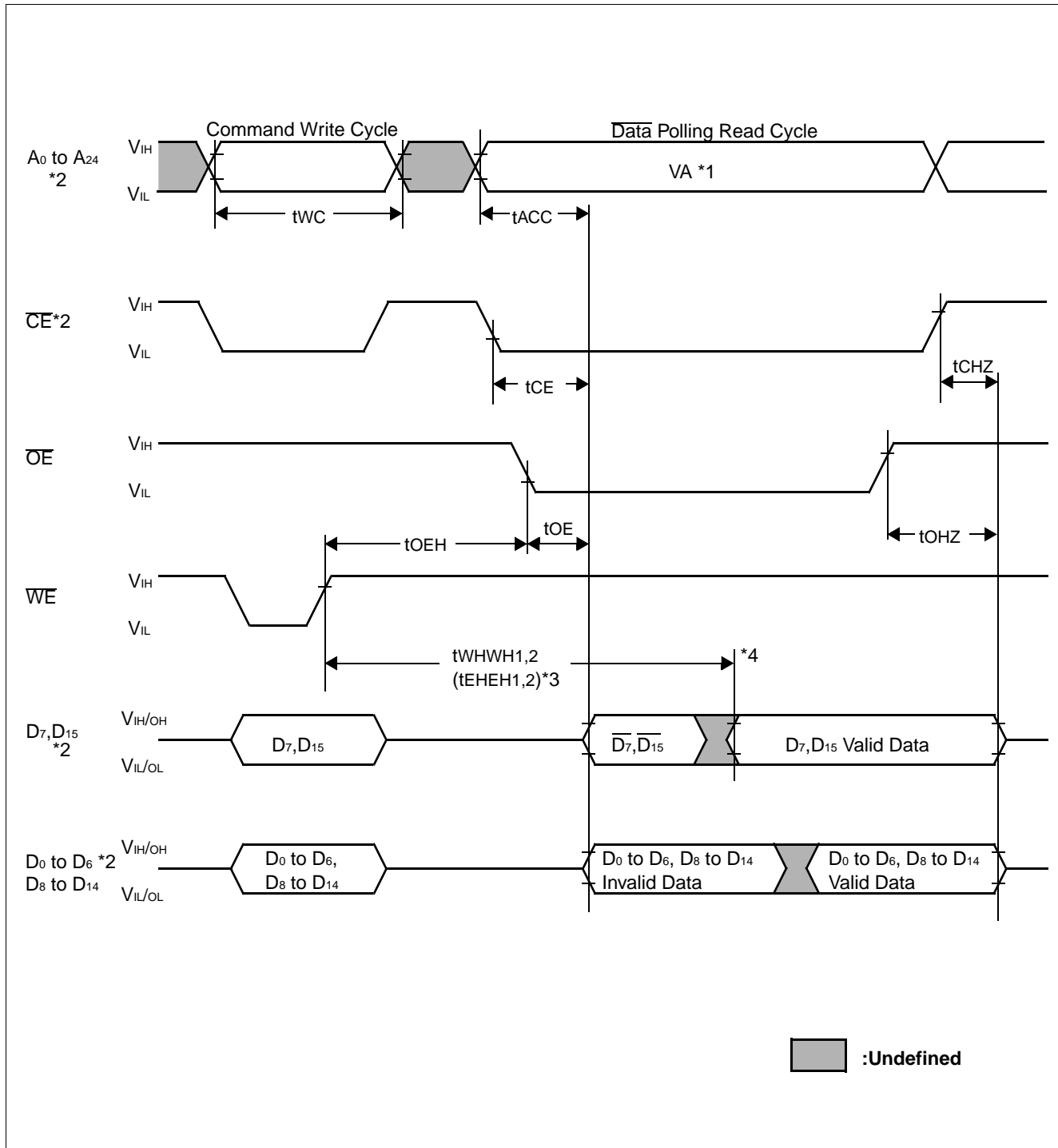
Notes:

*1 See "FUNCTION TRUTH TABLE".

*2 CCMA1/CCMA2 = Command Address for Chip Erase, SCMA1/SCMA2 = Command Address for Sector Erase, SA = Sector Address. See "COMMAND DEFINITION TABLE".

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■ TIMING DIAGRAM (Continued)

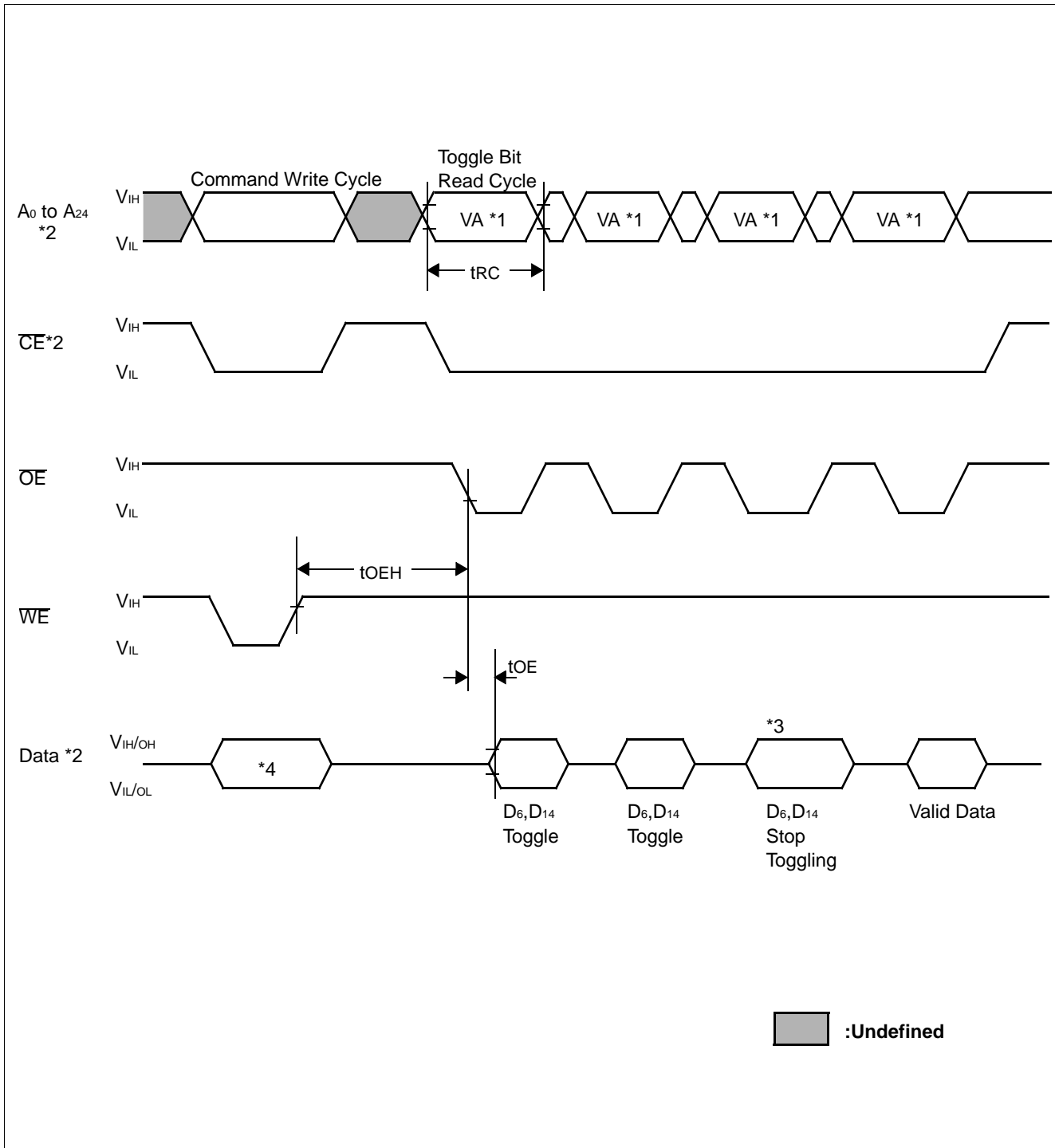
MAIN MEMORY DATA POLLING CYCLE TIMING DIAGRAM ($\overline{\text{REG}} = V_{\text{IH}}$)**Notes:**

- *1 $VA = PA$ for Programming Cycle, $VA = SA$ for Sector Erase, $VA = CA$ for Chip Erase.
- *2 See "FUNCTION TRUTH TABLE".
- *3 $t_{\text{EHEH1, 2}}$ for $\overline{\text{CE}}$ Control.
- *4 Program/Erase operation is finished.

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■ TIMING DIAGRAM (Continued)

MAIN MEMORY TOGGLE BIT TIMING DIAGRAM ($\overline{REG} = V_{IH}$)



Notes:

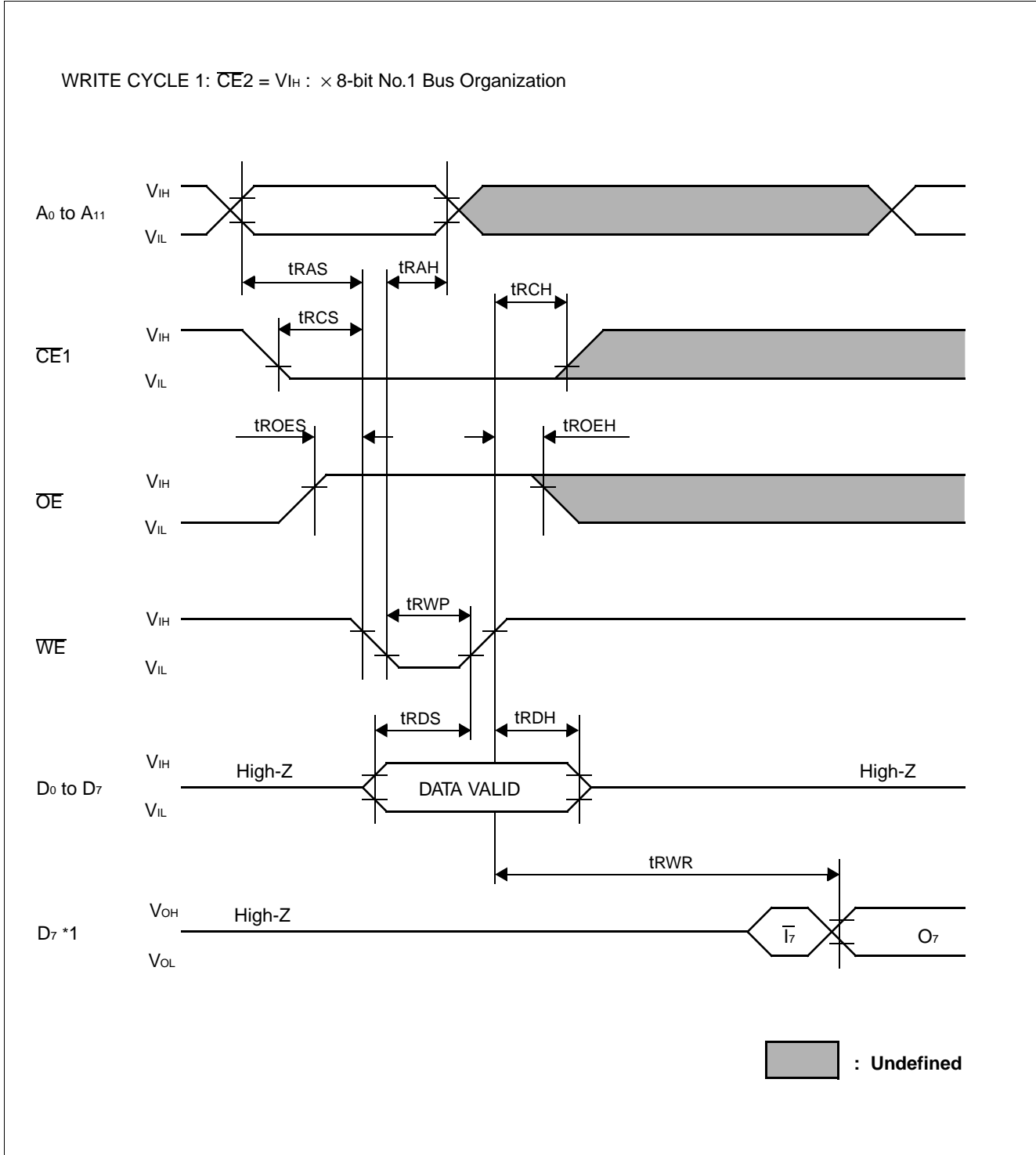
- *1 VA = PA for Programming Cycle, VA = SA for Sector Erase, VA = CA for Chip Erase.
- *2 See "FUNCTION TRUTH TABLE".
- *3 Program/Erase operation is finished.
- *4 PD, 10H (1010H) or 30H (3030H)

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■ AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{WE} = \text{CONTROLLED}$, $\overline{REG} = V_{IL}$)



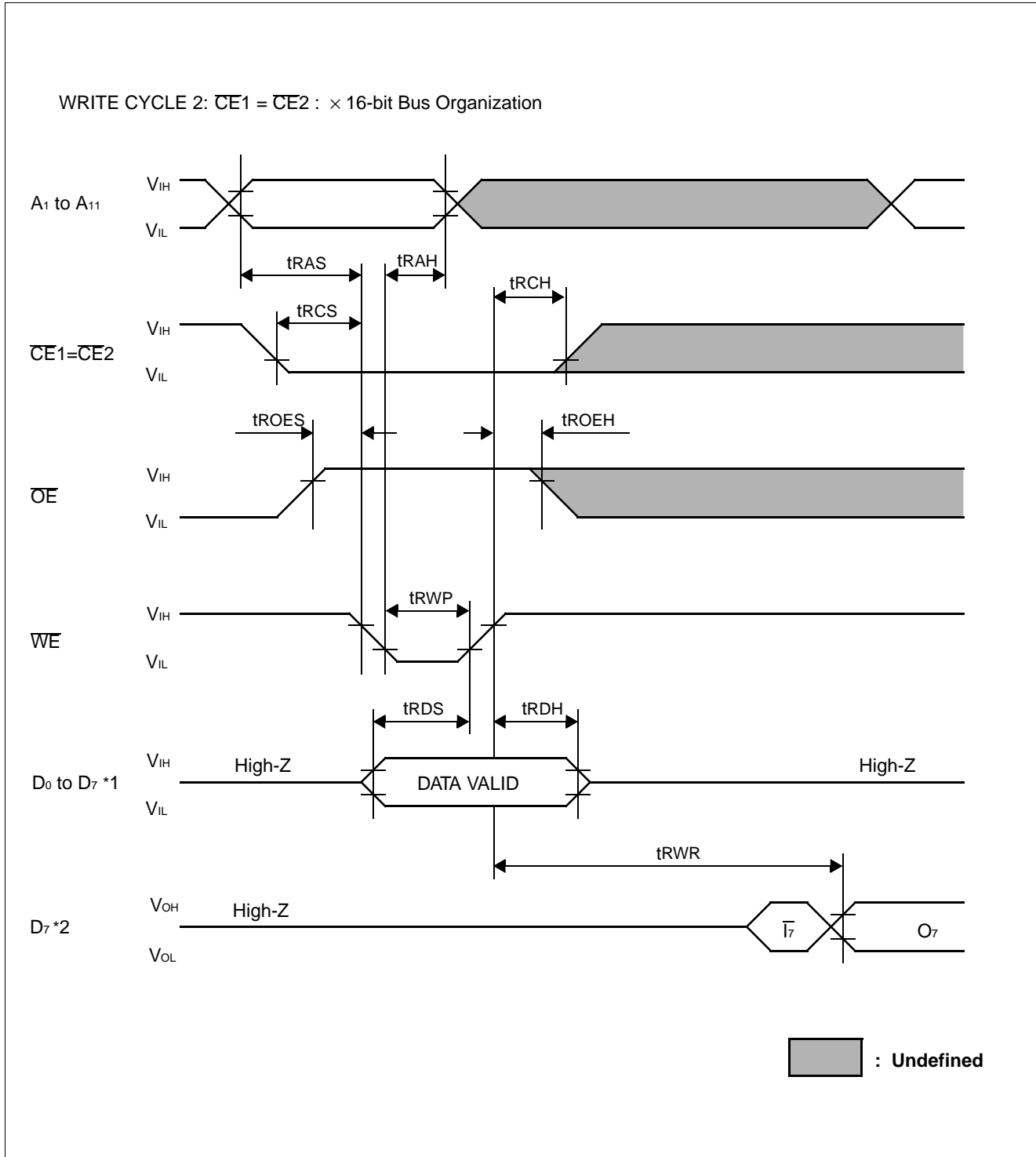
Note:

*1 $\overline{17}$ Data polling operation.

■ AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM (\overline{WE} = CONTROLLED, $\overline{REG} = V_{IL}$)



Notes:

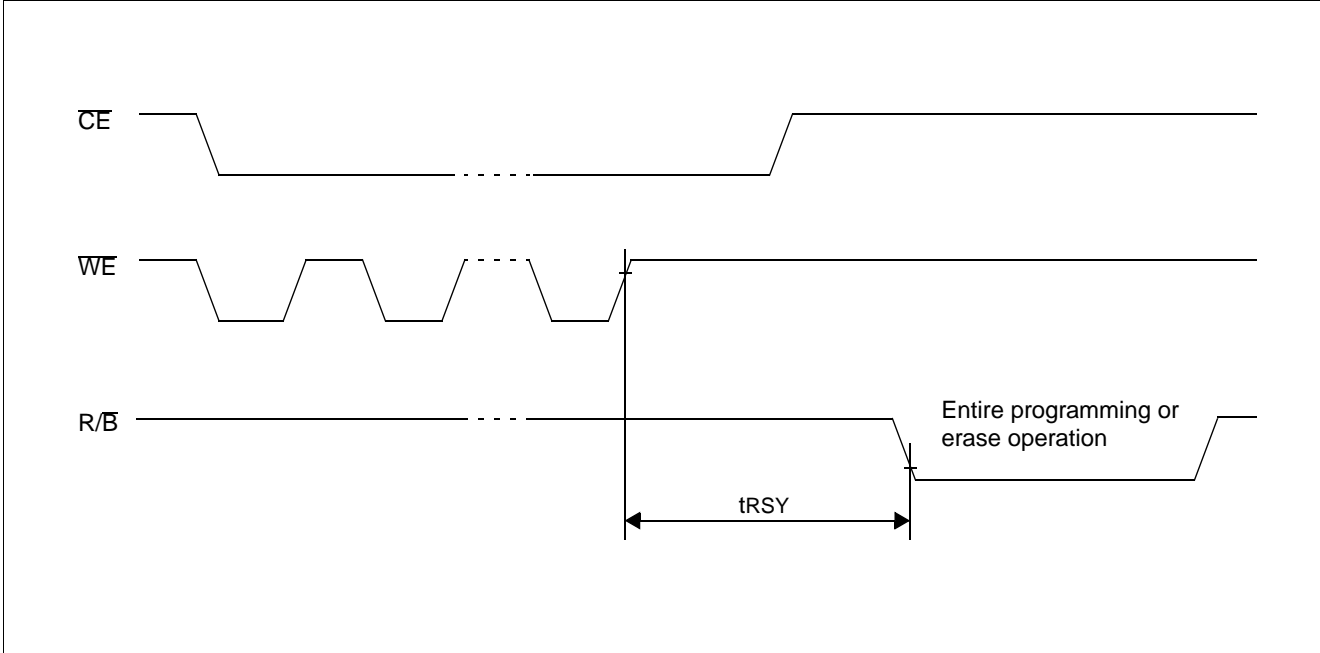
- *1 Inputs from D₈ to D₁₅ are not defined.
- *2 Data polling operation.

MB98A81063-15/81183-15/81273-15/81373-15/81473-15/81573-15

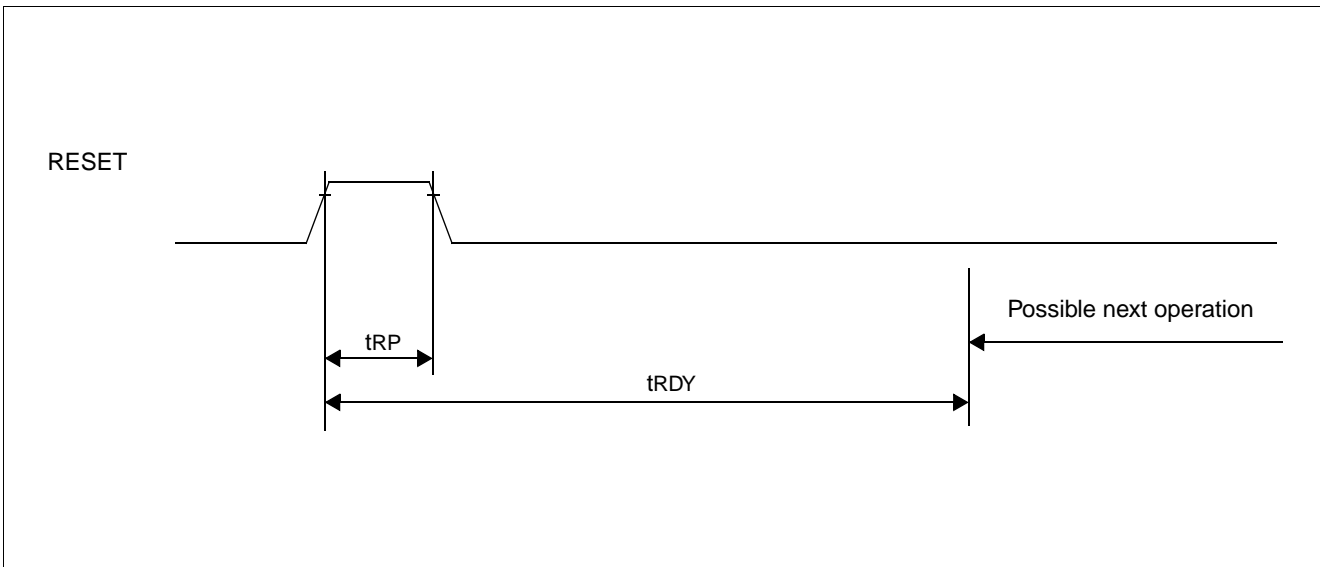
■ AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

R/B Timing Diagram During Program / Erase Operations (except for MB98A81063)



RESET Timing Diagram (except for MB98A81063)

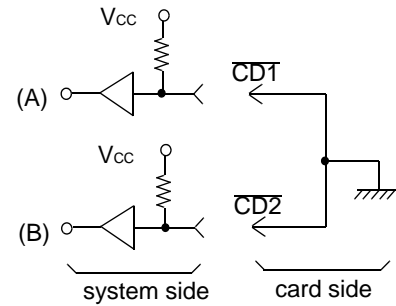


■ UNIQUE FEATURES FOR FLASH MEMORY CARD

1. SPECIAL MONITORING PINS

1.1 CD1, CD2: Card Detection Pins

$\overline{CD1}$ and $\overline{CD2}$ are to detect whether or not the card has been correctly inserted. (See Fig. 12.)
 When the memory card has been correctly inserted, $\overline{CD1}$ and $\overline{CD2}$ are detected by the system. $\overline{CD1}$, $\overline{CD2}$ are tied to ground on the card side as shown in Fig. 12.



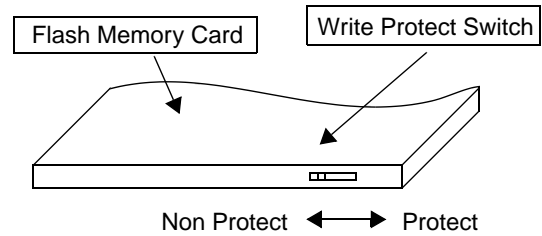
- Fig. 12-

1.2 WP: Write Protect Pins

This pin monitors the position of the Write Protect switch. As shown in Fig. 13, the Flash memory card has a Write Protect switch at the top of the card.

To write to the card, the switch must be turned to the "Non Protect" position and the \overline{WE} pin low. And at that time, L-level is output on the WP pin.

To prevent writing to the card, the switch must be turned to the "Protect" position. At that time, H-level is output on the WP pin.



- Fig. 13 -

| WP Switch | WP (output) |
|-------------|-------------|
| Protect | H |
| Non Protect | L |

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■ CARD INFORMATION

Memory Card have CIS (Card Information Structure) in Attribute memory.

1. CIS

| Address | MB98A81063 | MB98A81183 | MB98A81273 | MB98A81373 | MB98A81473 | MB98A81573 |
|---------|------------|------------|------------|------------|------------|------------|
| 0000 h | 01 h | | | | | |
| 0002 h | 03 h | | | | | |
| 0004 h | 53 h | | | | | |
| 0006 h | 0D h | 1D h | 0E h | 1E h | 3E h | 7E h |
| 0008 h | FF h | | | | | |
| 000A h | 15 h | | | | | |
| 000C h | 1C h | | | | | |
| 000E h | 04 h | | | | | |
| 0010 h | 01 h | | | | | |
| 0012 h | 46 h | | | | | |
| 0014 h | 55 h | | | | | |
| 0016 h | 4A h | | | | | |
| 0018 h | 49 h | | | | | |
| 001A h | 54 h | | | | | |
| 001C h | 53 h | | | | | |
| 001E h | 55 h | | | | | |
| 0020 h | 00 h | | | | | |
| 0022 h | 4D h | | | | | |
| 0024 h | 42 h | | | | | |
| 0026 h | 39 h | | | | | |
| 0028 h | 38 h | | | | | |
| 002A h | 41 h | | | | | |
| 002C h | 38 h | | | | | |
| 002E h | 30 h | | | | | |
| 0030 h | 30 h | | | | | |
| 0032 h | 36 h | 38 h | 37 h | | | |
| 0034 h | 33 h | | | | | |
| 0036 h | 73 h | | | | | |
| 0038 h | 65 h | | | | | |
| 003A h | 72 h | | | | | |
| 003C h | 69 h | | | | | |

(Continued)

MB98A81063-15/81183-15/81273-15/81373-15/81473-15/81573-15

(Continued)

| Address | MB98A81063 | MB98A81183 | MB98A81273 | MB98A81373 | MB98A81473 | MB98A81573 |
|---------|------------|------------|------------|------------|------------|------------|
| 003E h | | | | | | 65 h |
| 0040 h | | | | | | 73 h |
| 0042 h | | | | | | 00 h |
| 0044 h | | | | | | FF h |
| 0046 h | | | | | | 17 h |
| 0048 h | | | | | | 03 h |
| 004A h | | | | | | 41 h |
| 004C h | | | | | | 01 h |
| 004E h | | | | | | FF h |
| | | | | | | |
| 0050 h | | | | | | 18 h |
| 0052 h | | | | | | 03 h |
| 0054 h | | | | | | 04 h |
| 0056 h | A4 h | D5 h | | | | 3D h |
| 0058 h | | | | | | FF h |
| | | | | | | |
| 005A h | | | | | | 1E h |
| 005C h | | | | | | 07 h |
| 005E h | | | | | | 02 h |
| 0060 h | | | | | | 11 h |
| 0062 h | | | | | | 01 h |
| 0064 h | | | | | | 01 h |
| 0066 h | | | | | | 01 h |
| 0068 h | | | | | | 01 h |
| 006A h | | | | | | FF h |
| | | | | | | |
| 006C h | | | | | | 10 h |
| 006E h | | | | | | 06 h |
| 0070 h | | | | | | CA h |
| 0072 h | | | | | | FF h |
| 0074 h | | | | | | 3C h |
| 0076 h | | | | | | 00 h |
| 0078 h | 02 h | 45 h | 9D h | AD h | CD h | 0D h |
| 007A h | | | | | | FF h |
| | | | | | | |
| 007C h | | | | | | FF h |

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2. Explanation for CIS

| Address | MB98A81573 | Attribute |
|---------|------------|---|
| 0000 h | 01 h | Common memory device information tuple |
| 0002 h | 03 h | Link to next tuple |
| 0004 h | 53 h | Flash memory with 150 ns access time |
| 0006 h | 7E h | 32MB device size |
| 0008 h | FF h | End of list |
| | | |
| 000A h | 15 h | Level 1 version/product - information tuple |
| 000C h | 1C h | Link to next tuple |
| 000E h | 04 h | Conformed to JEIDA Ver.4.2/PCMCIA 2.1 |
| 0010 h | 01 h | |
| 0012 h | 46 h | Product/Maker Information for "FUJITSU MB98A80070 series" |
| 0014 h | 55 h | |
| 0016 h | 4A h | |
| 0018 h | 49 h | |
| 001A h | 54 h | |
| 001C h | 53 h | |
| 001E h | 55 h | |
| 0020 h | 00 h | |
| 0022 h | 4D h | |
| 0024 h | 42 h | |
| 0026 h | 39 h | |
| 0028 h | 38 h | |
| 002A h | 41 h | |
| 002C h | 38 h | |
| 002E h | 30 h | |
| 0030 h | 30 h | |
| 0032 h | 37 h | |
| 0034 h | 33 h | |
| 0036 h | 73 h | |
| 0038 h | 65 h | |
| 003A h | 72 h | |
| 003C h | 69 h | |
| 003E h | 65 h | |
| 0040 h | 73 h | |

(Continued)

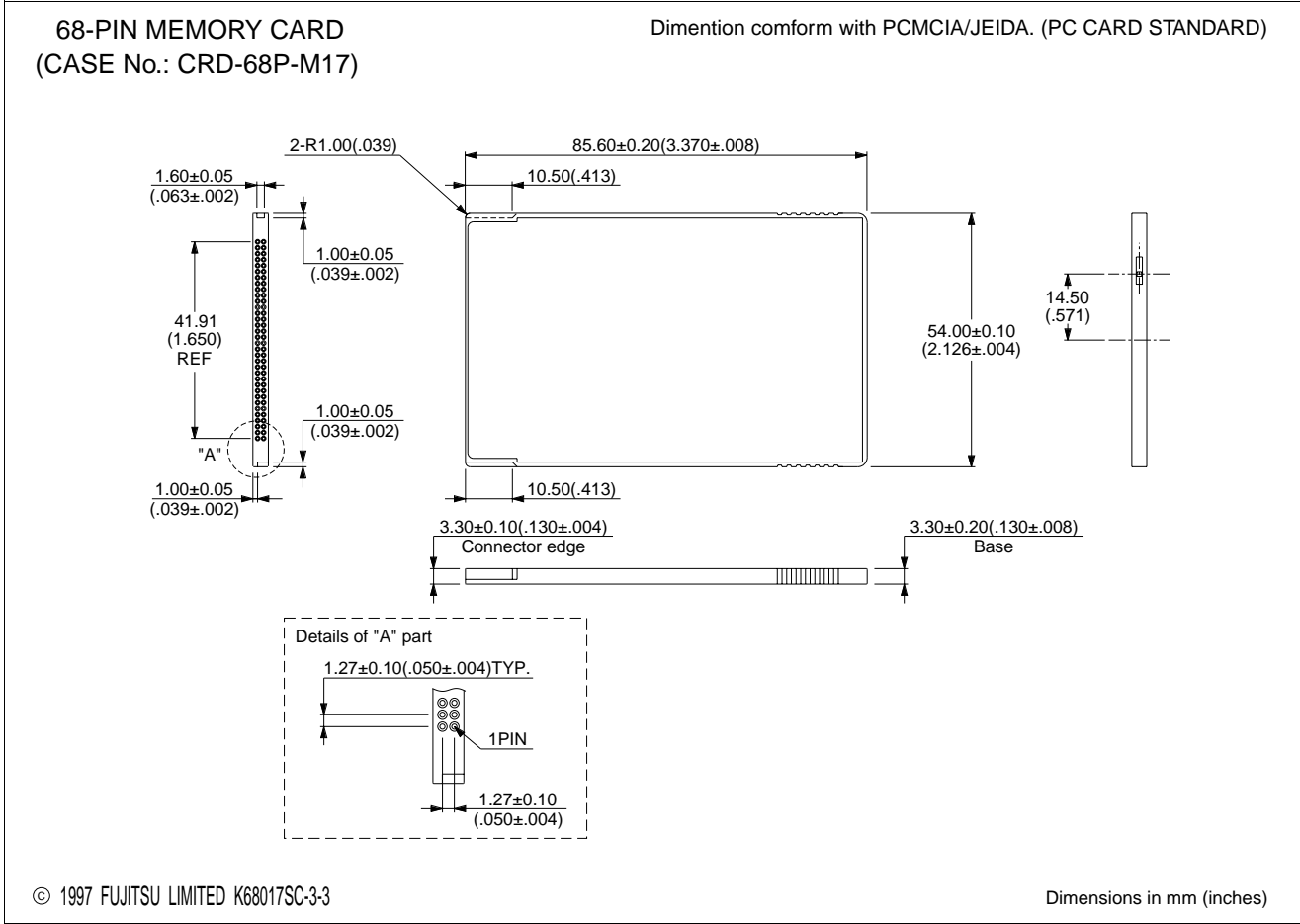
MB98A81063-15/81183-15/81273-15/81373-15/81473-15/81573-15

(Continued)

| Address | MB98A81573 | Attribute |
|---------|------------|--|
| 0042 h | 00 h | |
| 0044 h | FF h | End of list |
| 0046 h | 17 h | Attribute memory device information tuple |
| 0048 h | 03 h | Link to next tuple |
| 004A h | 41 h | EEPROM with 250 ns access time |
| 004C h | 01 h | 2 KB device size |
| 004E h | FF h | End of list |
| | | |
| 0050 h | 18 h | JEDEC device ID tuple for common memory |
| 0052 h | 03 h | Link to next tuple |
| 0054 h | 04 h | Manufacture ID |
| 0056 h | 3D h | Device ID |
| 0058 h | FF h | End of list |
| | | |
| 005A h | 1E h | Device geometry information for common memory device tuple |
| 005C h | 07 h | Link to next tuple |
| 005E h | 02 h | System bus width is 2 Bytes |
| 0060 h | 11 h | Erase block size is 64 KBytes |
| 0062 h | 01 h | Read block size is 1 Byte |
| 0064 h | 01 h | Program block size is 1 Byte |
| 0066 h | 01 h | No special partitioning requirements |
| 0068 h | 01 h | Non interleaved |
| 006A h | FF h | End of list |
| | | |
| 006C h | 10 h | Checksum tuple |
| 006E h | 06 h | Link to next tuple |
| 0070 h | CA h | Offset to checksum area |
| 0072 h | FF h | |
| 0074 h | 3C h | Length of check |
| 0076 h | 00 h | |
| 0078 h | 0D h | Checksum |
| 007A h | FF h | End of list |
| | | |
| 007C h | FF h | The end of chain tuple |

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PACKAGE DIMENSIONS



FUJITSU LIMITED

For further information please contact:

Japan

FUJITSU LIMITED
Corporate Global Business Support Division
Electronic Devices
KAWASAKI PLANT, 4-1-1, Kamikodanaka
Nakahara-ku, Kawasaki-shi
Kanagawa 211-8588, Japan
Tel: 81(44) 754-3763
Fax: 81(44) 754-3329

<http://www.fujitsu.co.jp/>

North and South America

FUJITSU MICROELECTRONICS, INC.
Semiconductor Division
3545 North First Street
San Jose, CA 95134-1804, USA
Tel: (408) 922-9000
Fax: (408) 922-9179

Customer Response Center
Mon. - Fri.: 7 am - 5 pm (PST)
Tel: (800) 866-8608
Fax: (408) 922-9179

<http://www.fujitsumicro.com/>

Europe

FUJITSU MIKROELEKTRONIK GmbH
Am Siebenstein 6-10
D-63303 Dreieich-Buchsschlag
Germany
Tel: (06103) 690-0
Fax: (06103) 690-122

<http://www.fujitsu-edc.com/>

Asia Pacific

FUJITSU MICROELECTRONICS ASIA PTE LTD
#05-08, 151 Lorong Chuan
New Tech Park
Singapore 556741
Tel: (65) 281-0770
Fax: (65) 281-0220

<http://www.fmap.com.sg/>

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