

*MEMORY*

CMOS

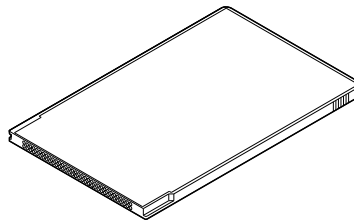
**MASK ROM CARD****PCMCIA Rel.2/JEIDA Ver.4 conformable****MB98A51121/51221/51321/51421/51521-17****MASK ROM CARD 2 M/4 M/8 M/16 M/32 M-BYTE****DESCRIPTION**

This card is a PCMCIA and JEIDA-compliant 68-pin two-piece Mask ROM card with the 16-bit mask ROM being installed on the common memory.

However, to use this card as PCMCIA Rel.2, JEIDA Ver.4, the card attribute information has to be stored in the Mask ROM.

**FEATURES**

- External dimensions: 85.6 mm × 54.0 mm × 3.3 mm
- +5 V single power supply
- Usable in 8 bits × 16 bits configuration
- Complete static operation
- I/O level TTL compatible
- Output tri-state
- Complete capacitive load without pull-up resistor or pull-down resistor except  $\overline{CE}_1$  and  $\overline{CE}_2$ .
- 68-pin two-piece connector form

**PACKAGE**

(CRD-68P-M04)

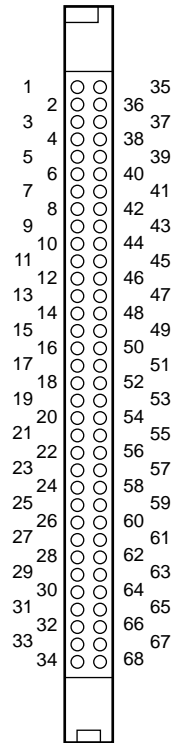
**MB98A51121/51221/51321/51421/51521-17****■ PRODUCT CLASS**

Part Number	Memory Device	Memory Configuration (word × bit)	Access Time (ns) (max.)
MB98A51121	16-Mbit Mask ROM ×1 pcs	2 M × 8/1 M × 16	170
MB98A51221	16-Mbit Mask ROM × 2 pcs	4 M × 8/2 M × 16	
MB98A51321	16-Mbit Mask ROM × 4 pcs	8 M × 8/4 M × 16	
MB98A51421	16-Mbit Mask ROM × 8 pcs	16 M × 8/8 M × 16	
MB98A51521	16-Mbit Mask ROM × 16 pcs	32 M × 8/16 M × 16	

## MB98A51121/51221/51321/51421/51521-17

## ■ PIN ASSIGNMENTS

(CONNECTOR SIDE)



(CRD-68P-M02)

## • Pin Name

Symbol	I/O	Pin Name
A <sub>0</sub> to A <sub>25</sub>	I	Address input
D <sub>0</sub> to D <sub>15</sub>	I/O	Data I/O
$\overline{CE}_1, \overline{CE}_2$	I	Card enable
$\overline{CD}_1, \overline{CD}_2$ *	O	Card detection
$\overline{VS}_1, \overline{VS}_2$	O	Voltage sense
$\overline{REG}$	I	Attribute memory space select
$\overline{OE}$	I	Output enable
$\overline{WE}$	I	Write enable
BVD1, BVD2 *	O	Battery voltage detection
WP *	O	Write protect
V <sub>cc</sub>	—	Supply voltage (+5 V)
GND	—	Ground
N.C.	—	No connection

\* : Those pins are internally connected; use care when handling.

Pin No.	Symbol	Pin No.	Symbol
1	GND	35	GND
2	D <sub>3</sub>	36	$\overline{CD}_1$
3	D <sub>4</sub>	37	D <sub>11</sub>
4	D <sub>5</sub>	38	D <sub>12</sub>
5	D <sub>6</sub>	39	D <sub>13</sub>
6	D <sub>7</sub>	40	D <sub>14</sub>
7	$\overline{CE}_1$	41	D <sub>15</sub>
8	A <sub>10</sub>	42	$\overline{CE}_2$
9	$\overline{OE}$	43	$\overline{VS}_1$ *
10	A <sub>11</sub>	44	N.C.
11	A <sub>9</sub>	45	N.C.
12	A <sub>8</sub>	46	A <sub>17</sub>
13	A <sub>13</sub>	47	A <sub>18</sub>
14	A <sub>14</sub>	48	A <sub>19</sub> *
15	$\overline{WE}/N.C.$ *	49	A <sub>20</sub> *
16	N.C.	50	A <sub>21}/N.C. *</sub>
17	V <sub>cc</sub>	51	V <sub>cc</sub>
18	N.C.	52	N.C.
19	A <sub>16</sub>	53	A <sub>22}/N.C. *</sub>
20	A <sub>15</sub>	54	A <sub>23}/N.C. *</sub>
21	A <sub>12</sub>	55	A <sub>24}/N.C. *</sub>
22	A <sub>7</sub>	56	A <sub>25}/N.C. *</sub>
23	A <sub>6</sub>	57	$\overline{VS}_2$ *
24	A <sub>5</sub>	58	N.C.
25	A <sub>4</sub>	59	N.C.
26	A <sub>3</sub>	60	N.C.
27	A <sub>2</sub>	61	$\overline{REG}/N.C.$ *
28	A <sub>1</sub>	62	BVD2
29	A <sub>0</sub>	63	BVD1
30	D <sub>0</sub>	64	D <sub>8</sub>
31	D <sub>1</sub>	65	D <sub>9</sub>
32	D <sub>2</sub>	66	D <sub>10</sub>
33	WP	67	$\overline{CD}_2$
34	GND	68	GND

\* : Whether a pin is an address pin or N.C. pin depends on the type of the models. See ■ DIFFERENCE OF PIN FUNCTIONS.

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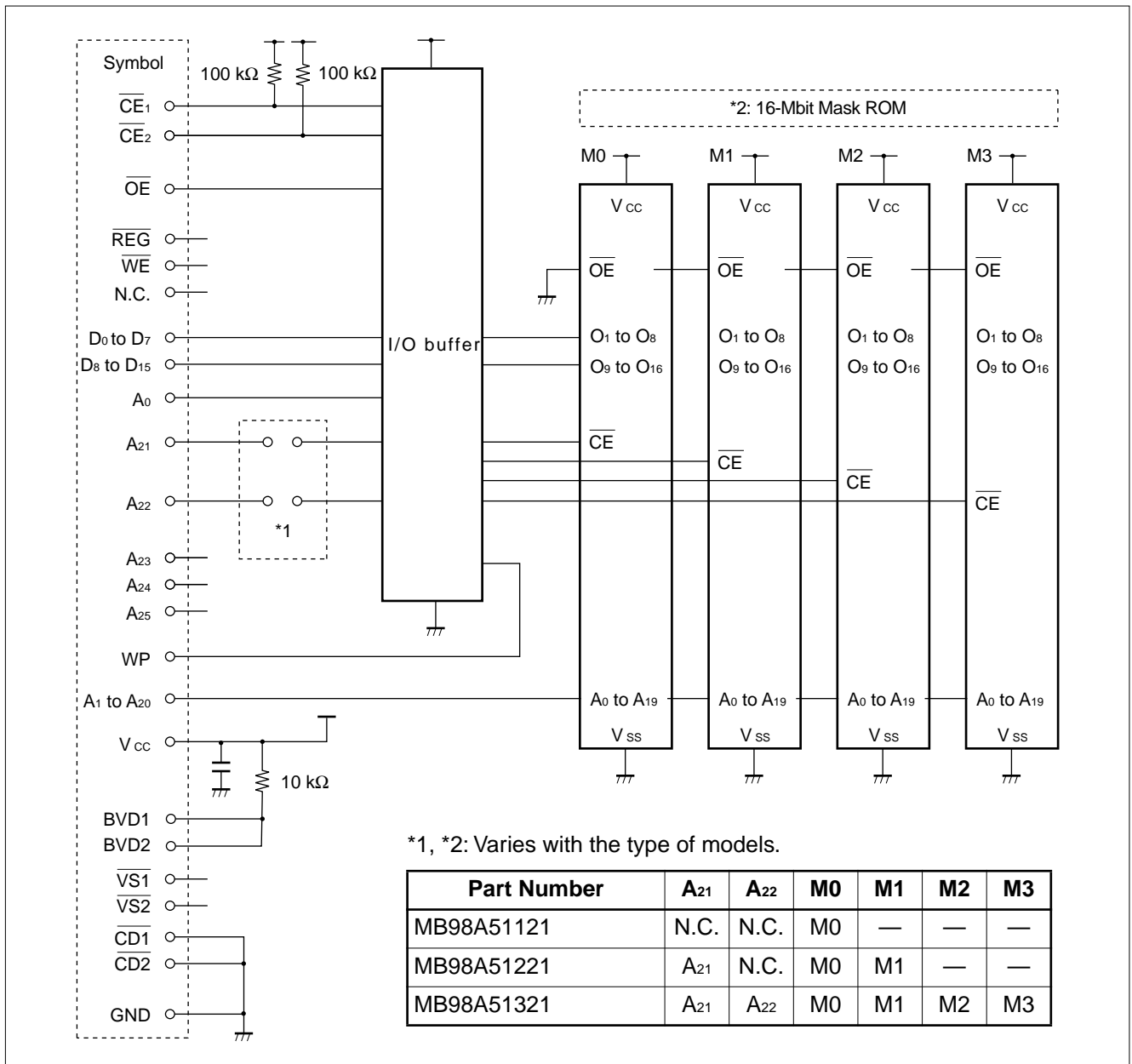
## ■ DIFFERENCE OF PIN FUNCTIONS

Part Name	A <sub>21</sub>	A <sub>22</sub>	A <sub>23</sub>	A <sub>24</sub>	A <sub>25</sub>	REG	WE	VS <sub>1</sub>	VS <sub>2</sub>
MB98A51121	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
MB98A51221									
MB98A51321									
MB98A51421									
MB98A51521									
	A <sub>21</sub>	A <sub>22</sub>	A <sub>23</sub>	A <sub>24</sub>					

# MB98A51121/51221/51321/51421/51521-17

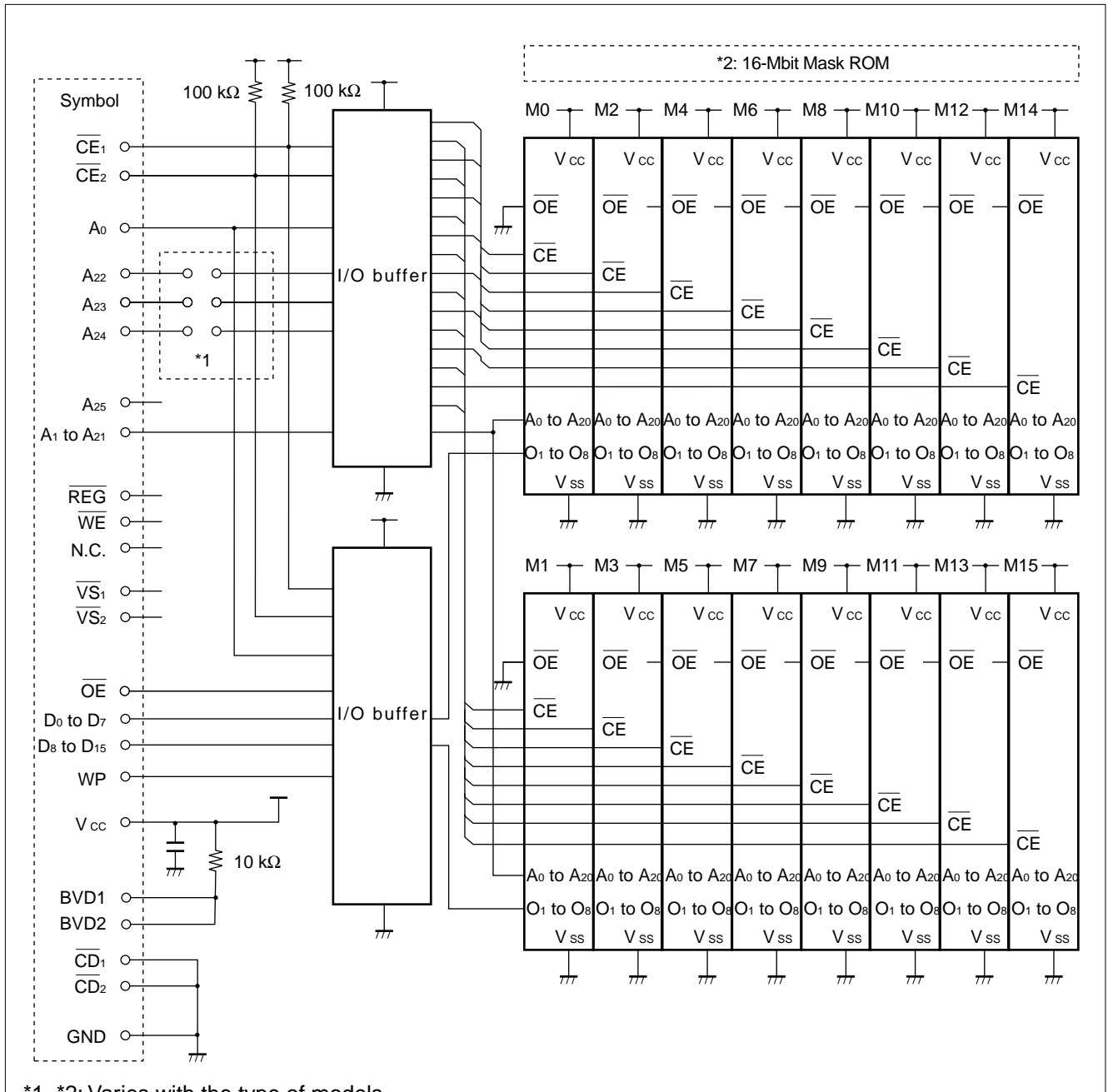
## ■ BLOCK DIAGRAM

### 1. 16-Mbit Mask ROM × 1/× 2/× 4 Being Mounted



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## 2. 16-Mbit Mask ROM × 8/× 16



\*1, \*2: Varies with the type of models.

Part Number	A22	A23	A24	M0/1	M2/3	M4/5	M6/7	M8/9	M10/11	M12/13	M14/15
MB98A51421	A22	A23	N.C.	M0/1	M2/3	M4/5	M6/7	—	—	—	—
MB98A51521	A22	A23	A24	M0/1	M2/3	M4/5	M6/7	M8/9	M10/11	M12/13	M14/15

# MB98A51121/51221/51321/51421/51521-17

## ■ FUNCTIONAL TRUTH TABLE

$\overline{CE}_2$	$\overline{CE}_1$	$A_0$ (BYTE)	$\overline{OE}$	Operating Mode	Output Pin (D <sub>8</sub> to D <sub>15</sub> )	Output Pin (D <sub>0</sub> to D <sub>7</sub> )
H	H	×	×	Standby	High-impedance	High-impedance
×	×	×	H	Output disable	High-impedance	High-impedance
H	L	L	L	Read (× 8 bit)	High-impedance	Output data (even bytes)
H	L	H	L	Read (× 8 bit)	High-impedance	Output data (odd bytes)
L	H	×	L	Read (× 8 bit)	Output data (odd bytes)	High-impedance
L	L	×	L	Read (× 16 bit)	Output data (odd bytes)	Output data (even bytes)

H: High level, L: Low level, ×: Don't care

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## ■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Value		Unit
		Max.	Min.	
Supply Voltage *	$V_{CC}$	-0.3	+6.0	V
Input Voltage *	$V_{IN}$	-0.3	$V_{CC} + 0.3$	V
Output Voltage *	$V_{OUT}$	-0.3	$V_{CC} + 0.3$	V
Ambient Temperature	$T_A$	-10	+60	°C
Storage Temperature	$T_{stg}$	-30	+70	°C

\* : The voltage values are with reference to GND = 0 V.

**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply Voltage *	$V_{CC}$	4.75	5.0	5.25	V
	GND	—	0	—	V
High Level Input Voltage *	$V_{IH}$	2.4	—	$V_{CC} + 0.3$	V
Low Level Input Voltage *	$V_{IL}$	-0.3	—	0.8	V
Ambient Temperature	$T_A$	0	—	+55	°C

\* : The voltage values are with reference to the GND = 0 V.

**WARNING:** Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.



## MB98A51121/51221/51321/51421/51521-17

## ■ ELECTRICAL CHARACTERISTICS

### 1. DC Characteristics

(On the recommended conditions)

Parameter	Notes	Symbol	Test Conditions	Value			Unit
				Min.	Typ.	Max.	
Standby Supply Current		$I_{SB1}$	$\overline{CE}_1, \overline{CE}_2 \geq V_{CC} - 0.2 V$ $I_{OUT} = 0 mA$	—	10	1600	$\mu A$
		$I_{SB2}$	$\overline{CE}_1, \overline{CE}_2 = V_{IH}$ $I_{OUT} = 0 mA$	—	—	10	mA
Averaging Operation Supply Current		$I_{CC}$	Cycle = min. Duty cycle = 100% $I_{OUT} = 0 mA, \overline{OE} = V_{IH}$ $V_{IN} = V_{IH}$ or $V_{IL}$	—	—	220	mA
Input Leak Current	*1	$I_{LI}$	$V_{IN} = 0 V$ to $V_{CC}$	-40	$\pm 0.1$	40	$\mu A$
Output Leak Current	*2	$I_{LO}$	$V_{OUT} = 0 V$ to $V_{CC}$ , $\overline{CE}_1, \overline{CE}_2 = V_{IH}$ or $\overline{OE} = V_{IH}$	-10	—	10	$\mu A$
High Level Output Voltage	*2	$V_{OH}$	$I_{OH} = -1 mA$	2.4	—	—	V
Low Level Output Voltage	*2	$V_{OL}$	$I_{OL} = 2.1 mA$	—	—	0.4	V

**Notes:** \*1. Excluding  $\overline{CE}_1$  and  $\overline{CE}_2$  pins.

\*2. Excluding WP, BVD1, BVD2,  $\overline{CD}_1$  and  $\overline{CD}_2$  pins.

### 2. AC Characteristics

#### (1) Common Memory read cycle

(On the recommended conditions)

Parameter	Notes	Symbol	Test Conditions	Value		Unit
				Min.	Max.	
Read Cycle Time		$t_{RC}$	—	170	—	ns
Address Cycle Time		$t_{ACC}$	$\overline{CE}_X = V_{IH}, V_{IL}$ $\overline{OE} = V_{IL}$	—	170	ns
Card Enable Access Time		$t_{CE}$	$\overline{OE} = V_{IL}$	—	170	ns
Output Enable Access Time	*1	$t_{OE}$	$\overline{CE}_X = V_{IH}, V_{IL}$	—	75	ns
Output Disable Time	*2	$t_{DF}$	—	—	60	ns
Output Hold Time		$t_{OH}$	$\overline{CE}_X = V_{IH}, V_{IL}$ $\overline{OE} = V_{IL}$	0	—	ns

**Notes:** \*1. The maximum delay of  $\overline{OE}$  is  $t_{ACC} - t_{OE}$  within the ranges in which the  $t_{ACC}$  is not affected.

\*2.  $t_{DF}$  is determined by either  $\overline{CE}_X$  or  $\overline{OE}$ , whichever is faster with rise time.

The decision level is determined by the time the output is in a high-impedance state.

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## 3. Input/output Terminal Capacitance

( $V_{IN}, V_{OUT} = GND, f = 1 \text{ MHz}, T_A = +25^\circ\text{C}$ )

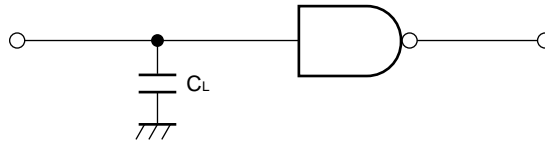
Parameter	Notes	Symbol	Value		Unit
			Min.	Max.	
Input Terminal Capacitance	*1	$C_{IN}$	—	75	pF
Output Terminal Capacitance	*2	$C_{I/O}$	—	50	pF

**Notes:** \*1. Excluding  $\overline{CE}_1$  and  $\overline{CE}_2$  pins.  
 \*2. Excluding WP, BVD1, BVD2,  $\overline{CD}_1$ , and  $\overline{CD}_2$  pins.

## 4. AC Characteristics Test Conditions

Input voltage		: $V_{IH} = 2.6 \text{ V}, V_{IL} = 0.6 \text{ V}$
Input pulse rise time, fall time		: $t_r, t_f = 5 \text{ ns} (0.8 \text{ V to } 2.4 \text{ V})$
Timing measurement reference voltage	: Input	: $V_{IH} = 2.4 \text{ V}$
	: Output	: $V_{OH} = 2.2 \text{ V}$
		: $V_{OL} = 0.8 \text{ V}$
Output load		: 1TTL + $C_L (100 \text{ pF})$

### • Output load circuit

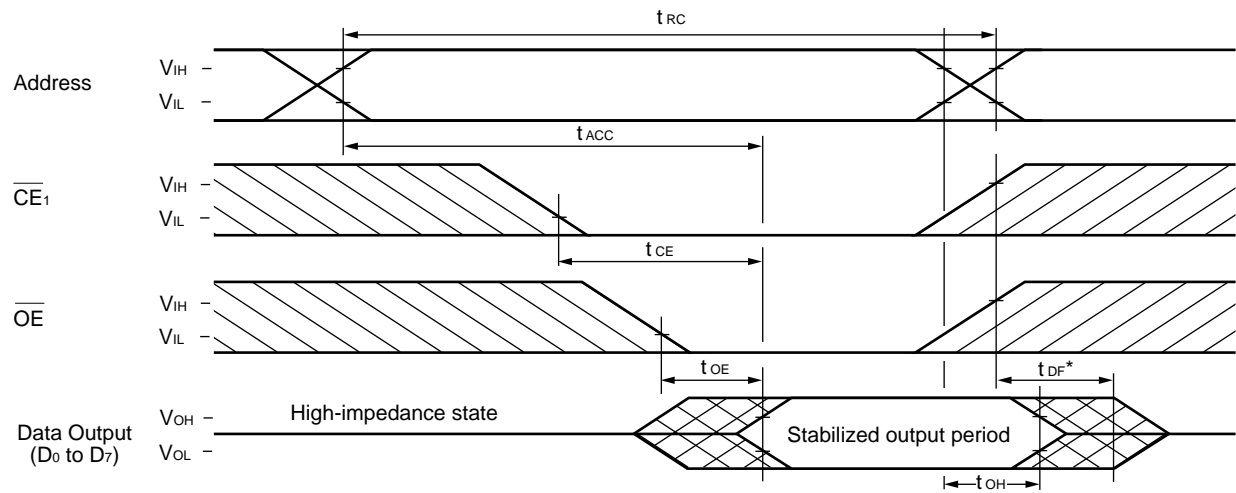


# MB98A51121/51221/51321/51421/51521-17

## ■ TIMING DIAGRAM

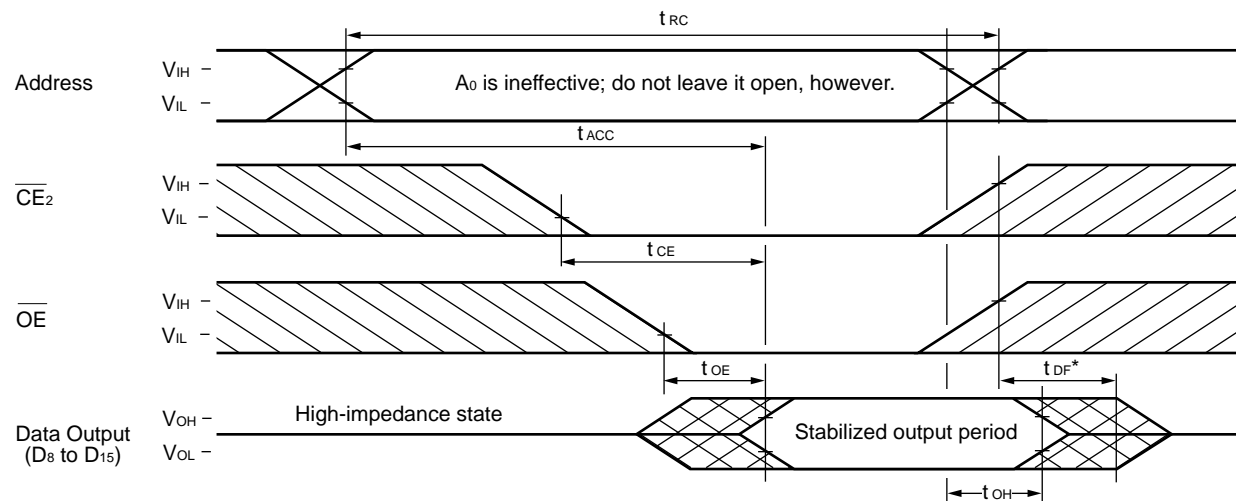
### 1. Common Memory Read Cycle

× 8 bit ( $\overline{CE}_2 = V_{IH}$ )



\*:  $t_{DF}$  is determined by either  $\overline{OE}$  or  $\overline{CE}_1$ , whichever is faster with rise time.  
The decision level is determined by the time the output is in a high-impedance state.

× 8 bit ( $\overline{CE}_1 = V_{IH}$ )

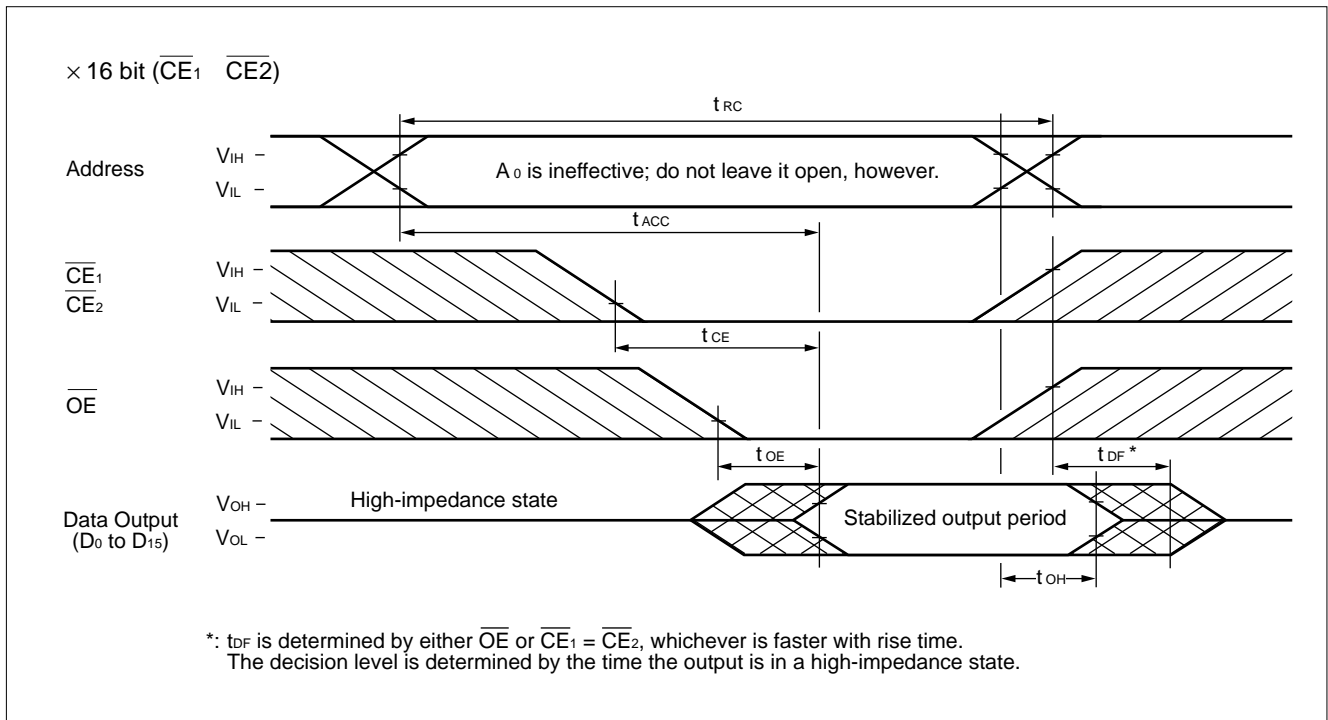


\*:  $t_{DF}$  is determined by either  $\overline{OE}$  or  $\overline{CE}_2$ , whichever is faster with rise time.  
The decision level is determined by the time the output is in a high-impedance state.

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## MB98A51121/51221/51321/51421/51521-17

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# MB98A51121/51221/51321/51421/51521-17

## ■ DATA RELEASE METHOD

Data release is accepted by the 8-Mbit EPROM (1 Mword × 8 bits).

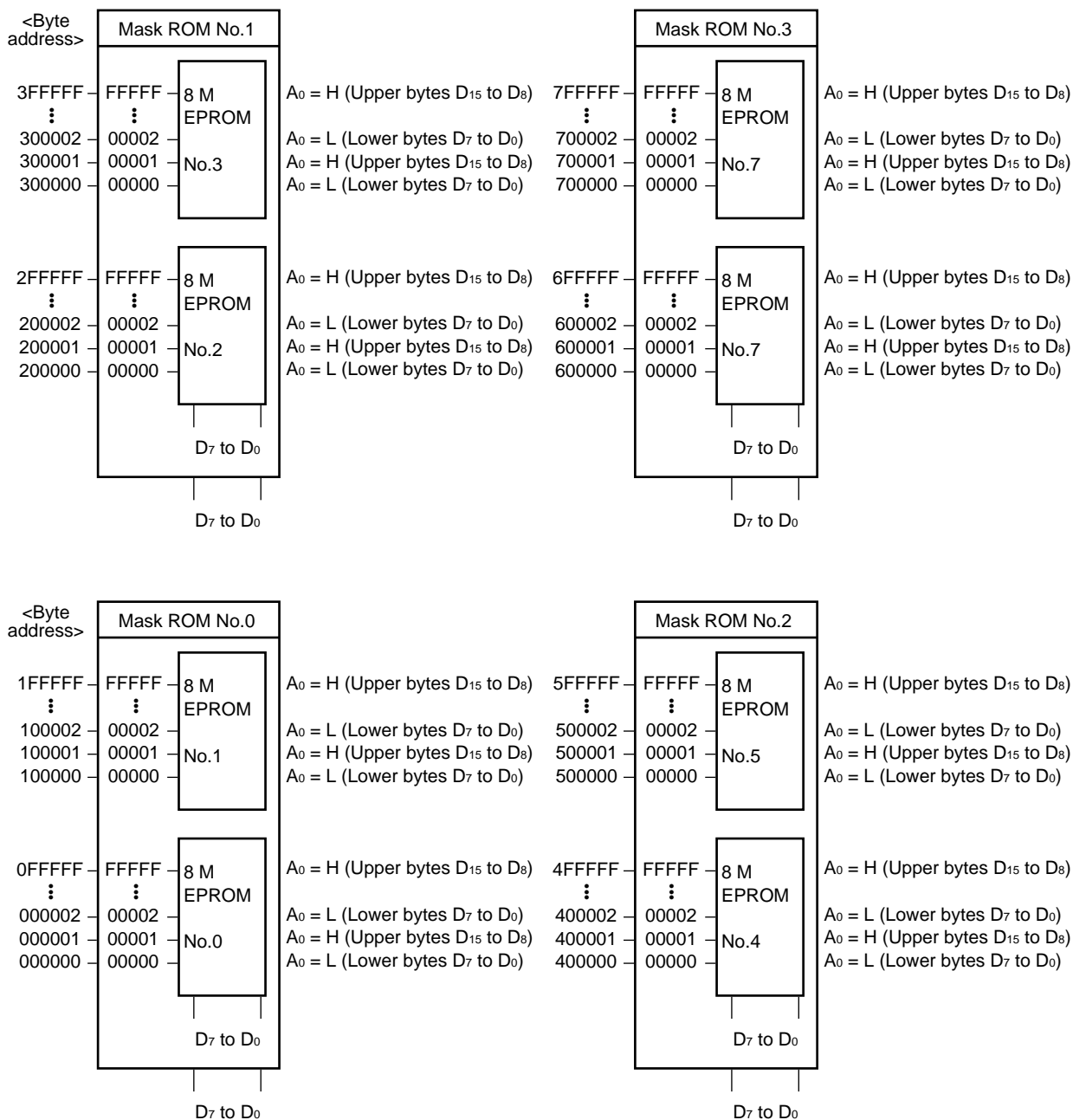
To prevent erroneous writing of data, provide three samples per piece of data. Also indicate the card memory address for writing.

- Mapping between release data EPROM address and memory card address (16 Mbit Mask ROM × 1/ × 2/ × 4 being mounted)

The range of the address for the MB98A51121 is 000000 to 1FFFFFF (2 Mbytes).

The range of the address for the MB98A51221 is 000000 to 3FFFFFF (4 Mbytes).

The range of the address for the MB98A51321 is 000000 to 7FFFFFF (8 Mbytes).

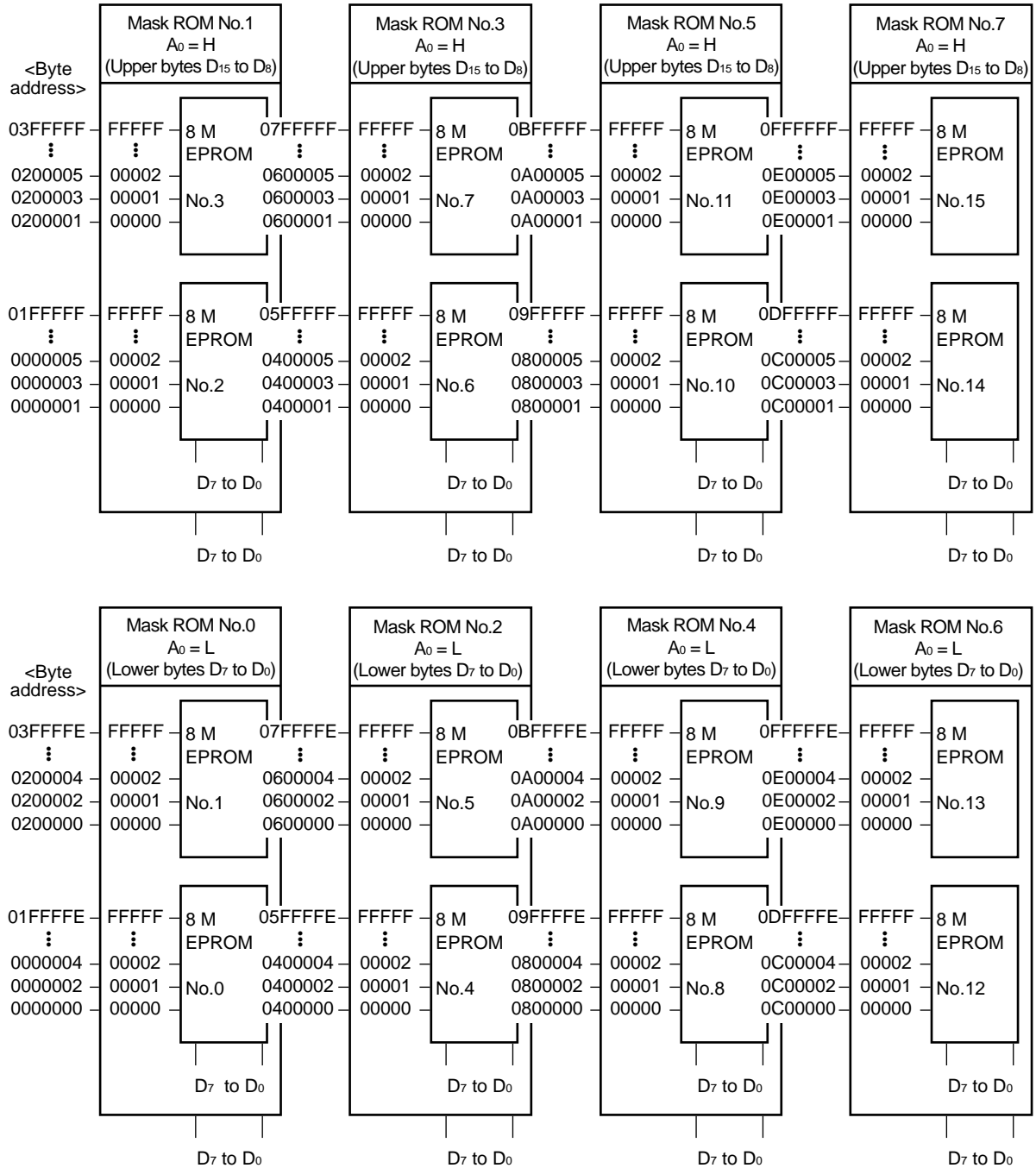


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# MB98A51121/51221/51321/51421/51521-17

- Mapping between release data EPROM address and memory card address (16 Mbit Mask ROM × 8/× 16 being mounted)

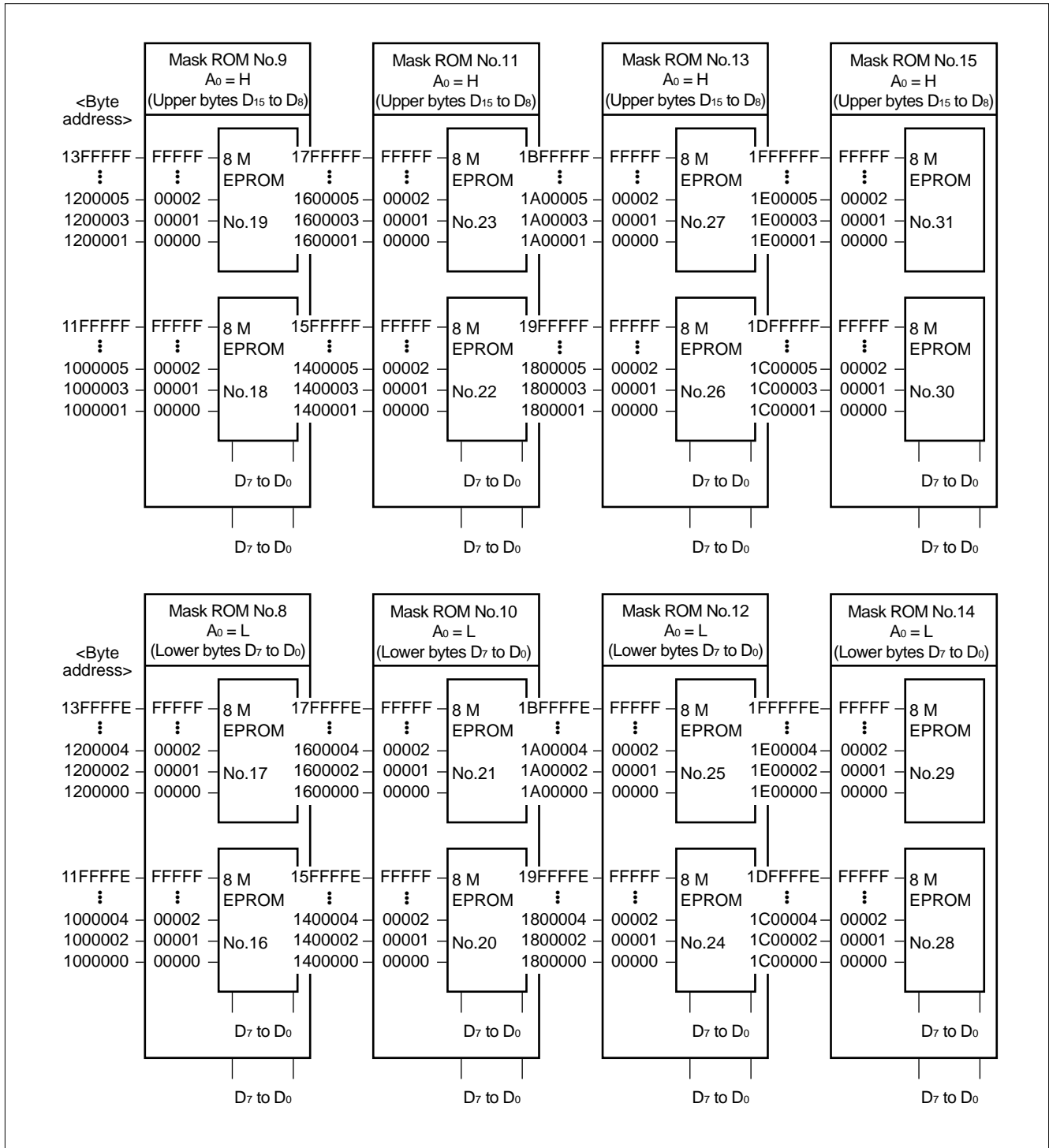
The range of the address for the MB98A51421 is 000000 to FFFFFFFF (16 Mbytes).  
 The range of the address for the MB98A51521 is 0000000 to 1FFFFFFF (32 Mbytes)



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# MB98A51121/51221/51321/51421/51521-17

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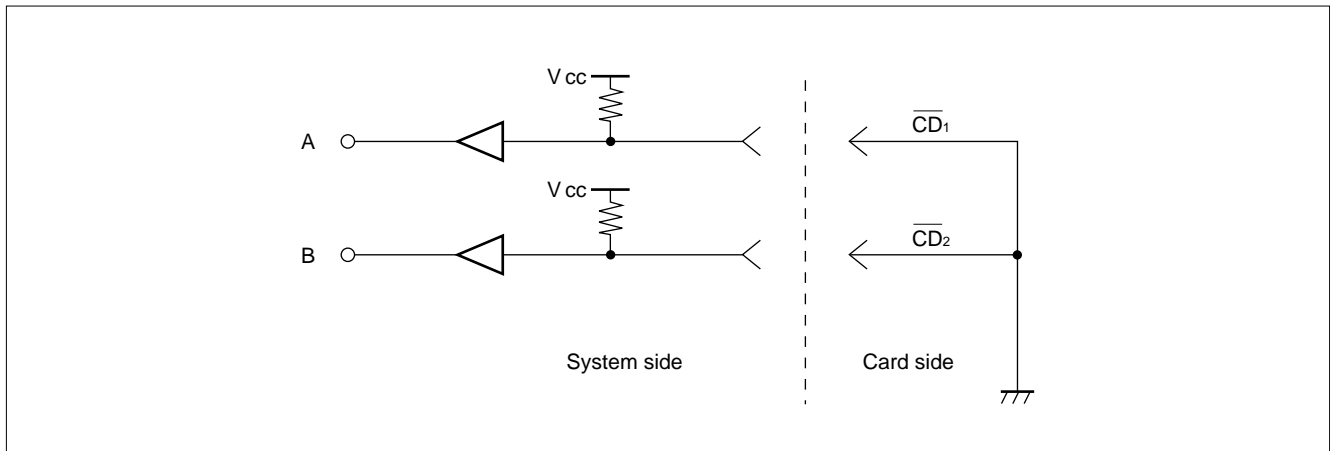
# MB98A51121/51221/51321/51421/51521-17

## ■ AUXILIARY CAPABILITIES

### 1. Card Detection Pins ( $\overline{CD}_1$ , $\overline{CD}_2$ )

These pins verify a card is correctly inserted into the system.

The two pins are internally connected to the ground; with the system side connection being pulled up to the  $V_{CC}$ , detection of the voltage of these pins allows the system to check the state of connectivity of a card (See the diagram below).



### 2. Write Protection Pin (WP)

The Mask ROM Card, whose common memory is write-protected, outputs a high-level write-protection signal.



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## ■ DEVICE HANDLING PRECAUTIONS

The device is composed of fine electronic parts, so take care in handling or keeping it as below.

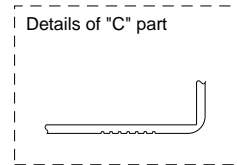
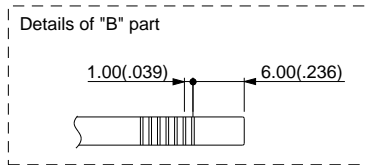
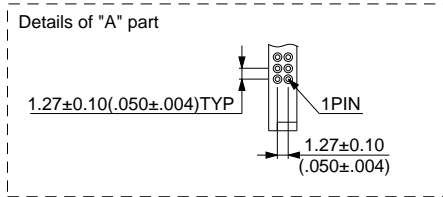
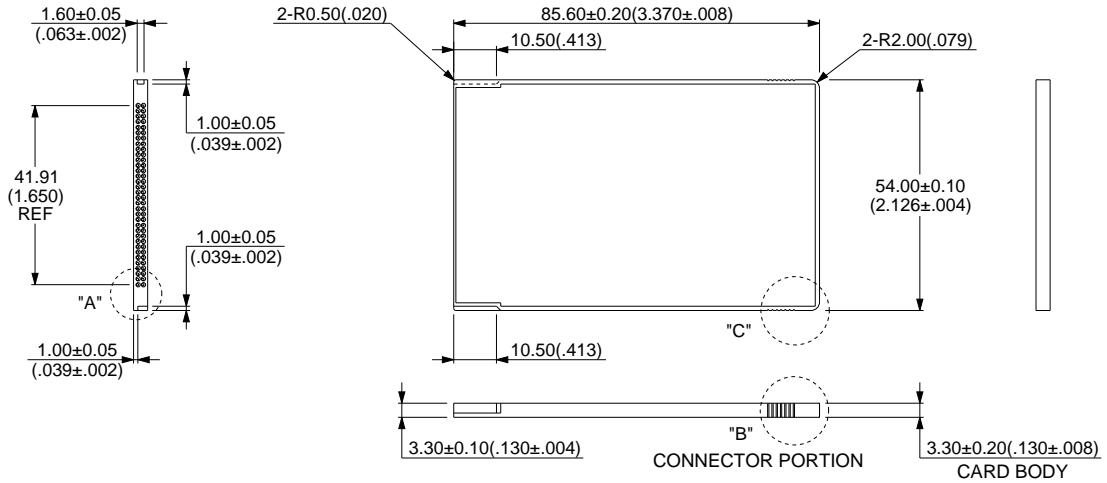
- The card is made fine, so do not keep it in the high temperature nor high humidity, place line in the direct sunshine nor near the heater.
- The card should not be bent, scratched, dropped nor be shocked violently.
- This device should never be taken a part. It could destroy the card or your personal computer hardware.
- To help you handle this device safely, request us the device specifications when purchasing this device.

# MB98A51121/51221/51321/51421/51521-17

## ■ PACKAGE DIMENSIONS

68-pin Memory Card  
(CRD-68P-M02)

Note: Dimensions conform with PCMCIA/JEIDA



# FUJITSU LIMITED

*For further information please contact:*

## **Japan**

FUJITSU LIMITED  
Corporate Global Business Support Division  
Electronic Devices  
KAWASAKI PLANT, 4-1-1, Kamikodanaka  
Nakahara-ku, Kawasaki-shi  
Kanagawa 211-88, Japan  
Tel: (044) 754-3763  
Fax: (044) 754-3329

## **North and South America**

FUJITSU MICROELECTRONICS, INC.  
Semiconductor Division  
3545 North First Street  
San Jose, CA 95134-1804, U.S.A.  
Tel: (408) 922-9000  
Fax: (408) 432-9044/9045

## **Europe**

FUJITSU MIKROELEKTRONIK GmbH  
Am Siebenstein 6-10  
63303 Dreieich-Buchsschlag  
Germany  
Tel: (06103) 690-0  
Fax: (06103) 690-122

## **Asia Pacific**

FUJITSU MICROELECTRONICS ASIA PTE. LIMITED  
#05-08, 151 Lorong Chuan  
New Tech Park  
Singapore 556741  
Tel: (65) 281-0770  
Fax: (65) 281-0220

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