

16-bit Proprietary Microcontroller

CMOS

F²MC-16F MB90220 Series

MB90223/224/P224A/W224A
MB90P224B/W224B/V220

■ OUTLINE

The MB90220 series of general-purpose high-performance 16-bit microcontrollers has been developed primarily for applications that demand high-speed real-time processing and is suited for industrial applications, office automation equipment, process control, and other applications. The F²MC-16F CPU is based on the F²MC*-16 Family with improved high-level language support functions and task switching functions, as well as additional addressing modes.

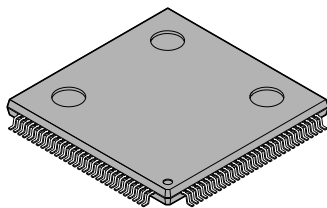
On-chip peripheral resources include a 4-channel PWC timer, a 4-channel ICU (Input Capture Unit), a 1-channel 24-bit timer counter, an 8-channel OCU (Output Compare Unit), a 6-channel 16-bit reload timer, a 2-channel 16-bit PPG timer, a 10-bit A/D converter with 16 inputs, and a 4-channel serial port with a UART function (one channel includes the CTS function).

The MB90P224B, MB90W224B, MB90224 is under development.

*: F²MC stands for FUJITSU Flexible Microcontroller.

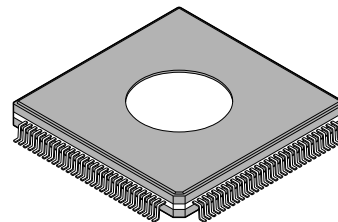
■ PACKAGE

120-pin Plastic QFP



(FPT-120P-M03)

120-pin Ceramic QFP



(FPT-120C-C02)

MB90220 Series

■ FEATURES

F²MC-16F CPU

- Minimum execution time: 62.5 ns/16 MHz oscillation (using a duty control system)
- Instruction sets optimized for controllers
 - Upward object-compatible with the F²MC-16(H)
 - Various data types (bit, byte, word, and long-word)
 - Instruction cycle improved to speed up operation
 - Extended addressing modes: 25 types
 - High coding efficiency
 - Access method (bank access with linear pointer)
 - Enhanced multiplication and division instructions (with signed instructions added)
 - Higher-precision operation using a 32-bit accumulator
- Extended intelligent I/O service (automatic transfer function independent of instructions)
 - Access area expanded to 64 Kbytes
- Enhanced instruction set applicable to high-level language (C) and multitasking
 - System stack pointer
 - Enhanced pointer-indirect instructions
 - Barrel shift instruction
 - Stack check function
- Increased execution speed: 8-byte instruction queue
- Powerful interrupt functions: 8 levels and 28 sources

Peripheral resources

- Mask ROM : 64 Kbytes (MB90223)
96 Kbytes (MB90224)
- EPROM : 96 Kbytes (MB90W224A/W224B)
- One-time PROM : 96 Kbytes (MB90P224A/P224B)
- RAM: 3 Kbytes (MB90223)
4.5 Kbytes (MB90224/MB90W224A/P224A/W224B/P224B)
5 Kbytes (MB90V220)
- General-purpose ports: max. 102 channels
- ICU (Input Capture Unit): 4 channels
- 24-bit timer counter: 1 channel
- OCU (Output Compare Unit): 8 channels
- PWC timer with time measurement function: 4 channels
- 10-bit A/D converter: 16 channels
- UART: 4 channels (one channel includes CTS function)
- 16-bit reload timer
 - Toggled output, external clock, and gate functions: 6 channels
- 16-bit PPG timer: 2 channels
- DTP/External-interrupt inputs: 8 channels (of which five have edge detection function only)
- Write-inhibit RAM: 0.5 Kbytes (1 Kbyte for MB90V220)
- Timebase counter: 18 bits
- Clock gear function
- Low-power consumption mode
 - Sleep mode
 - Stop mode
 - Hardware standby mode

MB90220 Series

Product description

- MB90223/224 are mask ROM product.
- MB90P224A/P224B are one-time PROM products.
- MB90W224A/W224B are EPROM products. ES only.
- Operating temperature of MB90P224A/W224A is -40°C to $+85^{\circ}\text{C}$.
(However, the AC characteristics is assured in -40°C to $+70^{\circ}\text{C}$)
- Operation clock cycle of MB90223 is 10 MHz to 12 MHz.
- MB90V220 is a evaluation device for the program development. ES only.

■ PRODUCT LINEUP

| Part number Item | MB90223 | MB90224 | MB90P224A MB90P224B | MB90W224A MB90W224B | MB90V220 |
|------------------------------|--|------------------|------------------------|------------------------|-------------------|
| Classification | Mask ROM product | Mask ROM product | One-time PROM product | EPROM product | Evaluation device |
| ROM size | 64 Kbytes | 96 Kbytes | 96 Kbytes | 96 Kbytes | None |
| RAM size | 3 Kbytes | 4.5 Kbytes | 4.5 Kbytes | 4.5 Kbytes | 5 Kbytes |
| CPU functions | The number of instructions: 412 Instruction bit length: 8 or 16 bits Instruction length: 1 to 7 bytes Data bit length: 1, 4, 8, 16, or 32 bits Minimum execution time: 62.5 ns/16 MHz Interrupt processing time: 1.0 μs /16 MHz (min.) | | | | |
| Ports | I/O ports (N-ch open-drain): 16 I/O ports (CMOS): 86 Total: 102 | | | | |
| ICU (Input Capture Unit) | Number of channels: 4 Rising edge/falling edge/both edges selectable | | | | |
| 24-bit timer counter | Number of channels: 1 Overflow interrupt, intermediate bit interrupt | | | | |
| OCU (Output Compare Unit) | Number of channels: 8 Pin change source (match signal causes register value transfer/general-purpose port) | | | | |
| PWC timer | Number of channels: 4 16-bit reload timer operation (operation clock cycle: 0.25 μs to 1.31 ms) 16-bit pulse-width count operation (Allowing continuous/one-shot measurement, H/L width measurement, inter-edge measurement, and divided-frequency measurement) | | | | |
| 10-bit A/D converter | Resolution: 10 bits Number of inputs: 16 Single conversion mode (conversion of each channel) Scan conversion mode (continuous conversion for up to 16 consecutive channels) Continuous conversion mode (repeated conversion of specified channel) Stop conversion mode (conversion every fixed cycle) | | | | |
| UART | Number of channels: 4 (1 channel with CTS function) Clock-synchronous transfer mode (full-duplex double buffering, 7 to 9-bit data length, 2400 to 62500 bps) Asynchronous transfer mode (full-duplex double buffering, 7 to 9-bit data length, 2400 to 62500 bps) | | | | |
| 16-bit reload timer | Number of channels: 6 16-bit reload timer operation (operation clock cycle: 0.25 μs to 1.05 s) | | | | |

(Continued)

MB90220 Series

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| Part number Item | MB90223 | MB90224 | MB90P224A MB90P224B | MB90W224A MB90W224B | MB90V220 |
|-------------------------|--|---------|------------------------|------------------------|--------------|
| 16-bit PPG timer | Number of channels: 2 16-bit PPG operation (operation clock cycle: 0.25 μ s to 6 s) | | | | |
| DTP/External interrupts | Number of inputs: 8 (of which five have edge detection function only) External interrupt mode (allowing interrupts to activate at four different request levels) Simple DMA transfer mode (allowing extended I ² O/S to activate at two different request levels) | | | | |
| Write-inhibited RAM | RAM size: 512 bytes (1 Kbyte for MB90V220) RAM write-protectable with \overline{WI} pin | | | | |
| Standby mode | stop mode (activated by software or hardware) and sleep mode | | | | |
| Gear function | Machine clock operation frequency switching: 16 MHz, 8 MHz, 4 MHz, 1 MHz (at 16-MHz oscillation) | | | | |
| Package | FPT-120P-M03 | | | FPT-120C-C02 | PGA-256C-A02 |

Note: MB90V220 is a evaluation device, therefore, the electrical characteristics are not assured.

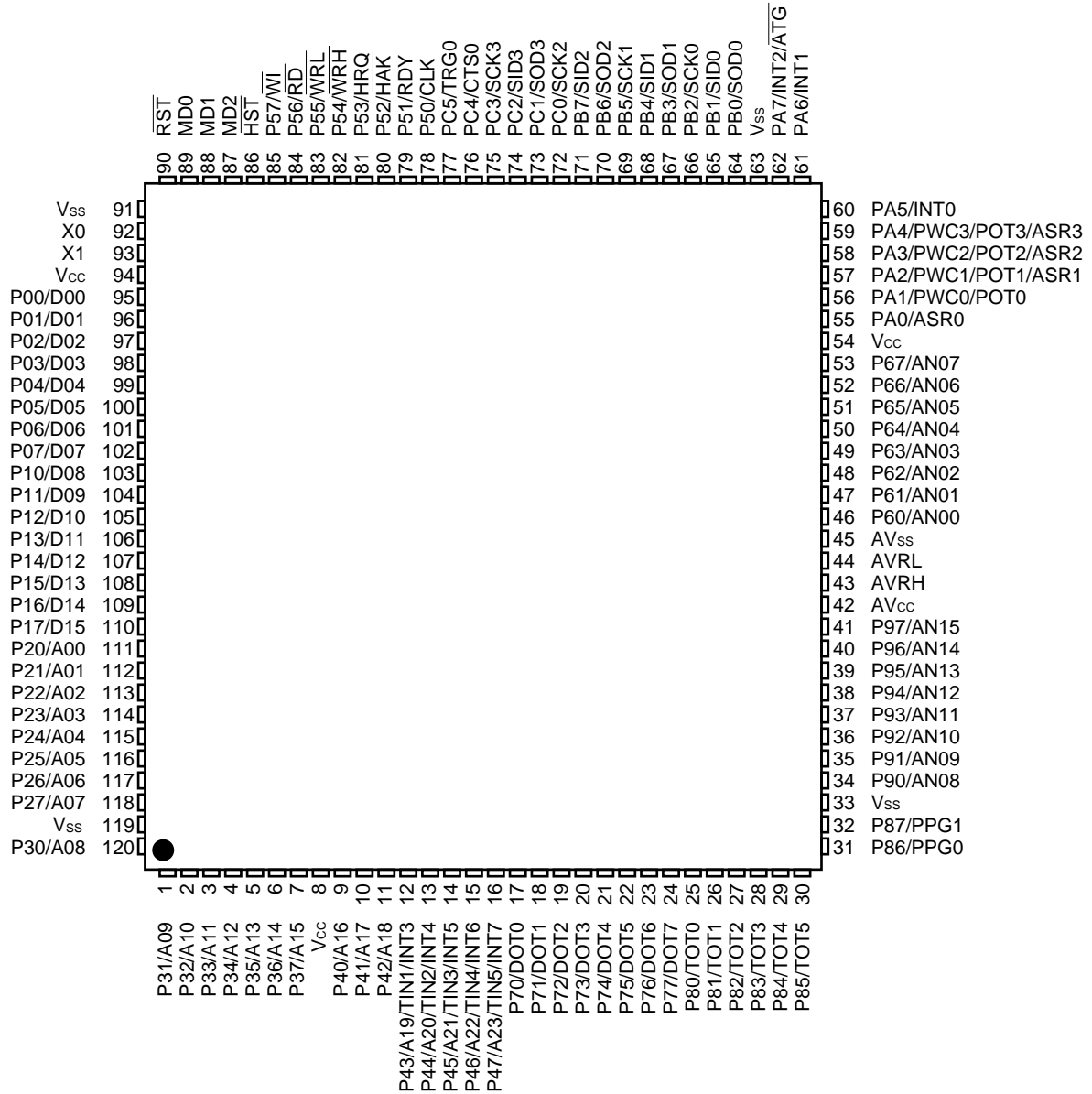
■ DIFFERENCES BETWEEN MB90223/224 (MASK ROM PRODUCT) AND MB90P224A/W224A/P224B/W224B

| Part number Item | MB90223 | MB90224 | MB90P224A MB90P224B | MB90W224A MB90W224B |
|-----------------------|-----------------------|-----------------------|-------------------------|------------------------|
| ROM | Mask ROM 64 Kbytes | Mask ROM 96 Kbytes | OTPROM 96 Kbytes | EPROM 96 Kbytes |
| Pin functions: pin 87 | MD2 pin | | MD2/V _{PP} pin | |

MB90220 Series

PIN ASSIGNMENT

(Top view)



(FPT-120P-M03)
(FPT-120C-C02)

MB90220 Series

■ PIN DESCRIPTION

| Pin no. QFP* | Pin name | Circuit type | Function |
|-----------------|--------------------|--------------|--|
| 92, 93 | X0, X1 | A | Crystal oscillation pins (16 MHz) |
| 89 to 87 | MD0 to MD2 | D | Operation mode specification input pins Connect directly to V_{CC} or V_{SS} . |
| 90 | RST | G | External reset request input |
| 86 | HST | E | Hardware standby input pin |
| 95 to 102 | P00 to P07 | C | General-purpose I/O ports This function is valid only in single-chip mode. |
| | D00 to D07 | | Output pins for low-order 8 bits of the external address bus. This function is valid only in modes where the external bus is enabled. |
| 103 to 110 | P10 to P17 | C | General-purpose I/O ports This function is valid only in single-chip mode or when the external bus is enabled and the 8-bit data bus specification has been made. |
| | D08 to D15 | | I/O pins for higher-order 8 bits of the external data bus This function is valid only when the external bus is enabled and the 16-bit bus specification has been made. |
| 111 to 118 | P20 to P27 | C | General-purpose I/O ports This function is valid only in single-chip mode. |
| | A00 to A07 | | Output pins for lower-order 8 bits of the external address bus This function is valid only in modes where the external bus is enabled. |
| 120, 1 to 7 | P30, P31 to P37 | C | General-purpose I/O ports This function is valid either in single-chip mode or when the address mid-order control register specification is "port". |
| | A08, A09 to A15 | | Output pins for mid-order 8 bits of the external address bus This function is valid in modes where the external bus is enabled and the address mid-order control register specification is "address". |
| 9 to 11 | P40 to P42 | C | General-purpose I/O ports This function is valid either in single-chip mode or when the address high-order control register specification is "port". |
| | A16 to A18 | | Output pins for higher-order 8 bits of the external address bus This function is valid in modes where the external bus is enabled and the address high-order control register specification is "address". |
| 12 to 16 | P43 to P47 | C | General-purpose I/O ports This function is valid when either single-chip mode is enabled or the address higher-order control register specification is "port". |
| | A19 to A23 | | Output pins for higher-order 8 bits of the external address bus This function is valid in modes where the external bus is enabled and the address higher-order control register specification is "address". |
| | TIN1 to TIN5 | | 16-bit reload timer input pins This function is valid when the timer input specification is "enabled". The data on the pins is read as timer input (TIN1 to TIN5). |

* : FPT-120P-M03, FPT-120C-C02

(Continued)

MB90220 Series

| Pin no. QFP* | Pin name | Circuit type | Function |
|-----------------|------------------|--------------|---|
| 12 to 16 | INT3 to INT7 | C | External interrupt request input pins When external interrupts are enabled, these inputs may be used suddenly at any time; therefore, it is necessary to stop output by other functions on these pins, except when using them for output deliberately. |
| 78 | P50 | C | General-purpose I/O port This function is valid in single-chip mode and when the CLK output specification is disabled. |
| | CLK | | CLK output pin This function is valid in modes where the external bus is enabled and the CLK output specification is enabled. |
| 79 | P51 | C | General-purpose I/O port This function is valid in single-chip mode or when the ready function is disabled. |
| | RDY | | Ready input pin This function is valid in modes where the external bus is enabled and the ready function is enabled. |
| 80 | P52 | C | General-purpose I/O port This function is valid in single-chip mode or when the hold function is disabled. |
| | HAK | | Hold acknowledge output pin This function is valid in modes where the external bus is enabled and the hold function is enabled. |
| 81 | P53 | C | General-purpose I/O port This function is valid in single-chip mode or external bus mode and when the hold function is disabled. |
| | HRQ | | Hold request input pin This function is valid in modes where the external bus is enabled and the hold function is enabled. During this operation, the input may be used suddenly at any time; therefore, it is necessary to stop output by other functions on this pin, except when using it for output deliberately. |
| 82 | P54 | C | General-purpose I/O port This function is valid in single-chip mode, when the external bus is in 8-bit mode, or when \overline{WRH} pin output is disabled. |
| | \overline{WRH} | | Write strobe output pin for the high-order 8 bits of the data bus This function is valid in modes where the external bus is enabled, the external bus is in 16-bit mode, and \overline{WRH} pin output is enabled. |
| 83 | P55 | C | General-purpose I/O port This function is valid in single-chip mode or when \overline{WRL} pin output is disabled. |
| | \overline{WRL} | | Write strobe output pin for the low-order 8 bits of the data bus This function is valid in modes where the external bus is enabled and \overline{WRL} pin output is enabled. |

* : FPT-120P-M03, FPT-120C-C02

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MB90220 Series

| Pin no. QFP* | Pin name | Circuit type | Function |
|-----------------|---------------|--------------|---|
| 84 | P56 | C | General-purpose I/O port This function is valid in single-chip mode. This function is valid in modes where the external bus is valid. |
| | RD | | Read strobe output pin for the data bus This function is valid in modes where the external bus is enabled. |
| 85 | P57 | B | General-purpose I/O port This function is always valid. When these pins are open in input mode, through current may leak in stop mode/reset mode, be sure to fix these pins to V_{CC}/V_{SS} level to use these pins in input mode. |
| | WI | | RAM write disable request input During this operation, the input may be used suddenly at any time; therefore, it is necessary to stop output by other functions on this pin, except when using it for output deliberately. |
| 46 to 53 | P60 to P67 | F | Open-drain I/O ports This function is valid when the analog input enable register specification is "port". |
| | AN00 to AN07 | | 10-bit A/D converter analog input pins This function is valid when the analog input enable register specification is "analog input". |
| 17 to 24 | P70 to P77 | C | General-purpose I/O ports This function is valid when the output specification for DOT0 to DOT7 is "disabled". |
| | DOT0 to DOT7 | | This function is valid when OCU (output compare unit) output is enabled. |
| 25 to 30 | P80 to P85 | C | General-purpose I/O ports This function is valid when the output specification for TOT0 to TOT5 is "disabled". |
| | TOT0 to TOT5 | | 16-bit reload timer output pins (TOT0 to TOT5) |
| 31, 32 | P86, P87 | C | General-purpose I/O ports This function is valid when the PPG0, and PPG1 output specification is "disabled". |
| | PPG0, PPG1 | | 16-bit PPG timer output pins This function is valid when the PPG control/status register specification is "PPG output pins". |
| 34 to 41 | P90 to P97 | F | Open-drain I/O ports This function is valid when the analog input enable register specification is "port". |
| | AN08 to AN15 | | 10-bit A/D converter analog input pins This function is valid when the analog input enable register specification is "analog input". |

* : FPT-120P-M03, FPT-120C-C02

(Continued)

MB90220 Series

| Pin no. QFP* | Pin name | Circuit type | Function |
|-----------------|---------------|--------------|--|
| 55 | PA0 | C | General-purpose I/O port This function is always valid. |
| | ASR0 | | ICU (input capture unit) input pin This function is valid during ICU (input capture unit) input operations. |
| 56 | PA1 | C | General-purpose I/O port This function is always valid. |
| | PWC0 | | PWC input pin During PWC0 input operations, this input may be used suddenly at any time; therefore, it is necessary to stop output by other functions on this pin, except when using it for output deliberately. |
| | POT0 | | PWC output pin This function is valid during PWC output operations. |
| 57 to 59 | PA2 to PA4 | C | General-purpose I/O ports This function is always valid. |
| | PWC1 to PWC3 | | PWC input pins This function is valid during PWC input operations. During PWC1 to PWC3 input operations, this input may be used suddenly at any time; therefore, it is necessary to stop output by other functions on this pin, except when using it for output deliberately. |
| | POT1 to POT3 | | PWC output pins This function is valid during PWC output operations. |
| | ASR1 to ASR3 | | ICU (input capture unit) input pins This function is valid during ICU (input capture unit) input operations. |
| 60, 61 | PA5, PA6 | B | General-purpose I/O ports This function is always valid. When these pins are open in input mode, through current may leak in stop mode/reset mode, be sure to fix these pins to V_{cc}/V_{ss} level to use these pins in input mode. |
| | INT0, INT1 | | DTP/External interrupt request input pins When DTP/external interrupts are enabled, these inputs may be used suddenly at any time; therefore, it is necessary to stop output by other functions on these pins, except when using them for output deliberately. When these pins are open in input mode, through current may leak in stop mode/reset mode, be sure to fix these pins to V_{cc}/V_{ss} level to use these pins in input mode. |
| 62 | PA7 | B | General-purpose I/O port This function is always valid. When these pins are open in input mode, through current may leak in stop mode/reset mode, be sure to fix these pins to V_{cc}/V_{ss} level to use these pins in input mode. |

* : FPT-120P-M03, FPT-120C-C02

(Continued)

MB90220 Series

| Pin no. QFP* | Pin name | Circuit type | Function |
|-----------------|----------|--------------|---|
| 62 | INT2 | B | DTP/External interrupt request input pin When DTP/external interrupts are enabled, these inputs may be used suddenly at any time; therefore, it is necessary to stop output by other functions on these pins, except when using them for output deliberately. When these pins are open in input mode, through current may leak in stop mode/reset mode, be sure to fix these pins to V_{cc}/V_{ss} level to use these pins in input mode. |
| | ATG | | 10-bit A/D converter external trigger input pin When these pins are open in input mode, through current may leak in stop mode/reset mode, be sure to fix these pins to V_{cc}/V_{ss} level to use these pins in input mode. |
| 64 | PB0 | C | General-purpose I/O port This function is valid when the UART0 (ch.0) serial data output specification is "disabled". |
| | SOD0 | | UART0 (ch.0) serial data output This function is valid when the UART0 (ch.0) serial data output specification is "enabled". |
| 65 | PB1 | C | General-purpose I/O port This function is always valid. |
| | SID0 | | UART0 (ch.0) serial data input pin During UART0 (ch.0) input operations, this input may be used suddenly at any time; therefore, it is necessary to stop output by other functions on this pin, except when using it for output deliberately. |
| 66 | PB2 | C | General-purpose output port This function is valid when the UART0 (ch.0) clock output specification is "disabled". |
| | SCK0 | | UART0 (ch.0) clock output pin The clock output function is valid when the UART0 (ch.0) clock output specification is "enabled". UART0 (ch.0) external clock input pin. This function is valid when the port is in input mode and the UART0 (ch.0) specification is external clock mode. |
| 67 | PB3 | C | General-purpose I/O port This function is valid when the UART0 (ch.1) serial data output specification is "disabled". |
| | SOD1 | | UART0 (ch.1) serial data output pin This function is valid when the UART0 (ch.1) serial data output specification is "enabled". |
| 68 | PB4 | C | General-purpose I/O port This function is always valid. |
| | SID1 | | UART0 (ch.1) serial data input pin During UART0 (ch.1) input operations, this input may be used suddenly at any time; therefore, it is necessary to stop output by other functions on this pin, except when using it for output deliberately. |

* : FPT-120P-M03, FPT-120C-C02

(Continued)

MB90220 Series

| Pin no. QFP* | Pin name | Circuit type | Function |
|-----------------|----------|--------------|---|
| 69 | PB5 | C | General-purpose I/O port This function is valid when the UART0 (ch.1) clock output specification is "disabled". |
| | SCK1 | | UART0 (ch.1) clock output pin The clock output function is valid when the UART0 (ch.1) clock output specification is "enabled". UART0 (ch.1) external clock input pin This function is valid when the port is in input mode and the UART0 (ch.1) specification is external clock mode. |
| 70 | PB6 | C | General-purpose I/O port This function is valid when the UART0 (ch.2) serial data output specification is "disabled". |
| | SOD2 | | UART0 (ch.2) serial data output pin This function is valid when the UART0 (ch.2) serial data output specification is "enabled". |
| 71 | PB7 | C | General-purpose I/O port This function is always valid. |
| | SID2 | | UART0 (ch.2) serial data input pin During UART0 (ch.2) input operations, this input may be used suddenly at any time; therefore, it is necessary to stop output by other functions on this pin, except when using it for output deliberately. |
| 72 | PC0 | C | General-purpose I/O port This function is valid when the UART0 (ch.2) clock output specification is "disabled". |
| | SCK2 | | UART0 (ch.2) clock output pin The clock output function is valid when the UART0 (ch.2) clock output specification is "enabled". UART0 (ch.2) external clock input pin This function is valid when the port is in input mode and the UART0 (ch.2) specification is external clock mode. |
| 73 | PC1 | C | General-purpose I/O port This function is valid when the UART1 serial data output specification is "disabled". |
| | SOD3 | | UART1 serial data output pin This function is valid when the UART1 serial data output specification is "enabled". |
| 74 | PC2 | C | General-purpose I/O port This function is always valid. |
| | SID3 | | UART1 serial data input pin During UART1 input operations, this input may be used suddenly at any time; therefore, it is necessary to stop output by other functions on this pin, except when using it for output deliberately. |

* : FPT-120P-M03, FPT-120C-C02

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MB90220 Series

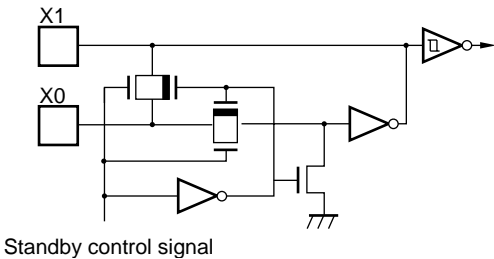
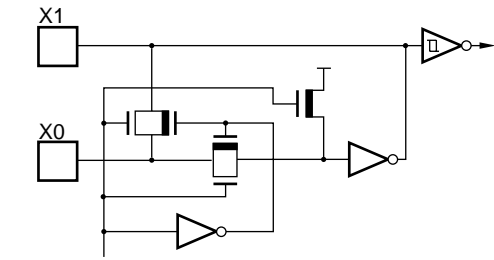
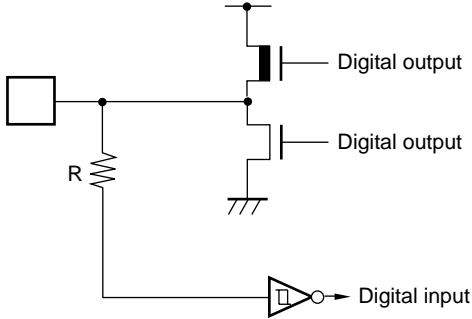
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| Pin no. QFP* | Pin name | Circuit type | Function |
|--------------------------|------------------|--------------|---|
| 75 | PC3 | C | General-purpose I/O port This function is valid when the UART1 clock output specification is “disabled”. |
| | SCK3 | | UART1 clock output pin The clock output function is valid when the UART1 clock output specification is “enabled”. UART1 external clock input pin This function is valid when the port is in input mode and the UART1 specification is external clock mode. |
| 76 | PC4 | C | General-purpose I/O port This function is always valid. |
| | CTS0 | | UART0 (ch.0) Clear To Send input pin When the UART0 (ch.0) CTS function is enabled, this input may be used suddenly at any time; therefore, it is necessary to stop output by other functions on this pin, except when using it for output deliberately. |
| 77 | PC5 | C | General-purpose I/O port This function is always valid. |
| | TRG0 | | 16-bit PPG timer trigger input pin This function is valid when the 16-bit PPG timer trigger input specification is enabled. The data on this pin is read as 16-bit PPG timer trigger input (TRG0). During this operation, the input may be used suddenly at any time; therefore, it is necessary to stop output by other functions on this pin, except when using it for output deliberately. |
| 8, 54, 94 | V _{CC} | Power supply | Power supply for digital circuitry |
| 33, 63, 91, 119 | V _{SS} | Power supply | Ground level for digital circuitry |
| 42 | AV _{CC} | Power supply | Power supply for analog circuitry When turning this power supply on or off, always be sure to first apply electric potential equal to or greater than AV _{CC} to V _{CC} . During normal operation AV _{CC} should be equal to V _{CC} . |
| 43 | AV _{RH} | Power supply | Reference voltage input for analog circuitry When turning this pin on or off, always be sure to first apply electric potential equal to or greater than AV _{RH} to AV _{CC} . |
| 44 | AV _{RL} | Power supply | Reference voltage input for analog circuitry |
| 45 | AV _{SS} | Power supply | Ground level for analog circuitry |

* : FPT-120P-M03, FPT-120C-C02

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■ I/O CIRCUIT TYPE

| Type | Circuit | Remarks |
|------|--|---|
| A |  <p>Standby control signal</p> | <ul style="list-style-type: none"> Oscillation feedback resistor: Approx. 1 MΩ MB90223 MB90224 MB90P224B MB90W224B |
| |  <p>Standby control signal</p> | <ul style="list-style-type: none"> Oscillation feedback resistor: Approx. 1 MΩ MB90P224A MB90W224A |
| B |  <p>Digital output</p> <p>Digital output</p> <p>Digital input</p> | <ul style="list-style-type: none"> CMOS-level output CMOS-level hysteresis input with no standby control |

Note: The pull-up and pull-down resistors are always connected, regardless of the state.

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MB90220 Series

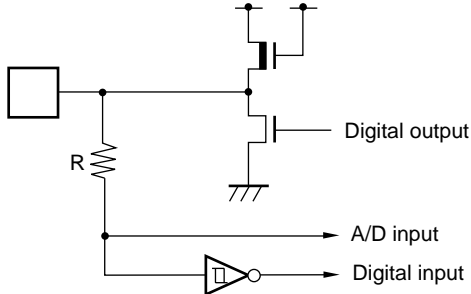
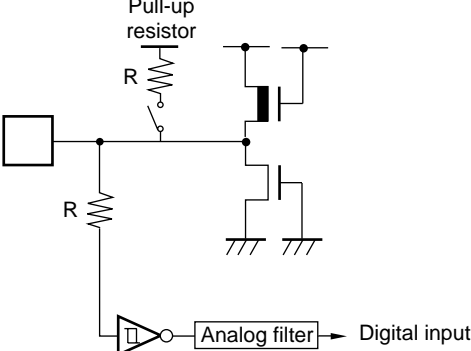
| Type | Circuit | Remarks |
|------|---------|---|
| C | | <ul style="list-style-type: none"> • CMOS-level output • CMOS-level hysteresis input with standby control |
| D | | <ul style="list-style-type: none"> • CMOS-level input with no standby control Mask ROM products only: MD2: with pull-down resistor MD1: with pull-up resistor MD0: with pull-down resistor |
| | | <ul style="list-style-type: none"> • CMOS-level input with no standby control MD2 of OTPROM products/EPROM products only |
| E | | <ul style="list-style-type: none"> • CMOS-level hysteresis input with no standby control • With input analog filter (40 ns Typ.) |

Note: The pull-up and pull-down resistors are always connected, regardless of the state.

(Continued)

MB90220 Series

(Continued)

| Type | Circuit | Remarks |
|------|--|--|
| F |  | <ul style="list-style-type: none"> • N-channel open-drain output • CMOS-level hysteresis input with A/D control and with standby control |
| G |  | <ul style="list-style-type: none"> • CMOS-level hysteresis input with no standby control and with pull-up resistor • With input analog filter (40 ns Typ.) <p>MB90223, MB90224: \overline{RST} pin can be set to with or without a pull-up resistor by a mask option.</p> <p>MB90P224A: With pull-up resistor MB90W224A: With pull-up resistor MB90P224B: With no pull-up resistor MB90W224B: With no pull-up resistor</p> |

 : P-type transistor
 : N-type transistor

Note: The pull-up and pull-down resistors are always connected, regardless of the state.

MB90220 Series

■ HANDLING DEVICES

1. Preventing Latchup

CMOS ICs may cause latchup when a voltage higher than V_{CC} or lower than V_{SS} is applied to input or output pins other than medium-and high-voltage pins, or when a voltage exceeding the rating is applied between V_{CC} and V_{SS} .

If latch-up occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Use meticulous care not to let any voltage exceed the maximum rating.

Also, take care to prevent the analog power supply (AV_{CC} and AV_{RH}) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Pins when A/D is not Used

Connect to be $AV_{CC} = AVRH = V_{CC}$ and $AV_{SS} = AV_{RL} = V_{SS}$ even if the A/D converter is not in use.

4. Precautions when Using an External Input

To reset the internal circuit properly by the “L” level input to the \overline{RST} pin, the “L” level input to the \overline{RST} pin must be maintained for at least five machine cycles. Pay attention to it if the chip uses external clock input.

5. V_{CC} and V_{SS} Pins

Apply equal potential to the V_{CC} and V_{SS} pins.

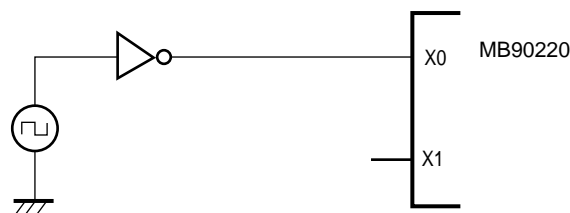
6. Supply Voltage Variation

The operation assurance range for the V_{CC} supply voltage is as given in the ratings. However, sudden changes in the supply voltage can cause misoperation, even if the voltage remains within the rated range. Therefore, it is important to supply a stable voltage to the IC. The recommended power supply control guidelines are that the commercial frequency (50 to 60 Hz) ripple variation (P-P value) on V_{CC} should be less than 10% of the standard V_{CC} value and that the transient rate of change during sudden changes, such as during power supply switching, should be less than 0.1 V/ms.

7. Notes on Using an External Clock

When using an external clock, drive the X0 pin as illustrated below. When an external clock is used, oscillation stabilization time is required even for power-on reset and wake-up from stop mode.

• Use of External Clock



Note: When using an external clock, be sure to input external clock more than 6 machine cycles after setting the \overline{RST} pin to “L” to transfer to the hardware standby mode.

8. Power-on Sequence for A/D Converter Power Supplies and Analog Inputs

Be sure to turn on the digital power supply (V_{CC}) before applying voltage to the A/D converter power supplies (AV_{CC} , $AVRH$, and $AVRL$) and analog inputs (AN00 to AN15).

When turning power supplies off, turn off the A/D converter power supplies (AV_{CC} , $AVRH$, and $AVRL$) and analog inputs (AN00 to AN15) first, then the digital power supply (V_{CC}).

When turning $AVRH$ on or off, be careful not to let it exceed AV_{CC} .

MB90220 Series

■ PROGRAMMING FOR MB90P224A/P224B/W224A/W224B

In EPROM mode, the MB90P224A/P224B/W224A/W224B functions equivalent to the MBM27C1000. This allows the EPROM to be programmed with a general-purpose EPROM programmer by using the dedicated socket adapter (do not use the electronic signature mode).

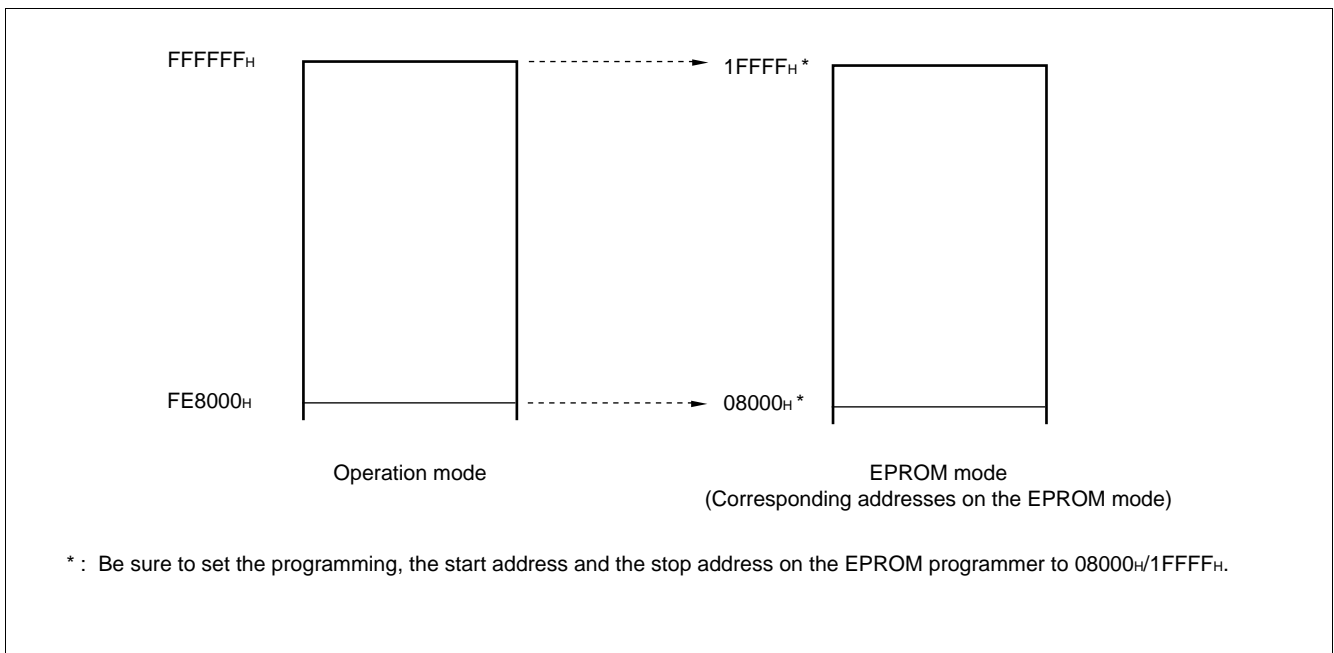
1. Program Mode

When shipped from Fujitsu, and after each erasure, all bits (96 K × 8 bits) in the MB90P224A/P224B/W224A/W224B are in the “1” state. Data is written to the ROM by selectively programming “0’s” into the desired bit locations. Bits cannot be set to “1” electrically.

2. Programming Procedure

- (1) Set the EPROM programmer to MBM27C1000.
- (2) Load program data into the EPROM programmer at 08000_H to 1FFFF_H.

Note that ROM addresses FE8000_H to FFFFFFF_H in the operation mode in the MB90P224A/P224B/W224A/W224B series assign to 08000_H to 1FFFF_H in the EPROM mode (on the EPROM programmer).



- (3) Mount the MB90P224A/P224B/W224A/W224B on the adapter socket, then fit the adapter socket onto the EPROM programmer. When mounting the device and the adapter socket, pay attention to their mounting orientations.
- (4) Start programming the program data to the device.
- (5) If programming has not successfully resulted, connect a capacitor of approx. 0.1 μF between V_{CC} and GND, between V_{PP} and GND.

Note: The mask ROM products (MB90223, MB90224) does not support EPROM mode. Data cannot, therefore, be read by the EPROM programmer.

MB90220 Series

3. EPROM Programmer Socket Adapter and Recommended Programmer Manufacturer

| | | | |
|--|-----------------|--|-------------|
| Part No. | | MB90P224B | |
| Package | | QFP-120 | |
| Compatible socket adapter Sun Hayato Co., Ltd. | | ROM-120QF-32DP-16F | |
| Recommended programmer manufacturer and programmer name | Advantest corp. | R4945A (main unit) + R49451A (adapter) | Recommended |

Inquiry: Sun Hayato Co., Ltd.: TEL: (81)-3-3986-0403

FAX: (81)-3-5396-9106

Advantest Corp.: TEL: Except JAPAN (81)-3-3930-4111

4. Erase Procedure

Data written in the MB90W224A/W224B is erased (from "0" to "1") by exposing the chip to ultraviolet rays with a wavelength of 2,537 Å through the translucent cover.

Recommended irradiation dosage for exposure is 10 Wsec/cm². This amount is reached in 15 to 20 minutes with a commercial ultraviolet lamp positioned 2 to 3 cm above the package (when the package surface illuminance is 1200 μW/cm²).

If the ultraviolet lamp has a filter, remove the filter before exposure. Attaching a mirrored plate to the lamp increases the illuminance by a factor of 1.4 to 1.8, thus shortening the required erasure time. If the translucent part of the package is stained with oil or adhesive, transmission of ultraviolet rays is degraded, resulting in a longer erasure time. In that case, clean the translucent part using alcohol (or other solvent not affecting the package).

The above recommended dosage is a value which takes the guard band into consideration and is a multiple of the time in which all bits can be evaluated to have been erased. Observe the recommended dosage for erasure; the purpose of the guard band is to ensure erasure in all temperature and supply voltage ranges. In addition, check the life span of the lamp and control the illuminance appropriately.

Data in the MB90W224A/W224B is erased by exposure to light with a wavelength of 4,000 Å or less.

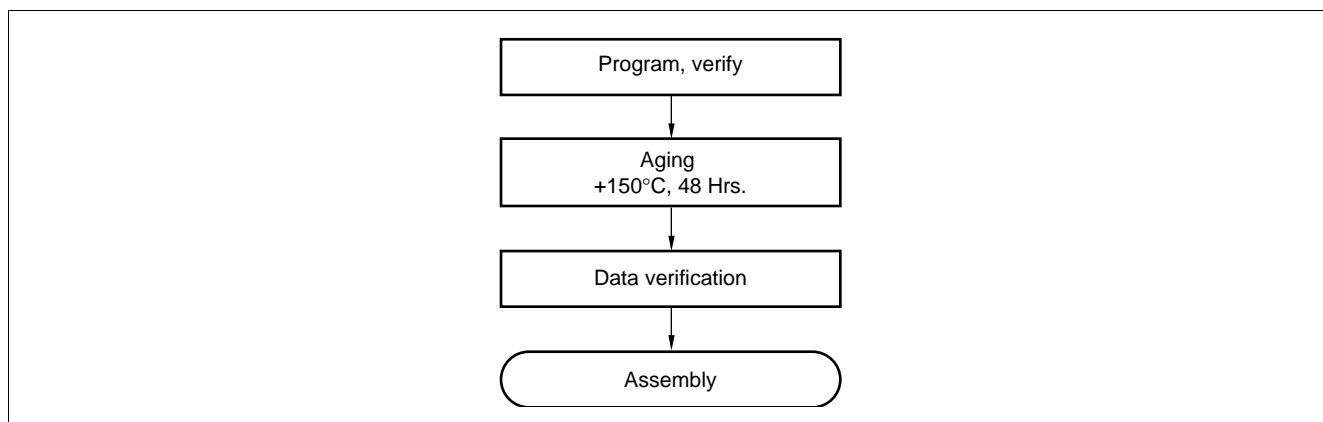
Data in the device is also erased even by exposure to fluorescent lamp light or sunlight although the exposure results in a much lower erasure rate than exposure to 2,537 Å ultraviolet rays. Note that exposure to such lights for an extended period will therefore affect system reliability. If the chip is used where it is exposed to any light with a wavelength of 4,000 Å or less, cover the translucent part, for example, with a protective seal to prevent the chip from being exposed to the light.

Exposure to light with a wavelength of 4,000 to 5,000 Å or more will not erase data in the device. If the light applied to the chip has a very high illuminance, however, the device may cause malfunction in the circuit for reasons of general semiconductor characteristics. Although the circuit will recover normal operation when exposure is stopped, the device requires proper countermeasures for use in a place exposed continuously to such light even though the wavelength is 4,000 Å or more.

MB90220 Series

5. Recommended Screening Conditions

High temperature aging is recommended as the pre-assembly screening procedure.



6. Programming Yield

MB90P224A/P224B cannot be write-tested for all bits due to their nature. Therefore the write yield cannot always be guaranteed to be 100%.

7. Pin Assignments in EPROM Mode

(1) Pins Compatible with MBM27C1000


| MBM27C1000 | | MB90P224A/P224B/ MB90W224A/W224B | | MBM27C1000 | | MB90P224A/P224B/ MB90W224A/W224B | |
|------------|-----------------|-------------------------------------|------------------------|------------|-----------------|-------------------------------------|-----------------|
| Pin no. | Pin name | Pin no. | Pin name | Pin no. | Pin name | Pin no. | Pin name |
| 1 | V _{PP} | 87 | MD2 (V _{PP}) | 32 | V _{CC} | 8, 54, 94 | V _{CC} |
| 2 | OE | 83 | P55 | 31 | PGM | 84 | P56 |
| 3 | A15 | 7 | P37 | 30 | N.C. | — | — |
| 4 | A12 | 4 | P34 | 29 | A14 | 6 | P36 |
| 5 | A07 | 118 | P27 | 28 | A13 | 5 | P35 |
| 6 | A06 | 117 | P26 | 27 | A08 | 120 | P30 |
| 7 | A05 | 116 | P25 | 26 | A09 | 1 | P31 |
| 8 | A04 | 115 | P24 | 25 | A11 | 3 | P33 |
| 9 | A03 | 114 | P23 | 24 | A16 | 9 | P40 |
| 10 | A02 | 113 | P22 | 23 | A10 | 2 | P32 |
| 11 | A01 | 112 | P21 | 22 | CE | 82 | P54 |
| 12 | A00 | 111 | P20 | 21 | D07 | 102 | P07 |
| 13 | D00 | 95 | P00 | 20 | D06 | 101 | P06 |
| 14 | D01 | 96 | P01 | 19 | D05 | 100 | P05 |
| 15 | D02 | 97 | P02 | 18 | D04 | 99 | P04 |
| 16 | GND | 33, 63, 91, 119 | V _{SS} | 17 | D03 | 98 | P03 |

MB90220 Series

(2) Power Supply and GND Connection Pins

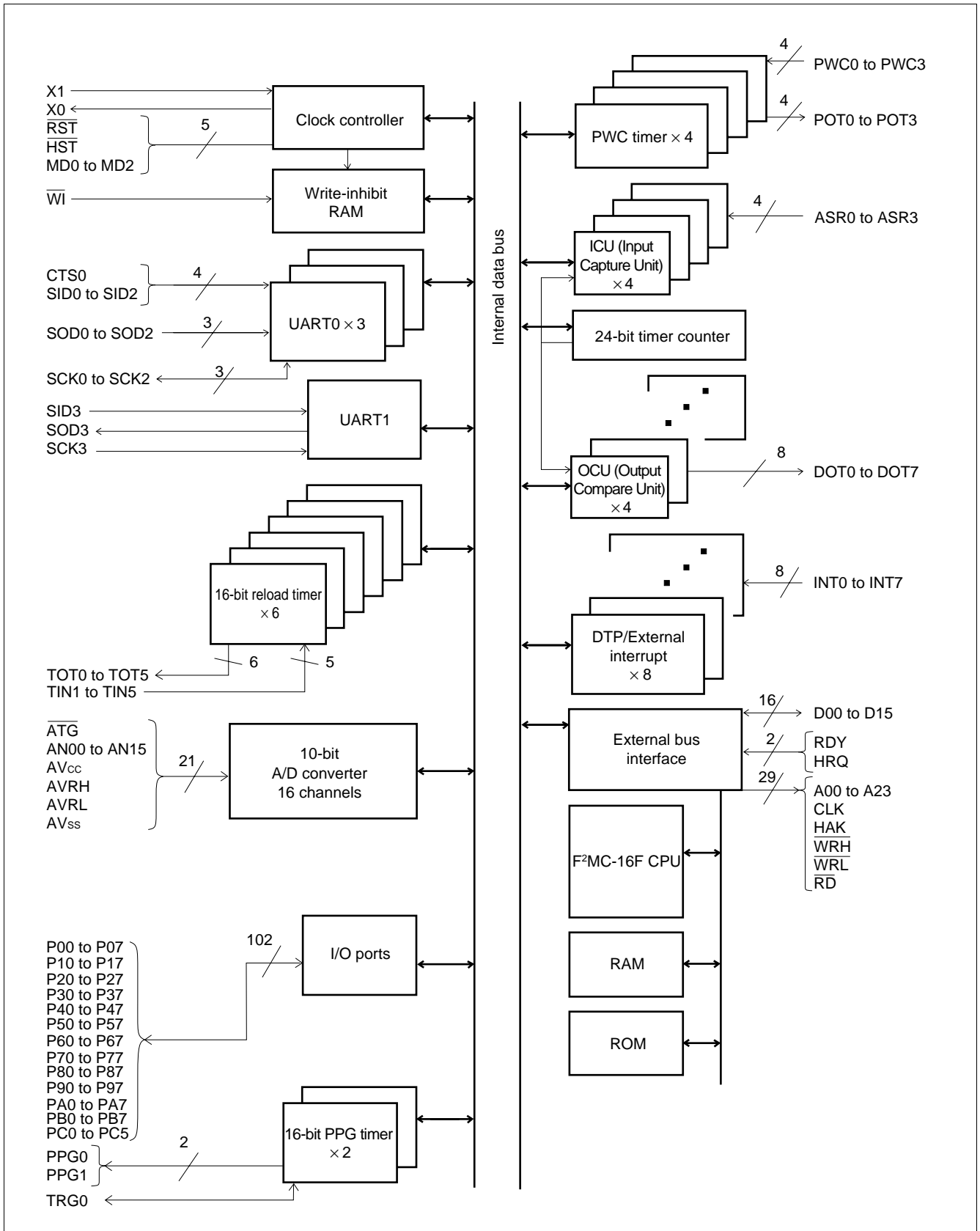
| Type | Pin no. | Pin name |
|--------------|-----------------|------------------|
| Power supply | 89 | MD0 |
| | 88 | MD1 |
| | 86 | HST |
| | 8, 54, 94 | V _{cc} |
| GND | 33, 63, 91, 119 | V _{ss} |
| | 44 | AVRL |
| | 45 | AV _{ss} |
| | 80 | P52 |
| | 81 | P53 |
| | 90 | RST |

(3) Pins other than MBM27C1000-compatible Pins

| Pin no. | Pin name | Treatment |
|--|---|--|
| 92 | X0 | Pull up with 4.7 K Ω resistor |
| 93 | X1 | OPEN |
| 109 110 10 to 16 42 43 46 47 48 to 53 17 to 24 25 to 32 34 to 41 55 to 61 63 to 70 71 to 76 78 79 85 103 to 108 | P16 P17 P41 to P47 AV _{cc} AVRH P60 P61 P62 to P67 P70 to P77 P80 to P82 P90 to P97 PA0 to PA7 PB0 to PB7 PC0 to PC5 P50 P51 P57 P10 to P15 |  <p>Connect pull-up resistor of about 1 MΩ to each pin</p> |

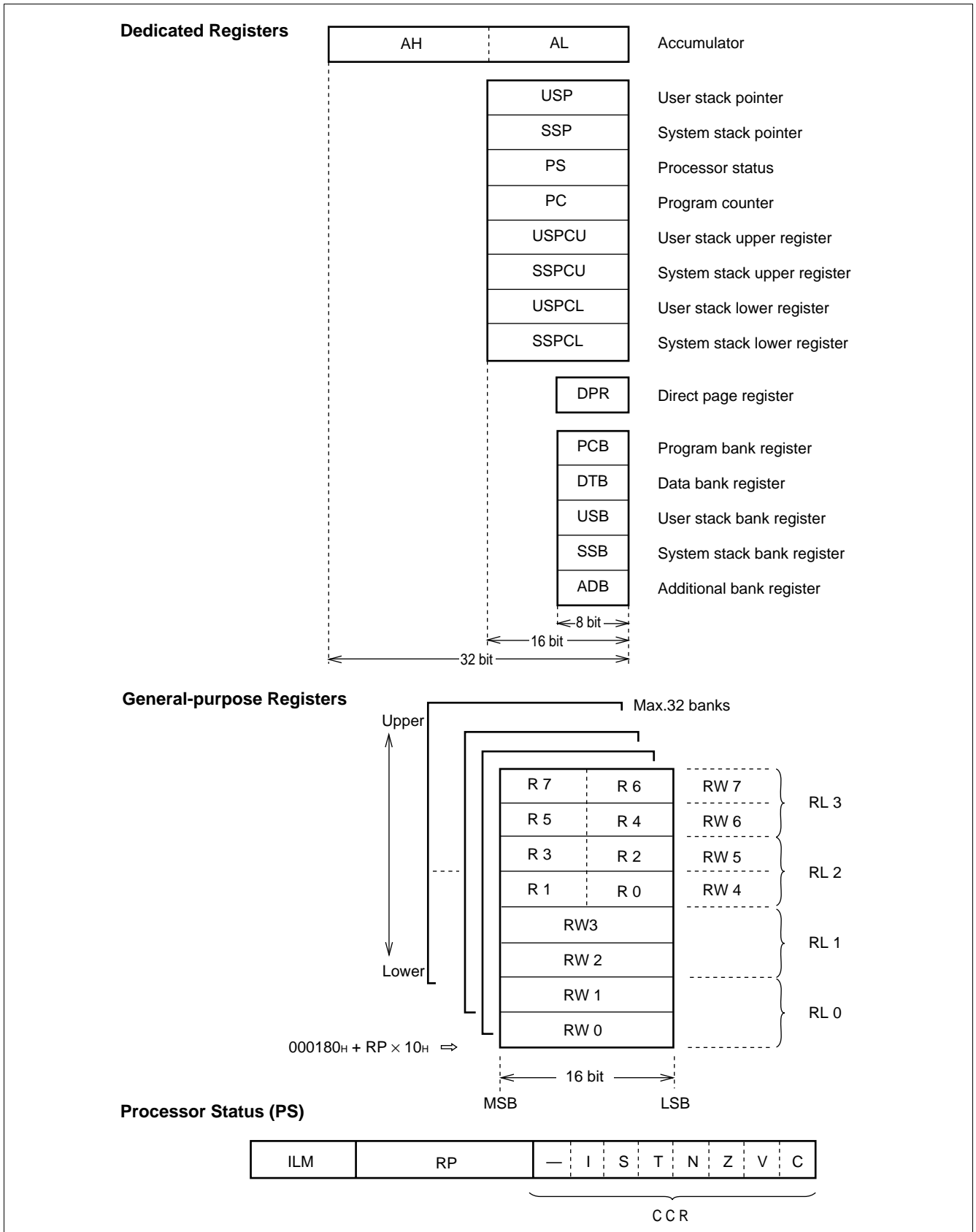
MB90220 Series

■ BLOCK DIAGRAM



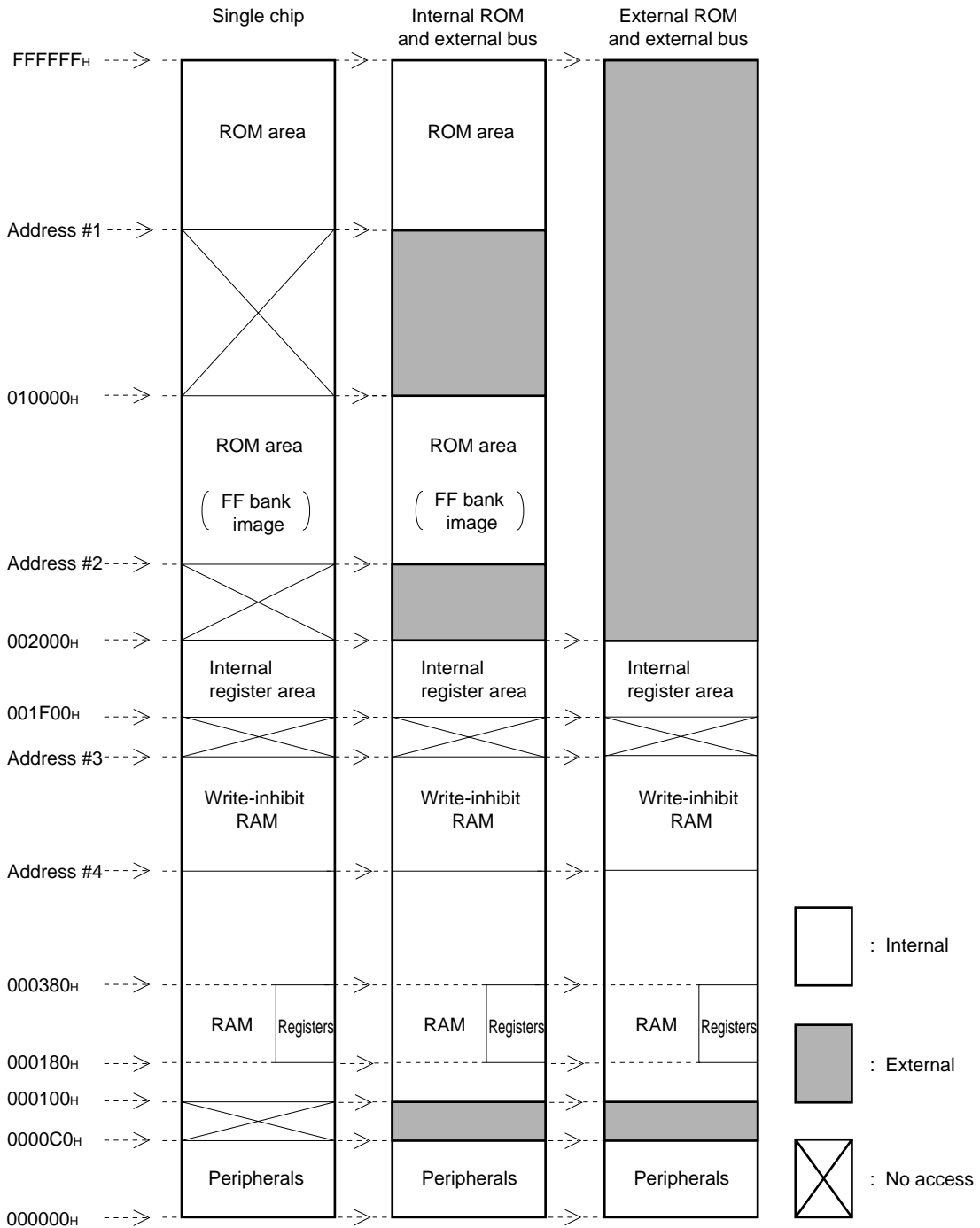
MB90220 Series

PROGRAMMING MODEL



MB90220 Series

MEMORY MAP



| Type | Address #1 | Address #2 | Address #3 | Address #4 |
|---|------------|------------|------------|------------|
| MB90223 | FF0000H | 004000H | 000F00H | 000D00H |
| MB90224 MB90P224A/P224B MB90W224A/W224B | FE8000H | 004000H | 001500H | 001300H |
| MB90V220 | (FE0000H) | 004000H | 001900H | 001500H |

MB90220 Series

■ I/O MAP

| Address | Register | Register name | Access | Resource name | Initial value |
|---|--|-----------------|--------|---------------|---------------|
| 000000 _H ^{*3} | Port 0 data register | PDR0 | R/W | Port 0 | XXXXXXXXXX |
| 000001 _H ^{*3} | Port 1 data register | PDR1 | R/W | Port 1 | XXXXXXXXXX |
| 000002 _H ^{*3} | Port 2 data register | PDR2 | R/W | Port 2 | XXXXXXXXXX |
| 000003 _H ^{*3} | Port 3 data register | PDR3 | R/W | Port 3 | XXXXXXXXXX |
| 000004 _H ^{*3} | Port 4 data register | PDR4 | R/W | Port 4 | XXXXXXXXXX |
| 000005 _H ^{*3} | Port 5 data register | PDR5 | R/W | Port 5 | XXXXXXXXXX |
| 000006 _H | Port 6 data register | PDR6 | R/W | Port 6 | 11111111 |
| 000007 _H | Port 7 data register | PDR7 | R | Port 7 | XXXXXXXXXX |
| 000008 _H | Port 8 data register | PDR8 | R/W | Port 8 | XXXXXXXXXX |
| 000009 _H | Port 9 data register | PDR9 | R/W | Port 9 | 11111111 |
| 00000A _H | Port A data register | PDRA | R/W | Port A | XXXXXXXXXX |
| 00000B _H | Port B data register | PDRB | R/W | Port B | XXXXXXXXXX |
| 00000C _H | Port C data register | PDRC | R/W | Port C | --XXXXXXXX |
| 00000D _H to 0F _H | (Reserved area) ^{*1} | | | | |
| 000010 _H ^{*3} | Port 0 data direction register | DDR0 | R/W | Port 0 | 00000000 |
| 000011 _H ^{*3} | Port 1 data direction register | DDR1 | R/W | Port 1 | 00000000 |
| 000012 _H ^{*3} | Port 2 data direction register | DDR2 | R/W | Port 2 | 00000000 |
| 000013 _H ^{*3} | Port 3 data direction register | DDR3 | R/W | Port 3 | 00000000 |
| 000014 _H ^{*3} | Port 4 data direction register | DDR4 | R/W | Port 4 | 00000000 |
| 000015 _H ^{*3} | Port 5 data direction register | DDR5 | R/W | Port 5 | 00000000 |
| 000016 _H | Port 6 analog input enable register | ADER0 | R/W | Port 6 | 11111111 |
| 000017 _H | Port 7 data direction register | DDR7 | R/W | Port 7 | 11111111 |
| 000018 _H | Port 8 data direction register | DDR8 | R/W | Port 8 | 00000000 |
| 000019 _H | Port 9 analog input enable register | ADER1 | R/W | Port 9 | 11111111 |
| 00001A _H | Port A data direction register | DDRA | R/W | Port A | 00000000 |
| 00001B _H | Port B data direction register | DDRB | R/W | Port B | 00000000 |
| 00001C _H | Port C data direction register | DDRC | R/W | Port C | --000000 |
| 00001D _H to 1F _H | (Reserved area) ^{*1} | | | | |
| 000020 _H | Mode control register 0 | UMC0 | R/W | UART 0 (ch.0) | 00000100 |
| 000021 _H | Status register 0 | USR0 | R/W | | 00010000 |
| 000022 _H | Input data register 0 /output data register 0 | UIDR0 /UODR0 | R/W | | XXXXXXXXXX |

(Continued)

MB90220 Series

| Address | Register | Register name | Access | Resource name | Initial value |
|---|--|-----------------|--------|---------------------------|-----------------|
| 000023 _H | Rate and data register 0 | URD0 | R/W | UART0 (ch.0) | 0 0 0 0 0 0 0 X |
| 000024 _H | Mode control register 1 | UMC1 | R/W | UART0 (ch.1) | 0 0 0 0 0 1 0 0 |
| 000025 _H | Status register 1 | USR1 | R/W | | 0 0 0 1 0 0 0 0 |
| 000026 _H | Input data register 1 /output data register 1 | UIDR1 /UODR1 | R/W | | X X X X X X X X |
| 000027 _H | Rate and data register 1 | URD1 | R/W | | 0 0 0 0 0 0 0 X |
| 000028 _H | Mode control register 2 | UMC2 | R/W | UART0 (ch.2) | 0 0 0 0 0 1 0 0 |
| 000029 _H | Status register 2 | USR2 | R/W | | 0 0 0 1 0 0 0 0 |
| 00002A _H | Input data register 2 /output data register 2 | UIDR2 /UODR2 | R/W | | X X X X X X X X |
| 00002B _H | Rate and data register 2 | URD2 | R/W | | 0 0 0 0 0 0 0 X |
| 00002C _H | UART CTS control register | UCCR | R/W | UART0 (ch.0) | --- 0 0 0 -- |
| 00002D _H | (Reserved area)* ¹ | | | | |
| 00002E _H | Mode register | SMR | R/W | UART1 | 0 0 0 0 0 0 0 0 |
| 00002F _H | Control register | SCR | R/W | | 0 0 0 0 0 1 0 0 |
| 000030 _H | Input data register /output data register | SIDR /SODR | R/W | | X X X X X X X X |
| 000031 _H | Status register | SSR | R/W | | 0 0 0 0 1 - 0 0 |
| 000032 _H | A/D channel setting register | ADCH | R/W | 10-bit A/D converter | 0 0 0 0 0 0 0 0 |
| 000033 _H | A/D mode register | ADMD | R/W | | --- X 0 0 0 0 |
| 000034 _H | A/D control status register | ADCS | R/W | | 0 0 0 0 -- 0 0 |
| 000035 _H | (Reserved area)* ¹ | | | | |
| 000036 _H | A/D data register | ADCD | R | 10-bit A/D converter | X X X X X X X X |
| 000037 _H | | | | | 0 0 0 0 0 0 X X |
| 000038 _H | (Reserved area)* ¹ | | | | |
| 000039 _H | (Reserved area)* ¹ | | | | |
| 00003A _H | DTP/interrupt enable register | ENIR | R/W | DTP/external interrupt | 0 0 0 0 0 0 0 0 |
| 00003B _H | DTP/interrupt source register | EIRR | R/W | | 0 0 0 0 0 0 0 0 |
| 00003C _H | Request level setting register | ELVR | R/W | | 0 0 0 0 0 0 0 0 |
| 00003D _H | | | | | 0 0 0 0 0 0 0 0 |
| 00003E _H to 3F _H | (Reserved area)* ¹ | | | | |
| 000040 _H | Timer control status register 0 | TMCSR0 | R/W | 16-bit reload timer 0 | 0 0 0 0 0 0 0 0 |
| 000041 _H | | | | | --- 0 0 0 0 |

(Continued)

MB90220 Series

| Address | Register | Register name | Access | Resource name | Initial value |
|---------------------|----------------------------------|---------------|--------|---------------------------|-----------------|
| 000042 _H | Timer control status register 1 | TMCSR1 | R/W | 16-bit reload timer 1 | 0 0 0 0 0 0 0 0 |
| 000043 _H | | | | | --- 0 0 0 0 |
| 000044 _H | Timer control status register 2 | TMCSR2 | R/W | 16-bit reload timer 2 | 0 0 0 0 0 0 0 0 |
| 000045 _H | | | | | --- 0 0 0 0 |
| 000046 _H | Timer control status register 3 | TMCSR3 | R/W | 16-bit reload timer 3 | 0 0 0 0 0 0 0 0 |
| 000047 _H | | | | | --- 0 0 0 0 |
| 000048 _H | Timer control status register 4 | TMCSR4 | R/W | 16-bit reload timer 4 | 0 0 0 0 0 0 0 0 |
| 000049 _H | | | | | --- 0 0 0 0 |
| 00004A _H | Timer control status register 5 | TMCSR5 | R/W | 16-bit reload timer 5 | 0 0 0 0 0 0 0 0 |
| 00004B _H | | | | | --- 0 0 0 0 |
| 00004C _H | PPG control status register 0 | PCNT0 | R/W | 16-bit PPG timer 0 | 0 0 0 0 0 0 0 0 |
| 00004D _H | | | | | 0 0 0 0 0 0 0 0 |
| 00004E _H | PPG control status register 1 | PCNT1 | R/W | 16-bit PPG timer 1 | 0 0 0 0 0 0 0 0 |
| 00004F _H | | | | | 0 0 0 0 0 0 0 0 |
| 000050 _H | PWC control status register 0 | PWCSR0 | R/W | PWC timer 0 | 0 0 0 0 0 0 0 0 |
| 000051 _H | | | | | 0 0 0 0 0 0 0 0 |
| 000052 _H | PWC control status register 1 | PWCSR1 | R/W | PWC timer 1 | 0 0 0 0 0 0 0 0 |
| 000053 _H | | | | | 0 0 0 0 0 0 0 0 |
| 000054 _H | PWC control status register 2 | PWCSR2 | R/W | PWC timer 2 | 0 0 0 0 0 0 0 0 |
| 000055 _H | | | | | 0 0 0 0 0 0 0 0 |
| 000056 _H | PWC control status register 3 | PWCSR3 | R/W | PWC timer 3 | 0 0 0 0 0 0 0 0 |
| 000057 _H | | | | | 0 0 0 0 0 0 0 0 |
| 000058 _H | ICU control register 0 | ICC0 | R/W | ICU (Input Capture Unit) | 0 0 0 0 0 0 0 0 |
| 000059 _H | (Reserved area)**1 | | | | |
| 00005A _H | Input capture control register 1 | ICC1 | R/W | ICU (Input Capture Unit) | 0 0 0 0 0 0 0 0 |
| 00005B _H | (Reserved area)**1 | | | | |
| 00005C _H | | | | | |
| 00005D _H | | | | | |
| 00005E _H | | | | | |
| 00005F _H | | | | | |
| 000060 _H | OCU control register 00 | CCR00 | R/W | OCU (Output Compare Unit) | 1 1 1 1 0 0 0 0 |
| 000061 _H | | | | | --- 0 0 0 0 |

(Continued)

MB90220 Series

| Address | Register | Register name | Access | Resource name | Initial value |
|---|--|---------------|--------|---------------------------|-----------------|
| 000062 _H | OCU0 control register 01 | CCR01 | R/W | OCU (Output Compare Unit) | 1 1 1 1 0 0 0 0 |
| 000063 _H | | | | | --- 0 0 0 0 |
| 000064 _H | (Reserved area) ^{*1} | | | | |
| 000065 _H | | | | | |
| 000066 _H | | | | | |
| 000067 _H | | | | | |
| 000068 _H | OCU0 control register 10 | CCR10 | R/W | OCU (Output Compare Unit) | --- 0 0 0 0 |
| 000069 _H | | | | | 0 0 0 0 0 0 0 0 |
| 00006A _H | OCU0 control register 11 | CCR11 | R/W | OCU (Output Compare Unit) | --- 0 0 0 0 |
| 00006B _H | | | | | 0 0 0 0 0 0 0 0 |
| 00006C _H | (Reserved area) ^{*1} | | | | |
| 00006D _H | | | | | |
| 00006E _H | | | | | |
| 00006F _H | | | | | |
| 000070 _H | Free-run timer control register | TCCR | R/W | 24-bit timer counter | 1 1 0 0 0 0 0 0 |
| 000071 _H | | | | | -- 1 1 1 1 1 1 |
| 000072 _H | Free-run timer lower-order data register | TCRL | R | 24-bit timer counter | 0 0 0 0 0 0 0 0 |
| 000073 _H | | | | | 0 0 0 0 0 0 0 0 |
| 000074 _H | Free-run timer upper-order data register | TCRH | R | 24-bit timer counter | 0 0 0 0 0 0 0 0 |
| 000075 _H | | | | | 0 0 0 0 0 0 0 0 |
| 000076 _H | (Reserved area) ^{*1} | | | | |
| 000077 _H | | | | | |
| 000078 _H | | | | | |
| 000079 _H | | | | | |
| 00007A _H | PWC divider ratio control register 0 | DIVR0 | R/W | PWC timer 0 | ----- 0 0 |
| 00007B _H | Reserved area ^{*1} | | | | |
| 00007C _H | PWC divider ratio control register 1 | DIVR1 | R/W | PWC timer 1 | ----- 0 0 |
| 00007D _H | Reserved area ^{*1} | | | | |
| 00007E _H | PWC divider ratio control register 2 | DIVR2 | R/W | PWC timer 2 | ----- 0 0 |
| 00007F _H | Reserved area ^{*1} | | | | |
| 000080 _H | PWC divider ratio control register 3 | DIVR3 | R/W | PWC timer 3 | ----- 0 0 |
| 000081 _H to 8D _H | (Reserved area) ^{*1} | | | | |

(Continued)

MB90220 Series

| Address | Register | Register name | Access | Resource name | Initial value |
|---|---|---------------|--------|-----------------------------------|---------------|
| 00008E _H | WI control register | WICR | R/W | Write-inhibit RAM | ---X--- |
| 00008F _H | (Reserved area) ^{*1} | | | | |
| 000090 _H to 9E _H | | | | | |
| 00009F _H | Delay interrupt source generation /release register | DIRR | R/W | Delay interrupt generation module | -----0 |
| 0000A0 _H | Standby control register | STBYC | R/W | Low power consumption | 0001**** |
| 0000A3 _H | Address mid-order control register | MACR | W | External pin | ##### |
| 0000A4 _H | Address higher-order control register | HACR | W | External pin | ##### |
| 0000A5 _H | External pin control register | EPCR | W | External pin | #0-0#00 |
| 0000A8 _H | Watchdog timer control register | WDTC | R/W | Watchdog timer | XXXXXXXX |
| 0000A9 _H | Timebase timer control register | TBTC | R/W | Timebase timer | ---00000 |
| 0000B0 _H | Interrupt control register 00 | ICR00 | R/W | Interrupt controller | 00000111 |
| 0000B1 _H | Interrupt control register 01 | ICR01 | R/W | | 00000111 |
| 0000B2 _H | Interrupt control register 02 | ICR02 | R/W | | 00000111 |
| 0000B3 _H | Interrupt control register 03 | ICR03 | R/W | | 00000111 |
| 0000B4 _H | Interrupt control register 04 | ICR04 | R/W | | 00000111 |
| 0000B5 _H | Interrupt control register 05 | ICR05 | R/W | | 00000111 |
| 0000B6 _H | Interrupt control register 06 | ICR06 | R/W | | 00000111 |
| 0000B7 _H | Interrupt control register 07 | ICR07 | R/W | | 00000111 |
| 0000B8 _H | Interrupt control register 08 | ICR08 | R/W | | 00000111 |
| 0000B9 _H | Interrupt control register 09 | ICR09 | R/W | | 00000111 |
| 0000BA _H | Interrupt control register 10 | ICR10 | R/W | | 00000111 |
| 0000BB _H | Interrupt control register 11 | ICR11 | R/W | | 00000111 |
| 0000BC _H | Interrupt control register 12 | ICR12 | R/W | | 00000111 |
| 0000BD _H | Interrupt control register 13 | ICR13 | R/W | | 00000111 |
| 0000BE _H | Interrupt control register 14 | ICR14 | R/W | | 00000111 |
| 0000BF _H | Interrupt control register 15 | ICR15 | R/W | | 00000111 |
| 0000C0 _H to FF _H | (External area) ^{*2} | | | | |
| 001F00 _H | PWC data buffer register 0 | PWCR0 | R/W | PWC timer 0 | 00000000 |
| 001F01 _H | | | | | 00000000 |

(Continued)

MB90220 Series

| Address | Register | Register name | Access | Resource name | Initial value |
|---|---|---------------|--------|-------------------|-----------------|
| 001F02 _H | PWC data buffer register 1 | PWCR1 | R/W | PWC timer 1 | 0 0 0 0 0 0 0 0 |
| 001F03 _H | | | | | 0 0 0 0 0 0 0 0 |
| 001F04 _H | PWC data buffer register 2 | PWCR2 | R/W | PWC timer 2 | 0 0 0 0 0 0 0 0 |
| 001F05 _H | | | | | 0 0 0 0 0 0 0 0 |
| 001F06 _H | PWC data buffer register 3 | PWCR3 | R/W | PWC timer 3 | 0 0 0 0 0 0 0 0 |
| 001F07 _H | | | | | 0 0 0 0 0 0 0 0 |
| 001F08 _H to 1F0F _H | (Reserved area)*1 | | | | |
| 001F10 _H | OCU compare lower-order data register 00 | CPR00L | R/W | Output compare 00 | 0 0 0 0 0 0 0 0 |
| 001F11 _H | | | | | 0 0 0 0 0 0 0 0 |
| 001F12 _H | OCU compare higher-order data register 00 | CPR00 | | | 0 0 0 0 0 0 0 0 |
| 001F13 _H | | | | | 0 0 0 0 0 0 0 0 |
| 001F14 _H | OCU compare lower-order data register 01 | CPR01L | R/W | Output compare 01 | 0 0 0 0 0 0 0 0 |
| 001F15 _H | | | | | 0 0 0 0 0 0 0 0 |
| 001F16 _H | OCU compare higher-order data register 01 | CPR01 | | | 0 0 0 0 0 0 0 0 |
| 001F17 _H | | | | | 0 0 0 0 0 0 0 0 |
| 001F18 _H | OCU compare lower-order data register 02 | CPR02L | R/W | Output compare 02 | 0 0 0 0 0 0 0 0 |
| 001F19 _H | | | | | 0 0 0 0 0 0 0 0 |
| 001F1A _H | OCU compare higher-order data register 02 | CPR02 | | | 0 0 0 0 0 0 0 0 |
| 001F1B _H | | | | | 0 0 0 0 0 0 0 0 |
| 001F1C _H | OCU compare lower-order data register 03 | CPR03L | R/W | Output compare 03 | 0 0 0 0 0 0 0 0 |
| 001F1D _H | | | | | 0 0 0 0 0 0 0 0 |
| 001F1E _H | OCU compare higher-order data register 03 | CPR03 | | | 0 0 0 0 0 0 0 0 |
| 001F1F _H | | | | | 0 0 0 0 0 0 0 0 |
| 001F20 _H | OCU compare lower-order data register 04 | CPR04L | R/W | Output compare 10 | 0 0 0 0 0 0 0 0 |
| 001F21 _H | | | | | 0 0 0 0 0 0 0 0 |
| 001F22 _H | OCU compare higher-order data register 04 | CPR04 | | | 0 0 0 0 0 0 0 0 |
| 001F23 _H | | | | | 0 0 0 0 0 0 0 0 |
| 001F24 _H | OCU compare lower-order data register 05 | CPR05L | R/W | Output compare 11 | 0 0 0 0 0 0 0 0 |
| 001F25 _H | | | | | 0 0 0 0 0 0 0 0 |
| 001F26 _H | OCU compare higher-order data register 05 | CPR05 | | | 0 0 0 0 0 0 0 0 |
| 001F27 _H | | | | | 0 0 0 0 0 0 0 0 |

(Continued)

MB90220 Series

| Address | Register | Register name | Access | Resource name | Initial value |
|---------------------|---|---------------|--------|-----------------------|-----------------|
| 001F28 _H | OCU compare lower-order data register 06 | CPR06L | R/W | Output compare 12 | 0 0 0 0 0 0 0 0 |
| 001F29 _H | | | | | 0 0 0 0 0 0 0 0 |
| 001F2A _H | OCU compare higher-order data register 06 | CPR06 | | | 0 0 0 0 0 0 0 0 |
| 001F2B _H | | | | | 0 0 0 0 0 0 0 0 |
| 001F2C _H | OCU compare lower-order data register 07 | CPR07L | R/W | Output compare 13 | 0 0 0 0 0 0 0 0 |
| 001F2D _H | | | | | 0 0 0 0 0 0 0 0 |
| 001F2E _H | OCU compare higher-order data register 07 | CPR07 | | | 0 0 0 0 0 0 0 0 |
| 001F2F _H | | | | | 0 0 0 0 0 0 0 0 |
| 001F30 _H | 16-bit timer register 0 | TMR0 | R | 16-bit reload timer 0 | XXXXXXXXXX |
| 001F31 _H | | | | | XXXXXXXXXX |
| 001F32 _H | 16-bit reload register 0 | TMRLR0 | W | | XXXXXXXXXX |
| 001F33 _H | | | | | XXXXXXXXXX |
| 001F34 _H | 16-bit timer register 1 | TMR1 | R | 16-bit reload timer 1 | XXXXXXXXXX |
| 001F35 _H | | | | | XXXXXXXXXX |
| 001F36 _H | 16-bit timer reload register 1 | TMRLR1 | W | | XXXXXXXXXX |
| 001F37 _H | | | | | XXXXXXXXXX |
| 001F38 _H | 16-bit timer register 2 | TMR2 | R | 16-bit reload timer 2 | XXXXXXXXXX |
| 001F39 _H | | | | | XXXXXXXXXX |
| 001F3A _H | 16-bit timer reload register 2 | TMRLR2 | W | | XXXXXXXXXX |
| 001F3B _H | | | | | XXXXXXXXXX |
| 001F3C _H | 16-bit timer register 3 | TMR3 | R | 16-bit reload timer 3 | XXXXXXXXXX |
| 001F3D _H | | | | | XXXXXXXXXX |
| 001F3E _H | 16-bit timer reload register 3 | TMRLR3 | W | | XXXXXXXXXX |
| 001F3F _H | | | | | XXXXXXXXXX |
| 001F40 _H | 16-bit timer register 4 | TMR4 | R | 16-bit reload timer 4 | XXXXXXXXXX |
| 001F41 _H | | | | | XXXXXXXXXX |
| 001F42 _H | 16-bit timer reload register 4 | TMRLR4 | W | | XXXXXXXXXX |
| 001F43 _H | | | | | XXXXXXXXXX |
| 001F44 _H | 16-bit timer register 5 | TMR5 | R | 16-bit reload timer 0 | XXXXXXXXXX |
| 001F45 _H | | | | | XXXXXXXXXX |
| 001F46 _H | 16-bit timer reload register 5 | TMRLR5 | W | | XXXXXXXXXX |
| 001F47 _H | | | | | XXXXXXXXXX |

(Continued)

MB90220 Series

(Continued)

| Address | Register | Register name | Access | Resource name | Initial value |
|---|----------------------------------|---------------|--------|--------------------|---------------|
| 001F48 _H | PPG cycle setting register 0 | PCSR0 | W | 16-bit PPG timer 0 | XXXXXXXXXX |
| 001F49 _H | | | | | XXXXXXXXXX |
| 001F4A _H | PPG duty setting register 0 | PDUT0 | W | | XXXXXXXXXX |
| 001F4B _H | | | | | XXXXXXXXXX |
| 001F4C _H | PPG cycle setting register 1 | PCSR1 | W | 16-bit PPG timer 1 | XXXXXXXXXX |
| 001F4D _H | | | | | XXXXXXXXXX |
| 001F4E _H | PPG duty setting register 1 | PDUT1 | W | | XXXXXXXXXX |
| 001F4F _H | | | | | XXXXXXXXXX |
| 001F50 _H | ICU lower-order data register 0 | ICRL0 | R | Input capture 0 | XXXXXXXXXX |
| 001F51 _H | | | | | XXXXXXXXXX |
| 001F52 _H | ICU higher-order data register 0 | ICRH0 | R | | XXXXXXXXXX |
| 001F53 _H | | | | | 00000000 |
| 001F54 _H | ICU lower-order data register 1 | ICRL1 | R | Input capture 1 | XXXXXXXXXX |
| 001F55 _H | | | | | XXXXXXXXXX |
| 001F56 _H | ICU higher-order data register 1 | ICRH1 | R | | XXXXXXXXXX |
| 001F57 _H | | | | | 00000000 |
| 001F58 _H | ICU lower-order data register 2 | ICRL2 | R | Input capture 2 | XXXXXXXXXX |
| 001F59 _H | | | | | XXXXXXXXXX |
| 001F5A _H | ICU higher-order data register 2 | ICRH2 | R | | XXXXXXXXXX |
| 001F5B _H | | | | | 00000000 |
| 001F5C _H | ICU lower-order data register 3 | ICRL3 | R | Input capture 3 | XXXXXXXXXX |
| 001F5D _H | | | | | XXXXXXXXXX |
| 001F5E _H | ICU higher-order data register 3 | ICRH3 | R | | XXXXXXXXXX |
| 001F5F _H | | | | | 00000000 |
| 001F60 _H to 1FFF _H | (Reserved area)*1 | | | | |

Initial value

0: The initial value of this bit is "0".

1: The initial value of this bit is "1".

X: The initial value of this bit is undefined.

–: This bit is not used. The initial value is undefined.

*: The initial value of this bit varies with the reset source.

#: The initial value of this bit varies with the operation mode.

*1: Access prohibited

*2: Only this area is open to external access in the area below address 0000FF_H (inclusive). All addresses which are not described in the table are reserved areas, and accesses to these areas are handled in the same manner as for internal areas. The access signal for the external bus is not generated.*3: When an external bus is enable mode, never access to registers which are not used as general ports in areas address 000000_H to 000005_H or 000010_H to 000015_H.

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■ INTERRUPT SOURCES AND INTERRUPT VECTORS/INTERRUPT CONTROL REGISTERS

| Interrupt source | EI ² OS support | Interrupt vector | | Interrupt control register | | |
|---|----------------------------|------------------|-----------------|----------------------------|---------|---------------------|
| | | No. | Address | ICR | Address | |
| Reset | × | #08 | 08 _H | FFFFDC _H | — | — |
| INT9 instruction | × | #09 | 09 _H | FFFFD8 _H | — | — |
| Exception | × | #10 | 0A _H | FFFFD4 _H | — | — |
| External interrupt #0 | △ | #11 | 0B _H | FFFFD0 _H | ICR00 | 0000B0 _H |
| External interrupt #1 | △ | #12 | 0C _H | FFFFCC _H | | |
| External interrupt #2 | △ | #13 | 0D _H | FFFFC8 _H | ICR01 | 0000B1 _H |
| Input capture 0 | △ | #14 | 0E _H | FFFFC4 _H | | |
| PWC0 count completed/overflow | △ | #15 | 0F _H | FFFFC0 _H | ICR02 | 0000B2 _H |
| PWC1 count completed/overflow/input capture 1 | △ | #16 | 10 _H | FFFFBC _H | | |
| PWC2 count completed/overflow/input capture 2 | △ | #17 | 11 _H | FFFFB8 _H | ICR03 | 0000B3 _H |
| PWC3 count completed/overflow/input capture 3 | △ | #18 | 12 _H | FFFFB4 _H | | |
| 24-bit timer, overflow | △ | #19 | 13 _H | FFFFB0 _H | ICR04 | 0000B4 _H |
| 24-bit timer, intermediate bit/timebase timer, interval interrupt | △ | #20 | 14 _H | FFFFAC _H | | |
| Compare 0 | △ | #21 | 15 _H | FFFFA8 _H | ICR05 | 0000B5 _H |
| Compare 1 | △ | #22 | 16 _H | FFFFA4 _H | | |
| Compare 2 | △ | #23 | 17 _H | FFFFA0 _H | ICR06 | 0000B6 _H |
| Compare 3 | △ | #24 | 18 _H | FFFF9C _H | | |
| Compare 4/6 | △ | #25 | 19 _H | FFFF98 _H | ICR07 | 0000B7 _H |
| Compare 5/7 | △ | #26 | 1A _H | FFFF94 _H | | |
| 16-bit timer 0/1/2, overflow/PPG0 | △ | #27 | 1B _H | FFFF90 _H | ICR08 | 0000B8 _H |
| 16-bit timer 3/4/5, overflow/PPG1 | △ | #28 | 1C _H | FFFF8C _H | | |
| 10-bit A/D converter count completed | □ | #29 | 1D _H | FFFF88 _H | ICR09 | 0000B9 _H |
| UART1 transmission completed | △ | #31 | 1F _H | FFFF80 _H | ICR10 | 0000BA _H |
| UART1 reception completed | △ | #32 | 20 _H | FFFF7C _H | | |
| UART0 (ch.1) transmission completed | △ | #33 | 21 _H | FFFF78 _H | ICR11 | 0000BB _H |
| UART0 (ch.2) transmission completed | △ | #34 | 22 _H | FFFF74 _H | | |
| UART0 (ch.1) reception completed | ○ | #35 | 23 _H | FFFF70 _H | ICR12 | 0000BC _H |
| UART0 (ch.2) reception completed | △ | #36 | 24 _H | FFFF6C _H | | |
| UART0 (ch.0) transmission completed | ◎ | #37 | 25 _H | FFFF68 _H | ICR13 | 0000BD _H |

(Continued)

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(Continued)

| Interrupt source | EI ² OS support | Interrupt vector | | Interrupt control register | | |
|-----------------------------------|----------------------------|------------------|-----------------|----------------------------|---------|---------------------|
| | | No. | Address | ICR | Address | |
| UART0 (ch.0) reception completed | ◎ | #39 | 27 _H | FFFF60 _H | ICR14 | 0000BE _H |
| Delay interrupt generation module | × | #42 | 2A _H | FFFF54 _H | ICR15 | 0000BF _H |
| Stack fault | × | #255 | FF _H | FFFC00 _H | — | — |

◎: EI²OS is supported (with stop request).

□: EI²OS is supported (without stop request).

○: EI²OS is supported; however, since two interrupt sources are allocated to a single ICR, in case EI²OS is used for one of the two, EI²OS and ordinary interrupt are not both available for the other (with stop request).

△: EI²OS is supported; however, since two interrupt sources are allocated to a single ICR, in case EI²OS is used for one of the two, EI²OS and ordinary interrupt are not both available for the other (without stop request).

×: EI²OS is not supported.

Note: Since the interrupt sources having interrupt vector Nos. 15 to 18, 20, and 25 to 28 are OR'ed, respectively, select them by means of the interrupt enable bits of each resource.

If EI²OS is used with the above-mentioned interrupt sources OR'ed with the interrupt vector Nos. 15 to 18, 20, and 25 to 28, be sure to activate one of the interrupt sources.

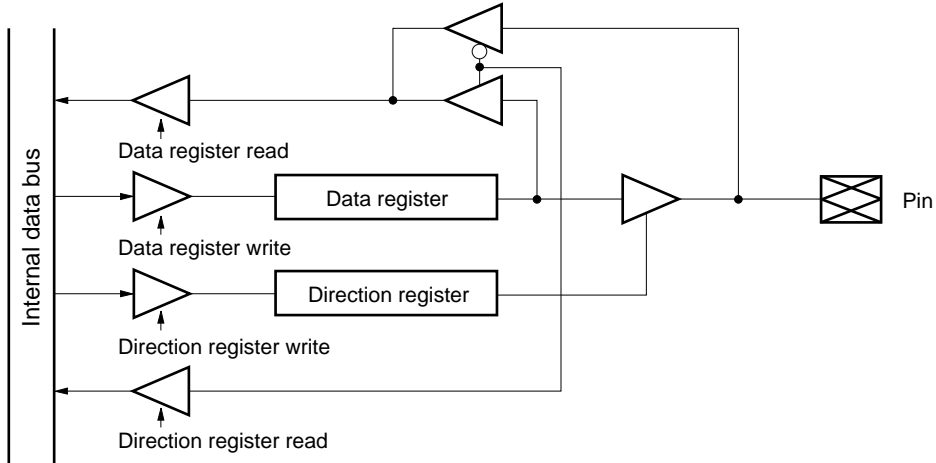
Also in this case, a request flag in the same series as the one interrupt source is likely to be cleared automatically by EI²OS.

Assume for example that an interrupt for compare 4 of the interrupt vector No. 25 is activated at this time by ICR07, so that the compare 6 is disabled. If EI²OS is activated at this time by ICR07, so that the compare 6 interrupt takes place during generation of or simultaneously with the compare 4 interrupt, not only the interrupt flag for the compare 4 but also that for the compare 6 will be automatically cleared after EI²OS is automatically transferred due to the compare 4 interrupt.

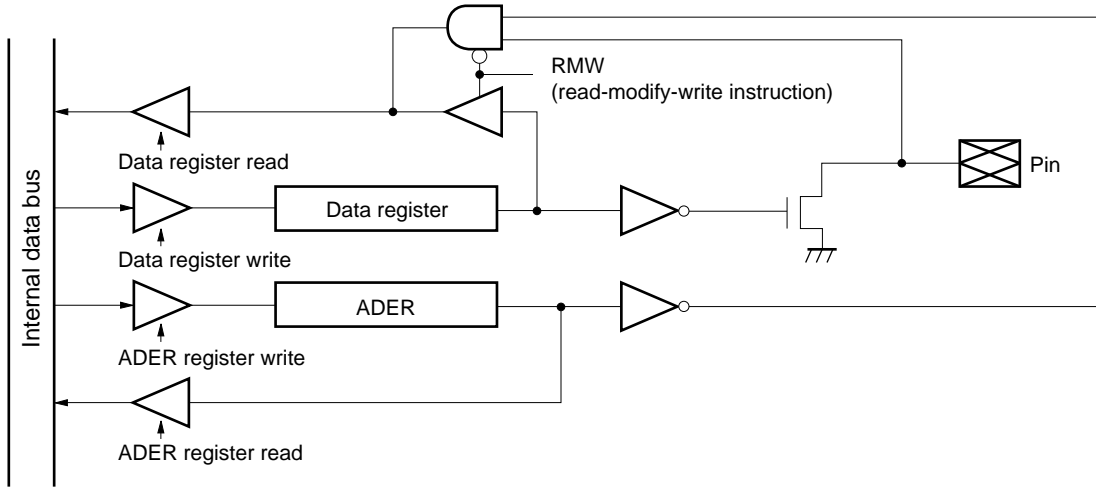
MB90220 Series

(2) Block Diagram

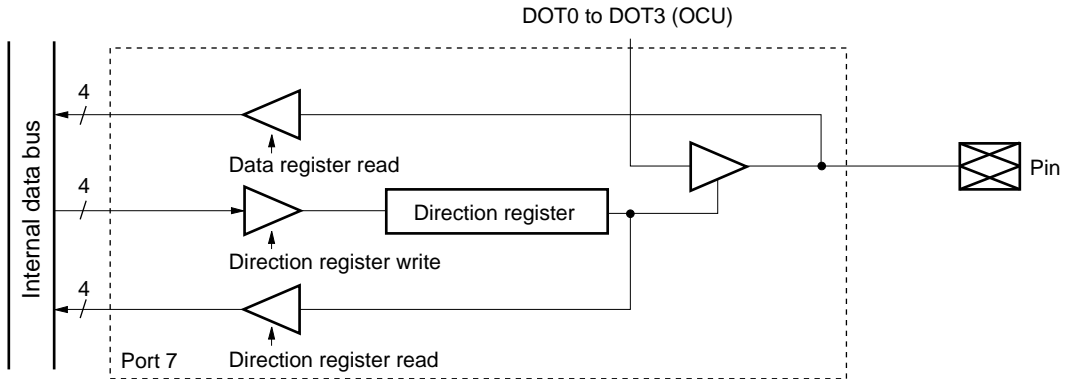
- I/O Port (Port 0 to 5, 8, and A to C)



- I/O Ports with an Open-drain output (Port 6, and 9)



- I/O Port (Port 7)



Note: Port 7 is input port. This pin also usable as I/O port for OCU internal function.

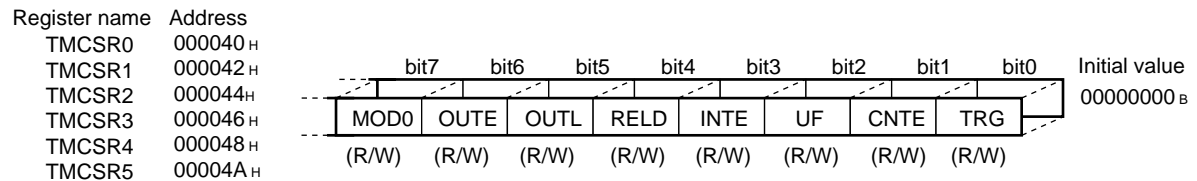
2. 16-bit Reload Timer (with Event Count Function)

The 16-bit reload timer 1 consists of a 16-bit down counter, a 16-bit reload register, an input pin (TIN), an output pin (TOT), and a control register. The input clock can be selected from among three internal clocks and one external clock. At the output pin (TOT), the pulses in the toggled output waveform are output in the reload mode; the rectangular pulses indicating that the timer is counting are in the single-shot mode. The input pin (TIN) can be used for event input in the event count mode, and for trigger input or gate input in the internal clock mode.

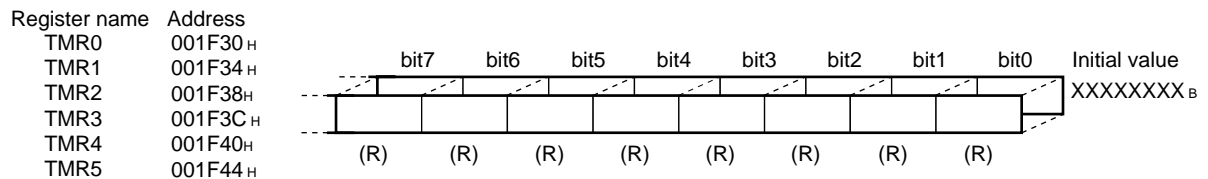
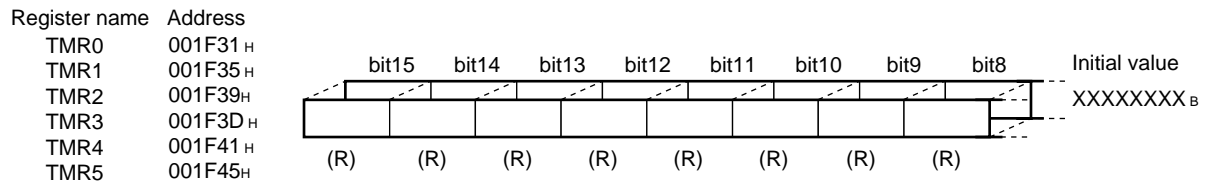
The MB90220 series has six channels for this timer.

(1) Register Configuration

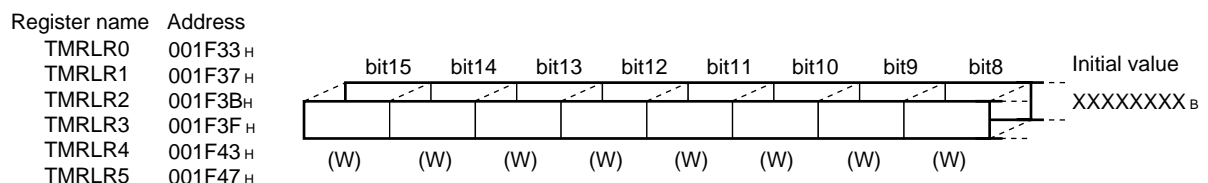
• Timer Control Status Register 0 to 5 (TMCSR0 to TMCSR5)



• 16-bit Timer Register 0 to 5 (TMR0 to TMR5)

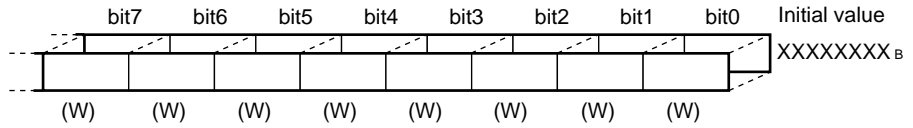


• 16-bit Timer Reload Register 0 to 5 (TMRLR0 to TMRLR5)

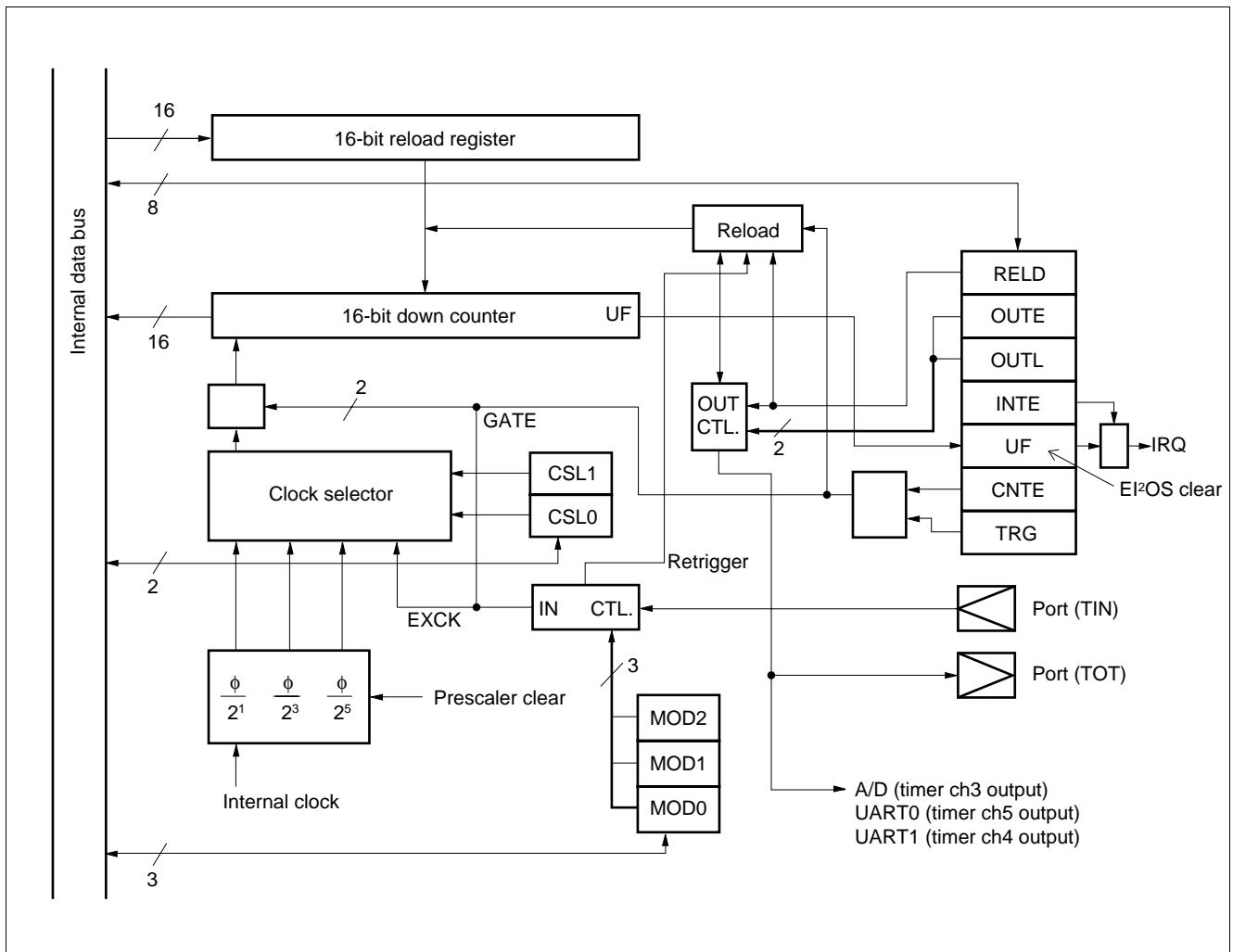


MB90220 Series

| Register name | Address |
|---------------|---------------------|
| TMRLR0 | 001F32 _H |
| TMRLR1 | 001F36 _H |
| TMRLR2 | 001F3A _H |
| TMRLR3 | 001F3E _H |
| TMRLR4 | 001F42 _H |
| TMRLR5 | 001F46 _H |



(2) Block Diagram



3. UART0

UART0 is a serial I/O port for synchronous or asynchronous communication with external resources. It has the following features:

- Full duplex double buffer
- CLK synchronous and CLK asynchronous data transfers capable
- Multiprocessor mode support (Mode 2)
- Built-in dedicated baud-rate generator (12 rates)
- Arbitrary baud-rate setting from external clock input or internal timer
- Variable data length (7 to 9 bits (without parity bit); 6 to 8 bits (with parity bit))
- Error detection function (Framing, overrun, parity)
- Interrupt function (Two sources for transmission and reception)
- Transfer in NRZ format

The MB90220 has three of these modules on chip.

(1) Register Configuration

• Mode Control Register 0 to 2 (UMC0 to UMC2)

Serial mode control register

| Register name | Address | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Initial value |
|---------------|---------------------|-------|-------|-------|-------|-------|-------|-------|-------|----------------------|
| UMC0 | 000020 _H | | | | | | | | | 0000100 _B |
| UMC1 | 000024 _H | PEN | SBL | MC1 | MC0 | SMDE | RFC | SCKE | SOE | |
| UMC2 | 000028 _H | | | | | | | | | |
| | | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | |

• Status Register 0 to 2 (USR0 to USR2)

| Register name | Address | bit15 | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 | Initial value |
|---------------|---------------------|-------|-------|-------|-------|-------|-------|------|------|-----------------------|
| USR0 | 000021 _H | | | | | | | | | 00001000 _B |
| USR1 | 000025 _H | RDRF | ORFE | PE | TDRE | RIE | TIE | RBF | TBF | |
| USR2 | 000029 _H | | | | | | | | | |
| | | (R) | (R) | (R) | (R) | (R/W) | (R/W) | (R) | (R) | |

• Input Data Register 0 to 2 (UIDR0 to UIDR2)/Output Data Register 0 to 2 (UODR0 to UODR2)

| Register name | Address | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Initial value |
|---------------|---------------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------------------|
| UIDR0/UODR0 | 000022 _H | | | | | | | | | XXXXXXXX _B |
| UIDR1/UODR1 | 000026 _H | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| UIDR2/UODR2 | 00002A _H | | | | | | | | | |
| | | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | |

• Rate and Data Register 0 to 2 (URD0 to URD2)

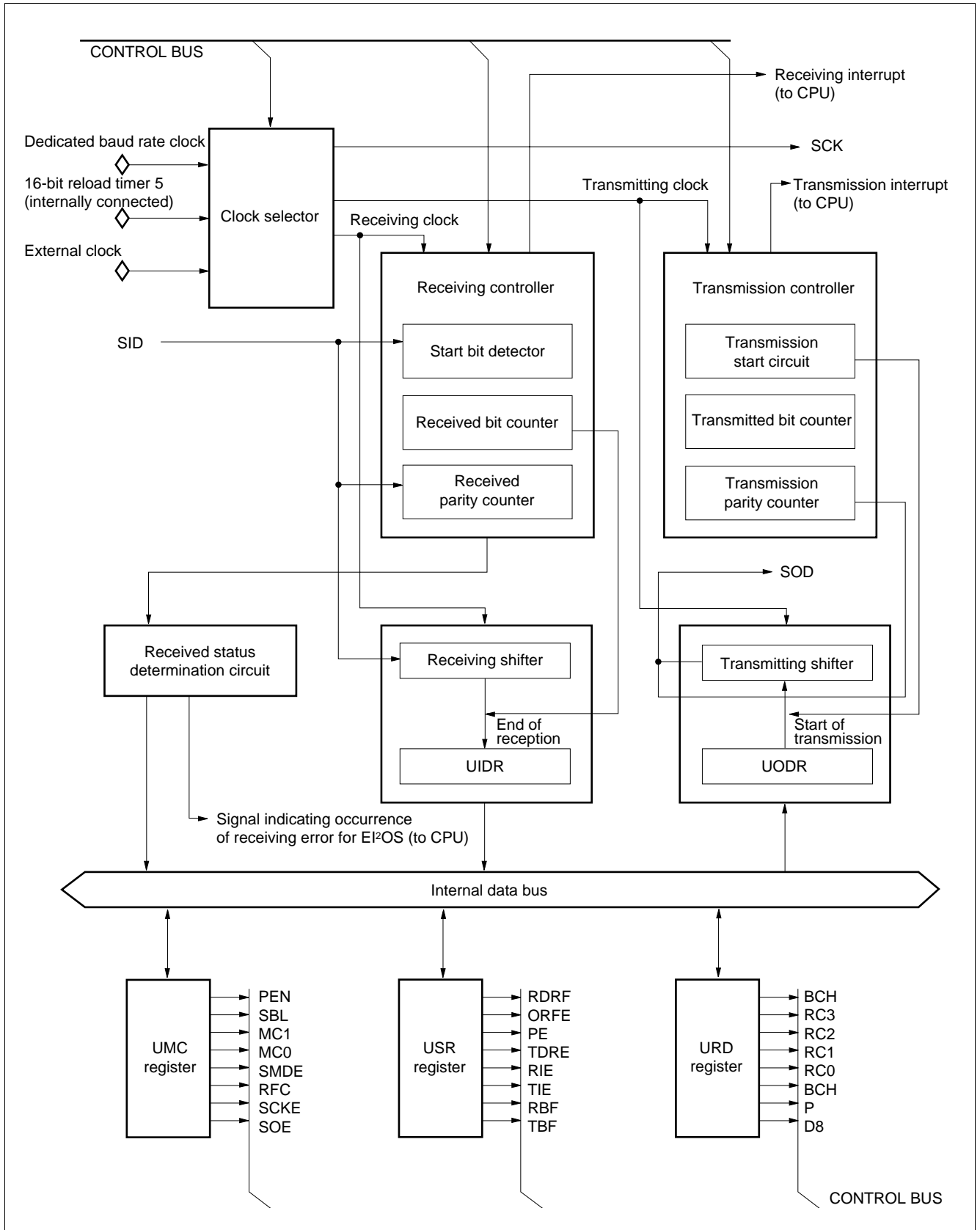
| Register name | Address | bit15 | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 | Initial value |
|---------------|---------------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------------------|
| URD0 | 000023 _H | | | | | | | | | 0000000X _B |
| URD1 | 000027 _H | BCH | RC3 | RC2 | RC1 | RC0 | BCH0 | P | D8 | |
| URD2 | 00002B _H | | | | | | | | | |
| | | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | |

• UART CTS Control Register (UCCR)

| Register name | Address | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Initial value |
|---------------|---------------------|------|------|------|-------|-------|-------|------|------|--------------------------|
| UCCR | 00002C _H | — | — | — | CTE | CSP | CTSE | — | — | --- 000 --- _B |
| | | (—) | (—) | (—) | (R/W) | (R/W) | (R/W) | (—) | (—) | |

MB90220 Series

(2) Block Diagram



4. UART1

The UART1 is a serial I/O port for asynchronous communications (start-stop synchronization) or CLK synchronized communications. It has the following features:

- Full-duplex double buffering
- Permits asynchronous (start-stop synchronization) and CLK synchronous communications
- Multiprocessor mode support
- Built-in dedicated baud rate generator
 - Asynchronous: 9615, 31250, 4808, 2404, and 1202 bps
 - CLK synchronization: 1 M, 500 K, 250 K bps
- Arbitray baud-rate setting from external clock input or internal timer
- Error detection function (parity errors, framing errors, and overrun errors)
- Transfer in format NRZ
- Extended supports intelligent I/O service

(1) Register Configuration

• Mode Register (SMR)

| Register name | Address | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Initial value |
|---------------|---------------------|-------|-------|-------|-------|-------|-------|-------|-------|----------------------|
| SMR | 00002E _H | MD1 | MD0 | CS2 | CS1 | CS0 | BCH | SCKE | SOE | 0000000 _B |
| | | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | |

• SCR (Control Register)

| Register name | Address | bit15 | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 | Initial value |
|---------------|---------------------|-------|-------|-------|-------|-------|-------|-------|-------|----------------------|
| SCR | 00002F _H | PEN | P | SBL | CL | A/D | REC | RXE | TXE | 0000010 _B |
| | | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R) | (R/W) | (R/W) | |

• Input Data Register (SIDR)/Serial Output Data Register (SODR)

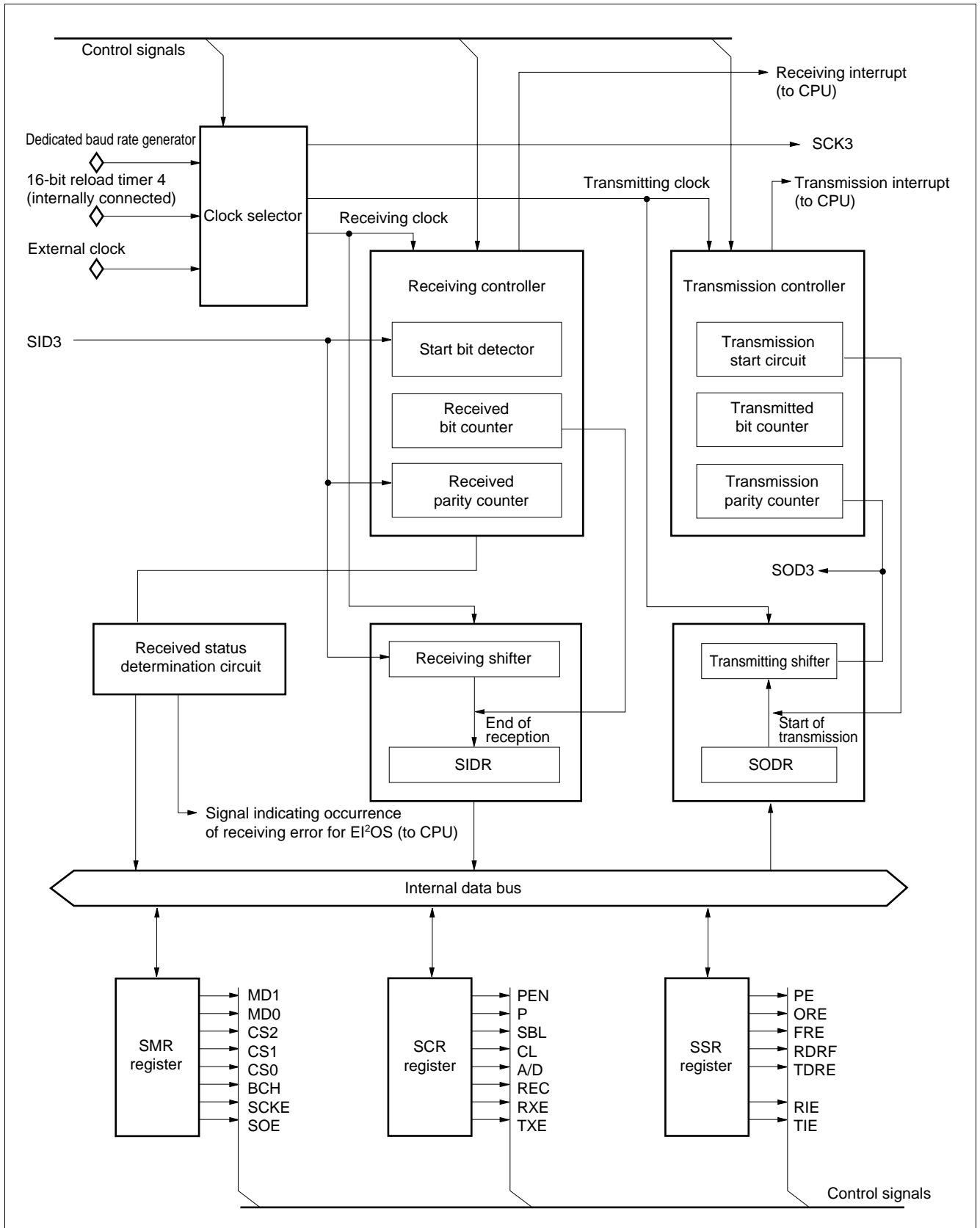
| Register name | Address | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Initial value |
|---------------|---------------------|------|------|------|------|------|------|------|------|-----------------------|
| SIDR | 000030 _H | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | XXXXXXXX _B |
| | | (R) | (R) | (R) | (R) | (R) | (R) | (R) | (R) | |
| Register name | Address | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Initial value |
| SODR | 000030 _H | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | XXXXXXXX _B |
| | | (W) | (W) | (W) | (W) | (W) | (W) | (W) | (W) | |

• SSR (Status Register)

| Register name | Address | bit15 | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 | Initial value |
|---------------|---------------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------------------|
| SSR | 000031 _H | PE | ORE | FRE | RDRF | TDRE | — | RIE | TIE | 00001-00 _B |
| | | (R) | (R) | (R) | (R) | (R) | | (R/W) | (R/W) | |

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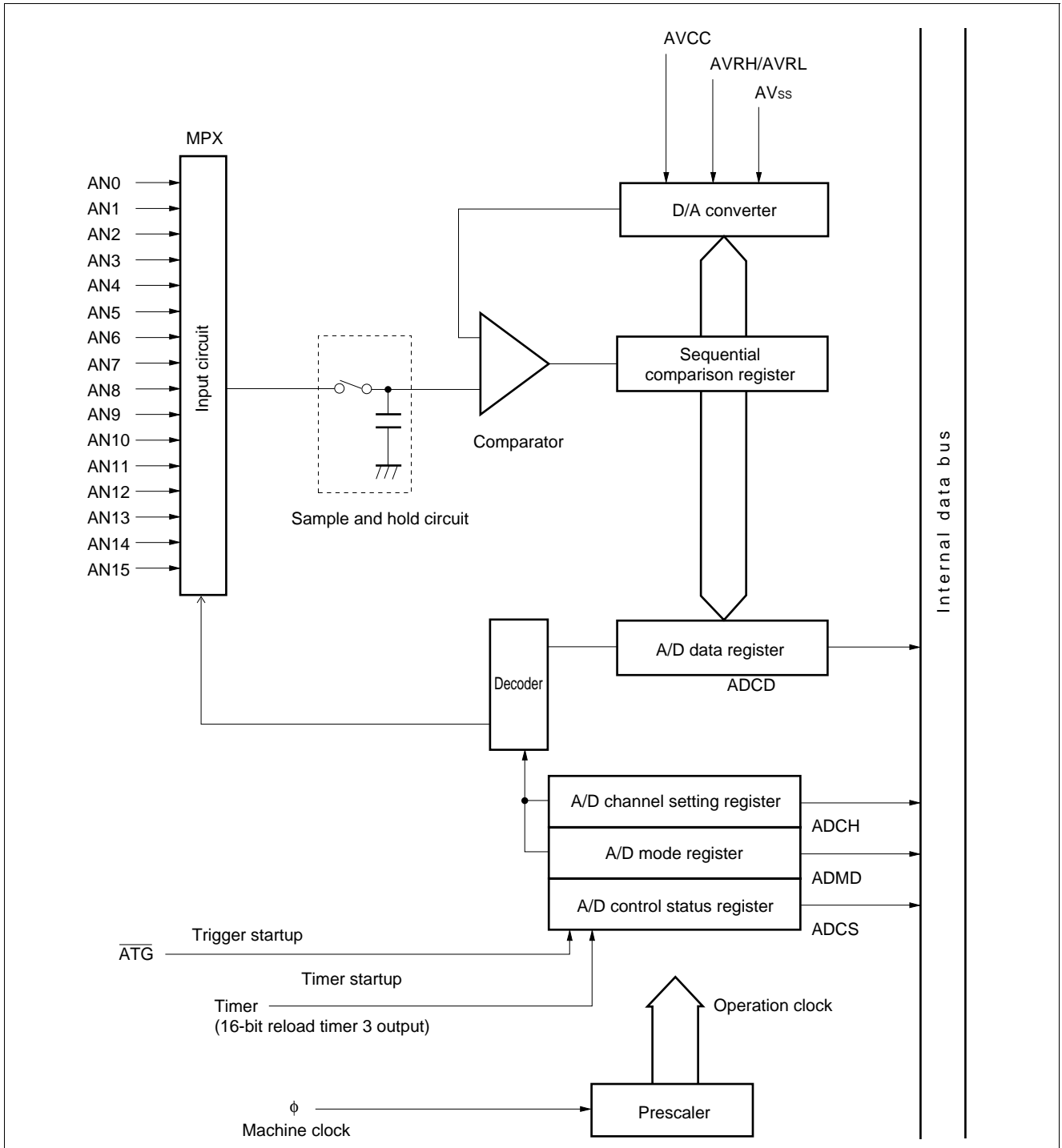
(2) Block Diagram



MB90220 Series

| Register name | Address | bit15 | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 | Initial value |
|---------------|---------|-------|-------|-------|-------|-------|-------|------|------|-----------------------|
| ADCD | 000037H | — | — | — | — | — | — | D9 | D8 | 000000XX _B |
| | | (R) | (R) | (R) | (R) | (R) | (R) | (R) | (R) | |

(2) Block Diagram

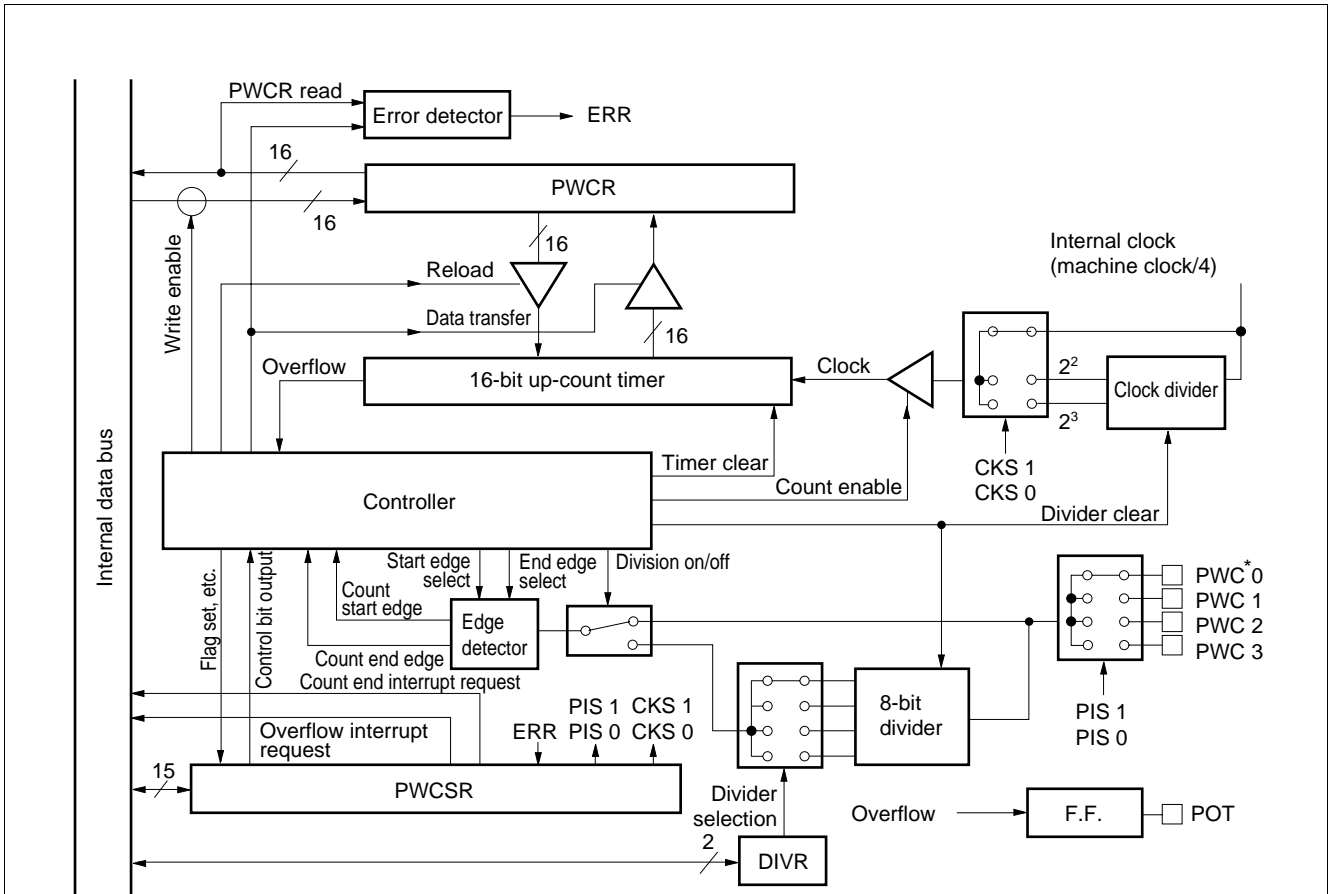


MB90220 Series

• PWC Division Ratio Control Register 0 to 3 (DIVR0 to DIVR3)

| Register name | Address | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Initial value |
|---------------|---------------------|------|------|------|------|------|------|-------|-------|-----------------|
| DIVR0 | 00007A _H | --- | --- | --- | --- | --- | --- | MOD1 | MOD0 | 00 _b |
| DIVR1 | 00007C _H | (-) | (-) | (-) | (-) | (-) | (-) | (R/W) | (R/W) | |
| DIVR2 | 00007E _H | | | | | | | | | |
| DIVR3 | 000080 _H | | | | | | | | | |

(2) Block Diagram



*: In the MB90220 series, only the module input PWC 0 of each channel is connected to the respective external pins.

| Channel | POT pin |
|-----------|------------------------|
| PWC ch. 0 | PA 1/PWC 0/POT 0 |
| PWC ch. 1 | PA 2/PWC 1/POT 1/ASR 1 |
| PWC ch. 2 | PA 3/PWC 2/POT 2/ASR 2 |
| PWC ch. 3 | PA 4/PWC 3/POT 3/ASR 3 |

7. DTP/External Interrupts

DTP (Data Transfer Peripheral) is located between external peripherals and the F²MC-16F CPU. It receives a DMA request or an interrupt request generated by the external peripherals and reports it to the F²MC-16F CPU to activate the extended intelligent I/O service or interrupt handler. The user can select two request levels of “H” and “L” for extended intelligent I/O service or, and four request levels of “H,” “L,” rising edge and falling edge for external interrupt requests. In MB90220, only parts corresponding to INT2 to INT0 are usable as external interrupt/DTP request.

Parts corresponding to INT7 to INT3 cannot be used as external interrupt/DTP request, but only for edge detection at external terminals.

Note: INT7 to INT3 are not usable as DTP/external interrupts.

(1) Register Configuration

• DTP/Interrupt Enable Register (ENIR)

| Register name | Address | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Initial value |
|---------------|---------------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------------------|
| ENIR | 00003A _H | EN7 | EN6 | EN5 | EN4 | EN3 | EN2 | EN1 | EN0 | 00000000 _B |
| | | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | |

• DTP/Interrupt Source Register (EIRR)

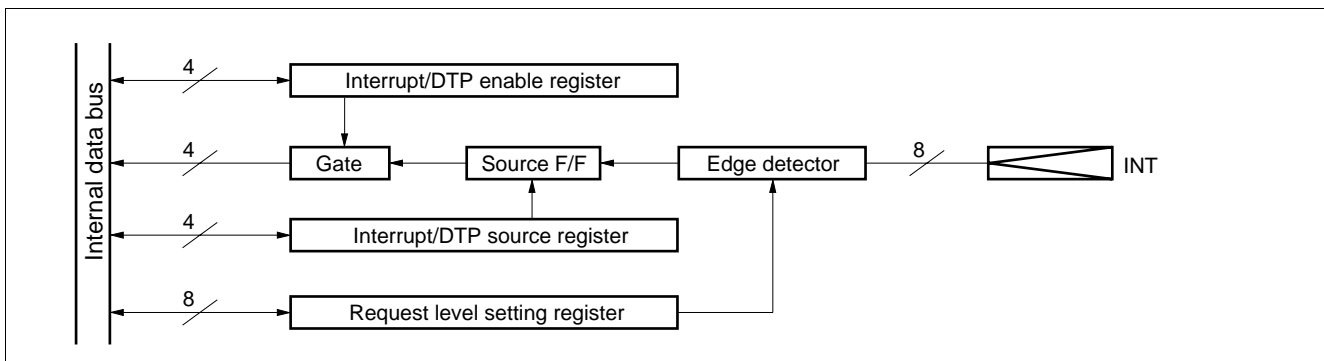
| Register name | Address | bit15 | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 | Initial value |
|---------------|---------------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------------------|
| EIRR | 00003B _H | ER7 | ER6 | ER5 | ER4 | ER3 | ER2 | ER1 | ER0 | 00000000 _B |
| | | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | |

• Request Level Setting Register (ELVR)

| Register name | Address | bit15 | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 | Initial value |
|---------------|---------------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------------------|
| ELVR | 00003D _H | LB7 | LA7 | LB6 | LA6 | LB5 | LA5 | LB4 | LA4 | 00000000 _B |
| | | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | |

| Register name | Address | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Initial value |
|---------------|---------------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------------------|
| ELVR | 00003C _H | LB3 | LA3 | LB2 | LA2 | LB1 | LA1 | LB0 | LA0 | 00000000 _B |
| | | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | |

(2) Block Diagram



MB90220 Series

8. 24-bit Timer Counter

The 24-bit timer counter consists of a 24-bit up-counter, an 8-bit output buffer register, and a control register. The count value output by this timer counter is used to generate the base time used for input capture and output compare.

The interrupt functions provided are timer overflow interrupts and timer intermediate bit interrupts. The intermediate bit interrupt permits four time settings.

The 24-bit timer counter value is cleared to all zeroes by a reset.

(1) Register Configuration

• Free-run Timer Control Register (TCCR)

| Register name | Address | bit15 | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 | Initial value |
|---------------|---------------------|-------|-------|----------|----------|----------|----------|----------|-------|------------------------|
| TCCR | 000071 _H | — | — | Reserved | Reserved | Reserved | Reserved | Reserved | PR0 | -- 111111 _B |
| | | (—) | (—) | (W) | (W) | (R/W) | (R/W) | (R/W) | (R/W) | |

| Register name | Address | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Initial value |
|---------------|---------------------|------|------|-------|-------|-------|-------|-------|-------|-----------------------|
| TCCR | 000070 _H | CLR2 | CLR | IVF | IVFE | TIM | TIME | TIS1 | TIS0 | 11000000 _B |
| | | (W) | (W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | |

• Free-run Timer Low-order Data Register (TCRL)

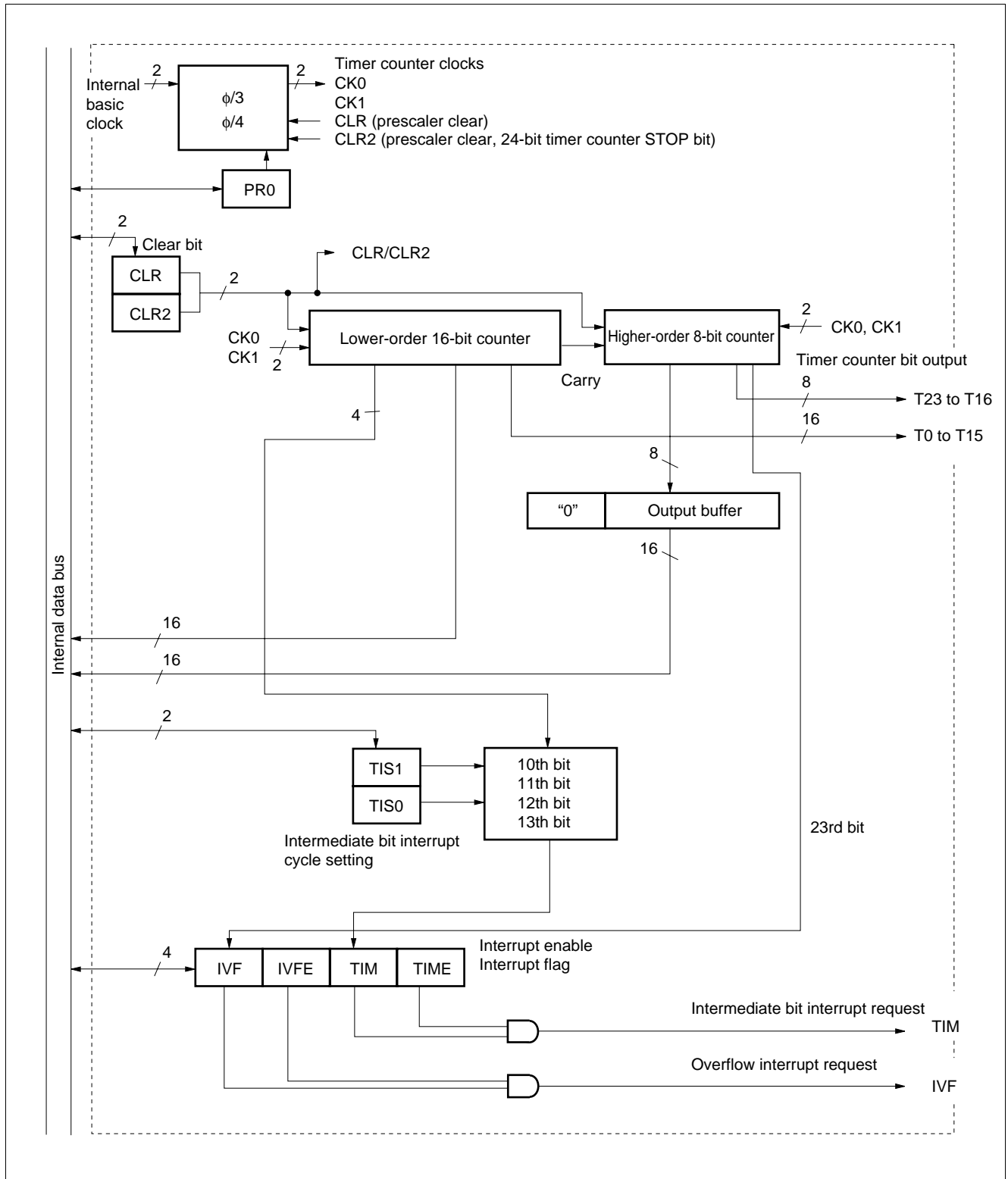
| Register name | Address | bit15 | bit0 | Initial value | Access |
|---------------|--|-------|------|-----------------------|--------|
| TCRL | 000072 _H 000073 _H | TCRL | | 00000000 _B | R |

• Free-run Timer High-order Data Register (TCRH)

| Register name | Address | bit15 | bit8 | bit7 | bit0 | Initial value | Access |
|---------------|--|-------|------|------|------|-----------------------|--------|
| TCRH | 000074 _H 000075 _H | — | | TCRH | | 00000000 _B | R |

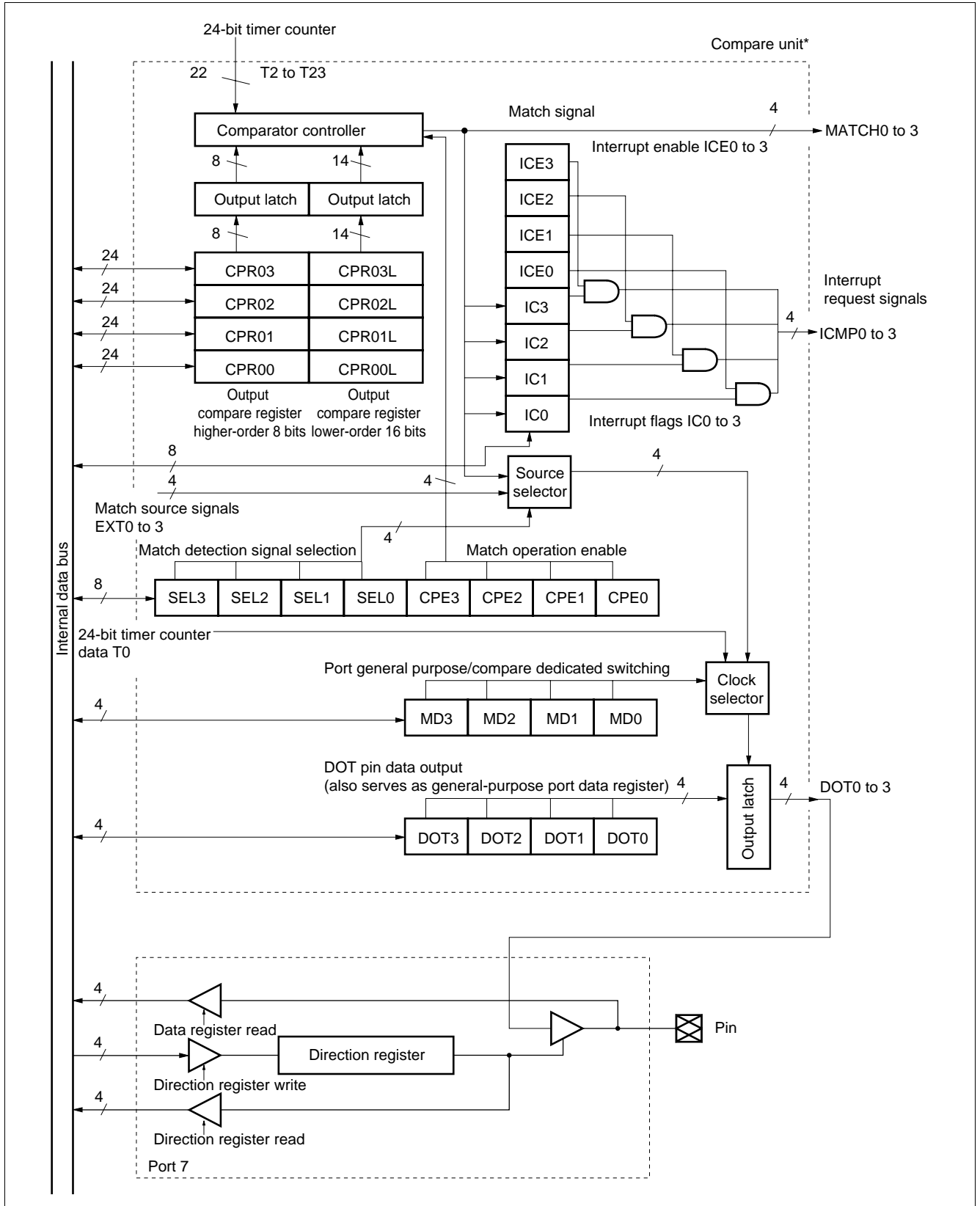
MB90220 Series

(2) Block Diagram



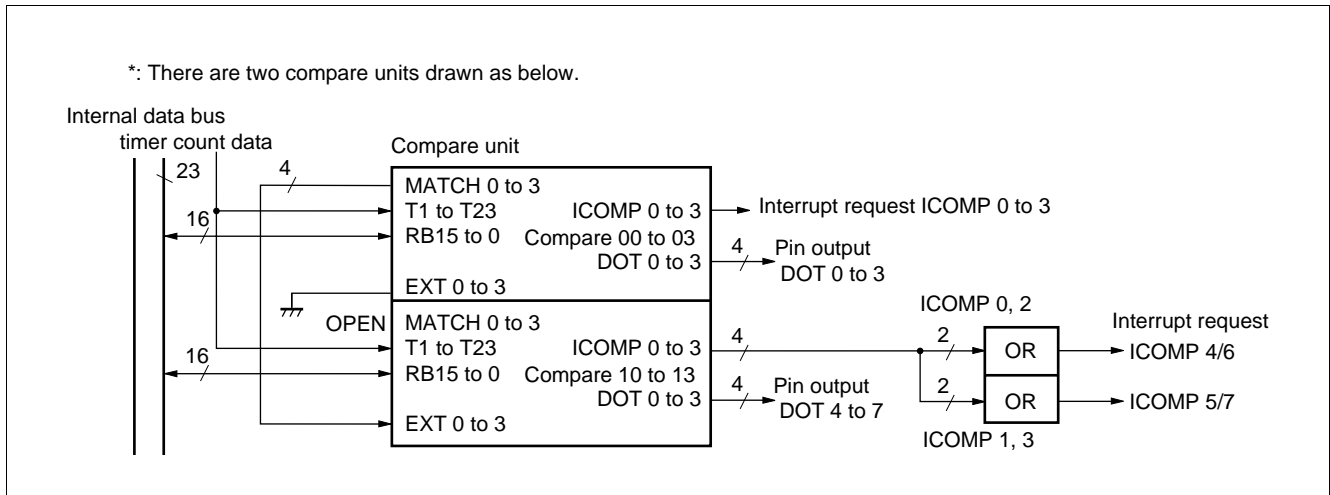
MB90220 Series

(2) Block Diagram



(Continued)

(Continued)



MB90220 Series

10. ICU (Input Capture Unit)

This module detects either the rising edge, falling edge, or both edges of an externally input waveform and holds the value of the 24-bit timer counter at that time, while at the same time the module generates an interrupt request for the CPU. The module consists of a 24-bit input capture data register and a control register. There are four external input pins (ASR0 to ASR3); the operation of each input is described below.

ASR0 to ASR3: Each of these input pins has a corresponding input capture register. When the specified valid edge (\uparrow or \downarrow or $\uparrow\downarrow$) is detected, the register can be used to store the 24-bit timer counter value.

(1) Register Configuration

• ICU Control Register 0 (ICC0)

| Register name | Address | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Initial value |
|---------------|---------------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------------------|
| ICC0 | 000058 _H | EG3B | EG3A | EG2B | EG2A | EG1B | EG1A | EG0B | EG0A | 00000000 _B |
| | | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | |

• ICU Control Register 1 (ICC1)

| Register name | Address | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Initial value |
|---------------|---------------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------------------|
| ICC1 | 00005A _H | IRE3 | IRE2 | IRE1 | IRE0 | IR3 | IR2 | IR1 | IR0 | 00000000 _B |
| | | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | |

• ICU Low-order Data Register (ICRL0 to ICRL3)

| Register name | Address | bit15 | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 | Initial value |
|---------------|---------------------|-------|-------|-------|-------|-------|-------|------|------|-----------------------|
| ICRL0 | 001F50 _H | | | | | | | | | XXXXXXXX _B |
| ICRL1 | 001F54 _H | | | | | | | | | |
| ICRL2 | 001F58 _H | | | | | | | | | |
| ICRL3 | 001F5C _H | | | | | | | | | |

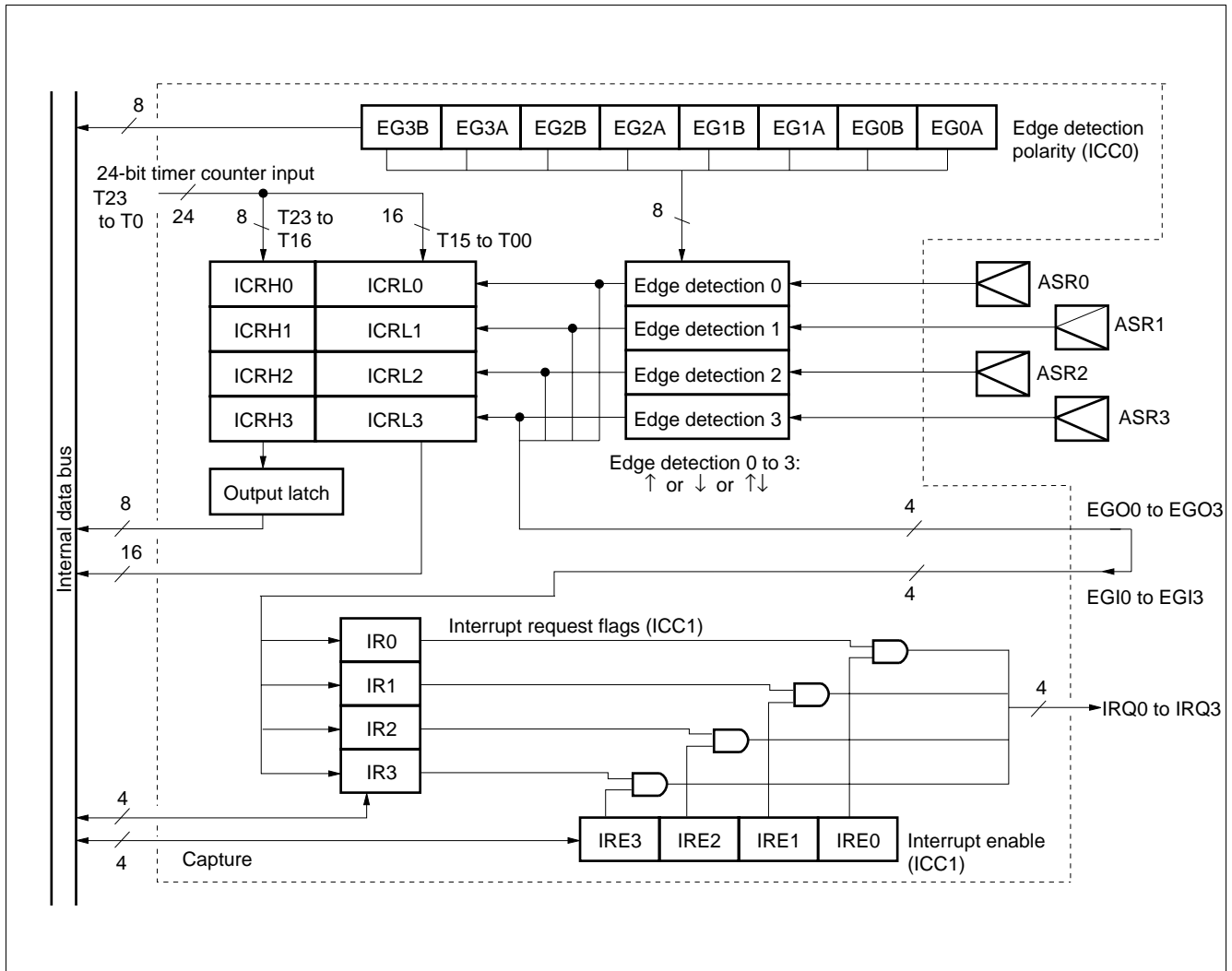
| Register name | Address | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Initial value |
|---------------|---------------------|------|------|------|------|------|------|------|------|-----------------------|
| ICRL0 | 001F51 _H | | | | | | | | | XXXXXXXX _B |
| ICRL1 | 001F55 _H | | | | | | | | | |
| ICRL2 | 001F59 _H | | | | | | | | | |
| ICRL3 | 001F5D _H | | | | | | | | | |

• ICU High-order Data Register (ICRH0 to ICRH3)

| Register name | Address | bit15 | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 | Initial value |
|---------------|---------------------|-------|-------|-------|-------|-------|-------|------|------|-----------------------|
| ICRH0 | 001F52 _H | | | | | | | | | XXXXXXXX _B |
| ICRH1 | 001F56 _H | | | | | | | | | |
| ICRH2 | 001F5A _H | | | | | | | | | |
| ICRH3 | 001F5E _H | | | | | | | | | |

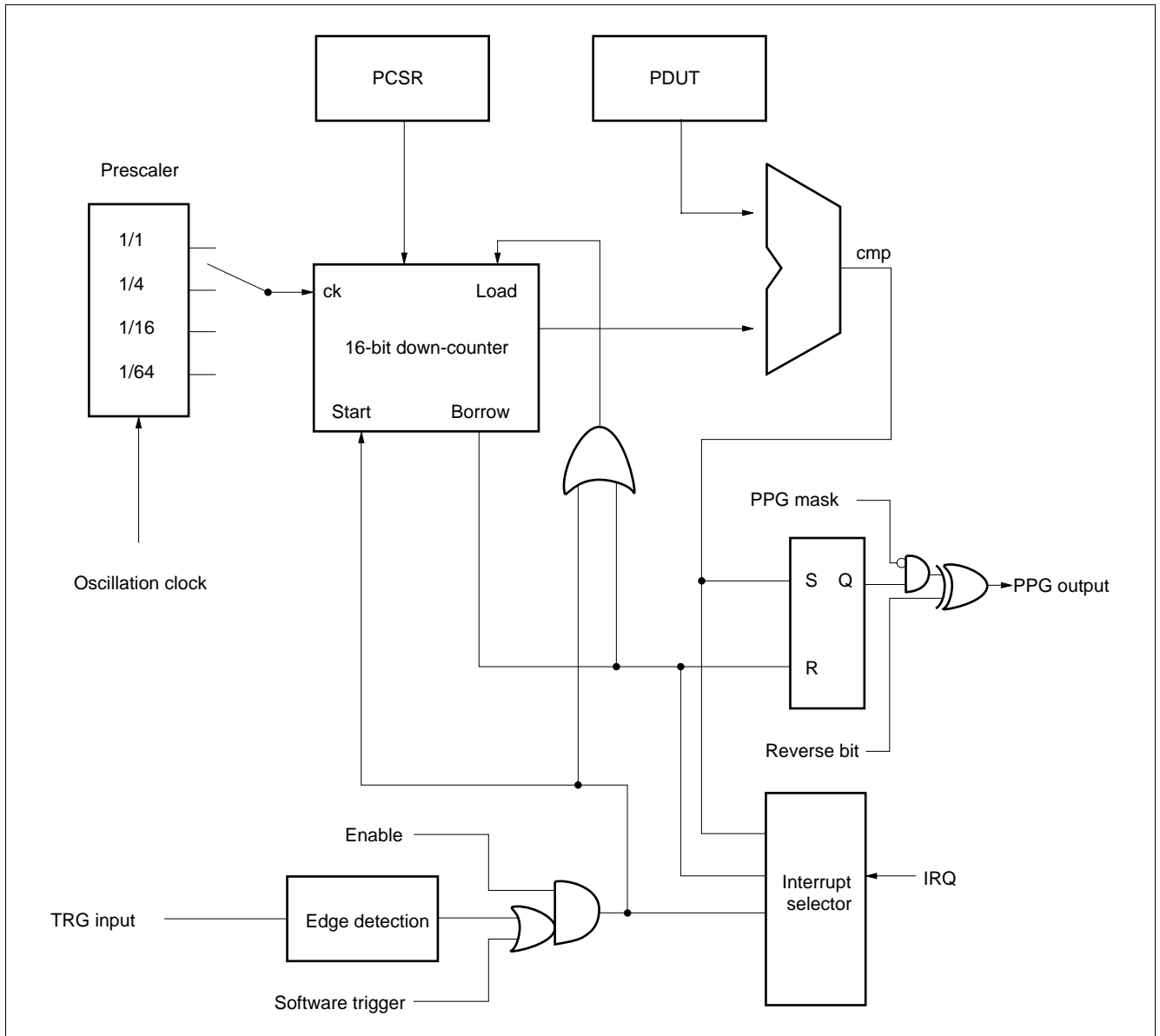
| Register name | Address | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Initial value |
|---------------|---------------------|------|------|------|------|------|------|------|------|-----------------------|
| ICRH0 | 001F53 _H | | | | | | | | | 00000000 _B |
| ICRH1 | 001F57 _H | | | | | | | | | |
| ICRH2 | 001F5B _H | | | | | | | | | |
| ICRH3 | 001F5F _H | | | | | | | | | |

(2) Block Diagram



MB90220 Series

(2) Block Diagram



MB90220 Series

12. Watchdog Timer and Timebase Timer Functions

The watchdog timer consists of a 2-bit watchdog counter using carry from an 18-bit timebase timer as the clock source, a control register, and a watchdog reset control section. The timebase timer consists of an 18-bit timer and an interval interrupt control circuit.

(1) Register Configuration

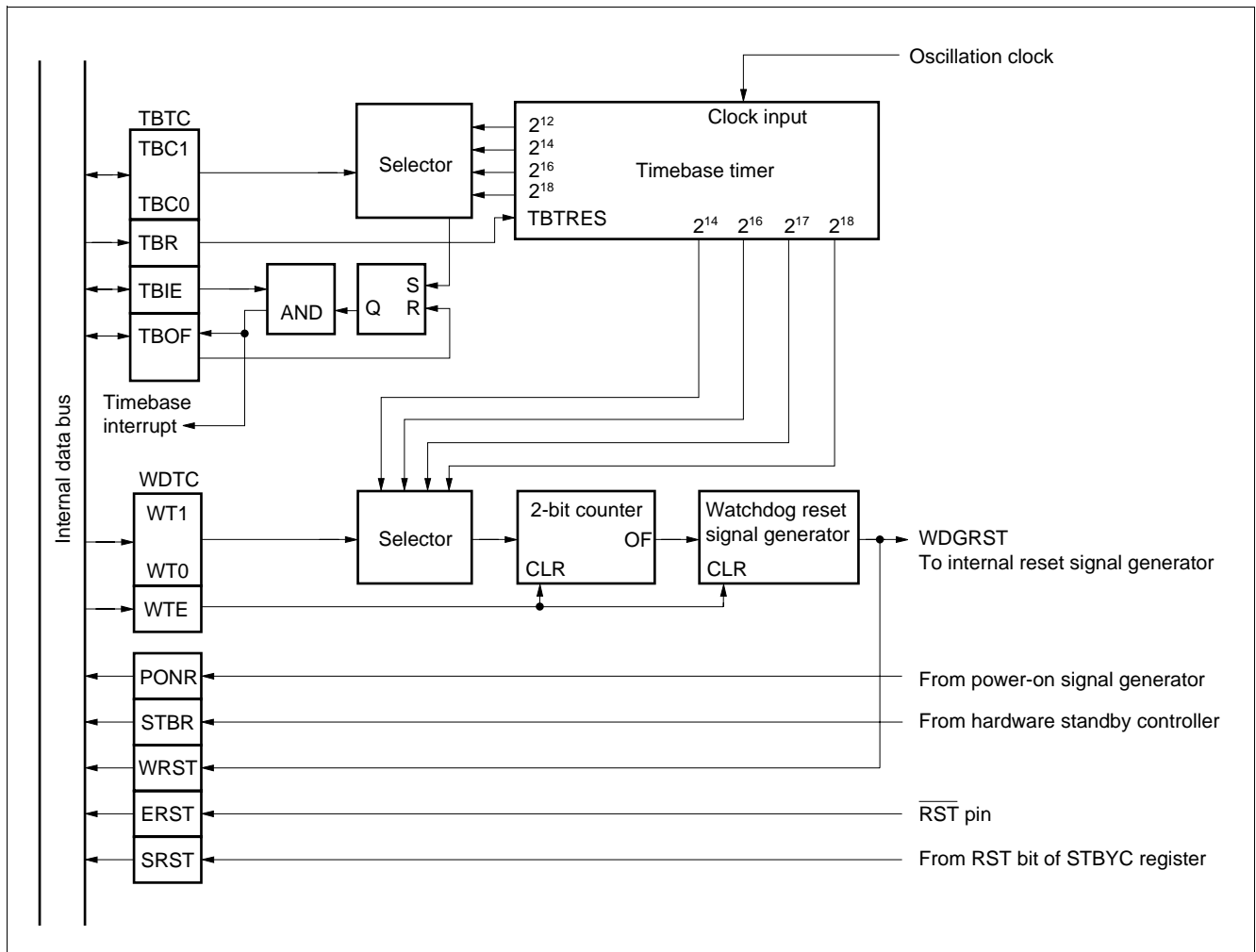
• Watchdog Timer Control Register (WDTC)

| Register name | Address | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Initial value |
|---------------|---------------------|------|------|------|------|------|------|------|------|---------------|
| WDTC | 0000A8 _H | PONR | STBR | WRST | ERST | SRST | WTE | WT1 | WT0 | XXXXXXXX |
| | | (R) | (R) | (R) | (R) | (R) | (W) | (W) | (W) | |

• Timebase Timer Control Register (TBTC)

| Register name | Address | bit15 | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 | Initial value |
|---------------|---------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| TBTC | 0000A9 _H | — | — | — | TBIE | TBOF | TBR | TBC1 | TBC0 | --- XXXXX |
| | | (—) | (—) | (—) | (R/W) | (R/W) | (R) | (R/W) | (R/W) | |

(2) Block Diagram



13. Delay Interrupt Generation Module

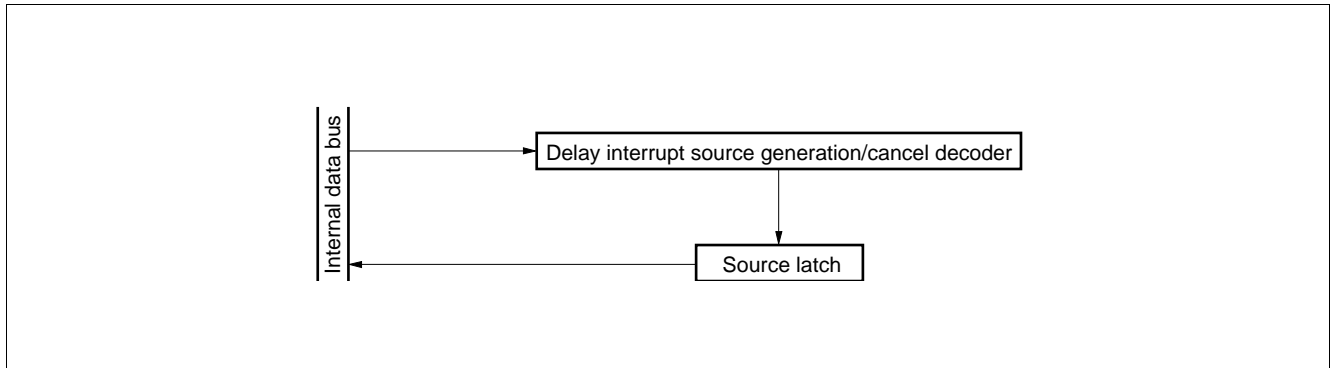
The delayed interrupt generation module is used to generate an interrupt task switching. Using this module allows an interrupt request to the F²MC-16F CPU to generated or cancel by software.

(1) Register Configuration

- Delay Interrupt Source Generation/Cancel Register (DIRR)

| Register name | Address | bit15 | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 | Initial value |
|---------------|---------------------|-------|-------|-------|-------|-------|-------|------|-------|---------------|
| DIRR | 00009F _H | — | — | — | — | — | — | — | R0 | 0 |
| | | (—) | (—) | (—) | (—) | (—) | (—) | (—) | (R/W) | |

(2) Block Diagram



MB90220 Series

14. Write-inhibit RAM

The write-inhibit RAM is write-protectable with the \overline{WI} pin input. Maintaining the “L” level input to the \overline{WI} pin prevents a certain area of RAM from being written. The \overline{WI} pin has a 4-machine-cycle filter.

(1) Register Configuration

- **WI Control Register (WICR)**

| Register name | Address | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Initial value |
|---------------|---------------------|------|------|------|-------|------|------|------|------|---------------|
| WICR | 00008E _H | — | — | — | WI | — | — | — | — | ---X--- |
| | | (—) | (—) | (—) | (R/W) | (—) | (—) | (—) | (—) | |

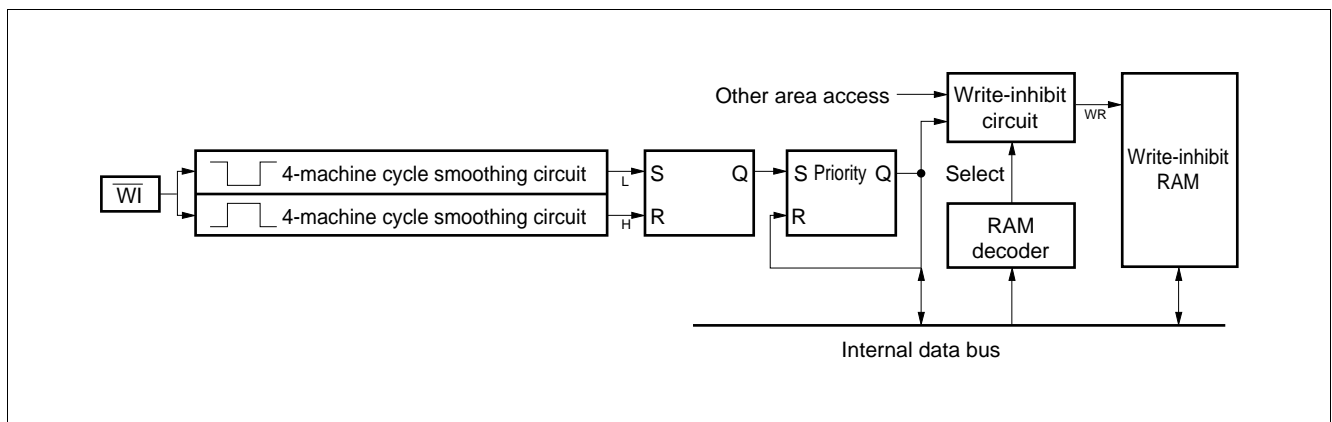
(2) Write-inhibit RAM Areas

Write-inhibit RAM areas: 000D00_H to 000EFF_H (MB90223)

001300_H to 0014FF_H (MB90224/P224A/P224B/W224A/W224B)

001500_H to 0018FF_H (MB90V220)

(3) Block Diagram



15. Low-power Consumption Modes, Oscillation Stabilization Delay Time, and Gear Function

The MB90220 series has three low-power consumption modes: the sleep mode, the stop mode, the hardware standby mode, and gear function.

Sleep mode is used to suspend only the CPU operation clock; the other components remain in operation. Stop mode and hardware standby mode stop oscillation, minimizing the power consumption while holding data.

The gear function divides the external clock frequency, which is used usually as it is, to provide a lower machine clock frequency. This function can therefore lower the overall operation speed without changing the oscillation frequency. The function can select the machine clock as a division of the frequency of crystal oscillation or external clock input by 1, 2, 4, or 16.

The OSC1 and OSC0 bits can be used to set the oscillation stabilization delay time for wake-up from stop mode or hardware standby mode.

(1) Register Configuration

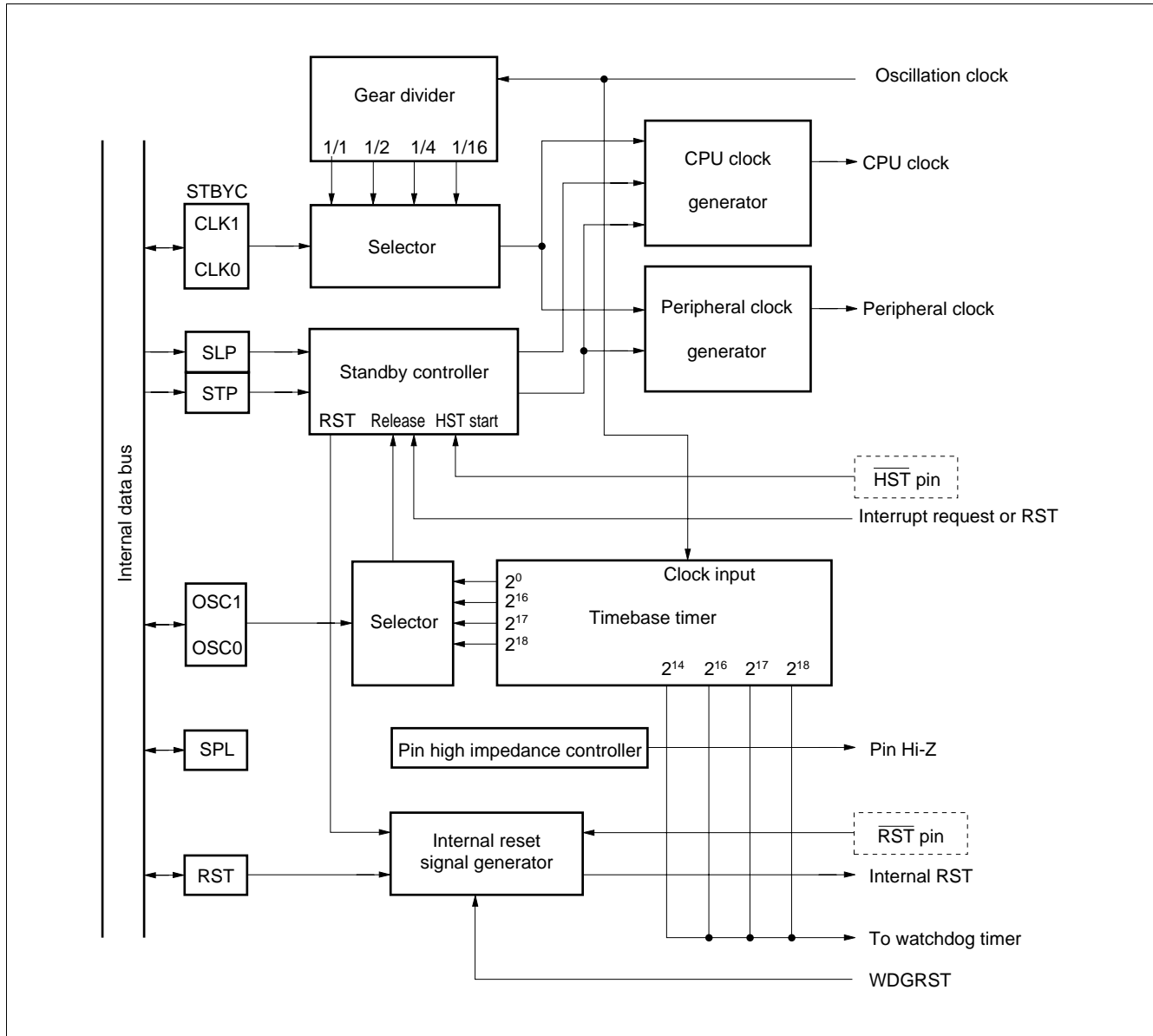
- **Standby Control Register (STBYC)**

| Register name | Address | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Initial value |
|---------------|---------------------|------|------|-------|-------|-------|-------|-------|-------|---------------|
| STBYC | 0000A0 _H | STP | SLP | SPL | RST | OSC1 | OSC0 | CLK1 | CLK0 | 0001**** |
| | | (W) | (W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | |

Note: The initial value (*) of bit0 to bit3 is changed by reset source.

MB90220 Series

(2) Block Diagram



MB90220 Series

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

($V_{SS} = AV_{SS} = 0.0\text{ V}$)

| Parameter | Symbol | Pin name | Value | | Unit | Remarks |
|--------------------------------|-----------------|--------------|----------------|----------------|------|--|
| | | | Min. | Max. | | |
| Power supply voltage | V_{CC} | V_{CC} | $V_{SS} - 0.3$ | $V_{SS} + 7.0$ | V | |
| Program voltage | V_{PP} | V_{PP} | $V_{SS} - 0.3$ | 13.0 | V | MB90P224A/P224B MB90W224A/W224B |
| Analog power supply voltage | AV_{CC} | AV_{CC} | $V_{SS} - 0.3$ | $V_{CC} + 0.3$ | V | Power supply voltage for A/D converter |
| | AVRH AVRL | AVRH AVRL | $V_{SS} - 0.3$ | AV_{CC} | V | Reference voltage for A/D converter |
| Input voltage | V_I^{*1} | — | $V_{SS} - 0.3$ | $V_{CC} + 0.3$ | V | |
| Output voltage | V_O | *2 | $V_{SS} - 0.3$ | $V_{CC} + 0.3$ | V | |
| “L” level output current | I_{OL} | *3 | — | 20 | mA | Rush current |
| “L” level total output current | ΣI_{OL} | *3 | — | 50 | mA | Total output current |
| “H” level output current | I_{OH} | *2 | — | -10 | mA | Rush current |
| “H” level total output current | ΣI_{OH} | *2 | — | -48 | mA | Total output current |
| Power consumption | P_D | — | — | 650 | mW | |
| Operating temperature | T_A | — | -40 | +105 | °C | MB90223/224/P224B /W224B |
| | | | -40 | +85 | °C | MB90P224A/W224A |
| Storage temperature | T_{stg} | — | -55 | +150 | °C | |

*1: V_I must not exceed $V_{CC} + 0.3\text{ V}$.

*2: Output pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P70 to P77, P80 to P87, PA0 to PA7, PB0 to PB7, PC0 to PC5

*3: Output pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0 to PA7, PB0 to PB7, PC0 to PC5

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

MB90220 Series

2. Recommended Operating Condition

($V_{SS} = AV_{SS} = 0.0\text{ V}$)

| Parameter | Symbol | Pin name | Value | | Unit | Remarks |
|-----------------------------|-----------|-----------|-----------|----------------|------|---|
| | | | Min. | Max. | | |
| Power supply voltage | V_{CC} | V_{CC} | 4.5 | 5.5 | V | When operating |
| | | | 3.0 | 5.5 | V | Retains the RAM state in stop mode |
| Analog power supply voltage | AV_{CC} | AV_{CC} | 4.5 | $V_{CC} + 0.3$ | V | Power supply voltage for A/D converter |
| | AV_{RH} | AV_{RH} | AV_{RL} | AV_{CC} | V | Reference voltage for A/D converter |
| | AV_{RL} | AV_{RL} | AV_{SS} | AV_{RH} | V | |
| Clock frequency | F_C | — | 10 | 16 | MHz | MB90224/P224A/W224A MB90P224B/W224B |
| | | | 10 | 12 | MHz | MB90223 |
| Operating temperature | T_A^* | — | -40 | +105 | °C | Single-chip mode MB90223/224/P224B/ W224B |
| | | | -40 | +85 | °C | Single-chip mode MB90P224A/W224A |
| | | | -40 | +70 | °C | External bus mode |

* : Excluding the temperature rise due to the heat produced.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

MB90220 Series

3. DC Characteristics

Single-chip mode MB90223/224/P224B/W224B : ($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+105^\circ\text{C}$)
 MB90P224A/W224A : ($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$)
 External bus mode : ($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+70^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|--------------------------|-----------|-------------------------|---|----------------|-----------|----------------|------------------|---|
| | | | | Min. | Typ. | Max. | | |
| “H” level input voltage | V_{IH} | X0 | — | $0.7 V_{CC}$ | — | $V_{CC} + 0.3$ | V | CMOS level input |
| | V_{IHS} | *1 | — | $0.8 V_{CC}$ | — | $V_{CC} + 0.3$ | V | Hysteresis input |
| | V_{IHM} | MD0 to MD2 | — | $V_{CC} - 0.3$ | — | $V_{CC} + 0.3$ | V | |
| “L” level input voltage | V_{IL} | X0 | — | $V_{SS} - 0.3$ | — | $0.3 V_{CC}$ | V | CMOS level input |
| | V_{ILS} | *1 | — | $V_{SS} - 0.3$ | — | $0.2 V_{CC}$ | V | Hysteresis input |
| | V_{ILM} | MD0 to MD2 | — | $V_{SS} - 0.3$ | — | $V_{SS} + 0.3$ | V | |
| “H” level output voltage | V_{OH} | *2 | $V_{CC} = 4.5\text{ V}$ $I_{OH} = -4.0\text{ mA}$ | $V_{CC} - 0.5$ | — | V_{CC} | V | |
| | V_{OH1} | X1 | $V_{CC} = 4.5\text{ V}$ $I_{OH} = -2.0\text{ mA}$ | $V_{CC} - 2.5$ | — | V_{CC} | V | |
| “L” level output voltage | V_{OL} | *3 | $V_{CC} = 4.5\text{ V}$ $I_{OL} = 4.0\text{ mA}$ | 0 | — | 0.4 | V | |
| | V_{OL1} | X1 | $V_{CC} = 4.5\text{ V}$ $I_{OL} = 2.0\text{ mA}$ | 0 | — | $V_{CC} - 2.5$ | V | |
| Input leakage current | I_i | *1 | $V_{CC} = 5.5\text{ V}$ $0.2 V_{CC} < V_i < 0.8 V_{CC}$ | — | — | ± 10 | μA | Hysteresis input Except pins with pull-up/pull-down resistor and RST pin |
| | I_{i2} | X0 | $V_{CC} = 5.5\text{ V}$ $0.2 V_{CC} < V_{i2} < 0.8 V_{CC}$ | — | — | ± 20 | μA | |
| Pull-up resistor | R_{pU} | $\overline{\text{RST}}$ | — | 22 | 50 | 110 | $\text{k}\Omega$ | *4 MB90223/224 MB90P224A/ W224A |
| | | MD1 | — | 22 | 50 | 150 | $\text{k}\Omega$ | *4 MB90223/224 |
| Pull-down resistor | R_{pD} | MD0 MD2 | — | 22 | 50 | 150 | $\text{k}\Omega$ | *4 MB90223/224 |
| Power supply voltage*8 | I_{CC} | V_{CC} | $F_C = 12\text{ MHz}$ | — | 70^{*5} | 100 | mA | MB90223 |
| | | | $F_C = 16\text{ MHz}$ | — | 70^{*5} | 100 | mA | MB90224 |
| | | | $F_C = 16\text{ MHz}$ | — | 90^{*5} | 125 | mA | MB90P224A/ P224B MB90W224A/ W224B |
| | I_{CCS} | V_{CC} | $f_c = 16\text{ MHz}^{*9}$ | — | — | 60 | mA | At sleep mode |
| | I_{CCH} | V_{CC} | — | — | 5 | 10 | μA | In stop mode $T_A = +25^\circ\text{C}$ At hardware standby |

(Continued)

MB90220 Series

(Continued)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|-----------------------------|-----------------|------------------|---------------------------------------|-------|-----------------|------|--------------|---------|
| | | | | Min. | Typ. | Max. | | |
| Analog power supply voltage | I _A | AV _{CC} | f _c = 16 MHz* ⁹ | — | 3 | 7 | mA | |
| | I _{AH} | | — | — | 5* ⁶ | μA | At stop mode | |
| Input capacitance | C _{IN} | * ⁷ | — | — | 10 | — | pF | |

*1: Hysteresis input pins

RST, HST, P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P80 to P87, P90 to P97, PA0 to PA7, PB0 to PB7, PC0 to PC5

*2: Output pins

P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P70 to P77, P80 to P87, PA0 to PA7, PB0 to PB7, PC0 to PC5

*3: Output pins

P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0 to PA7, PB0 to PB7, PC0 to PC5

*4: A list of availabilities of pull-up/pull-down resistors

| Pin name | MB90223/224 | MB90P224A/W224A | MB90P224B/W224B |
|----------|--|-----------------------------|-----------------|
| RST | Availability of pull-up resistors is optionally defined. | Pull-up resistors available | Unavailable |
| MD1 | Pull-up resistors available | Unavailable | Unavailable |
| MD0, MD2 | Pull-up resistors available | Unavailable | Unavailable |

*5: V_{CC} = +5.0 V, V_{SS} = 0.0 V, T_A = +25°C, F_C = 16 MHz

*6: The current value applies to the CPU stop mode with A/D converter inactive (V_{CC} = AV_{CC} = AVRH = +5.5 V).

*7: Other than V_{CC}, V_{SS}, AV_{CC} and AV_{SS}

*8: Measurement condition of power supply current; external clock pin and output pin are open.

Measurement condition of V_{CC}; see the table above mentioned.

*9: F_C = 12 MHz for MB90223

MB90220 Series

4. AC Characteristics

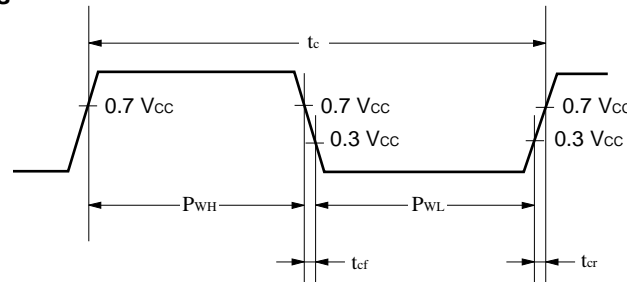
(1) Clock Timing Standards

Single-chip mode MB90223/224/P224B/W224B : ($V_{CC} = +4.5$ to $+5.5$ V, $V_{SS} = 0.0$ V, $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$)
 MB90P224A/W224A : ($V_{CC} = +4.5$ to $+5.5$ V, $V_{SS} = 0.0$ V, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)
 External bus mode : ($V_{CC} = +4.5$ to $+5.5$ V, $V_{SS} = 0.0$ V, $T_A = -40^\circ\text{C}$ to $+70^\circ\text{C}$)

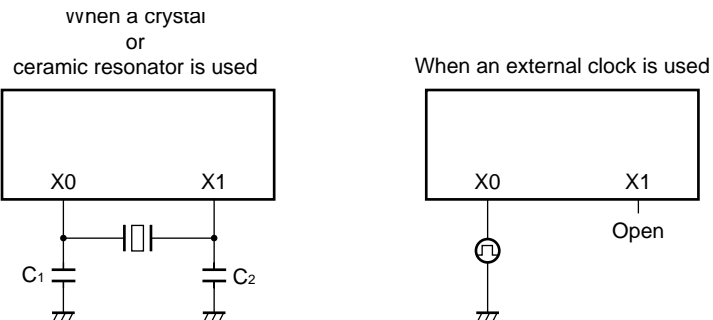
| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|----------------------------------|----------------------|----------|-----------|-----------|------|-----------|------|--|
| | | | | Min. | Typ. | Max. | | |
| Clock frequency | f_c | X0, X1 | — | 10 | — | 16 | MHz | MB90224/ P224A/P224B MB90W224A/ W224B |
| | | | | 10 | — | 12 | MHz | MB90223 |
| Clock cycle time | t_c | X0, X1 | — | 62.5 | — | 100 | ns | MB90224/ P224A/P224B MB90W224A/ W224B |
| | | | | 83.4 | — | 100 | ns | MB90223 |
| Input clock pulse width | P_{WH} P_{WL} | X0 | — | $0.4 t_c$ | — | $0.6 t_c$ | ns | Equivalent to 60% duty ratio |
| Input clock rising/falling times | t_{cr} t_{cf} | X0 | — | — | — | 8 | ns | $t_{cr} + t_{cf}$ |

$$t_c = 1/f_c$$

• Clock Input Timings



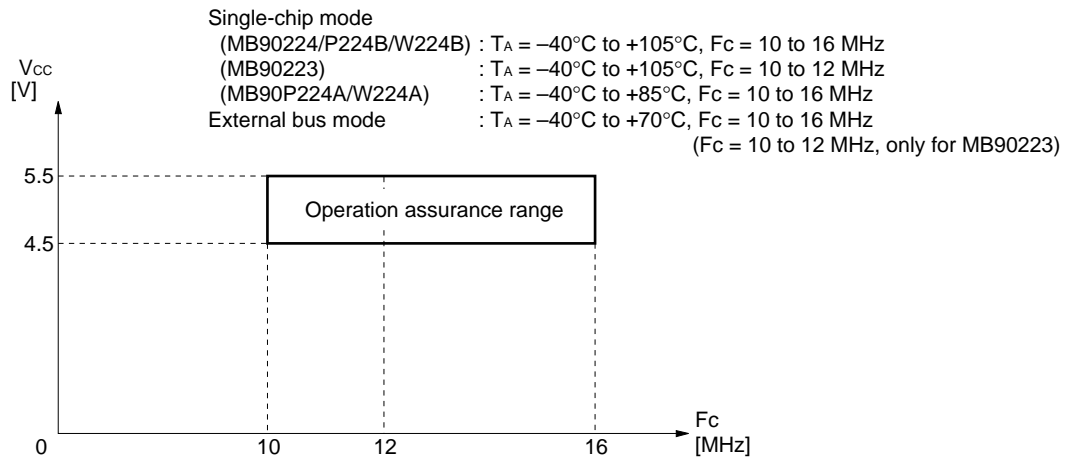
• Clock Conditions



$C_1 = C_2 = 10$ pF
 Select the optimum capacity value for the resonator

MB90220 Series

• Relationship between Clock Frequency and Supply Voltage



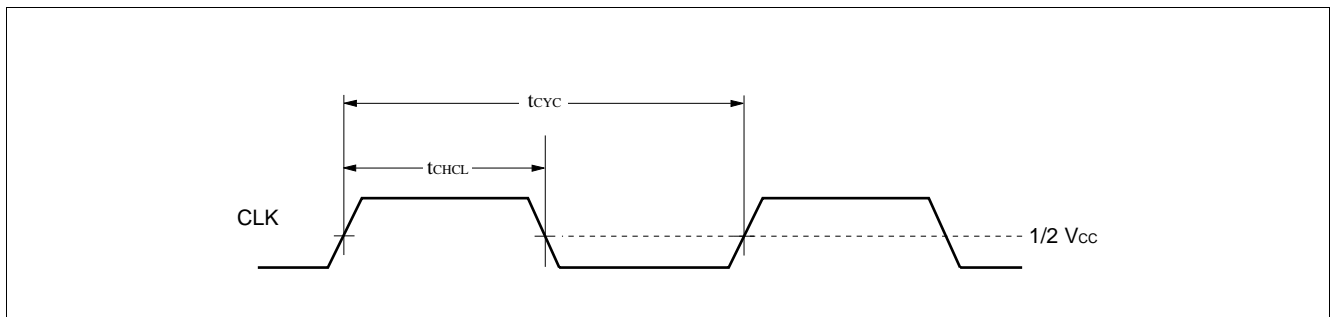
MB90220 Series

(2) Clock Output Timing

(External bus mode: $V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+70^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|---|------------|----------|--------------------------|------------------|------|-------------|------|---|
| | | | | Min. | Typ. | Max. | | |
| Machine cycle time | t_{CYC} | CLK | Load condition: 80 pF | 62.5 | — | 1600 | ns | MB90224/ P224A/P224B MB90W224A/ 224B |
| | | | | 83.4 | — | 1600 | ns | MB90223 |
| CLK $\uparrow \rightarrow$ CLK \downarrow | t_{CHCL} | CLK | | $t_{CYC}/2 - 20$ | — | $t_{CYC}/2$ | ns | |

$t_{CYC} = n/F_c$, n gear ratio (1, 2, 4, 16)



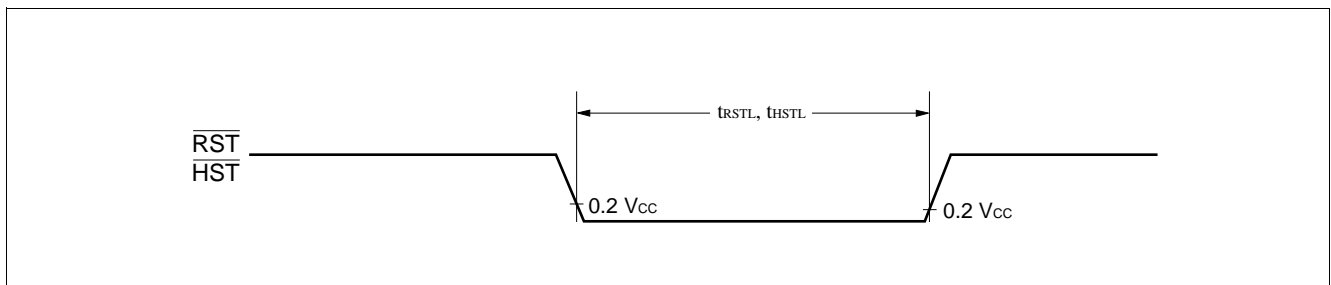
(3) Reset and Hardware Standby Input Standards

Single-chip mode MB90223/224/P224B/W224B: ($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+105^\circ\text{C}$)
 MB90P224A/W224A : ($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$)

External bus mode : ($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+70^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|-----------------------------|------------|----------|-----------|-------------|------|------|------|---------|
| | | | | Min. | Typ. | Max. | | |
| Reset input time | t_{RSTL} | RST | — | $5 t_{CYC}$ | — | — | ns | |
| Hardware standby input time | t_{HSTL} | HST | — | $5 t_{CYC}$ | — | — | ns | * |

*: The machine cycle time (t_{CYC}) at hardware standby is set to 1/16 divided oscillation.



MB90220 Series

(4) Power on Supply Specifications (Power-on Reset)

Single-chip mode MB90223/224/P224B/W224B: ($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+105^\circ\text{C}$)
 MB90P224A/W224A : ($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$)
 External bus mode : ($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+70^\circ\text{C}$)

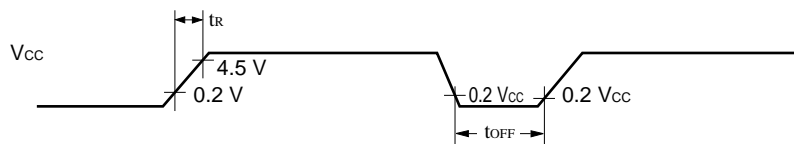
| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|---------------------------|-----------|----------|-----------|-------|------|------|------|---------|
| | | | | Min. | Typ. | Max. | | |
| Power supply rising time | t_R | V_{CC} | — | — | — | 30 | ms | * |
| Power supply cut-off time | t_{OFF} | V_{CC} | — | 1 | — | — | ms | |

* : Before power supply rising, it is required to be $V_{CC} < 0.2\text{ V}$.

Notes: • Power-on reset assumes the above values.

- Whether the power-on reset is required or not, turn the power on according to these characteristics and trigger the power-on reset.
- There are internal registers (STBYC, etc.) which is initialized only by the power-on reset in the device.

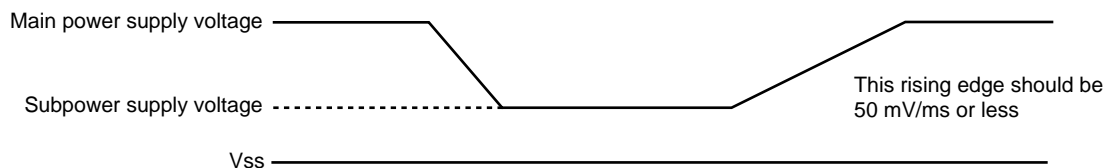
• Power-on Reset



Note: Note on changing power supply

Even if above characteristics are not insufficient, abrupt changes in power supply voltage may cause a power-on reset. Therefore, at the time of a momentary changes such as when power is turned on, rise the power smoothly as shown below.

• Changing Power Supply

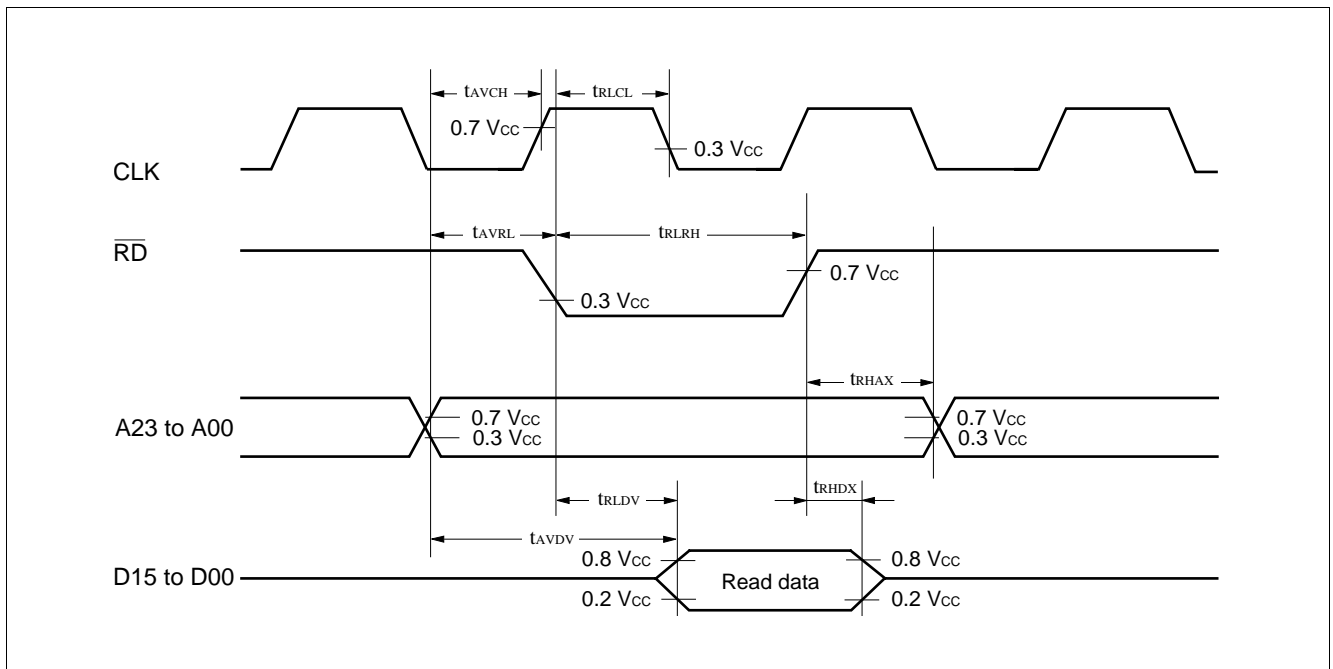


MB90220 Series

(5) Bus Read Timing

($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+70^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|-------------------|------------------------------|--------------------------|-------------------------|---------------------------|------|---------|
| | | | | Min. | Max. | | |
| Valid address $\rightarrow \overline{\text{RD}} \downarrow$ time | t_{AVRL} | A23 to A00 | Load condition: 80 pF | $t_{\text{CYC}}/2 - 20$ | — | ns | |
| $\overline{\text{RD}}$ pulse width | t_{RLRH} | $\overline{\text{RD}}$ | | $t_{\text{CYC}} - 25$ | — | ns | |
| $\overline{\text{RD}} \downarrow \rightarrow$ Valid data input | t_{RLDV} | D15 to D00 | | — | $t_{\text{CYC}} - 30$ | ns | |
| $\overline{\text{RD}} \uparrow \rightarrow$ Data hold time | t_{RHDX} | | | 0 | — | ns | |
| Valid address \rightarrow Valid data input | t_{AVDV} | | | — | $3 t_{\text{CYC}}/2 - 40$ | ns | |
| $\overline{\text{RD}} \uparrow \rightarrow$ Address valid time | t_{RHAX} | A23 to A00 | | $t_{\text{CYC}}/2 - 20$ | — | ns | |
| Valid address \rightarrow CLK \uparrow time | t_{AVCH} | A23 to A00 CLK | | $t_{\text{CYC}}/2 - 25$ | — | ns | |
| $\overline{\text{RD}} \downarrow \rightarrow$ CLK \downarrow time | t_{RLCL} | $\overline{\text{RD}}$, CLK | | $t_{\text{CYC}}/2 - 25$ | — | ns | |

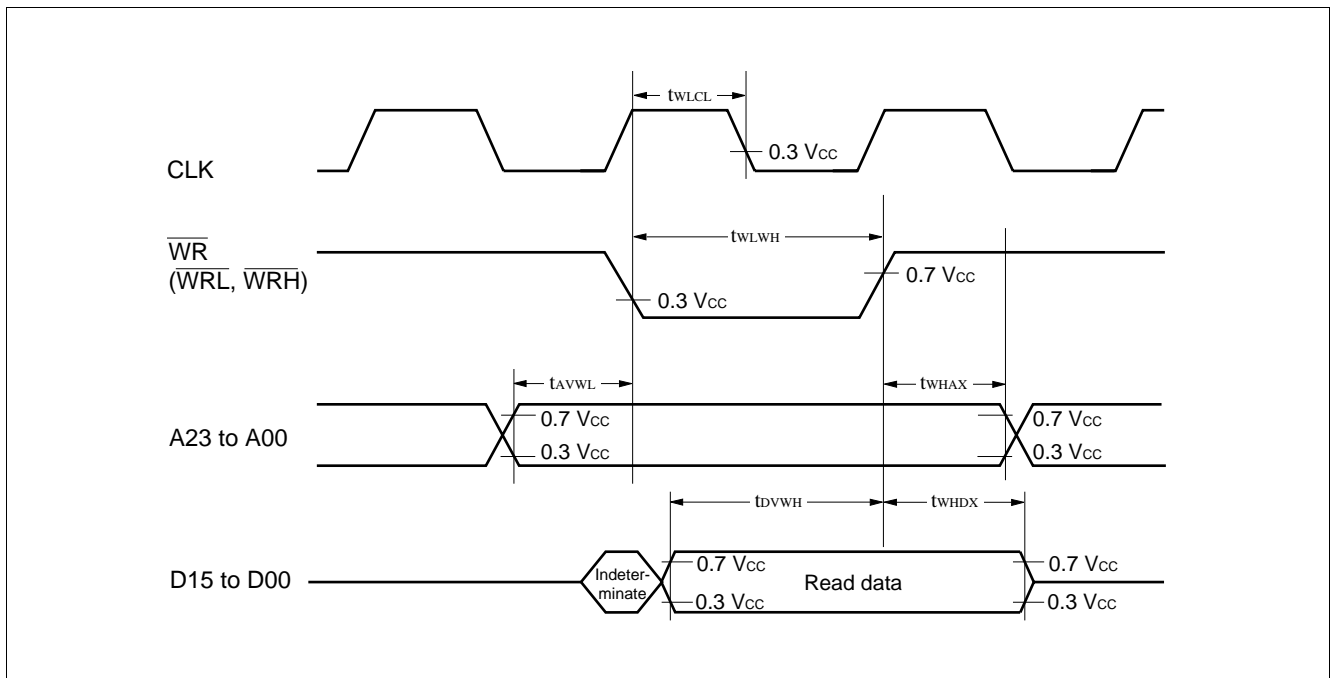


MB90220 Series

(6) Bus Write Timing

($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+70^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|--|------------|------------------|-----------------------------|------------------|------|------|---------|
| | | | | Min. | Max. | | |
| Valid address $\rightarrow \overline{WR} \downarrow$ time | t_{AVWL} | A23 to A00 | Load condition: 80 pF | $t_{CYC}/2 - 20$ | — | ns | |
| \overline{WR} pulse width | t_{WLWH} | WRL, WRH | | $t_{CYC} - 25$ | — | ns | |
| Valid data output $\rightarrow \overline{WR} \uparrow$ time | t_{DVWH} | D15 to D00 | | $t_{CYC} - 40$ | — | ns | |
| $\overline{WR} \uparrow \rightarrow$ Data hold time | t_{WHDX} | D15 to D00 | | $t_{CYC}/2 - 20$ | — | ns | |
| $\overline{WR} \uparrow \rightarrow$ Address valid time | t_{WHAX} | A23 to A00 | | $t_{CYC}/2 - 20$ | — | ns | |
| $\overline{WR} \downarrow \rightarrow$ CLK \downarrow time | t_{WLCL} | WRL, WRH, CLK | | $t_{CYC}/2 - 25$ | — | ns | |



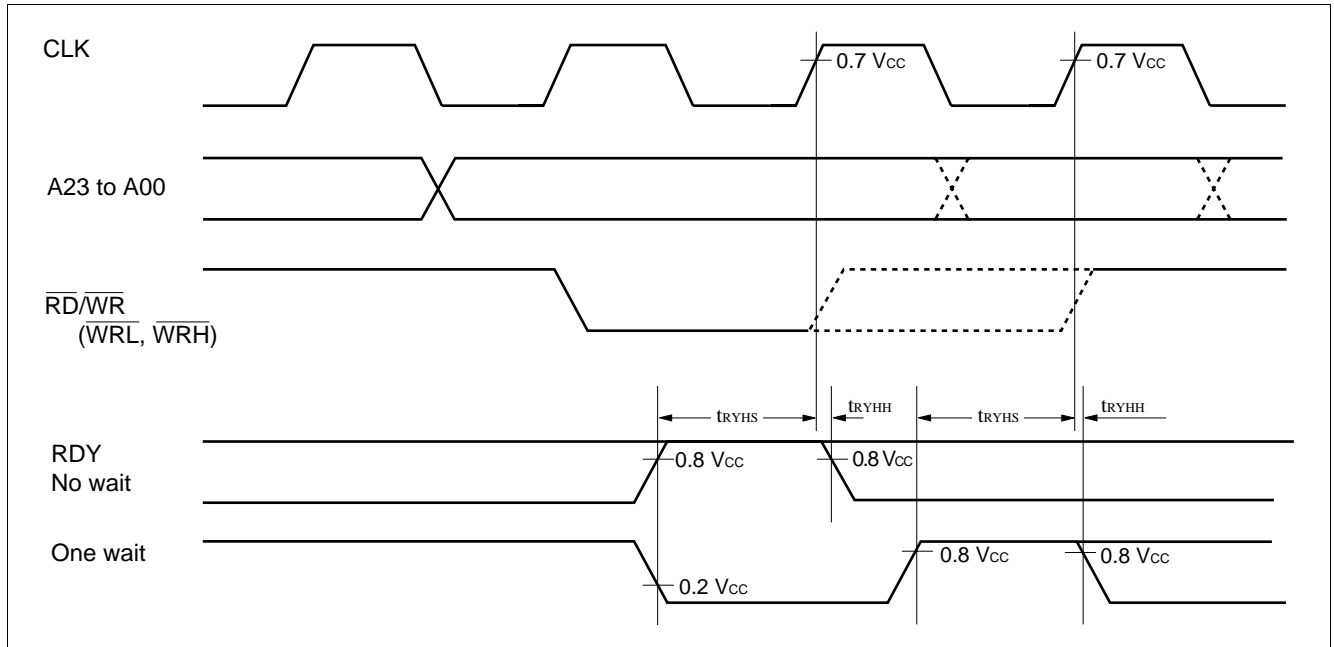
MB90220 Series

(7) Ready Input Timing

($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+70^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|----------------|------------|----------|--------------------------|-------|------|------|---------|
| | | | | Min. | Max. | | |
| RDY setup time | t_{RYHS} | RDY | Load condition: 80 pF | 40 | — | ns | |
| RDY hold time | t_{RYHH} | RDY | | 0 | — | ns | |

Note: Use the auto-ready function if the RDY setup time is insufficient.

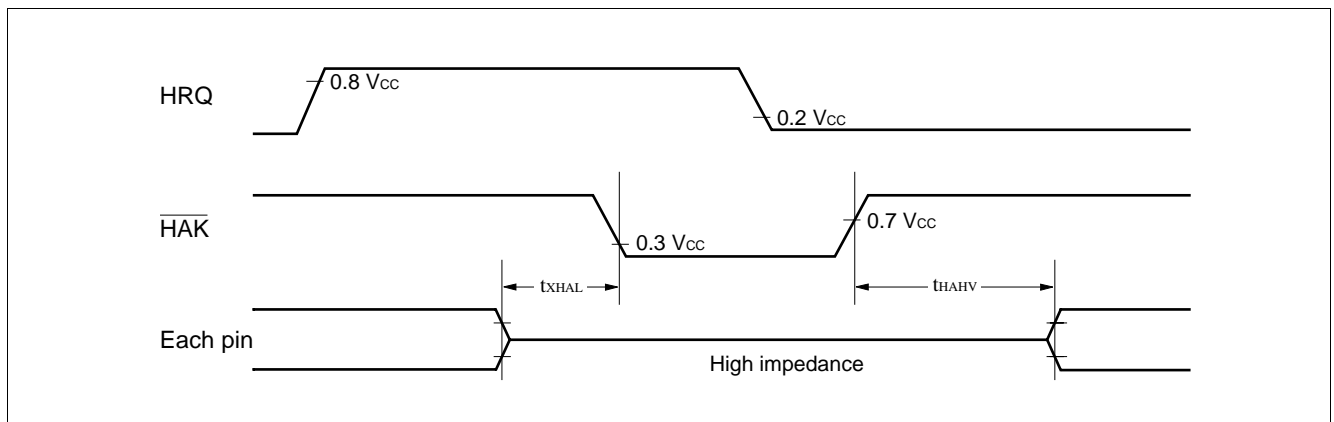


(8) Hold Timing

($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+70^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|--|------------|------------------|--------------------------|-----------|-------------|------|---------|
| | | | | Min. | Max. | | |
| Pin floating → \overline{HAK} ↓ time | t_{XHAL} | \overline{HAK} | Load condition: 80 pF | 30 | t_{CYC} | ns | |
| \overline{HAK} ↑ time → pin valid time | t_{HAHV} | \overline{HAK} | | t_{CYC} | $2 t_{CYC}$ | ns | |

Note: It takes at least one machine cycle for \overline{HAK} to vary after HRQ is fetched.



MB90220 Series

(9) UART Timing

Single-chip mode MB90223/224/P224B/W224B: ($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+105^\circ\text{C}$)
 MB90P224A/W224A : ($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$)

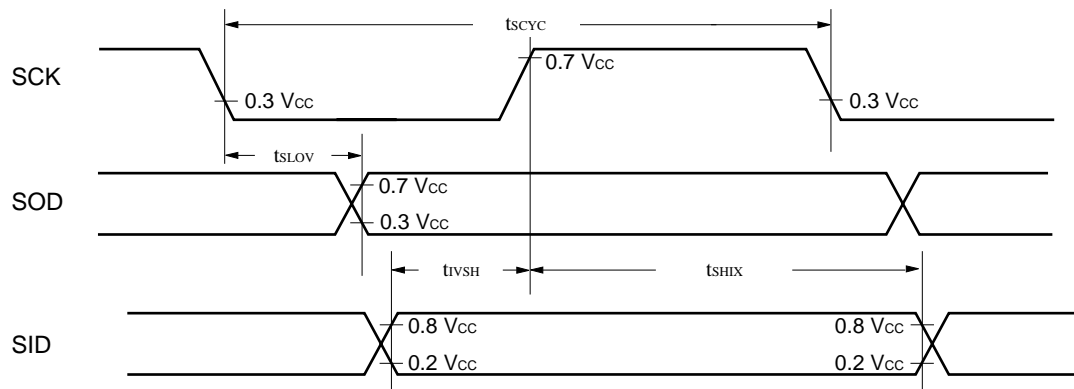
External bus mode : ($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+70^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|------------|----------|--------------------------|-------------|------|------|-------------------------------------|
| | | | | Min. | Max. | | |
| Serial clock cycle time | t_{SCYC} | — | Load condition: 80 pF | 8 t_{CYC} | — | ns | Internal clock operation output pin |
| SCLK $\downarrow \rightarrow$ SOUT delay time | t_{SLOV} | — | | -80 | 80 | ns | |
| Valid SIN \rightarrow SCLK \uparrow | t_{IVSH} | — | | 100 | — | ns | |
| SCLK $\uparrow \rightarrow$ Valid SIN hold time | t_{SHIX} | — | | 60 | — | ns | |
| Serial clock "H" pulse width | t_{SHSL} | — | Load condition: 80 pF | 4 t_{CYC} | — | ns | External clock operation output pin |
| Serial clock "L" pulse width | t_{SLSH} | — | | 4 t_{CYC} | — | ns | |
| SCLK $\downarrow \rightarrow$ SOUT delay time | t_{SLOV} | — | | — | 150 | ns | |
| Valid SIN \rightarrow SCLK \uparrow | t_{IVSH} | — | | 60 | — | ns | |
| SCLK $\uparrow \rightarrow$ valid SIN hold time | t_{SHIX} | — | | 60 | — | ns | |

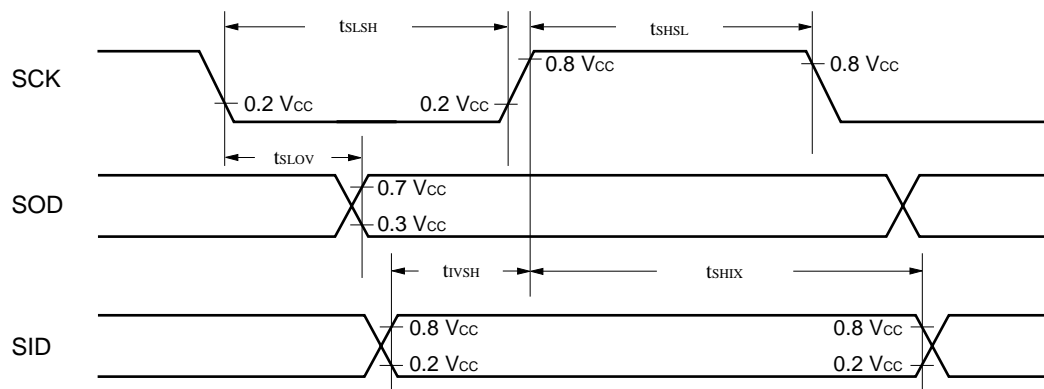
Notes: • These AC characteristics assume in CLK synchronization mode.

• " t_{CYC} " is the machine cycle (unit: ns).

- Internal Shift Clock Mode



- External Shift Clock Input Mode



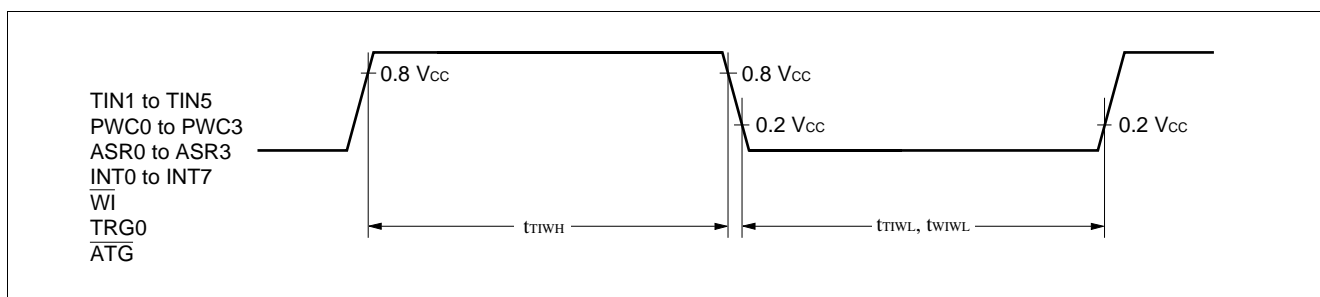
MB90220 Series

(10) Resourse Input Timing

Single-chip mode MB90223/224/P224B/W224B: ($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+105^\circ\text{C}$)
 MB90P224A/W224A : ($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$)

External bus mode : ($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+70^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|-------------------|--------------------------|--------------|--------------------------|-------------|------|------|------|---------------------------------|
| | | | | Min. | Typ. | Max. | | |
| Input pulse width | t_{TIWH} t_{TIWL} | TIN1 to TIN5 | Load condition: 80 pF | 4 t_{CYC} | — | — | ns | External event count input mode |
| | | | | 2 t_{CYC} | — | — | ns | Trigger input/gate input mode |
| | | PWC0 to PWC3 | | 2 t_{CYC} | — | — | ns | |
| | | ASR0 to ASR3 | | 2 t_{CYC} | — | — | ns | |
| | | INT0 to INT7 | | 3 t_{CYC} | — | — | ns | |
| | | TRG0 | | 2 t_{CYC} | — | — | ns | |
| | | ATG | | 2 t_{CYC} | — | — | ns | |
| | t_{WIWL} | WI | | 4 t_{CYC} | — | — | ns | |

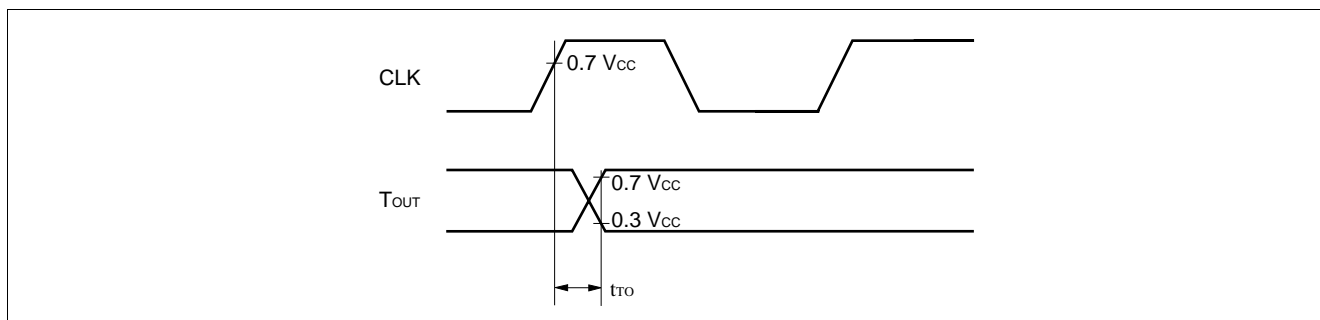


(11) Resourse Output Timing

Single-chip mode MB90223/224/P224B/W224B: ($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+105^\circ\text{C}$)
 MB90P224A/W224A : ($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$)

External bus mode : ($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+70^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|--|----------|--|--------------------------|-------|------|------|------|---------|
| | | | | Min. | Typ. | Max. | | |
| CLK \uparrow \rightarrow T_{OUT} transition time | t_{TO} | TOT0 to TOT5 PPG0 to PPG1 POT0 to POT3 DOT0 to DOT7 | Load condition: 80 pF | — | — | 30 | ns | |



MB90220 Series

5. A/D Converter Electrical Characteristics

Single-chip mode MB90223/224/P224B/W224B

: ($V_{CC} = V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+105^\circ\text{C}$, $+4.5\text{ V} \leq \text{AVRH} - \text{AVRL}$)

MB90P224A/W224A

: ($V_{CC} = V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$, $+4.5\text{ V} \leq \text{AVRH} - \text{AVRL}$)

External bus mode

: ($V_{CC} = V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+70^\circ\text{C}$, $+4.5\text{ V} \leq \text{AVRH} - \text{AVRL}$)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|----------------------------------|-----------------|--------------|----------------------------|------------|------------|------------|---------------|-------------------|
| | | | | Min. | Typ. | Max. | | |
| Resolution | n | — | — | — | — | 10 | bit | |
| Total error | — | — | — | — | — | ± 3.0 | LSB | |
| Linearity error | — | — | — | — | — | ± 2.0 | LSB | |
| Differential linearity error | — | — | — | — | — | ± 1.5 | LSB | |
| Zero transition voltage | V_{0T} | AN00 to AN15 | — | AVRL - 1.5 | AVRL + 0.5 | AVRL + 2.5 | LSB | |
| Full-scale transition voltage | V_{FST} | | — | AVRH - 3.5 | AVRH - 1.5 | AVRH + 0.5 | LSB | |
| Conversion time*1 | T_{CONV} | — | $t_{CYC} = 62.5\text{ ns}$ | 6.125 | — | — | μs | 98 machine cycles |
| | Sampling period | T_{SAMP} | | — | 3.75 | — | — | μs |
| Analog port input current | I_{AIN} | AN00 to AN15 | — | — | — | ± 0.1 | μA | |
| Analog input voltage | V_{AIN} | | — | AVRL | — | AVRH | V | |
| Analog reference voltage | — | AVRH | — | AVRL | — | V_{CC} | V | |
| | | AVRL | — | V_{SS} | — | AVRH | V | |
| Reference voltage supply current | I_R | AVRH | — | — | 200 | 500 | μA | |
| | I_{RH} | | — | — | — | 5^{*2} | μA | |
| Variation between channels | — | AN00 to AN15 | — | — | — | 4 | LSB | |

*1: These standards in this table are for MB90224/P224A/P224B/W224A/W224B.

MB90223: Minimum conversion time is $8.17\text{ }\mu\text{s}$ and minimum sampling time is $5\text{ }\mu\text{s}$ at $t_{CYC} = 83.4\text{ ns}$.

*2: The current value applies to the CPU stop mode with the A/D converter inactive ($V_{CC} = V_{CC} = \text{AVRH} = +5.5\text{ V}$).

Notes: (1) The error becomes larger as $|\text{AVRH} - \text{AVRL}|$ becomes smaller.

(2) Use the output impedance of the external circuit for analog input under the following conditions:

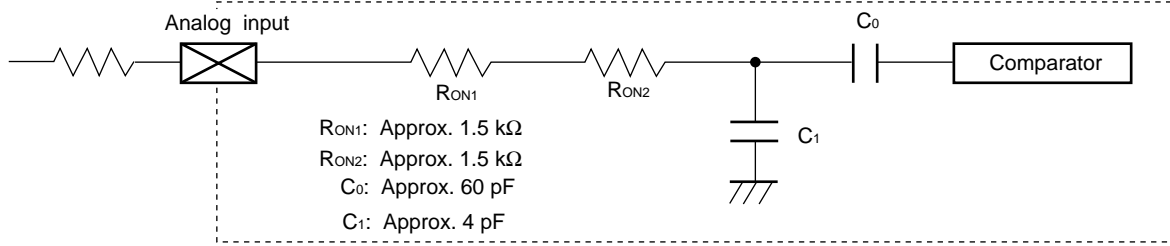
External circuit output impedance < approx. $10\text{ k}\Omega$ (Sampling time approx. $3.75\text{ }\mu\text{s}$, $t_{CYC} = 62.5\text{ ns}$)

(3) Precision values are standard values applicable to sleep mode.

(4) If V_{CC}/V_{CC} or V_{SS}/V_{SS} is caused by a noise to drop to below the analog input voltage, the analog input current is likely to increase. In such cases, a bypass capacitor or the like should be provided in the external circuit to suppress the noise.

MB90220 Series

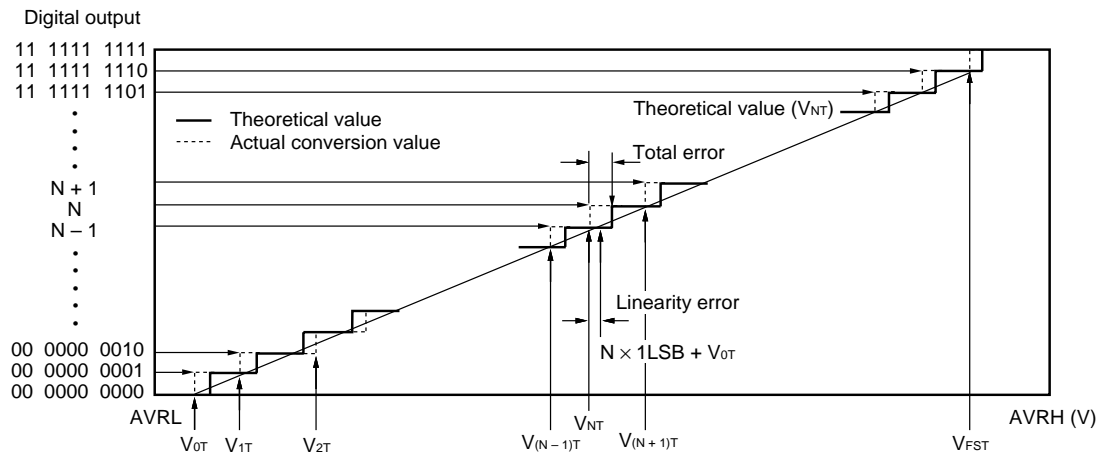
• Analog Input Circuit Mode



Note: The values shown here are reference values.

6. A/D Converter Glossary

- Resolution:** Analog changes that are identifiable with the A/D converter
- Total error:** When the number of bits is 10, analog voltage can be divided into $2^{10} = 1024$. Difference between actual and logical values. This error is caused by a zero transition error, full-scale transition error, linearity error, differential linearity error, or by noise.
- Linearity error:** The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1111” ↔ “11 1111 1110”) from actual conversion characteristics
- Differential linearity error:** The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value



$$1 \text{ LSB} = \frac{V_{FST} - V_{0T}}{1022}$$

$$1 \text{ LSB theoretical value} = \frac{AVRH - AVRL}{1022}$$

$$\text{Linearity error} = \frac{V_{NT} - (N \times 1 \text{ LSB} + V_{0T})}{1 \text{ LSB}}$$

$$\text{Differential linearity error} = \frac{V_{NT} - V_{(N-1)T}}{1 \text{ LSB}} - 1$$

$$\text{Total error} = \frac{V_{NT} - \{(N + 0.5) \times 1 \text{ LSB theoretical value}\}}{1 \text{ LSB theoretical value}}$$

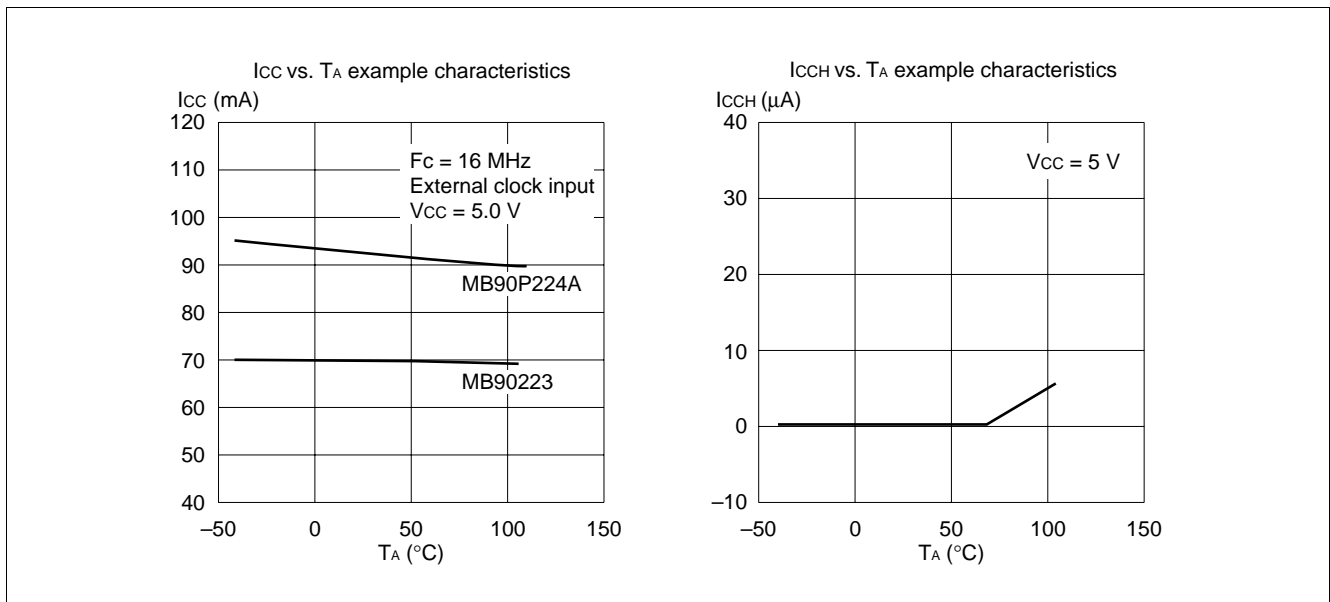
$$\left[\begin{array}{l} N = 0 \text{ to } 1022 \\ V_{NT(N=0)} = V_{0T} \\ V_{NT(N=1022)} = V_{FST} \end{array} \right.$$

$$N = 1 \text{ to } 1022$$

$$N = 0 \text{ to } 1022$$

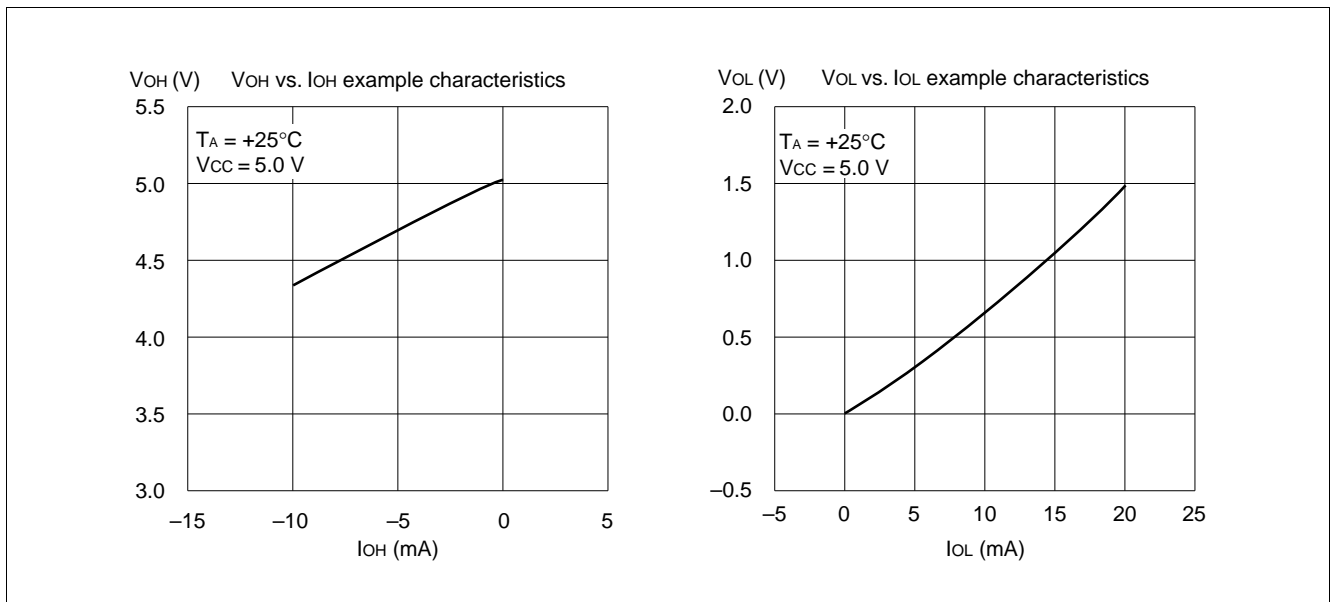
EXAMPLE CHARACTERISTICS

(1) Power Supply Current



Note: These are not assured value of characteristics but example characteristics.

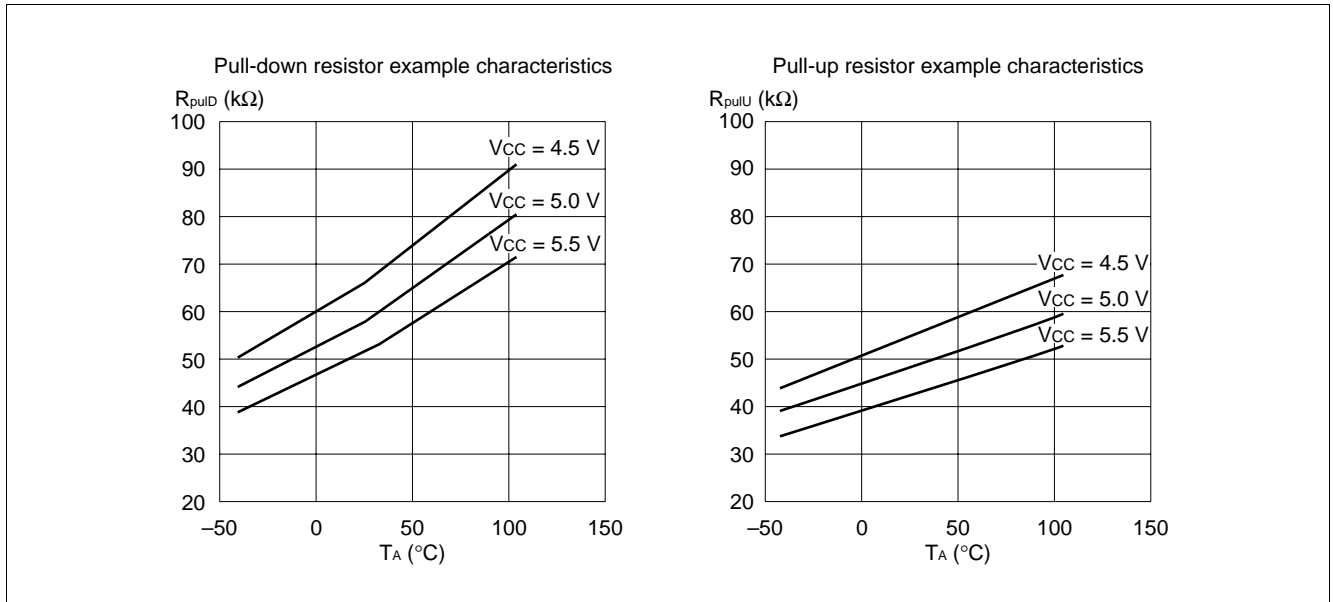
(2) Output Voltage



Note: These are not assured value of characteristics but example characteristics.

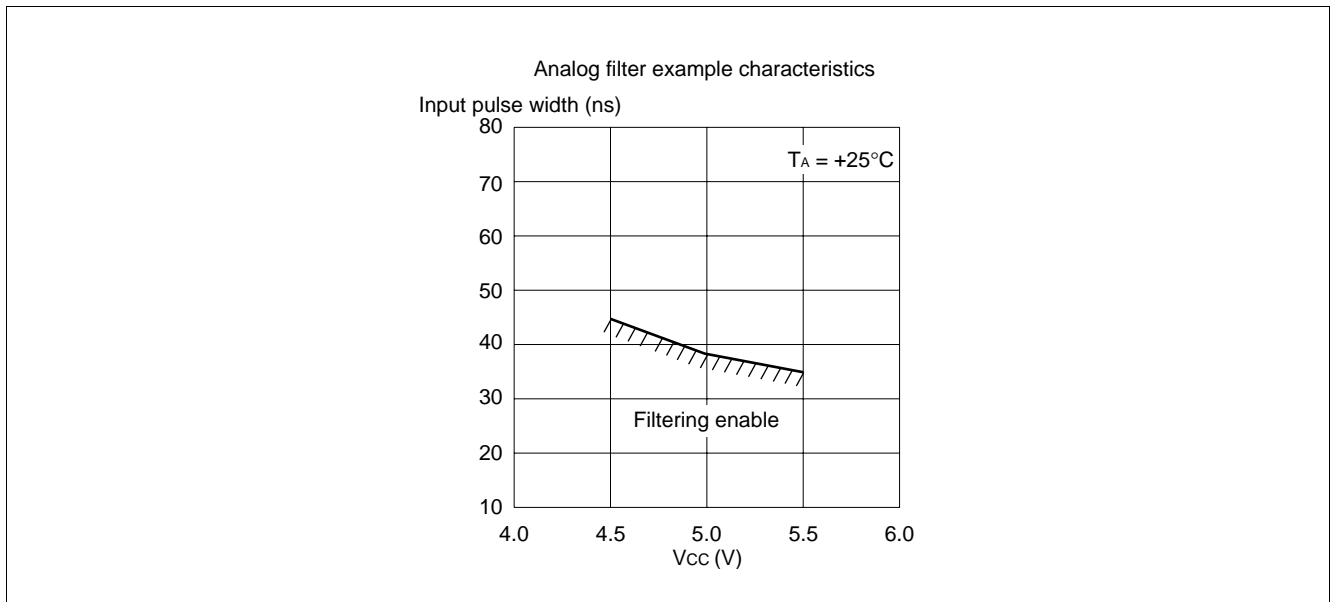
MB90220 Series

(3) Pull-up/Pull-down Resistor



Note: These are not assured value of characteristics but example characteristics.

(4) Analog Filter



Note: These are not assured value of characteristics but example characteristics.

■ INSTRUCTION SET (412 INSTRUCTIONS)

Table 1 Explanation of Items in Table of Instructions

| Item | Explanation |
|-----------|--|
| Mnemonic | Upper-case letters and symbols: Represented as they appear in assembler Lower-case letters: Replaced when described in assembler. Numbers after lower-case letters: Indicate the bit width within the instruction. |
| # | Indicates the number of bytes. |
| ~ | Indicates the number of cycles. See Table 4 for details about meanings of letters in items. |
| B | Indicates the correction value for calculating the number of actual cycles during execution of instruction. The number of actual cycles during execution of instruction is summed with the value in the "cycles" column. |
| Operation | Indicates operation of instruction. |
| LH | Indicates special operations involving the bits 15 through 08 of the accumulator. Z: Transfers "0". X: Extends before transferring. —: Transfers nothing. |
| AH | Indicates special operations involving the high-order 16 bits in the accumulator. *: Transfers from AL to AH. —: No transfer. Z: Transfers 00 _H to AH. X: Transfers 00 _H or FF _H to AH by extending AL. |
| I | Indicates the status of each of the following flags: I (interrupt enable), S (stack), T (sticky bit), N (negative), Z (zero), V (overflow), and C (carry). *: Changes due to execution of instruction. —: No change. S: Set by execution of instruction. R: Reset by execution of instruction. |
| S | |
| T | |
| N | |
| Z | |
| V | |
| C | |
| RMW | Indicates whether the instruction is a read-modify-write instruction (a single instruction that reads data from memory, etc., processes the data, and then writes the result to memory). *: Instruction is a read-modify-write instruction —: Instruction is not a read-modify-write instruction Note: Cannot be used for addresses that have different meanings depending on whether they are read or written. |

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Table 2 Explanation of Symbols in Table of Instructions

| Symbol | Explanation |
|-----------------|--|
| A | 32-bit accumulator The number of bits used varies according to the instruction. Byte: Low order 8 bits of AL Word: 16 bits of AL Long: 32 bits of AL, AH |
| AH | High-order 16 bits of A |
| AL | Low-order 16 bits of A |
| SP | Stack pointer (USP or SSP) |
| PC | Program counter |
| SPCU | Stack pointer upper limit register |
| SPCL | Stack pointer lower limit register |
| PCB | Program bank register |
| DTB | Data bank register |
| ADB | Additional data bank register |
| SSB | System stack bank register |
| USB | User stack bank register |
| SPB | Current stack bank register (SSB or USB) |
| DPR | Direct page register |
| brg1 | DTB, ADB, SSB, USB, DPR, PCB, SPB |
| brg2 | DTB, ADB, SSB, USB, DPR, SPB |
| Ri | R0, R1, R2, R3, R4, R5, R6, R7 |
| RWi | RW0, RW1, RW2, RW3, RW4, RW5, RW6, RW7 |
| RWj | RW0, RW1, RW2, RW3 |
| RLi | RL0, RL1, RL2, RL3 |
| dir | Compact direct addressing |
| addr16 | Direct addressing |
| addr24 | Physical direct addressing |
| addr24 0 to 15 | Bits 0 to 15 of addr24 |
| addr24 16 to 23 | Bits 16 to 23 of addr24 |
| io | I/O area (000000 _H to 0000FF _H) |

(Continued)

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(Continued)

| Symbol | Explanation |
|--|---|
| #imm4 #imm8 #imm16 #imm32 ext (imm8) | 4-bit immediate data 8-bit immediate data 16-bit immediate data 32-bit immediate data 16-bit data signed and extended from 8-bit immediate data |
| disp8 disp16 | 8-bit displacement 16-bit displacement |
| bp | Bit offset value |
| vct4 vct8 | Vector number (0 to 15) Vector number (0 to 255) |
| ()b | Bit address |
| rel ear eam | Branch specification relative to PC Effective addressing (codes 00 to 07) Effective addressing (codes 08 to 1F) |
| rlst | Register list |

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Table 3 Effective Address Fields

| Code | Notation | Address format | Number of bytes in address extension* |
|--|--|--|---------------------------------------|
| 00 01 02 03 04 05 06 07 | R0 RW0 RL0 R1 RW1 (RL0) R2 RW2 RL1 R3 RW3 (RL1) R4 RW4 RL2 R5 RW5 (RL2) R6 RW6 RL3 R7 RW7 (RL3) | Register direct "ea" corresponds to byte, word, and long-word types, starting from the left | — |
| 08 09 0A 0B | @RW0 @RW1 @RW2 @RW3 | Register indirect | 0 |
| 0C 0D 0E 0F | @RW0 + @RW1 + @RW2 + @RW3 + | Register indirect with post-increment | 0 |
| 10 11 12 13 14 15 16 17 | @RW0 + disp8 @RW1 + disp8 @RW2 + disp8 @RW3 + disp8 @RW4 + disp8 @RW5 + disp8 @RW6 + disp8 @RW7 + disp8 | Register indirect with 8-bit displacement | 1 |
| 18 19 1A 1B | @RW0 + disp16 @RW1 + disp16 @RW2 + disp16 @RW3 + disp16 | Register indirect with 16-bit displacement | 2 |
| 1C 1D 1E 1F | @RW0 + RW7 @RW1 + RW7 @PC + dip16 addr16 | Register indirect with index Register indirect with index PC indirect with 16-bit displacement Direct address | 0 0 2 2 |

* : The number of bytes for address extension is indicated by the "+" symbol in the "#" (number of bytes) column in the Table of Instructions.

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Table 4 Number of Execution Cycles for Each Form of Addressing

| Code | Operand | (a)* |
|----------|------------------|--|
| | | Number of execution cycles for each form of addressing |
| 00 to 07 | Ri RWi RLi | Listed in Table of Instructions |
| 08 to 0B | @RWj | 1 |
| 0C to 0F | @RWj + | 4 |
| 10 to 17 | @RWi + disp8 | 1 |
| 18 to 1B | @RWj + disp16 | 1 |
| 1C | @RW0 + RW7 | 2 |
| 1D | @RW1 + RW7 | 2 |
| 1E | @PC + dip16 | 2 |
| 1F | @addr16 | 1 |

* :“(a)” is used in the “cycles” (number of cycles) column and column B (correction value) in the Table of Instructions.

Table 5 Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles

| Operand | (b)* | | (c)* | | (d)* | |
|----------------------------------|------|------|------|------|------|------|
| | + | byte | + | word | + | long |
| Internal register | + | 0 | + | 0 | + | 0 |
| Internal RAM even address | + | 0 | + | 0 | + | 0 |
| Internal RAM odd address | + | 0 | + | 1 | + | 2 |
| Even address not in internal RAM | + | 1 | + | 1 | + | 2 |
| Odd address not in internal RAM | + | 1 | + | 3 | + | 6 |
| External data bus (8 bits) | + | 1 | + | 3 | + | 6 |

* :“(b)”,“(c)”, and“(d)” are used in the “cycles” (number of cycles) column and column B (correction value) in the Table of Instructions.

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Table 6 Transfer Instructions (Byte) [50 Instructions]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|--------------------|----|--------|-----|----------------------------|----|----|---|---|---|---|---|---|---|-----|
| MOV A, dir | 2 | 2 | (b) | byte (A) ← (dir) | Z | * | — | — | — | * | * | — | — | — |
| MOV A, addr16 | 3 | 2 | (b) | byte (A) ← (addr16) | Z | * | — | — | — | * | * | — | — | — |
| MOV A, Ri | 1 | 1 | 0 | byte (A) ← (Ri) | Z | * | — | — | — | * | * | — | — | — |
| MOV A, ear | 2 | 1 | 0 | byte (A) ← (ear) | Z | * | — | — | — | * | * | — | — | — |
| MOV A, eam | 2+ | 2+ (a) | (b) | byte (A) ← (eam) | Z | * | — | — | — | * | * | — | — | — |
| MOV A, io | 2 | 2 | (b) | byte (A) ← (io) | Z | * | — | — | — | * | * | — | — | — |
| MOV A, #imm8 | 2 | 2 | 0 | byte (A) ← imm8 | Z | * | — | — | — | * | * | — | — | — |
| MOV A, @A | 2 | 2 | (b) | byte (A) ← ((A)) | Z | — | — | — | — | * | * | — | — | — |
| MOV A, @RLi+disp8 | 3 | 6 | (b) | byte (A) ← ((RLi))+disp8) | Z | * | — | — | — | * | * | — | — | — |
| MOV A, @SP+disp8 | 3 | 3 | (b) | byte (A) ← ((SP)+disp8) | Z | * | — | — | — | * | * | — | — | — |
| MOVP A, addr24 | 5 | 3 | (b) | byte (A) ← (addr24) | Z | * | — | — | — | * | * | — | — | — |
| MOVP A, @A | 2 | 2 | (b) | byte (A) ← ((A)) | Z | — | — | — | — | * | * | — | — | — |
| MOVN A, #imm4 | 1 | 1 | 0 | byte (A) ← imm4 | Z | * | — | — | — | R | * | — | — | — |
| MOVX A, dir | 2 | 2 | (b) | byte (A) ← (dir) | X | * | — | — | — | * | * | — | — | — |
| MOVX A, addr16 | 3 | 2 | (b) | byte (A) ← (addr16) | X | * | — | — | — | * | * | — | — | — |
| MOVX A, Ri | 2 | 1 | 0 | byte (A) ← (Ri) | X | * | — | — | — | * | * | — | — | — |
| MOVX A, ear | 2 | 1 | 0 | byte (A) ← (ear) | X | * | — | — | — | * | * | — | — | — |
| MOVX A, eam | 2+ | 2+ (a) | (b) | byte (A) ← (eam) | X | * | — | — | — | * | * | — | — | — |
| MOVX A, io | 2 | 2 | (b) | byte (A) ← (io) | X | * | — | — | — | * | * | — | — | — |
| MOVX A, #imm8 | 2 | 2 | 0 | byte (A) ← imm8 | X | * | — | — | — | * | * | — | — | — |
| MOVX A, @A | 2 | 2 | (b) | byte (A) ← ((A)) | X | — | — | — | — | * | * | — | — | — |
| MOVX A, @RWi+disp8 | 2 | 3 | (b) | byte (A) ← ((RWi))+disp8) | X | * | — | — | — | * | * | — | — | — |
| MOVX A, @RLi+disp8 | 3 | 6 | (b) | byte (A) ← ((RLi))+disp8) | X | * | — | — | — | * | * | — | — | — |
| MOVX A, @SP+disp8 | 3 | 3 | (b) | byte (A) ← ((SP)+disp8) | X | * | — | — | — | * | * | — | — | — |
| MOVXPX A, addr24 | 5 | 3 | (b) | byte (A) ← (addr24) | X | * | — | — | — | * | * | — | — | — |
| MOVXPX A, @A | 2 | 2 | (b) | byte (A) ← ((A)) | X | — | — | — | — | * | * | — | — | — |
| MOV dir, A | 2 | 2 | (b) | byte (dir) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOV addr16, A | 3 | 2 | (b) | byte (addr16) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOV Ri, A | 1 | 1 | 0 | byte (Ri) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOV ear, A | 2 | 2 | 0 | byte (ear) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOV eam, A | 2+ | 2+ (a) | (b) | byte (eam) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOV io, A | 2 | 2 | (b) | byte (io) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOV @RLi+disp8, A | 3 | 6 | (b) | byte ((RLi) + disp8) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOV @SP+disp8, A | 3 | 3 | (b) | byte ((SP)+disp8) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOVP addr24, A | 5 | 3 | (b) | byte (addr24) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOV Ri, ear | 2 | 2 | 0 | byte (Ri) ← (ear) | — | — | — | — | — | * | * | — | — | — |
| MOV Ri, eam | 2+ | 3+ (a) | (b) | byte (Ri) ← (eam) | — | — | — | — | — | * | * | — | — | — |
| MOVP @A, Ri | 2 | 3 | (b) | byte ((A)) ← (Ri) | — | — | — | — | — | * | * | — | — | — |
| MOV ear, Ri | 2 | 3 | 0 | byte (ear) ← (Ri) | — | — | — | — | — | * | * | — | — | — |
| MOV eam, Ri | 2+ | 3+ (a) | (b) | byte (eam) ← (Ri) | — | — | — | — | — | * | * | — | — | — |
| MOV Ri, #imm8 | 2 | 2 | 0 | byte (Ri) ← imm8 | — | — | — | — | — | * | * | — | — | — |
| MOV io, #imm8 | 3 | 3 | (b) | byte (io) ← imm8 | — | — | — | — | — | — | — | — | — | — |
| MOV dir, #imm8 | 3 | 3 | (b) | byte (dir) ← imm8 | — | — | — | — | — | — | — | — | — | — |
| MOV ear, #imm8 | 3 | 2 | 0 | byte (ear) ← imm8 | — | — | — | — | — | * | * | — | — | — |
| MOV eam, #imm8 | 3+ | 2+ (a) | (b) | byte (eam) ← imm8 | — | — | — | — | — | — | — | — | — | — |
| MOV @AL, AH | 2 | 2 | (b) | byte ((A)) ← (AH) | — | — | — | — | — | * | * | — | — | — |

(Continued)

MB90220 Series*(Continued)*

| Mnemonic | | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|----------|---------|----|--------|--------|-------------------|----|----|---|---|---|---|---|---|---|-----|
| XCH | A, ear | 2 | 3 | 0 | byte (A) ↔ (ear) | Z | – | – | – | – | – | – | – | – | – |
| XCH | A, eam | 2+ | 3+ (a) | 2× (b) | byte (A) ↔ (eam) | Z | – | – | – | – | – | – | – | – | – |
| XCH | Ri, ear | 2 | 4 | 0 | byte (Ri) ↔ (ear) | – | – | – | – | – | – | – | – | – | – |
| XCH | Ri, eam | 2+ | 5+ (a) | 2× (b) | byte (Ri) ↔ (eam) | – | – | – | – | – | – | – | – | – | – |

For an explanation of “(a)” and “(b)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

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Table 7 Transfer Instructions (Word) [40 Instructions]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|--------------------|----|--------|--------|---------------------------|----|----|---|---|---|---|---|---|---|-----|
| MOVW A, dir | 2 | 2 | (c) | word (A) ← (dir) | — | * | — | — | — | * | * | — | — | — |
| MOVW A, addr16 | 3 | 2 | (c) | word (A) ← (addr16) | — | * | — | — | — | * | * | — | — | — |
| MOVW A, SP | 1 | 2 | 0 | word (A) ← (SP) | — | * | — | — | — | * | * | — | — | — |
| MOVW A, RWi | 1 | 1 | 0 | word (A) ← (RWi) | — | * | — | — | — | * | * | — | — | — |
| MOVW A, ear | 2 | 1 | 0 | word (A) ← (ear) | — | * | — | — | — | * | * | — | — | — |
| MOVW A, eam | 2+ | 2+ (a) | (c) | word (A) ← (eam) | — | * | — | — | — | * | * | — | — | — |
| MOVW A, io | 2 | 2 | (c) | word (A) ← (io) | — | * | — | — | — | * | * | — | — | — |
| MOVW A, @A | 2 | 2 | (c) | word (A) ← ((A)) | — | — | — | — | — | * | * | — | — | — |
| MOVW A, #imm16 | 3 | 2 | 0 | word (A) ← imm16 | — | * | — | — | — | * | * | — | — | — |
| MOVW A, @RWi+disp8 | 2 | 3 | (c) | word (A) ← ((RWi) +disp8) | — | * | — | — | — | * | * | — | — | — |
| MOVW A, @RLi+disp8 | 3 | 6 | (c) | word (A) ← ((RLi) +disp8) | — | * | — | — | — | * | * | — | — | — |
| MOVW A, @SP+disp8 | 3 | 3 | (c) | word (A) ← ((SP) +disp8) | — | * | — | — | — | * | * | — | — | — |
| MOVW A, @A | 2 | 2 | (c) | word (A) ← ((A)) | — | — | — | — | — | * | * | — | — | — |
| MOVW dir, A | 2 | 2 | (c) | word (dir) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOVW addr16, A | 3 | 2 | (c) | word (addr16) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOVW SP, # imm16 | 4 | 2 | 0 | word (SP) ← imm16 | — | — | — | — | — | * | * | — | — | — |
| MOVW SP, A | 1 | 2 | 0 | word (SP) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOVW RWi, A | 1 | 1 | 0 | word (RWi) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOVW ear, A | 2 | 2 | 0 | word (ear) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOVW eam, A | 2+ | 2+ (a) | (c) | word (eam) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOVW io, A | 2 | 2 | (c) | word (io) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOVW @RWi+disp8, A | 2 | 3 | (c) | word ((RWi) +disp8) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOVW @RLi+disp8, A | 3 | 6 | (c) | word ((RLi) +disp8) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOVW @SP+disp8, A | 3 | 3 | (c) | word ((SP) +disp8) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOVW addr24, A | 5 | 3 | (c) | word (addr24) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOVW @A, RWi | 2 | 3 | (c) | word ((A)) ← (RWi) | — | — | — | — | — | * | * | — | — | — |
| MOVW RWi, ear | 2 | 2 | 0 | word (RWi) ← (ear) | — | — | — | — | — | * | * | — | — | — |
| MOVW RWi, eam | 2+ | 3+ (a) | (c) | word (RWi) ← (eam) | — | — | — | — | — | * | * | — | — | — |
| MOVW ear, RWi | 2 | 3 | 0 | word (ear) ← (RWi) | — | — | — | — | — | * | * | — | — | — |
| MOVW eam, RWi | 2+ | 3+ (a) | (c) | word (eam) ← (RWi) | — | — | — | — | — | * | * | — | — | — |
| MOVW RWi, #imm16 | 3 | 2 | 0 | word (RWi) ← imm16 | — | — | — | — | — | * | * | — | — | — |
| MOVW io, #imm16 | 4 | 3 | (c) | word (io) ← imm16 | — | — | — | — | — | — | — | — | — | — |
| MOVW ear, #imm16 | 4 | 2 | 0 | word (ear) ← imm16 | — | — | — | — | — | * | * | — | — | — |
| MOVW eam, #imm16 | 4+ | 2+ (a) | (c) | word (eam) ← imm16 | — | — | — | — | — | — | — | — | — | — |
| MOVW @AL, AH | 2 | 2 | (c) | word ((A)) ← (AH) | — | — | — | — | — | * | * | — | — | — |
| XCHW A, ear | 2 | 3 | 0 | word (A) ↔ (ear) | — | — | — | — | — | — | — | — | — | — |
| XCHW A, eam | 2+ | 3+ (a) | 2× (c) | word (A) ↔ (eam) | — | — | — | — | — | — | — | — | — | — |
| XCHW RWi, ear | 2 | 4 | 0 | word (RWi) ↔ (ear) | — | — | — | — | — | — | — | — | — | — |
| XCHW RWi, eam | 2+ | 5+ (a) | 2× (c) | word (RWi) ↔ (eam) | — | — | — | — | — | — | — | — | — | — |

Note: For an explanation of “(a)” and “(c)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

MB90220 Series

Table 8 Transfer Instructions (Long Word) [11 Instructions]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|---------------------|----|--------|-----|---------------------------|----|----|---|---|---|---|---|---|---|-----|
| MOVL A, ear | 2 | 1 | 0 | long (A) ← (ear) | – | – | – | – | – | * | * | – | – | – |
| MOVL A, eam | 2+ | 3+ (a) | (d) | long (A) ← (eam) | – | – | – | – | – | * | * | – | – | – |
| MOVL A, # imm32 | 5 | 3 | 0 | long (A) ← imm32 | – | – | – | – | – | * | * | – | – | – |
| MOVL A, @SP + disp8 | 3 | 4 | (d) | long (A) ← ((SP) + disp8) | – | – | – | – | – | * | * | – | – | – |
| MOVPL A, addr24 | 5 | 4 | (d) | long (A) ← (addr24) | – | – | – | – | – | * | * | – | – | – |
| MOVPL A, @A | 2 | 3 | (d) | long (A) ← ((A)) | – | – | – | – | – | * | * | – | – | – |
| MOVPL @A, RLi | 2 | 5 | (d) | long ((A)) ← (RLi) | – | – | – | – | – | * | * | – | – | – |
| MOVL @SP + disp8, A | 3 | 4 | (d) | long ((SP) + disp8) ← (A) | – | – | – | – | – | * | * | – | – | – |
| MOVPL addr24, A | 5 | 4 | (d) | long (addr24) ← (A) | – | – | – | – | – | * | * | – | – | – |
| MOVL ear, A | 2 | 2 | 0 | long (ear) ← (A) | – | – | – | – | – | * | * | – | – | – |
| MOVL eam, A | 2+ | 3+ (a) | (d) | long (eam) ← (A) | – | – | – | – | – | * | * | – | – | – |

For an explanation of “(a)” and “(d)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

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Table 9 Addition and Subtraction Instructions (Byte/Word/Long Word) [42 Instructions]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|----------------|----|--------|--------|--|----|----|---|---|---|---|---|---|---|-----|
| ADD A, #imm8 | 2 | 2 | 0 | byte (A) ← (A) +imm8 | Z | – | – | – | – | * | * | * | * | – |
| ADD A, dir | 2 | 3 | (b) | byte (A) ← (A) +(dir) | Z | – | – | – | – | * | * | * | * | – |
| ADD A, ear | 2 | 2 | 0 | byte (A) ← (A) +(ear) | Z | – | – | – | – | * | * | * | * | – |
| ADD A, eam | 2+ | 3+ (a) | (b) | byte (A) ← (A) +(eam) | Z | – | – | – | – | * | * | * | * | – |
| ADD ear, A | 2 | 2 | 0 | byte (ear) ← (ear) + (A) | – | – | – | – | – | * | * | * | * | * |
| ADD eam, A | 2+ | 3+ (a) | 2× (b) | byte (eam) ← (eam) + (A) | Z | – | – | – | – | * | * | * | * | * |
| ADDC A | 1 | 2 | 0 | byte (A) ← (AH) + (AL) + (C) | Z | – | – | – | – | * | * | * | * | – |
| ADDC A, ear | 2 | 2 | 0 | byte (A) ← (A) + (ear) + (C) | Z | – | – | – | – | * | * | * | * | – |
| ADDC A, eam | 2+ | 3+ (a) | (b) | byte (A) ← (A) + (eam) + (C) | Z | – | – | – | – | * | * | * | * | – |
| ADDC A | 1 | 3 | 0 | byte (A) ← (AH) + (AL) + (C) (Decimal) | Z | – | – | – | – | * | * | * | * | – |
| SUB A, #imm8 | 2 | 2 | 0 | byte (A) ← (A) –imm8 | Z | – | – | – | – | * | * | * | * | – |
| SUB A, dir | 2 | 3 | (b) | byte (A) ← (A) – (dir) | Z | – | – | – | – | * | * | * | * | – |
| SUB A, ear | 2 | 2 | 0 | byte (A) ← (A) – (ear) | Z | – | – | – | – | * | * | * | * | – |
| SUB A, eam | 2+ | 3+ (a) | (b) | byte (A) ← (A) – (eam) | Z | – | – | – | – | * | * | * | * | – |
| SUB ear, A | 2 | 2 | 0 | byte (ear) ← (ear) – (A) | – | – | – | – | – | * | * | * | * | * |
| SUB eam, A | 2+ | 3+ (a) | 2× (b) | byte (eam) ← (eam) – (A) | – | – | – | – | – | * | * | * | * | * |
| SUBC A | 1 | 2 | 0 | byte (A) ← (AH) – (AL) – (C) | Z | – | – | – | – | * | * | * | * | – |
| SUBC A, ear | 2 | 2 | 0 | byte (A) ← (A) – (ear) – (C) | Z | – | – | – | – | * | * | * | * | – |
| SUBC A, eam | 2+ | 3+ (a) | (b) | byte (A) ← (A) – (eam) – (C) | Z | – | – | – | – | * | * | * | * | – |
| SUBC A | 1 | 3 | 0 | byte (A) ← (AH) – (AL) – (C) (Decimal) | Z | – | – | – | – | * | * | * | * | – |
| ADDW A | 1 | 2 | 0 | word (A) ← (AH) + (AL) | – | – | – | – | – | * | * | * | * | – |
| ADDW A, ear | 2 | 2 | 0 | word (A) ← (A) +(ear) | – | – | – | – | – | * | * | * | * | – |
| ADDW A, eam | 2+ | 3+ (a) | (c) | word (A) ← (A) +(eam) | – | – | – | – | – | * | * | * | * | – |
| ADDW A, #imm16 | 3 | 2 | 0 | word (A) ← (A) +imm16 | – | – | – | – | – | * | * | * | * | – |
| ADDW ear, A | 2 | 2 | 0 | word (ear) ← (ear) + (A) | – | – | – | – | – | * | * | * | * | * |
| ADDW eam, A | 2+ | 3+ (a) | 2× (c) | word (eam) ← (eam) + (A) | – | – | – | – | – | * | * | * | * | * |
| ADDCW A, ear | 2 | 2 | 0 | word (A) ← (A) + (ear) + (C) | – | – | – | – | – | * | * | * | * | – |
| ADDCW A, eam | 2+ | 3+ (a) | (c) | word (A) ← (A) + (eam) + (C) | – | – | – | – | – | * | * | * | * | – |
| SUBW A | 1 | 2 | 0 | word (A) ← (AH) – (AL) | – | – | – | – | – | * | * | * | * | – |
| SUBW A, ear | 2 | 2 | 0 | word (A) ← (A) – (ear) | – | – | – | – | – | * | * | * | * | – |
| SUBW A, eam | 2+ | 3+ (a) | (c) | word (A) ← (A) – (eam) | – | – | – | – | – | * | * | * | * | – |
| SUBW A, #imm16 | 3 | 2 | 0 | word (A) ← (A) –imm16 | – | – | – | – | – | * | * | * | * | – |
| SUBW ear, A | 2 | 2 | 0 | word (ear) ← (ear) – (A) | – | – | – | – | – | * | * | * | * | * |
| SUBW eam, A | 2+ | 3+ (a) | 2× (c) | word (eam) ← (eam) – (A) | – | – | – | – | – | * | * | * | * | * |
| SUBCW A, ear | 2 | 2 | 0 | word (A) ← (A) – (ear) – (C) | – | – | – | – | – | * | * | * | * | – |
| SUBCW A, eam | 2+ | 3+ (a) | (c) | word (A) ← (A) – (eam) – (C) | – | – | – | – | – | * | * | * | * | – |
| ADDL A, ear | 2 | 5 | 0 | long (A) ← (A) + (ear) | – | – | – | – | – | * | * | * | * | – |
| ADDL A, eam | 2+ | 6+ (a) | (d) | long (A) ← (A) + (eam) | – | – | – | – | – | * | * | * | * | – |
| ADDL A, #imm32 | 5 | 4 | 0 | long (A) ← (A) +imm32 | – | – | – | – | – | * | * | * | * | – |
| SUBL A, ear | 2 | 5 | 0 | long (A) ← (A) – (ear) | – | – | – | – | – | * | * | * | * | – |
| SUBL A, eam | 2+ | 6+ (a) | (d) | long (A) ← (A) – (eam) | – | – | – | – | – | * | * | * | * | – |
| SUBL A, #imm32 | 5 | 4 | 0 | long (A) ← (A) –imm32 | – | – | – | – | – | * | * | * | * | – |

For an explanation of “(a)”, “(b)”, “(c)” and “(d)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

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Table 10 Increment and Decrement Instructions (Byte/Word/Long Word) [12 Instructions]

| Mnemonic | | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|----------|-----|----|--------|--------|-----------------------|----|----|---|---|---|---|---|---|---|-----|
| INC | ear | 2 | 2 | 0 | byte (ear) ← (ear) +1 | – | – | – | – | – | * | * | * | – | * |
| INC | eam | 2+ | 3+ (a) | 2× (b) | byte (eam) ← (eam) +1 | – | – | – | – | – | * | * | * | – | * |
| DEC | ear | 2 | 2 | 0 | byte (ear) ← (ear) –1 | – | – | – | – | – | * | * | * | – | * |
| DEC | eam | 2+ | 3+ (a) | 2× (b) | byte (eam) ← (eam) –1 | – | – | – | – | – | * | * | * | – | * |
| INCW | ear | 2 | 2 | 0 | word (ear) ← (ear) +1 | – | – | – | – | – | * | * | * | – | * |
| INCW | eam | 2+ | 3+ (a) | 2× (c) | word (eam) ← (eam) +1 | – | – | – | – | – | * | * | * | – | * |
| DECW | ear | 2 | 2 | 0 | word (ear) ← (ear) –1 | – | – | – | – | – | * | * | * | – | * |
| DECW | eam | 2+ | 3+ (a) | 2× (c) | word (eam) ← (eam) –1 | – | – | – | – | – | * | * | * | – | * |
| INCL | ear | 2 | 4 | 0 | long (ear) ← (ear) +1 | – | – | – | – | – | * | * | * | – | * |
| INCL | eam | 2+ | 5+ (a) | 2× (d) | long (eam) ← (eam) +1 | – | – | – | – | – | * | * | * | – | * |
| DECL | ear | 2 | 4 | 0 | long (ear) ← (ear) –1 | – | – | – | – | – | * | * | * | – | * |
| DECL | eam | 2+ | 5+ (a) | 2× (d) | long (eam) ← (eam) –1 | – | – | – | – | – | * | * | * | – | * |

For an explanation of “(a)”, “(b)”, “(c)” and “(d)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 11 Compare Instructions (Byte/Word/Long Word) [11 Instructions]

| Mnemonic | | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|----------|-----------|----|--------|-----|------------------|----|----|---|---|---|---|---|---|---|-----|
| CMP | A | 1 | 2 | 0 | byte (AH) – (AL) | – | – | – | – | – | * | * | * | * | – |
| CMP | A, ear | 2 | 2 | 0 | byte (A) – (ear) | – | – | – | – | – | * | * | * | * | – |
| CMP | A, eam | 2+ | 2+ (a) | (b) | byte (A) – (eam) | – | – | – | – | – | * | * | * | * | – |
| CMP | A, #imm8 | 2 | 2 | 0 | byte (A) – imm8 | – | – | – | – | – | * | * | * | * | – |
| CMPW | A | 1 | 2 | 0 | word (AH) – (AL) | – | – | – | – | – | * | * | * | * | – |
| CMPW | A, ear | 2 | 2 | 0 | word (A) – (ear) | – | – | – | – | – | * | * | * | * | – |
| CMPW | A, eam | 2+ | 2+ (a) | (c) | word (A) – (eam) | – | – | – | – | – | * | * | * | * | – |
| CMPW | A, #imm16 | 3 | 2 | 0 | word (A) – imm16 | – | – | – | – | – | * | * | * | * | – |
| CMPL | A, ear | 2 | 3 | 0 | long (A) – (ear) | – | – | – | – | – | * | * | * | * | – |
| CMPL | A, eam | 2+ | 4+ (a) | (d) | long (A) – (eam) | – | – | – | – | – | * | * | * | * | – |
| CMPL | A, #imm32 | 5 | 3 | 0 | long (A) – imm32 | – | – | – | – | – | * | * | * | * | – |

For an explanation of “(a)”, “(b)”, “(c)” and “(d)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

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Table 12 Unsigned Multiplication and Division Instructions (Word/Long Word) [11 Instructions]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|--------------|----|--------|-----|--|----|----|---|---|---|---|---|---|---|-----|
| DIVU A | 1 | *1 | 0 | word (AH) /byte (AL) Quotient → byte (AL) Remainder → byte (AH) | — | — | — | — | — | — | — | * | * | — |
| DIVU A, ear | 2 | *2 | 0 | word (A)/byte (ear) Quotient → byte (A) Remainder → byte (ear) | — | — | — | — | — | — | — | * | * | — |
| DIVU A, eam | 2+ | *3 | *6 | word (A)/byte (eam) Quotient → byte (A) Remainder → byte (eam) | — | — | — | — | — | — | — | * | * | — |
| DIVUW A, ear | 2 | *4 | 0 | long (A)/word (ear) Quotient → word (A) Remainder → word (ear) | — | — | — | — | — | — | — | * | * | — |
| DIVUW A, eam | 2+ | *5 | *7 | long (A)/word (eam) Quotient → word (A) Remainder → word (eam) | — | — | — | — | — | — | — | * | * | — |
| MULU A | 1 | *8 | 0 | byte (AH) × byte (AL) → word (A) | — | — | — | — | — | — | — | — | — | — |
| MULU A, ear | 2 | *9 | 0 | byte (A) × byte (ear) → word (A) | — | — | — | — | — | — | — | — | — | — |
| MULU A, eam | 2+ | *10 | (b) | byte (A) × byte (eam) → word (A) | — | — | — | — | — | — | — | — | — | — |
| MULUW A | 1 | *11 | 0 | word (AH) × word (AL) → long (A) | — | — | — | — | — | — | — | — | — | — |
| MULUW A, ear | 2 | *12 | 0 | word (A) × word (ear) → long (A) | — | — | — | — | — | — | — | — | — | — |
| MULUW A, eam | 2+ | *13 | (c) | word (A) × word (eam) → long (A) | — | — | — | — | — | — | — | — | — | — |

For an explanation of “(b)” and “(c), refer to Table 5, “Correction Values for Number of Cycle Used to Calculate Number of Actual Cycles.”

*1: 3 when dividing into zero, 6 when an overflow occurs, and 14 normally.

*2: 3 when dividing into zero, 5 when an overflow occurs, and 13 normally.

*3: 5 + (a) when dividing into zero, 7 + (a) when an overflow occurs, and 17 + (a) normally.

*4: 3 when dividing into zero, 5 when an overflow occurs, and 21 normally.

*5: 4 + (a) when dividing into zero, 7 + (a) when an overflow occurs, and 25 + (a) normally.

*6: (b) when dividing into zero or when an overflow occurs, and 2 × (b) normally.

*7: (c) when dividing into zero or when an overflow occurs, and 2 × (c) normally.

*8: 3 when byte (AH) is zero, and 7 when byte (AH) is not 0.

*9: 3 when byte (ear) is zero, and 7 when byte (ear) is not 0.

*10: 4 + (a) when byte (eam) is zero, and 8 + (a) when byte (eam) is not 0.

*11: 3 when word (AH) is zero, and 11 when word (AH) is not 0.

*12: 3 when word (ear) is zero, and 11 when word (ear) is not 0.

*13: 4 + (a) when word (eam) is zero, and 12 + (a) when word (eam) is not 0.

Table 13 Signed Multiplication and Division Instructions (Word/Long Word) [11 Instructions]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|-------------|----|--------|-----|--|----|----|---|---|---|---|---|---|---|-----|
| DIV A | 2 | *1 | 0 | word (AH) /byte (AL) Quotient → byte (AL) Remainder → byte (AH) | Z | – | – | – | – | – | – | * | * | – |
| DIV A, ear | 2 | *2 | 0 | word (A)/byte (ear) Quotient → byte (A) Remainder → byte (ear) | Z | – | – | – | – | – | – | * | * | – |
| DIV A, eam | 2+ | *3 | *6 | word (A)/byte (eam) Quotient → byte (A) Remainder → byte (eam) | Z | – | – | – | – | – | – | * | * | – |
| DIVWA, ear | 2 | *4 | 0 | long (A)/word (ear) Quotient → word (A) Remainder → word (ear) | – | – | – | – | – | – | – | * | * | – |
| DIVWA, eam | 2+ | *5 | *7 | long (A)/word (eam) Quotient → word (A) Remainder → word (eam) | – | – | – | – | – | – | – | * | * | – |
| MUL A | 2 | *8 | 0 | byte (AH) × byte (AL) → word (A) | – | – | – | – | – | – | – | – | – | – |
| MUL A, ear | 2 | *9 | 0 | byte (A) × byte (ear) → word (A) | – | – | – | – | – | – | – | – | – | – |
| MUL A, eam | 2+ | *10 | (b) | byte (A) × byte (eam) → word (A) | – | – | – | – | – | – | – | – | – | – |
| MULW A | 2 | *11 | 0 | word (AH) × word (AL) → long (A) | – | – | – | – | – | – | – | – | – | – |
| MULW A, ear | 2 | *12 | 0 | word (A) × word (ear) → long (A) | – | – | – | – | – | – | – | – | – | – |
| MULW A, eam | 2+ | *13 | (b) | word (A) × word (eam) → long (A) | – | – | – | – | – | – | – | – | – | – |

For an explanation of “(b)” and “(c)”, refer to Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

*1: 3 when dividing into zero, 8 or 18 when an overflow occurs, and 18 normally.

*2: 3 when dividing into zero, 10 or 21 when an overflow occurs, and 22 normally.

*3: 4 + (a) when dividing into zero, 11 + (a) or 22 + (a) when an overflow occurs, and 23 + (a) normally.

*4: When the dividend is positive: 4 when dividing into zero, 10 or 29 when an overflow occurs, and 30 normally.
When the dividend is negative: 4 when dividing into zero, 11 or 30 when an overflow occurs, and 31 normally.

*5: When the dividend is positive: 4 + (a) when dividing into zero, 11 + (a) or 30 + (a) when an overflow occurs, and 31 + (a) normally.

When the dividend is negative: 4 + (a) when dividing into zero, 12 + (a) or 31 + (a) when an overflow occurs, and 32 + (a) normally.

*6: (b) when dividing into zero or when an overflow occurs, and 2 × (b) normally.

*7: (c) when dividing into zero or when an overflow occurs, and 2 × (c) normally.

*8: 3 when byte (AH) is zero, 12 when the result is positive, and 13 when the result is negative.

*9: 3 when byte (ear) is zero, 12 when the result is positive, and 13 when the result is negative.

*10: 4 + (a) when byte (eam) is zero, 13 + (a) when the result is positive, and 14 + (a) when the result is negative.

*11: 3 when word (AH) is zero, 12 when the result is positive, and 13 when the result is negative.

*12: 3 when word (ear) is zero, 16 when the result is positive, and 19 when the result is negative.

*13: 4 + (a) when word (eam) is zero, 17 + (a) when the result is positive, and 20 + (a) when the result is negative.

Note: Which of the two values given for the number of execution cycles applies when an overflow error occurs in a DIV or DIVW instruction depends on whether the overflow was detected before or after the operation.

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Table 14 Logical 1 Instructions (Byte, Word) [39 Instructions]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|----------------|----|--------|--------|----------------------------|----|----|---|---|---|---|---|---|---|-----|
| AND A, #imm8 | 2 | 2 | 0 | byte (A) ← (A) and imm8 | — | — | — | — | — | * | * | R | — | — |
| AND A, ear | 2 | 2 | 0 | byte (A) ← (A) and (ear) | — | — | — | — | — | * | * | R | — | — |
| AND A, eam | 2+ | 3+ (a) | (b) | byte (A) ← (A) and (eam) | — | — | — | — | — | * | * | R | — | — |
| AND ear, A | 2 | 3 | 0 | byte (ear) ← (ear) and (A) | — | — | — | — | — | * | * | R | — | * |
| AND eam, A | 2+ | 3+ (a) | 2× (b) | byte (eam) ← (eam) and (A) | — | — | — | — | — | * | * | R | — | * |
| OR A, #imm8 | 2 | 2 | 0 | byte (A) ← (A) or imm8 | — | — | — | — | — | * | * | R | — | — |
| OR A, ear | 2 | 2 | 0 | byte (A) ← (A) or (ear) | — | — | — | — | — | * | * | R | — | — |
| OR A, eam | 2+ | 3+ (a) | (b) | byte (A) ← (A) or (eam) | — | — | — | — | — | * | * | R | — | — |
| OR ear, A | 2 | 3 | 0 | byte (ear) ← (ear) or (A) | — | — | — | — | — | * | * | R | — | * |
| OR eam, A | 2+ | 3+ (a) | 2× (b) | byte (eam) ← (eam) or (A) | — | — | — | — | — | * | * | R | — | * |
| XOR A, #imm8 | 2 | 2 | 0 | byte (A) ← (A) xor imm8 | — | — | — | — | — | * | * | R | — | — |
| XOR A, ear | 2 | 2 | 0 | byte (A) ← (A) xor (ear) | — | — | — | — | — | * | * | R | — | — |
| XOR A, eam | 2+ | 3+ (a) | (b) | byte (A) ← (A) xor (eam) | — | — | — | — | — | * | * | R | — | — |
| XOR ear, A | 2 | 3 | 0 | byte (ear) ← (ear) xor (A) | — | — | — | — | — | * | * | R | — | * |
| XOR eam, A | 2+ | 3+ (a) | 2× (b) | byte (eam) ← (eam) xor (A) | — | — | — | — | — | * | * | R | — | * |
| NOT A | 1 | 2 | 0 | byte (A) ← not (A) | — | — | — | — | — | * | * | R | — | — |
| NOT ear | 2 | 2 | 0 | byte (ear) ← not (ear) | — | — | — | — | — | * | * | R | — | * |
| NOT eam | 2+ | 3+ (a) | 2× (b) | byte (eam) ← not (eam) | — | — | — | — | — | * | * | R | — | * |
| ANDW A | 1 | 2 | 0 | word (A) ← (AH) and (A) | — | — | — | — | — | * | * | R | — | — |
| ANDW A, #imm16 | 3 | 2 | 0 | word (A) ← (A) and imm16 | — | — | — | — | — | * | * | R | — | — |
| ANDW A, ear | 2 | 2 | 0 | word (A) ← (A) and (ear) | — | — | — | — | — | * | * | R | — | — |
| ANDW A, eam | 2+ | 3+ (a) | (c) | word (A) ← (A) and (eam) | — | — | — | — | — | * | * | R | — | — |
| ANDW ear, A | 2 | 3 | 0 | word (ear) ← (ear) and (A) | — | — | — | — | — | * | * | R | — | * |
| ANDW eam, A | 2+ | 3+ (a) | 2× (c) | word (eam) ← (eam) and (A) | — | — | — | — | — | * | * | R | — | * |
| ORW A | 1 | 2 | 0 | word (A) ← (AH) or (A) | — | — | — | — | — | * | * | R | — | — |
| ORW A, #imm16 | 3 | 2 | 0 | word (A) ← (A) or imm16 | — | — | — | — | — | * | * | R | — | — |
| ORW A, ear | 2 | 2 | 0 | word (A) ← (A) or (ear) | — | — | — | — | — | * | * | R | — | — |
| ORW A, eam | 2+ | 3+ (a) | (c) | word (A) ← (A) or (eam) | — | — | — | — | — | * | * | R | — | — |
| ORW ear, A | 2 | 3 | 0 | word (ear) ← (ear) or (A) | — | — | — | — | — | * | * | R | — | * |
| ORW eam, A | 2+ | 3+ (a) | 2× (c) | word (eam) ← (eam) or (A) | — | — | — | — | — | * | * | R | — | * |
| XORW A | 1 | 2 | 0 | word (A) ← (AH) xor (A) | — | — | — | — | — | * | * | R | — | — |
| XORW A, #imm16 | 3 | 2 | 0 | word (A) ← (A) xor imm16 | — | — | — | — | — | * | * | R | — | — |
| XORW A, ear | 2 | 2 | 0 | word (A) ← (A) xor (ear) | — | — | — | — | — | * | * | R | — | — |
| XORW A, eam | 2+ | 3+ (a) | (c) | word (A) ← (A) xor (eam) | — | — | — | — | — | * | * | R | — | — |
| XORW ear, A | 2 | 3 | 0 | word (ear) ← (ear) xor (A) | — | — | — | — | — | * | * | R | — | * |
| XORW eam, A | 2+ | 3+ (a) | 2× (c) | word (eam) ← (eam) xor (A) | — | — | — | — | — | * | * | R | — | * |
| NOTW A | 1 | 2 | 0 | word (A) ← not (A) | — | — | — | — | — | * | * | R | — | — |
| NOTW ear | 2 | 2 | 0 | word (ear) ← not (ear) | — | — | — | — | — | * | * | R | — | * |
| NOTW eam | 2+ | 3+ (a) | 2× (c) | word (eam) ← not (eam) | — | — | — | — | — | * | * | R | — | * |

For an explanation of “(a)”, “(b)”, “(c)” and “(d)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

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Table 15 Logical 2 Instructions (Long Word) [6 Instructions]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|-------------|----|--------|-----|--------------------------|----|----|---|---|---|---|---|---|---|-----|
| ANDL A, ear | 2 | 5 | 0 | long (A) ← (A) and (ear) | – | – | – | – | – | * | * | R | – | – |
| ANDL A, eam | 2+ | 6+ (a) | (d) | long (A) ← (A) and (eam) | – | – | – | – | – | * | * | R | – | – |
| ORL A, ear | 2 | 5 | 0 | long (A) ← (A) or (ear) | – | – | – | – | – | * | * | R | – | – |
| ORL A, eam | 2+ | 6+ (a) | (d) | long (A) ← (A) or (eam) | – | – | – | – | – | * | * | R | – | – |
| XORL A, ear | 2 | 5 | 0 | long (A) ← (A) xor (ear) | – | – | – | – | – | * | * | R | – | – |
| XORL A, eam | 2+ | 6+ (a) | (d) | long (A) ← (A) xor (eam) | – | – | – | – | – | * | * | R | – | – |

For an explanation of “(a)” and “(d)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 16 Sign Inversion Instructions (Byte/Word) [6 Instructions]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|----------|----|--------|--------|------------------------|----|----|---|---|---|---|---|---|---|-----|
| NEG A | 1 | 2 | 0 | byte (A) ← 0 – (A) | X | – | – | – | – | * | * | * | * | – |
| NEG ear | 2 | 2 | 0 | byte (ear) ← 0 – (ear) | – | – | – | – | – | * | * | * | * | * |
| NEG eam | 2+ | 3+ (a) | 2× (b) | byte (eam) ← 0 – (eam) | – | – | – | – | – | * | * | * | * | * |
| NEGW A | 1 | 2 | 0 | word (A) ← 0 – (A) | – | – | – | – | – | * | * | * | * | – |
| NEGW ear | 2 | 2 | 0 | word (ear) ← 0 – (ear) | – | – | – | – | – | * | * | * | * | * |
| NEGW eam | 2+ | 3+ (a) | 2× (c) | word (eam) ← 0 – (eam) | – | – | – | – | – | * | * | * | * | * |

For an explanation of “(a)”, “(b)” and “(c)” and refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 17 Absolute Value Instructions (Byte/Word/Long Word) [3 Instructions]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|----------|---|--------|---|-------------------------------|----|----|---|---|---|---|---|---|---|-----|
| ABS A | 2 | 2 | 0 | byte (A) ← absolute value (A) | Z | – | – | – | – | * | * | * | – | – |
| ABSW A | 2 | 2 | 0 | word (A) ← absolute value (A) | – | – | – | – | – | * | * | * | – | – |
| ABSL A | 2 | 4 | 0 | long (A) ← absolute value (A) | – | – | – | – | – | * | * | * | – | – |

Table 18 Normalize Instructions (Long Word) [1 Instruction]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|------------|---|--------|---|---|----|----|---|---|---|---|---|---|---|-----|
| NRML A, R0 | 2 | * | 0 | long (A) ← Shifts to the position at which “1” was set first byte (R0) ← current shift count | – | – | – | – | * | – | – | – | – | – |

* : 5 when the contents of the accumulator are all zeroes, 5 + (R0) in all other cases.

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Table 19 Shift Instructions (Byte/Word/Long Word) [27 Instructions]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|---------------|----|--------|--------|--|----|----|---|---|---|---|---|---|---|-----|
| RORC A | 2 | 2 | 0 | byte (A) ← Right rotation with carry | – | – | – | – | – | * | * | – | * | – |
| ROLC A | 2 | 2 | 0 | byte (A) ← Left rotation with carry | – | – | – | – | – | * | * | – | * | – |
| RORC ear | 2 | 2 | 0 | byte (ear) ← Right rotation with carry | – | – | – | – | – | * | * | – | * | * |
| RORC eam | 2+ | 3+ (a) | 2× (b) | byte (eam) ← Right rotation with carry | – | – | – | – | – | * | * | – | * | * |
| ROLC ear | 2 | 2 | 0 | byte (ear) ← Left rotation with carry | – | – | – | – | – | * | * | – | * | * |
| ROLC eam | 2+ | 3+ (a) | 2× (b) | byte (eam) ← Left rotation with carry | – | – | – | – | – | * | * | – | * | * |
| ASR A, R0 | 2 | *1 | 0 | byte (A) ← Arithmetic right barrel shift (A, R0) | – | – | – | – | * | * | * | – | * | – |
| LSR A, R0 | 2 | *1 | 0 | byte (A) ← Logical right barrel shift (A, R0) | – | – | – | – | * | * | * | – | * | – |
| LSL A, R0 | 2 | *1 | 0 | byte (A) ← Logical left barrel shift (A, R0) | – | – | – | – | – | * | * | – | * | – |
| ASR A, #imm8 | 3 | *3 | 0 | byte (A) ← Arithmetic right barrel shift (A, imm8) | – | – | – | – | * | * | * | – | * | – |
| LSR A, #imm8 | 3 | *3 | 0 | byte (A) ← Logical right barrel shift (A, imm8) | – | – | – | – | * | * | * | – | * | – |
| LSL A, #imm8 | 3 | *3 | 0 | byte (A) ← Logical left barrel shift (A, imm8) | – | – | – | – | – | * | * | – | * | – |
| ASRW A | 1 | 2 | 0 | word (A) ← Arithmetic right shift (A, 1 bit) | – | – | – | – | * | * | * | – | * | – |
| LSRW A/SHRW A | 1 | 2 | 0 | word (A) ← Logical right shift (A, 1 bit) | – | – | – | – | * | R | * | – | * | – |
| LSLW A/SHLW A | 1 | 2 | 0 | word (A) ← Logical left shift (A, 1 bit) | – | – | – | – | – | * | * | – | * | – |
| ASRW A, R0 | 2 | *1 | 0 | word (A) ← Arithmetic right barrel shift (A, R0) | – | – | – | – | * | * | * | – | * | – |
| LSRW A, R0 | 2 | *1 | 0 | word (A) ← Logical right barrel shift (A, R0) | – | – | – | – | * | * | * | – | * | – |
| LSLW A, R0 | 2 | *1 | 0 | word (A) ← Logical left barrel shift (A, R0) | – | – | – | – | – | * | * | – | * | – |
| ASRW A, #imm8 | 3 | *3 | 0 | word (A) ← Arithmetic right barrel shift (A, imm8) | – | – | – | – | * | * | * | – | * | – |
| LSRW A, #imm8 | 3 | *3 | 0 | word (A) ← Logical right barrel shift (A, imm8) | – | – | – | – | * | * | * | – | * | – |
| LSLW A, #imm8 | 3 | *3 | 0 | word (A) ← Logical left barrel shift (A, imm8) | – | – | – | – | – | * | * | – | * | – |
| ASRL A, R0 | 2 | *2 | 0 | long (A) ← Arithmetic right shift (A, R0) | – | – | – | – | * | * | * | – | * | – |
| LSRL A, R0 | 2 | *2 | 0 | long (A) ← Logical right barrel shift (A, R0) | – | – | – | – | * | * | * | – | * | – |
| LSLL A, R0 | 2 | *2 | 0 | long (A) ← Logical left barrel shift (A, R0) | – | – | – | – | – | * | * | – | * | – |
| ASRL A, #imm8 | 3 | *4 | 0 | long (A) ← Arithmetic right shift (A, imm8) | – | – | – | – | * | * | * | – | * | – |
| LSRL A, #imm8 | 3 | *4 | 0 | long (A) ← Logical right barrel shift (A, imm8) | – | – | – | – | * | * | * | – | * | – |
| LSLL A, #imm8 | 3 | *4 | 0 | long (A) ← Logical left barrel shift (A, imm8) | – | – | – | – | – | * | * | – | * | – |

For an explanation of “(a)” and “(b)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

*1: 3 when R0 is 0, 3 + (R0) in all other cases.

*2: 3 when R0 is 0, 4 + (R0) in all other cases.

*3: 3 when imm8 is 0, 3 + (imm8) in all other cases.

*4: 3 when imm8 is 0, 4 + (imm8) in all other cases.

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Table 20 Branch 1 Instructions [31 Instructions]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|-----------------|----|--------|--------|--|----|----|---|---|---|---|---|---|---|-----|
| BZ/BEQ rel | 2 | *1 | 0 | Branch when (Z) = 1 | - | - | - | - | - | - | - | - | - | - |
| BNZ/BNE rel | 2 | *1 | 0 | Branch when (Z) = 0 | - | - | - | - | - | - | - | - | - | - |
| BC/BLO rel | 2 | *1 | 0 | Branch when (C) = 1 | - | - | - | - | - | - | - | - | - | - |
| BNC/BHS rel | 2 | *1 | 0 | Branch when (C) = 0 | - | - | - | - | - | - | - | - | - | - |
| BN rel | 2 | *1 | 0 | Branch when (N) = 1 | - | - | - | - | - | - | - | - | - | - |
| BP rel | 2 | *1 | 0 | Branch when (N) = 0 | - | - | - | - | - | - | - | - | - | - |
| BV rel | 2 | *1 | 0 | Branch when (V) = 1 | - | - | - | - | - | - | - | - | - | - |
| BNV rel | 2 | *1 | 0 | Branch when (V) = 0 | - | - | - | - | - | - | - | - | - | - |
| BT rel | 2 | *1 | 0 | Branch when (T) = 1 | - | - | - | - | - | - | - | - | - | - |
| BNT rel | 2 | *1 | 0 | Branch when (T) = 0 | - | - | - | - | - | - | - | - | - | - |
| BLT rel | 2 | *1 | 0 | Branch when (V) xor (N) = 1 | - | - | - | - | - | - | - | - | - | - |
| BGE rel | 2 | *1 | 0 | Branch when (V) xor (N) = 0 | - | - | - | - | - | - | - | - | - | - |
| BLE rel | 2 | *1 | 0 | ((V) xor (N)) or (Z) = 1 | - | - | - | - | - | - | - | - | - | - |
| BGT rel | 2 | *1 | 0 | ((V) xor (N)) or (Z) = 0 | - | - | - | - | - | - | - | - | - | - |
| BLS rel | 2 | *1 | 0 | Branch when (C) or (Z) = 1 | - | - | - | - | - | - | - | - | - | - |
| BHI rel | 2 | *1 | 0 | Branch when (C) or (Z) = 0 | - | - | - | - | - | - | - | - | - | - |
| BRA rel | 2 | *1 | 0 | Branch unconditionally | - | - | - | - | - | - | - | - | - | - |
| JMP @A | 1 | 2 | 0 | word (PC) ← (A) | - | - | - | - | - | - | - | - | - | - |
| JMP addr16 | 3 | 2 | 0 | word (PC) ← addr16 | - | - | - | - | - | - | - | - | - | - |
| JMP @ear | 2 | 3 | 0 | word (PC) ← (ear) | - | - | - | - | - | - | - | - | - | - |
| JMP @eam | 2+ | 4+ (a) | (c) | word (PC) ← (eam) | - | - | - | - | - | - | - | - | - | - |
| JMPP @ear *3 | 2 | 3 | 0 | word (PC) ← (ear), (PCB) ← (ear +2) | - | - | - | - | - | - | - | - | - | - |
| JMPP @eam *3 | 2+ | 4+ (a) | (d) | word (PC) ← (eam), (PCB) ← (eam +2) | - | - | - | - | - | - | - | - | - | - |
| JMPP addr24 | 4 | 3 | 0 | word (PC) ← ad24 0 to 15 (PCB) ← ad24 16 to 23 | - | - | - | - | - | - | - | - | - | - |
| CALL @ear *4 | 2 | 4 | (c) | word (PC) ← (ear) | - | - | - | - | - | - | - | - | - | - |
| CALL @eam *4 | 2+ | 5+ (a) | 2× (c) | word (PC) ← (eam) | - | - | - | - | - | - | - | - | - | - |
| CALL addr16 *5 | 3 | 5 | (c) | word (PC) ← addr16 | - | - | - | - | - | - | - | - | - | - |
| CALLV #vct4 *5 | 1 | 5 | 2× (c) | Vector call instruction | - | - | - | - | - | - | - | - | - | - |
| CALLP @ear *6 | 2 | 7 | 2× (c) | word (PC) ← (ear) 0 to 15, (PCB) ← (ear) 16 to 23 | - | - | - | - | - | - | - | - | - | - |
| CALLP @eam *6 | 2+ | 8+ (a) | *2 | word (PC) ← (eam) 0 to 15, (PCB) ← (eam) 16 to 23 | - | - | - | - | - | - | - | - | - | - |
| CALLP addr24 *7 | 4 | 7 | 2× (c) | word (PC) ← addr 0 to 15, (PCB) ← addr 16 to 23 | - | - | - | - | - | - | - | - | - | - |

For an explanation of “(a)”, “(c)” and “(d)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

*1: 3 when branching, 2 when not branching.

*2: $3 \times (c) + (b)$

*3: Read (word) branch address.

*4: W: Save (word) to stack; R: Read (word) branch address.

*5: Save (word) to stack.

*6: W: Save (long word) to W stack; R: Read (long word) branch address.

*7: Save (long word) to stack.

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Table 21 Branch 2 Instructions [20 Instructions]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|------------------------|----|--------|----------------|--|----|----|---|---|---|---|---|---|---|-----|
| CBNE A, #imm8, rel | 3 | *1 | 0 | Branch when byte (A) \neq imm8 | — | — | — | — | — | * | * | * | * | — |
| CWBNE A, #imm16, rel | 4 | *1 | 0 | Branch when byte (A) \neq imm16 | — | — | — | — | — | * | * | * | * | — |
| CBNE ear, #imm8, rel | 4 | *1 | 0 | Branch when byte (ear) \neq imm8 | — | — | — | — | — | * | * | * | * | — |
| CBNE eam, #imm8, rel | 4+ | *3 | (b) | Branch when byte (eam) \neq imm8 | — | — | — | — | — | * | * | * | * | — |
| CWBNE ear, #imm16, rel | 5 | *3 | 0 | Branch when word (ear) \neq imm16 | — | — | — | — | — | * | * | * | * | — |
| CWBNE eam, #imm16, rel | 5+ | *2 | (c) | Branch when word (eam) \neq imm16 | — | — | — | — | — | * | * | * | * | — |
| DBNZ ear, rel | 3 | *4 | 0 | Branch when byte (ear) = (ear) – 1, and (ear) \neq 0 | — | — | — | — | — | * | * | * | — | — |
| DBNZ eam, rel | 3+ | *2 | 2 \times (b) | Branch when byte (ear) = (eam) – 1, and (eam) \neq 0 | — | — | — | — | — | * | * | * | — | * |
| DWBNZ ear, rel | 3 | *4 | 0 | Branch when word (ear) = (ear) – 1, and (ear) \neq 0 | — | — | — | — | — | * | * | * | — | — |
| DWBNZ eam, rel | 3+ | | 2 \times (c) | Branch when word (eam) = (eam) – 1, and (eam) \neq 0 | — | — | — | — | — | * | * | * | — | * |
| | | 14 | | | | | | | | | | | | |
| | | 12 | | | | | | | | | | | | |
| INT #vct8 | 2 | 13 | 8 \times (c) | Software interrupt | — | — | R | S | — | — | — | — | — | — |
| INT addr16 | 3 | 14 | 6 \times (c) | Software interrupt | — | — | R | S | — | — | — | — | — | — |
| INTP addr24 | 4 | 9 | 6 \times (c) | Software interrupt | — | — | R | S | — | — | — | — | — | — |
| INT9 | 1 | 11 | 8 \times (c) | Software interrupt | — | — | R | S | — | — | — | — | — | — |
| RETI | 1 | | 6 \times (c) | Return from interrupt | — | — | * | * | * | * | * | * | * | — |
| RETIQ *6 | 2 | 6 | *5 | Return from interrupt | — | — | * | * | * | * | * | * | * | — |
| LINK #imm8 | 2 | | (c) | At constant entry, save old frame pointer to stack, set new frame pointer, and allocate local pointer area | — | — | — | — | — | — | — | — | — | — |
| | | 5 | | | | | | | | | | | | |
| UNLINK | 1 | | (c) | At constant entry, retrieve old frame pointer from stack. | — | — | — | — | — | — | — | — | — | — |
| | | 4 | | | | | | | | | | | | |
| | | 5 | | | | | | | | | | | | |
| RET *7 | 1 | | (c) | Return from subroutine | — | — | — | — | — | — | — | — | — | — |
| RETP *8 | 1 | | (d) | Return from subroutine | — | — | — | — | — | — | — | — | — | — |

For an explanation of “(b)”, “(c)” and “(d)”, refer to Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

*1: 4 when branching, 3 when not branching

*2: 5 when branching, 4 when not branching

*3: 5 + (a) when branching, 4 + (a) when not branching

*4: 6 + (a) when branching, 5 + (a) when not branching

*5: 3 \times (b) + 2 \times (c) when an interrupt request is generated, 6 \times (c) when returning from the interrupt.

*6: High-speed interrupt return instruction. When an interrupt request is detected during this instruction, the instruction branches to the interrupt vector without performing stack operations when the interrupt is generated.

*7: Return from stack (word)

*8: Return from stack (long word)

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Table 22 Other Control Instructions (Byte/Word/Long Word) [36 Instructions]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|-------------------|----|--------|--------|--|----|----|---|---|---|---|---|---|---|-----|
| PUSHW A | 1 | 3 | (c) | word (SP) ← (SP) - 2, ((SP)) ← (A) | - | - | - | - | - | - | - | - | - | - |
| PUSHW AH | 1 | 3 | (c) | word (SP) ← (SP) - 2, ((SP)) ← (AH) | - | - | - | - | - | - | - | - | - | - |
| PUSHW PS | 1 | 3 | (c) | word (SP) ← (SP) - 2, ((SP)) ← (PS) | - | - | - | - | - | - | - | - | - | - |
| PUSHW rlst | 2 | *3 | *4 | (SP) ← (SP) - 2n, ((SP)) ← (rlst) | - | - | - | - | - | - | - | - | - | - |
| POPW A | 1 | 3 | (c) | word (A) ← ((SP)), (SP) ← (SP) + 2 | - | * | - | - | - | - | - | - | - | - |
| POPW AH | 1 | 3 | (c) | word (AH) ← ((SP)), (SP) ← (SP) + 2 | - | - | - | - | - | - | - | - | - | - |
| POPW PS | 1 | 3 | (c) | word (PS) ← ((SP)), (SP) ← (SP) + 2 | - | - | * | * | * | * | * | * | * | - |
| POPW rlst | 2 | *2 | *4 | (rlst) ← ((SP)), (SP) ← (SP) | - | - | - | - | - | - | - | - | - | - |
| JCTX @A | 1 | 9 | 6× (c) | Context switch instruction | - | - | * | * | * | * | * | * | * | - |
| AND CCR, #imm8 | 2 | 3 | 0 | byte (CCR) ← (CCR) and imm8 | - | - | * | * | * | * | * | * | * | - |
| OR CCR, #imm8 | 2 | 3 | 0 | byte (CCR) ← (CCR) or imm8 | - | - | * | * | * | * | * | * | * | - |
| MOV RP, #imm8 | 2 | 2 | 0 | byte (RP) ← imm8 | - | - | - | - | - | - | - | - | - | - |
| MOV ILM, #imm8 | 2 | 2 | 0 | byte (ILM) ← imm8 | - | - | - | - | - | - | - | - | - | - |
| MOVEA RWi, ear | 2 | 3 | 0 | word (RWi) ← ear | - | - | - | - | - | - | - | - | - | - |
| MOVEA RWi, eam | 2+ | 2+ (a) | 0 | word (RWi) ← eam | - | - | - | - | - | - | - | - | - | - |
| MOVEA A, ear | 2 | 2 | 0 | word (A) ← ear | - | * | - | - | - | - | - | - | - | - |
| MOVEA A, eam | 2+ | 1+ (a) | 0 | word (A) ← eam | - | * | - | - | - | - | - | - | - | - |
| ADDSP #imm8 | 2 | 3 | 0 | word (SP) ← ext (imm8) | - | - | - | - | - | - | - | - | - | - |
| ADDSP #imm16 | 3 | 3 | 0 | word (SP) ← imm16 | - | - | - | - | - | - | - | - | - | - |
| MOV A, brgl | 2 | *1 | 0 | byte (A) ← (brgl) | Z | * | - | - | - | * | * | - | - | - |
| MOV brg2, A | 2 | 1 | 0 | byte (brg2) ← (A) | - | - | - | - | - | * | * | - | - | - |
| MOV brg2, #imm8 | 3 | 2 | 0 | byte (brg2) ← imm8 | - | - | - | - | - | * | * | - | - | - |
| NOP | 1 | 1 | 0 | No operation | - | - | - | - | - | - | - | - | - | - |
| ADB | 1 | 1 | 0 | Prefix code for AD space access | - | - | - | - | - | - | - | - | - | - |
| DTB | 1 | 1 | 0 | Prefix code for DT space access | - | - | - | - | - | - | - | - | - | - |
| PCB | 1 | 1 | 0 | Prefix code for PC space access | - | - | - | - | - | - | - | - | - | - |
| SPB | 1 | 1 | 0 | Prefix code for SP space access | - | - | - | - | - | - | - | - | - | - |
| NCC | 1 | 1 | 0 | Prefix code for no flag change | - | - | - | - | - | - | - | - | - | - |
| CMR | 1 | 1 | 0 | Prefix code for the common register bank | - | - | - | - | - | - | - | - | - | - |
| MOVW SPCU, #imm16 | 4 | 2 | 0 | word (SPCU) ← (imm16) | - | - | - | - | - | - | - | - | - | - |
| MOVW SPCL, #imm16 | 4 | 2 | 0 | word (SPCL) ← (imm16) | - | - | - | - | - | - | - | - | - | - |
| SETSPC | 2 | 2 | 0 | Stack check operation enable | - | - | - | - | - | - | - | - | - | - |
| CLRSPC | 2 | 2 | 0 | Stack check operation disable | - | - | - | - | - | - | - | - | - | - |
| BTSCN A | 2 | *5 | 0 | byte (A) ← position of "1" bit in word (A) | Z | - | - | - | - | - | * | - | - | - |
| BTSCNS A | 2 | *6 | 0 | byte (A) ← position of "1" bit in word (A) × 2 | Z | - | - | - | - | - | * | - | - | - |
| BTSCND A | 2 | *7 | 0 | byte (A) ← position of "1" bit in word (A) × 4 | Z | - | - | - | - | - | * | - | - | - |

For an explanation of "(a)" and "(c)", refer to Tables 4 and 5.

*1: PCB, ADB, SSB, USB, and SPB: 1 cycle

DTB: 2 cycles

DPR: 3 cycles

*2: 3 + 4 × (pop count)

*3: 3 + 4 × (push count)

*4: Pop count × (c), or push count × (c)

*5: 3 when AL is 0, 5 when AL is not 0.

*6: 4 when AL is 0, 6 when AL is not 0.

*7: 5 when AL is 0, 7 when AL is not 0.

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Table 23 Bit Manipulation Instructions [21 Instructions]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|---------------------|---|--------|--------|--|----|----|---|---|---|---|---|---|---|-----|
| MOVB A, dir:bp | 3 | 3 | (b) | byte (A) ← (dir:bp) b | Z | * | — | — | — | * | * | — | — | — |
| MOVB A, addr16:bp | 4 | 3 | (b) | byte (A) ← (addr16:bp) b | Z | * | — | — | — | * | * | — | — | — |
| MOVB A, io:bp | 3 | 3 | (b) | byte (A) ← (io:bp) b | Z | * | — | — | — | * | * | — | — | — |
| MOVB dir:bp, A | 3 | 4 | 2× (b) | bit (dir:bp) b ← (A) | — | — | — | — | — | * | * | — | — | * |
| MOVB addr16:bp, A | 4 | 4 | 2× (b) | bit (addr16:bp) b ← (A) | — | — | — | — | — | * | * | — | — | * |
| MOVB io:bp, A | 3 | 4 | 2× (b) | bit (io:bp) b ← (A) | — | — | — | — | — | * | * | — | — | * |
| SETB dir:bp | 3 | 4 | 2× (b) | bit (dir:bp) b ← 1 | — | — | — | — | — | — | — | — | — | * |
| SETB addr16:bp | 4 | 4 | 2× (b) | bit (addr16:bp) b ← 1 | — | — | — | — | — | — | — | — | — | * |
| SETB io:bp | 3 | 4 | 2× (b) | bit (io:bp) b ← 1 | — | — | — | — | — | — | — | — | — | * |
| CLRB dir:bp | 3 | 4 | 2× (b) | bit (dir:bp) b ← 0 | — | — | — | — | — | — | — | — | — | * |
| CLRB addr16:bp | 4 | 4 | 2× (b) | bit (addr16:bp) b ← 0 | — | — | — | — | — | — | — | — | — | * |
| CLRB io:bp | 3 | 4 | 2× (b) | bit (io:bp) b ← 0 | — | — | — | — | — | — | — | — | — | * |
| BBC dir:bp, rel | 4 | *1 | (b) | Branch when (dir:bp) b = 0 | — | — | — | — | — | — | * | — | — | — |
| BBC addr16:bp, rel | 5 | *1 | (b) | Branch when (addr16:bp) b = 0 | — | — | — | — | — | — | * | — | — | — |
| BBC io:bp, rel | 4 | *1 | (b) | Branch when (io:bp) b = 0 | — | — | — | — | — | — | * | — | — | — |
| BBS dir:bp, rel | 4 | *1 | (b) | Branch when (dir:bp) b = 1 | — | — | — | — | — | — | * | — | — | — |
| BBS addr16:bp, rel | 5 | *1 | (b) | Branch when (addr16:bp) b = 1 | — | — | — | — | — | — | * | — | — | — |
| BBS io:bp, rel | 4 | *1 | (b) | Branch when (io:bp) b = 1 | — | — | — | — | — | — | * | — | — | — |
| SBBS addr16:bp, rel | 5 | *2 | 2× (b) | Branch when (addr16:bp) b = 1, bit = 1 | — | — | — | — | — | — | * | — | — | * |
| WBTS io:bp | 3 | *3 | *4 | Wait until (io:bp) b = 1 | — | — | — | — | — | — | — | — | — | — |
| WBTC io:bp | 3 | *3 | *4 | Wait until (io:bp) b = 0 | — | — | — | — | — | — | — | — | — | — |

For an explanation of “(b)”, refer to Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

*1: 5 when branching, 4 when not branching

*2: 7 when condition is satisfied, 6 when not satisfied

*3: Undefined count

*4: Until condition is satisfied

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Table 24 Accumulator Manipulation Instructions (Byte/Word) [6 Instructions]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|----------|---|--------|---|---|----|----|---|---|---|---|---|---|---|-----|
| SWAP | 1 | 3 | 0 | byte (A) 0 to 7 \leftrightarrow (A) 8 to 15 | - | - | - | - | - | - | - | - | - | - |
| SWAPW | 1 | 2 | 0 | word (AH) \leftrightarrow (AL) | - | * | - | - | - | - | - | - | - | - |
| EXT | 1 | 1 | 0 | Byte code extension | X | - | - | - | - | * | * | - | - | - |
| EXTW | 1 | 2 | 0 | Word code extension | - | X | - | - | - | * | * | - | - | - |
| ZEXT | 1 | 1 | 0 | Byte zero extension | Z | - | - | - | - | R | * | - | - | - |
| ZEXTW | 1 | 2 | 0 | Word zero extension | - | Z | - | - | - | R | * | - | - | - |

Table 25 String Instructions [10 Instructions]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|--------------|---|--------|----|---|----|----|---|---|---|---|---|---|---|-----|
| MOVS/MOVS | 2 | *2 | *3 | Byte transfer @AH+ \leftarrow @AL+, counter = RW0 | - | - | - | - | - | - | - | - | - | - |
| MOVSD | 2 | *2 | *3 | Byte transfer @AH- \leftarrow @AL-, counter = RW0 | - | - | - | - | - | - | - | - | - | - |
| SCEQ/SCEQI | 2 | *1 | *4 | Byte retrieval @AH+ - AL, counter = RW0 | - | - | - | - | - | * | * | * | * | - |
| SCEQD | 2 | *1 | *4 | Byte retrieval @AH- - AL, counter = RW0 | - | - | - | - | - | * | * | * | * | - |
| FILS/FILSI | 2 | 5m +3 | *5 | Byte filling @AH+ \leftarrow AL, counter = RW0 | - | - | - | - | - | * | * | - | - | - |
| MOVSW/MOVSWI | 2 | *2 | *6 | Word transfer @AH+ \leftarrow @AL+, counter = RW0 | - | - | - | - | - | - | - | - | - | - |
| MOVSWD | 2 | *2 | *6 | Word transfer @AH- \leftarrow @AL-, counter = RW0 | - | - | - | - | - | - | - | - | - | - |
| SCWEQ/SCWEQI | 2 | *1 | *7 | Word retrieval @AH+ - AL, counter = RW0 | - | - | - | - | - | * | * | * | * | - |
| SCWEQD | 2 | *1 | *7 | Word retrieval @AH- - AL, counter = RW0 | - | - | - | - | - | * | * | * | * | - |
| FILSW/FILSWI | 2 | 5m +3 | *8 | Word filling @AH+ \leftarrow AL, counter = RW0 | - | - | - | - | - | * | * | - | - | - |

m: RW0 value (counter value)

*1: 3 when RW0 is 0, $2 + 6 \times (RW0)$ for count out, and $6n + 4$ when match occurs

*2: 4 when RW0 is 0, $2 + 6 \times (RW0)$ in any other case

*3: $(b) \times (RW0)$

*4: $(b) \times n$

*5: $(b) \times (RW0)$

*6: $(c) \times (RW0)$

*7: $(c) \times n$

*8: $(c) \times (RW0)$

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Table 26 Multiple Data Transfer Instructions [18 Instructions]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|---------------------------|----|--------|----|--|----|----|---|---|---|---|---|---|---|-----|
| MOVM @A, @RLi, #imm8 | 3 | *1 | *3 | Multiple data transfer byte ((A)) ← ((RLi)) | — | — | — | — | — | — | — | — | — | — |
| MOVM @A, eam, #imm8 | 3+ | *2 | *3 | Multiple data transfer byte ((A)) ← (eam) | — | — | — | — | — | — | — | — | — | — |
| MOVM addr16, @RLi, #imm8 | 5 | *1 | *3 | Multiple data transfer byte (addr16) ← ((RLi)) | — | — | — | — | — | — | — | — | — | — |
| MOVM addr16, eam, #imm8 | 5+ | *2 | *3 | Multiple data transfer byte (addr16) ← (eam) | — | — | — | — | — | — | — | — | — | — |
| MOVMW @A, @RLi, #imm8 | 3 | *1 | *4 | Multiple data transfer word ((A)) ← ((RLi)) | — | — | — | — | — | — | — | — | — | — |
| MOVMW @A, eam, #imm8 | 3+ | *2 | *4 | Multiple data transfer word ((A)) ← (eam) | — | — | — | — | — | — | — | — | — | — |
| MOVMW addr16, @RLi, #imm8 | 5 | *1 | *4 | Multiple data transfer word (addr16) ← ((RLi)) | — | — | — | — | — | — | — | — | — | — |
| MOVMW addr16, eam, #imm8 | 5+ | *2 | *4 | Multiple data transfer word (addr16) ← (eam) | — | — | — | — | — | — | — | — | — | — |
| MOVM @RLi, @A, #imm8 | 3 | *1 | *3 | Multiple data transfer byte ((RLi)) ← ((A)) | — | — | — | — | — | — | — | — | — | — |
| MOVM eam, @A, #imm8 | 3+ | *2 | *3 | Multiple data transfer byte (eam) ← ((A)) | — | — | — | — | — | — | — | — | — | — |
| MOVM @RLi, addr16, #imm8 | 5 | *1 | *3 | Multiple data transfer byte ((RLi)) ← (addr16) | — | — | — | — | — | — | — | — | — | — |
| MOVM eam, addr16, #imm8 | 5+ | *2 | *3 | Multiple data transfer byte (eam) ← (addr16) | — | — | — | — | — | — | — | — | — | — |
| MOVMW @RLi, @A, #imm8 | 3 | *1 | *4 | Multiple data transfer word ((RLi)) ← ((A)) | — | — | — | — | — | — | — | — | — | — |
| MOVMW eam, @A, #imm8 | 3+ | *2 | *4 | Multiple data transfer word (eam) ← ((A)) | — | — | — | — | — | — | — | — | — | — |
| MOVMW@RLi, addr16, #imm8 | 5 | *1 | *4 | Multiple data transfer word ((RLi)) ← (addr16) | — | — | — | — | — | — | — | — | — | — |
| MOVMW eam, addr16, #imm8 | 5+ | *2 | *4 | Multiple data transfer word (eam) ← (addr16) | — | — | — | — | — | — | — | — | — | — |
| MOVM bnk : addr16, *5 | 7 | *1 | *3 | Multiple data transfer | — | — | — | — | — | — | — | — | — | — |
| bnk : addr16, #imm8 | | | | byte (bnk:addr16) ← (bnk:addr16) | | | | | | | | | | |
| MOVMW bnk : addr16, *5 | 7 | *1 | *4 | Multiple data transfer | — | — | — | — | — | — | — | — | — | — |
| bnk : addr16, #imm8 | | | | word (bnk:addr16) ← (bnk:addr16) | | | | | | | | | | |

*1: $5 + \text{imm8} \times 5$, 256 times when imm8 is zero.

*2: $5 + \text{imm8} \times 5 + (a)$, 256 times when imm8 is zero.

*3: Number of transfers $\times (b) \times 2$

*4: Number of transfers $\times (c) \times 2$

*5: The bank register specified by "bnk" is the same as for the MOVS instruction.

MB90220 Series

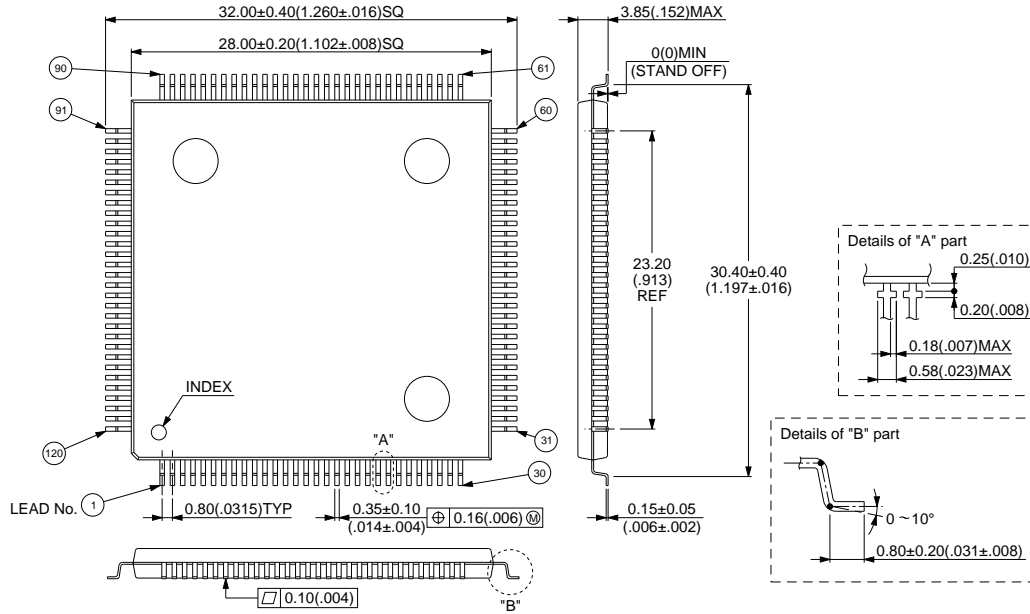
■ ORDERING INFORMATION

| Part number | Type | Package | Remarks |
|--|---|---------------------------------------|----------------|
| MB90224 MB90223 MB90P224A MB90P224B | MB90224PF MB90223PF MB90P224PF MB90P224BPF | 120-pin Plastic QFP (FPT-120P-M03) | |
| MB90W224A MB90W224B | MB90W224ZF MB90W224BZF | 120-pin Ceramic QFP (FPT-120C-C02) | ES level only |
| MB90V220 | MB90V220CR | 256-pin Ceramic PGA (PGA-256C-A02) | For evaluation |

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PACKAGE DIMENSIONS

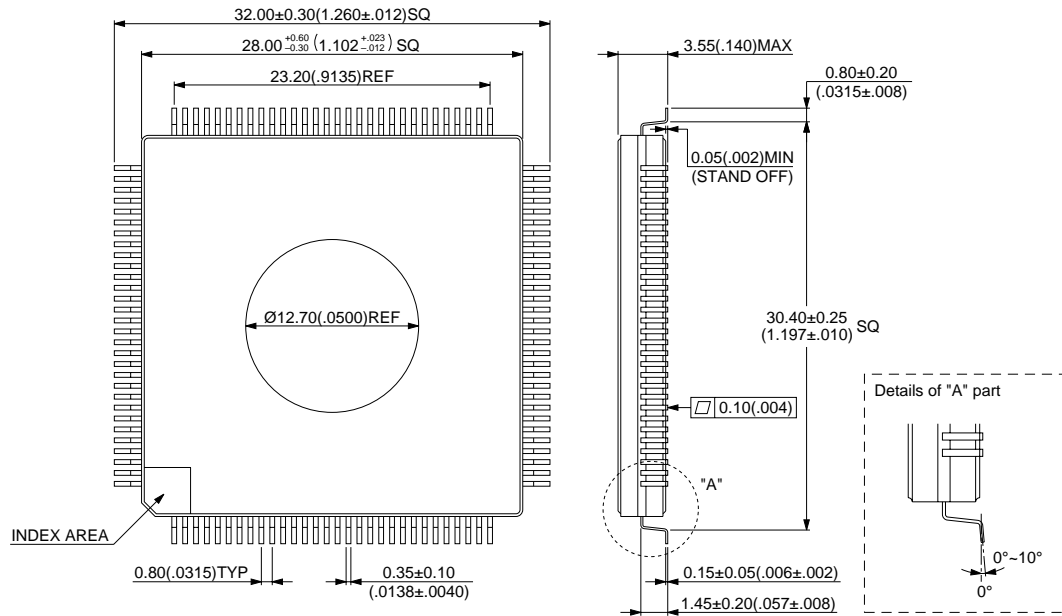
120-pin Plastic QFP
(FPT-120P-M03)



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Dimensions in mm (inches)

120-pin Ceramic QFP
(FPT-120C-C02)



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Dimensions in mm (inches)

Note: See to the latest version of Package Data Book for official package dimensions.

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