

MCP (Multi-Chip Package) FLASH MEMORY & SRAM CMOS

8M (× 8) FLASH MEMORY & 2M (× 8) STATIC RAM

MB84VA2000-10/MB84VA2001-10

■ FEATURES

- Power supply voltage of 2.7 to 3.6 V
- High performance
100 ns maximum access time
- Operating Temperature
-20 to +85°C

— FLASH MEMORY

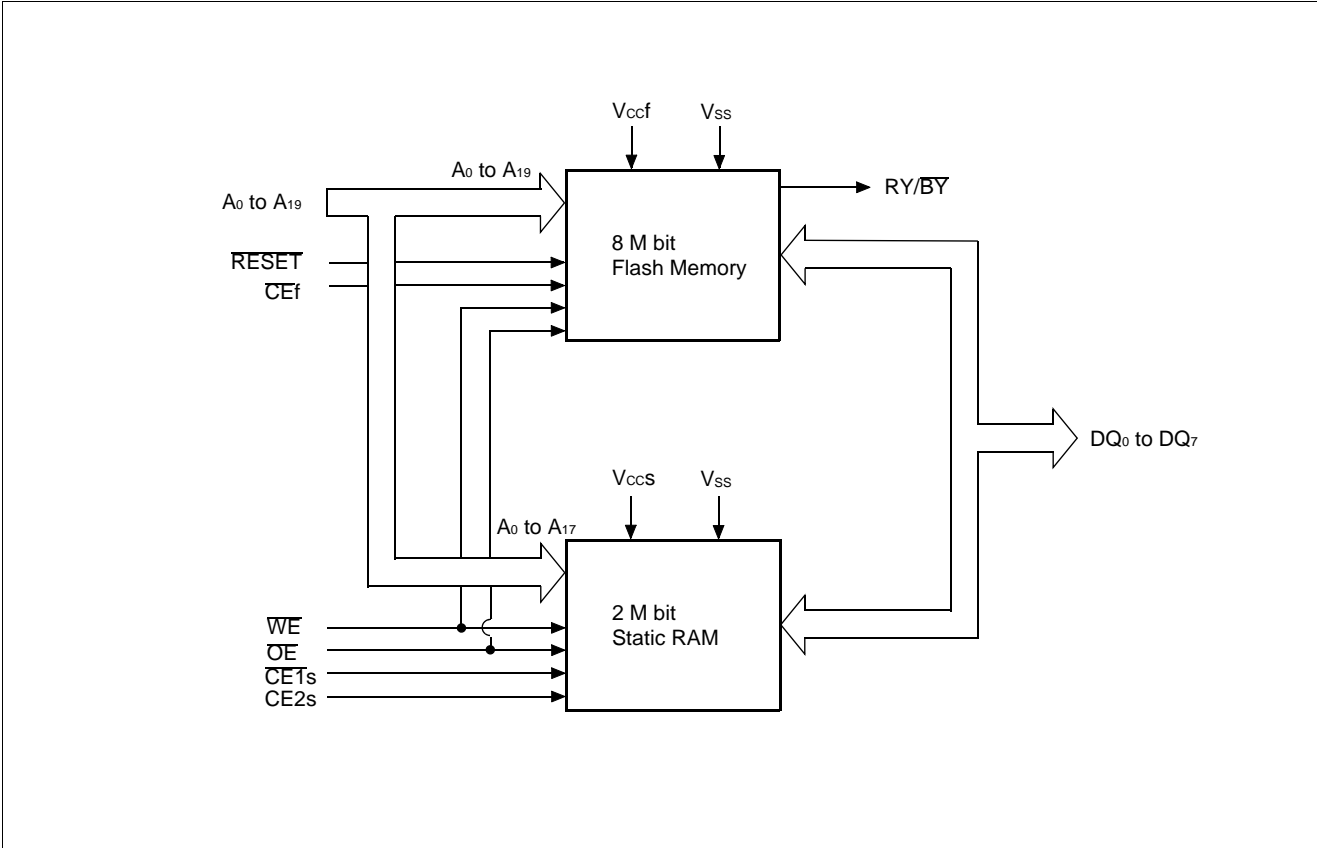
- Minimum 100,000 write/erase cycles
- Sector erase architecture
One 16 K byte, two 8 K bytes, one 32 K byte, and fifteen 64 K bytes.
Any combination of sectors can be concurrently erased. Also supports full chip erase.
- Boot Code Sector Architecture
MB84VA2000: Top sector
MB84VA2001: Bottom sector
- Embedded Erase™ Algorithms
Automatically pre-programs and erases the chip or any sector
- Embedded Program™ Algorithms
Automatically writes and verifies data at specified address
- Data Polling and Toggle Bit feature for detection of program or erase cycle completion
- Ready-Busy output (RY/BY)
Hardware method for detection of program or erase cycle completion
- Automatic sleep mode
When addresses remain stable, automatically switch themselves to low power mode.
- Low V_{cc} write inhibit ≤ 2.5 V
- Erase Suspend/Resume
Suspends the erase operation to allow a read in another sector within the same device
- Please refer to "MBM29LV800TA/BA" data sheet in detailed function

— SRAM

- Power dissipation
Operating : 35 mA max.
Standby : 50 μA max.
- Power down features using $\overline{CE1}$ s and CE2s
- Data retention supply voltage: 2.0 V to 3.6 V

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■ BLOCK DIAGRAM



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■ PIN ASSIGNMENTS

(Top View)

	A	B	C	D	E	F	G	H
6	$\overline{CE1s}$	V _{SS}	DQ ₁	A ₁	A ₂	A ₄	CE _{2s}	A ₉
5	A ₁₀	DQ ₅	DQ ₂	A ₀	A ₃	A ₇	RY/BY	A ₁₅
4	\overline{OE}	DQ ₇	DQ ₄	DQ ₀	A ₆	A ₁₉	RESET	A ₁₆
3	A ₁₁	A ₈	A ₅	N.C.	DQ ₃	N.C.	A ₁₃	N.C.
2	A ₁₄	A ₁₈	N.C.	\overline{CEf}	N.C.	V _{ccf}	DQ ₆	A ₁₂
1	WE	V _{ccs}	A ₁₇	V _{SS}	N.C.	N.C.	N.C.	N.C.

Table 1 Pin Configuration

Pin	Function	Input/ Output
A ₀ to A ₁₇	Address Inputs (Common)	I
A ₁₈ to A ₁₉	Address Input (Flash)	I
DQ ₀ to DQ ₇	Data Inputs/Outputs (Common)	I/O
\overline{CEf}	Chip Enable (Flash)	I
$\overline{CE1s}$	Chip Enable (SRAM)	I
CE _{2s}	Chip Enable (SRAM)	I
\overline{OE}	Output Enable (Common)	I
WE	Write Enable (Common)	I
RY/BY	Ready/Busy Outputs (Flash)	O
RESET	Hardware Reset Pin/Sector Protection Unlock (Flash)	I
N.C.	No Internal Connection	—
V _{SS}	Device Ground (Common)	Power
V _{ccf}	Device Power Supply (Flash)	Power
V _{ccs}	Device Power Supply (SRAM)	Power

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■ PRODUCT LINE UP

		Flash Memory	SRAM
Ordering Part No.	$V_{CC} = 3.0\text{ V}$ ^{+0.6V} / _{-0.3V}	MB84VA2000-10/MB84VA2001-10	
Max. Address Access Time (ns)		100	100
Max. \overline{CE} Access Time (ns)		100	100
Max. \overline{OE} Access Time (ns)		40	50

■ BUS OPERATIONS

Table 2 User Bus Operations

Operation (1), (3)	\overline{CEf}	$\overline{CE1s}$	$CE2s$	\overline{OE}	\overline{WE}	DQ_0 to DQ_7	RESET
Full Standby	H	H	X	X	X	HIGH-Z	H
		X	L				
Output Disable	X	X	X	H	H	HIGH-Z	H
Read from Flash (2)	L	H	X	L	H	D_{OUT}	H
		X	L				
Write to Flash	L	H	X	H	L	D_{IN}	H
		X	L				
Read from SRAM	H	L	H	L	H	D_{OUT}	H
Write to SRAM	H	L	H	X	L	D_{IN}	H
Flash Hardware Reset	X	H	X	X	X	HIGH-Z	L
		X	L				

Legend: L = V_{IL} , H = V_{IH} , X = V_{IL} or V_{IH} . See DC Characteristics for voltage levels.

- Notes:**
1. Other operations except for indicated this column are inhibited.
 2. \overline{WE} can be V_{IL} if \overline{OE} is V_{IL} , \overline{OE} at V_{IH} initiates the write operations.
 3. Do not apply $\overline{CEf} = V_{IL}$, $\overline{CE1s} = V_{IL}$ and $CE2s = V_{IH}$ at a time.

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■ FLEXIBLE SECTOR-ERASE ARCHITECTURE on FLASH MEMORY

- One 16 K byte, two 8 K bytes, one 32 K byte, and fifteen 64 K bytes.
- Individual-sector, multiple-sector, or bulk-erase capability.

16K byte	FFFFFH	64K byte	FFFFFH
8K byte	FC000H	64K byte	F0000H
8K byte	FA000H	64K byte	E0000H
32K byte	F8000H	64K byte	D0000H
64K byte	F0000H	64K byte	C0000H
64K byte	E0000H	64K byte	B0000H
64K byte	D0000H	64K byte	A0000H
64K byte	C0000H	64K byte	90000H
64K byte	B0000H	64K byte	80000H
64K byte	A0000H	64K byte	70000H
64K byte	90000H	64K byte	60000H
64K byte	80000H	64K byte	50000H
64K byte	70000H	64K byte	40000H
64K byte	60000H	64K byte	30000H
64K byte	50000H	64K byte	20000H
64K byte	40000H	64K byte	10000H
64K byte	30000H	32K byte	08000H
64K byte	20000H	8K byte	06000H
64K byte	10000H	8K byte	04000H
64K byte	00000H	16K byte	00000H

MB84VA2000 Sector Architecture

MB84VA2001 Sector Architecture

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Table 3 Sector Address Tables (MB84VA2000)

Sector Address	A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	Address Range
SA0	0	0	0	0	X	X	X	00000H to 0FFFFH
SA1	0	0	0	1	X	X	X	10000H to 1FFFFH
SA2	0	0	1	0	X	X	X	20000H to 2FFFFH
SA3	0	0	1	1	X	X	X	30000H to 3FFFFH
SA4	0	1	0	0	X	X	X	40000H to 4FFFFH
SA5	0	1	0	1	X	X	X	50000H to 5FFFFH
SA6	0	1	1	0	X	X	X	60000H to 6FFFFH
SA7	0	1	1	1	X	X	X	70000H to 7FFFFH
SA8	1	0	0	0	X	X	X	80000H to 8FFFFH
SA9	1	0	0	1	X	X	X	90000H to 9FFFFH
SA10	1	0	1	0	X	X	X	A0000H to AFFFFH
SA11	1	0	1	1	X	X	X	B0000H to BFFFFH
SA12	1	1	0	0	X	X	X	C0000H to CFFFFH
SA13	1	1	0	1	X	X	X	D0000H to DFFFFH
SA14	1	1	1	0	X	X	X	E0000H to EFFFFH
SA15	1	1	1	1	0	X	X	F0000H to F7FFFH
SA16	1	1	1	1	1	0	0	F8000H to F9FFFH
SA17	1	1	1	1	1	0	1	FA000H to FBFFFH
SA18	1	1	1	1	1	1	X	FC000H to FFFFFH

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Table 4 Sector Address Tables (MB84VA2001)

Sector Address	A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	Address Range
SA0	0	0	0	0	0	0	X	00000H to 03FFFFH
SA1	0	0	0	0	0	1	0	04000H to 05FFFFH
SA2	0	0	0	0	0	1	1	06000H to 07FFFFH
SA3	0	0	0	0	1	X	X	08000H to 0FFFFH
SA4	0	0	0	1	X	X	X	10000H to 1FFFFH
SA5	0	0	1	0	X	X	X	20000H to 2FFFFH
SA6	0	0	1	1	X	X	X	30000H to 3FFFFH
SA7	0	1	0	0	X	X	X	40000H to 4FFFFH
SA8	0	1	0	1	X	X	X	50000H to 5FFFFH
SA9	0	1	1	0	X	X	X	60000H to 6FFFFH
SA10	0	1	1	1	X	X	X	70000H to 7FFFFH
SA11	1	0	0	0	X	X	X	80000H to 8FFFFH
SA12	1	0	0	1	X	X	X	90000H to 9FFFFH
SA13	1	0	1	0	X	X	X	A0000H to AFFFFH
SA14	1	0	1	1	X	X	X	B0000H to BFFFFH
SA15	1	1	0	0	X	X	X	C0000H to CFFFFH
SA16	1	1	0	1	X	X	X	D0000H to DFFFFH
SA17	1	1	1	0	X	X	X	E0000H to EFFFFH
SA18	1	1	1	1	X	X	X	F0000H to FFFFFH

MB84VA2000-10/MB84VA2001-10**Table 5. 1 Flash Memory Autoselect Code**

Type		A ₁₂	A ₆	A ₁	A ₀	Code (HEX)
Manufacturer's Code		V _{IL}	V _{IL}	V _{IL}	V _{IL}	04H
Device Code	MB84VA2000	V _{IL}	V _{IL}	V _{IL}	V _{IH}	DAH
	MB84VA2001	V _{IL}	V _{IL}	V _{IL}	V _{IH}	5BH

Table 5. 2 Expanded Autoselect Code Table

Type		Code	DQ ₇	DQ ₆	DQ ₅	DQ ₄	DQ ₃	DQ ₂	DQ ₁	DQ ₀
Manufacturer's Code		04H	0	0	0	0	0	1	0	0
Device Code	MB84VA2000	DAH	1	1	0	1	1	0	1	0
	MB84VA2001	5BH	0	1	0	1	1	0	1	1

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Table 6 Flash Memory Command Definitions

Command Sequence	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset	1	XXXH	F0H	—	—	—	—	—	—	—	—	—	—
Read/Reset	3	555H	AAH	2AAH	55H	555H	F0H	RA	RD	—	—	—	—
Autoselect	3	555H	AAH	2AAH	55H	555H	90H	—	—	—	—	—	—
Program	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD	—	—	—	—
Chip Erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
Sector Erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA	30H
Sector Erase Suspend	Erase can be suspended during sector erase with Addr ("H" or "L"). Data (B0H)												
Sector Erase Resume	Erase can be resumed after suspend with Addr ("H" or "L"). Data (30H)												
Set to Fast Mode	3	555H	AAH	2AAH	55H	555H	20H	—	—	—	—	—	—
Fast Program (Note)	2	XXXH	A0H	PA	PD	—	—	—	—	—	—	—	—
Reset from Fast Mode (Note)	2	XXXH	90H	XXXH	F0H	—	—	—	—	—	—	—	—
Extended Sector Protect	4	XXXH	60H	SPA	60H	SPA	40H	SPA	SD	—	—	—	—

Address bits A_{11} to $A_{20} = X = "H"$ or $"L"$ for all address commands except for Program Address (PA) and Sector Address (SA).

Bus operations are defined in Table 2.

Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.

RA =Address of the memory location to be read.

PA =Address of the memory location to be programmed. Addresses are latched on the falling edge of the write pulse.

SA =Address of the sector to be erased. The combination of A_{20} , A_{19} , A_{18} , A_{17} , A_{16} , A_{15} , A_{14} , and A_{13} will uniquely select any sector.

RD =Data read from location RA during read operation.

PD =Data to be programmed at location PA.

SPA =Sector address to be protected. Set sector address (SA) and $(A_6, A_1, A_0) = (0, 1, 0)$.

SD =Sector protection verify data. Output 01H at protected sector addresses and output 00H at unprotected sector addresses.

Note:This command is valid while Fast Mode.

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■ ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-25°C to +85°C
Voltage with Respect to Ground All pins (Note)	-0.3 V to $V_{ccf} + 0.5$ V
	-0.3 V to $V_{ccs} + 0.5$ V
V_{ccf}/V_{ccs} Supply (Note)	-0.3 V to +4.6 V

Note: Minimum DC voltage on input or I/O pins are -0.5 V. During voltage transitions, inputs may negativeovershoot V_{ss} to -2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins are $V_{ccf} + 0.5$ V or $V_{ccs} + 0.5$ V. During voltage transitions, outputs may positive overshoot to $V_{cc} + 2.0$ V for periods of up to 20 ns.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum rating conditions. Do not exceed these ratings.

■ RECOMMENDED OPERATING RANGES

Commercial Devices	
Ambient Temperature (T_A)	-20°C to +85°C
V_{ccf}/V_{ccs} Supply Voltages.....	+2.7 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

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■ DC CHARACTERISTICS

Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ.	Max.	Unit	
I _{LI}	Input Leakage Current	—		-1.0	—	+1.0	μA	
I _{LO}	Output Leakage Current	—		-1.0	—	+1.0	μA	
I _{CC1f}	Flash V _{CC} Active Current (Read)	V _{CCf} = V _{CC} Max., $\overline{CE}f = V_{IL}$ OE = V _{IH}	t _{CYCLE} = 10 MHz	—	—	22	mA	
			t _{CYCLE} = 5 MHz	—	—	12		
I _{CC2f}	Flash V _{CC} Active Current (Program/Erase)	V _{CCf} = V _{CC} Max., $\overline{CE}f = V_{IL}$, OE = V _{IH}		—	—	35	mA	
I _{CC1S}	SRAM V _{CC} Active Current	V _{CCS} = V _{CC} Max., $\overline{CE}1s = V_{IL}$, CE2s = V _{IH}	t _{CYCLE} = 10 MHz	—	—	40	mA	
			t _{CYCLE} = 1 MHz	—	—	12	mA	
I _{CC2S}	SRAM V _{CC} Active Current	$\overline{CE}1s = 0.2$ V, CE2s = V _{CCS} - 0.2 V, WE = V _{CCS} - 0.2 V	t _{CYCLE} = 10 MHz	—	—	35	mA	
			t _{CYCLE} = 1 MHz	—	—	6	mA	
I _{SB1f}	Flash V _{CC} Standby Current	V _{CCf} = V _{CC} Max., $\overline{CE}f = V_{CCf} \pm 0.3$ V RESET = V _{CCf} ± 0.3 V		—	—	5	μA	
I _{SB2f}	Flash V _{CC} Standby Current (RESET)	V _{CCf} = V _{CC} Max., RESET = V _{SS} ± 0.3 V		—	—	5	μA	
I _{SB1S}	SRAM V _{CC} Standby Current	$\overline{CE}1s = V_{IH}$ or CE2s = V _{IL}		—	—	2	mA	
I _{SB2S**}	SRAM V _{CC} Standby Current	$\overline{CE}1s = V_{CC} - 0.2$ V or CE2s = 0.2 V	V _{CCS} = 3.0 V ± 10%	T _A = 25°C	—	1	2.5	μA
				T _A = -20 to +85°C	—	—	55	μA
			V _{CCS} = 3.3 V ± 0.3 V	T _A = 25°C	—	1.5	3	μA
				T _A = -20 to +85°C	—	—	60	μA
			V _{CCS} = 3.0 V	T _A = 25°C	—	1	2	μA
				T _A = -20 to +85°C	—	—	5	μA
V _{IL}	Input Low Level	—		-0.3	—	0.6	V	
V _{IH}	Input High Level	—		2.2	—	V _{CC} +0.3*	V	
V _{OL}	Output Low Voltage Level	I _{OL} = 2.1 mA, V _{CCf} = V _{CCS} = V _{CC} Min.		—	—	0.4	V	
V _{OH}	Output High Voltage Level	I _{OH} = -500 μA, V _{CCf} = V _{CCS} = V _{CC} Min.		V _{CC} - 0.5	—	—	V	
V _{LKO}	Flash Low V _{CC} Lock-Out Voltage	—		2.3	—	2.5	V	

* : V_{CC} indicate lower of V_{CCf} or V_{CCS}** : During standby mode with $\overline{CE}1s = V_{CCS} - 0.2$ V, CE2s should be CE2s < 0.2V or CE2s > V_{CCS} - 0.2V

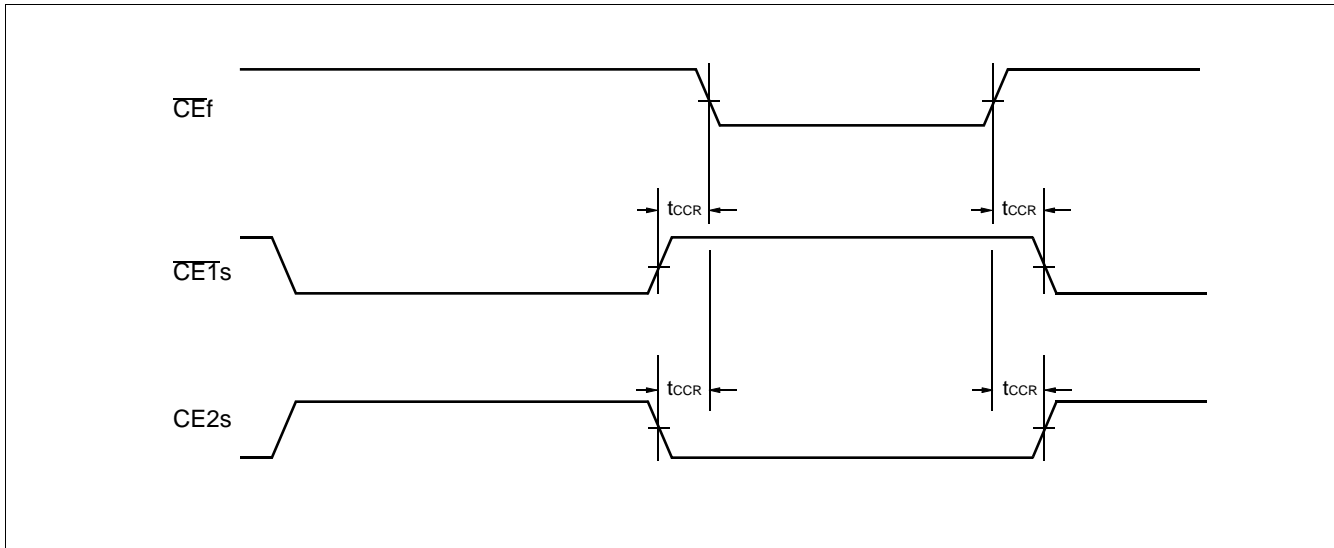
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■ AC CHARACTERISTICS

• CE Timing

Parameter Symbols		Description	Test Setup		-10	Unit
JEDEC	Standard					
—	t_{CCR}	CE Recover Time	—	Min.	0	ns

• Timing Diagram for alternating SRAM to Flash



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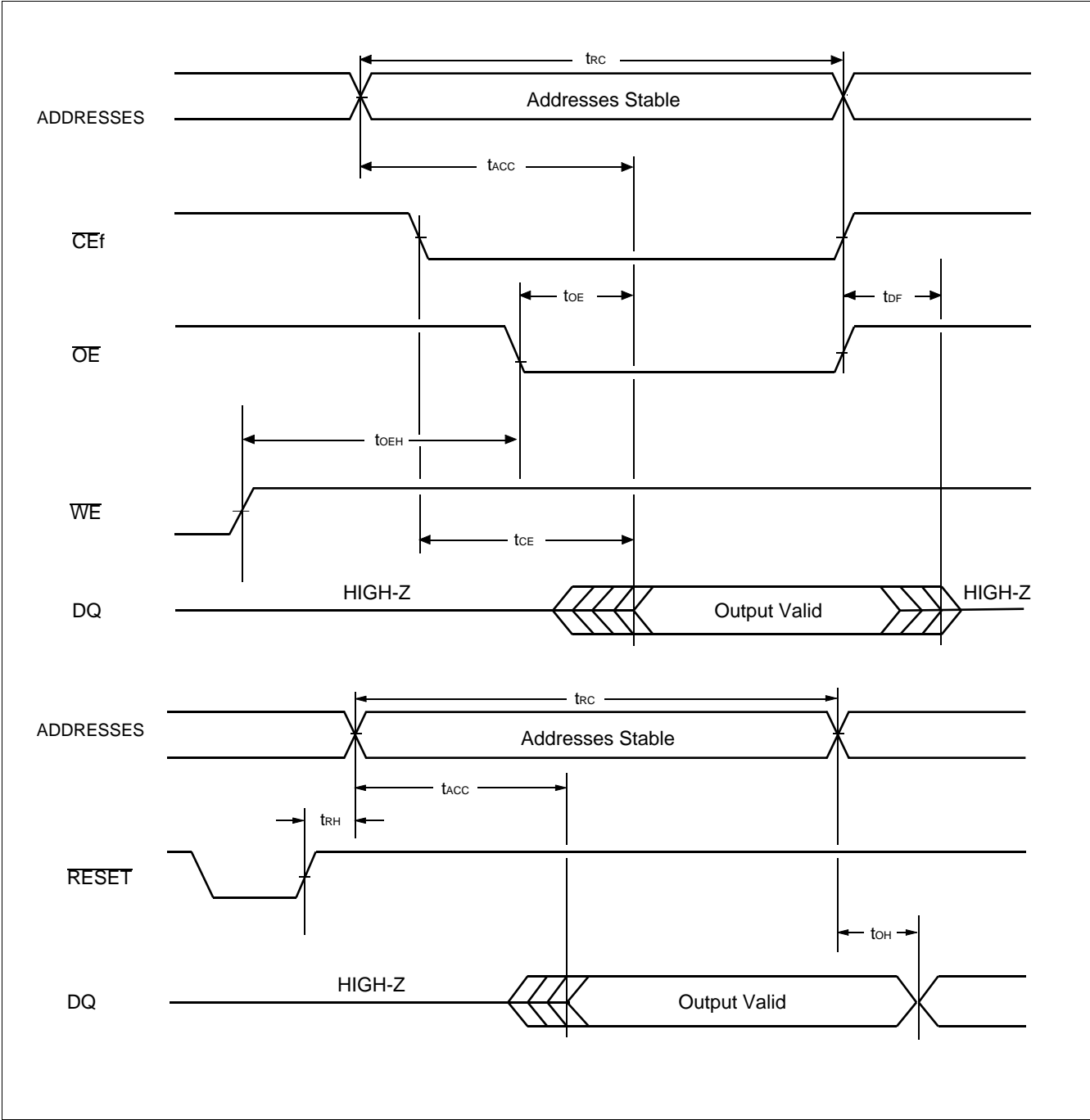
• Read Only Operations Characteristics (Flash)

Parameter Symbols		Description	Test Setup	-10 (Note)		Unit
JEDEC	Standard			Min.	Max.	
t _{AVAV}	t _{RC}	Read Cycle Time	—	100	—	ns
t _{AVQV}	t _{ACC}	Address to Output Delay	$\overline{CE}f = V_{IL}$ $\overline{OE} = V_{IL}$	—	100	ns
t _{ELQV}	t _{CEf}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	—	100	ns
t _{GLQV}	t _{OE}	Output Enable to Output Delay	—	—	40	ns
t _{EHQZ}	t _{DF}	Chip Enable to Output High-Z	—	—	30	ns
t _{GHQZ}	t _{DF}	Output Enable to Output High-Z	—	—	30	ns
t _{AXQX}	t _{OH}	Output Hold Time From Addresses, $\overline{CE}f$ or \overline{OE} , Whichever Occurs First	—	0	—	ns
—	t _{READY}	RESET Pin Low to Read Mode	—	—	20	μs

Note: Test Conditions—Output Load: 1 TTL gate and 30 pF
 Input rise and fall times: 5 ns
 Input pulse levels: 0.0 V to 3.0 V
 Timing measurement reference level
 Input: 1.5 V
 Output: 1.5 V

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• Read Cycle (Flash)



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• Erase/Program Operations (Flash)

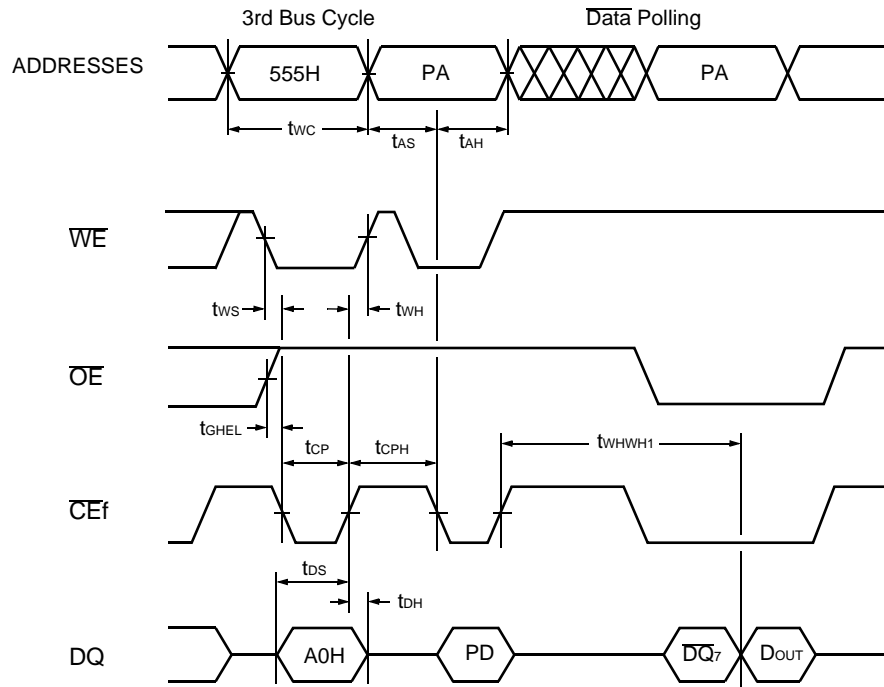
Parameter Symbols		Description	-10			Unit
JEDEC	Standard		Min.	Typ.	Max.	
tAVAV	tWC	Write Cycle Time	100	—	—	ns
tAVWL	tAS	Address Setup Time (\overline{WE} to Addr.)	0	—	—	ns
tAVEL	tAS	Address Setup Time (\overline{CEf} to Addr.)	0	—	—	ns
tWLAX	tAH	Address Hold Time (\overline{WE} to Addr.)	50	—	—	ns
tELAX	tAH	Address Hold Time (\overline{CEf} to Addr.)	50	—	—	ns
tdVWH	tdS	Data Setup Time	50	—	—	ns
tWHDX	tdH	Data Hold Time	0	—	—	ns
—	toES	Output Enable Setup Time	0	—	—	ns
—	toEH	Output Enable Hold Time	0	—	—	ns
		Read Toggle and \overline{Data} Polling	10	—	—	ns
tGHEL	tGHEL	Read Recover Time Before Write (\overline{OE} to \overline{CEf})	0	—	—	ns
tGHWL	tGHWL	Read Recover Time Before Write (\overline{OE} to \overline{WE})	0	—	—	ns
tWLEL	tWS	\overline{WE} Setup Time (\overline{CEf} to \overline{WE})	0	—	—	ns
tELWL	tCS	\overline{CEf} Setup Time (\overline{WE} to \overline{CEf})	0	—	—	ns
tEHWL	tWH	\overline{WE} Hold Time (\overline{CEf} to \overline{WE})	0	—	—	ns
tWHEH	tCH	\overline{CEf} Hold Time (\overline{WE} to \overline{CEf})	0	—	—	ns
tWLWH	tWP	Write Pulse Width	50	—	—	ns
tELEH	tCP	\overline{CEf} Pulse Width	50	—	—	ns
tWHWL	tWPH	Write Pulse Width High	30	—	—	ns
tEHEL	tCPH	\overline{CEf} Pulse Width High	30	—	—	ns
tWHWH1	tWHWH1	Byte Programming Operation	—	8	—	μ s
tWHWH2	tWHWH2	Sector Erase Operation (Note 1)	—	1	—	sec
			—	—	15	sec
—	tVCS	Vccf Setup Time	50	—	—	μ s
—	tVLHT	Voltage Transition Time (Note 2)	4	—	—	μ s
—	tVIDR	Rise Time to V _{ID} (Note 2)	500	—	—	ns
—	tRB	Recover Time from RY/BY	0	—	—	ns
—	tRP	RESET Pulse Width	500	—	—	ns
—	tRH	RESET Hold Time Before Read	200	—	—	ns
—	tEOE	Delay Time from Embedded Output Enable	—	—	100	ns
—	tBUSY	Program/Erase Valid to RY/BY Delay	—	—	90	ns

Note : 1. This does not include the preprogramming time.

2. This timing is for Sector Protection Operation.

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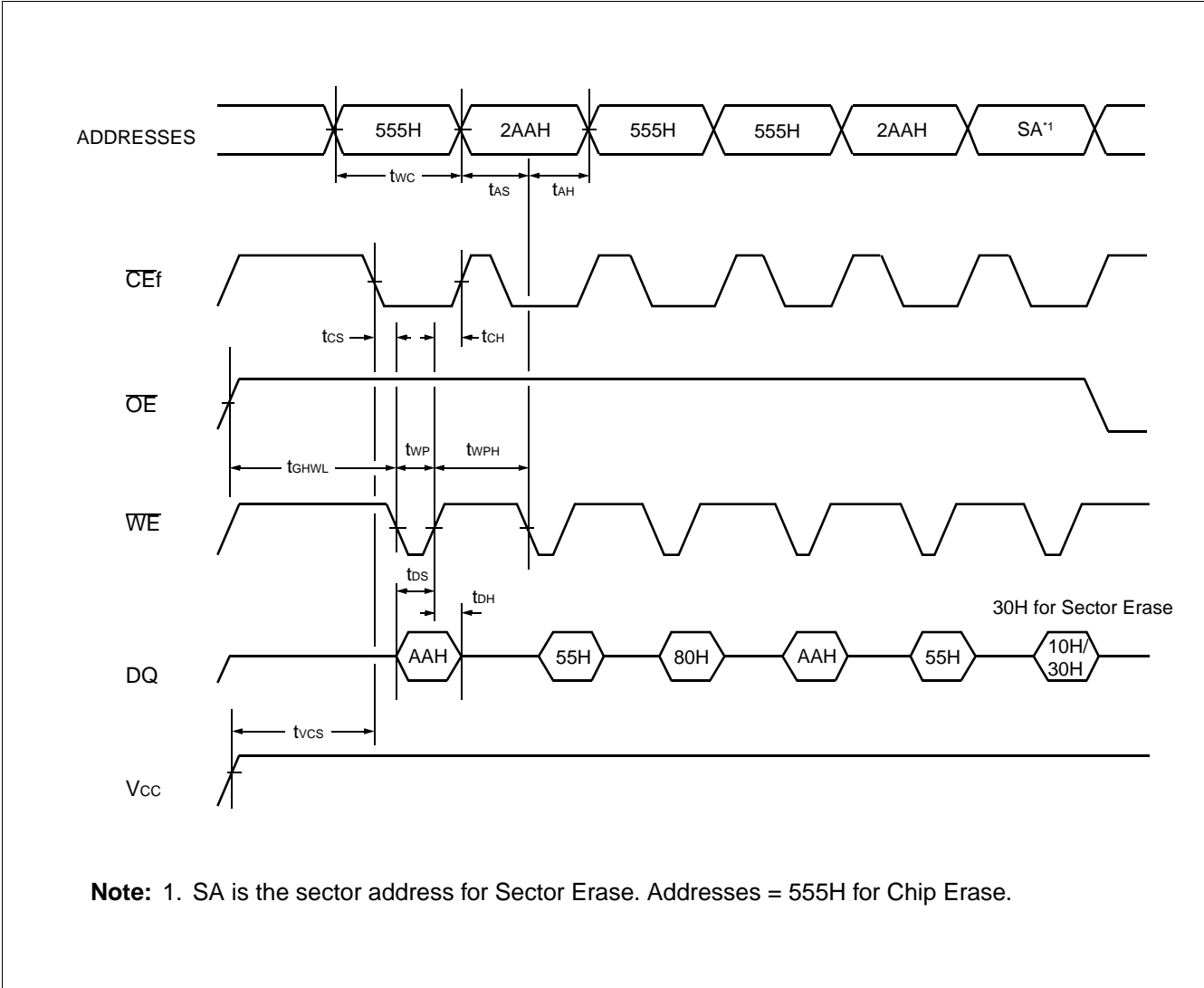
• Write Cycle (\overline{CEf} control) (Flash)



- Notes:**
1. PA is address of the memory location to be programmed.
 2. PD is data to be programmed at byte address.
 3. $\overline{DQ_7}$ is the output of the complement of the data written to the device.
 4. D_{OUT} is the output of the data written to the device.
 5. Figure indicates last two bus cycles out of four bus cycle sequence.

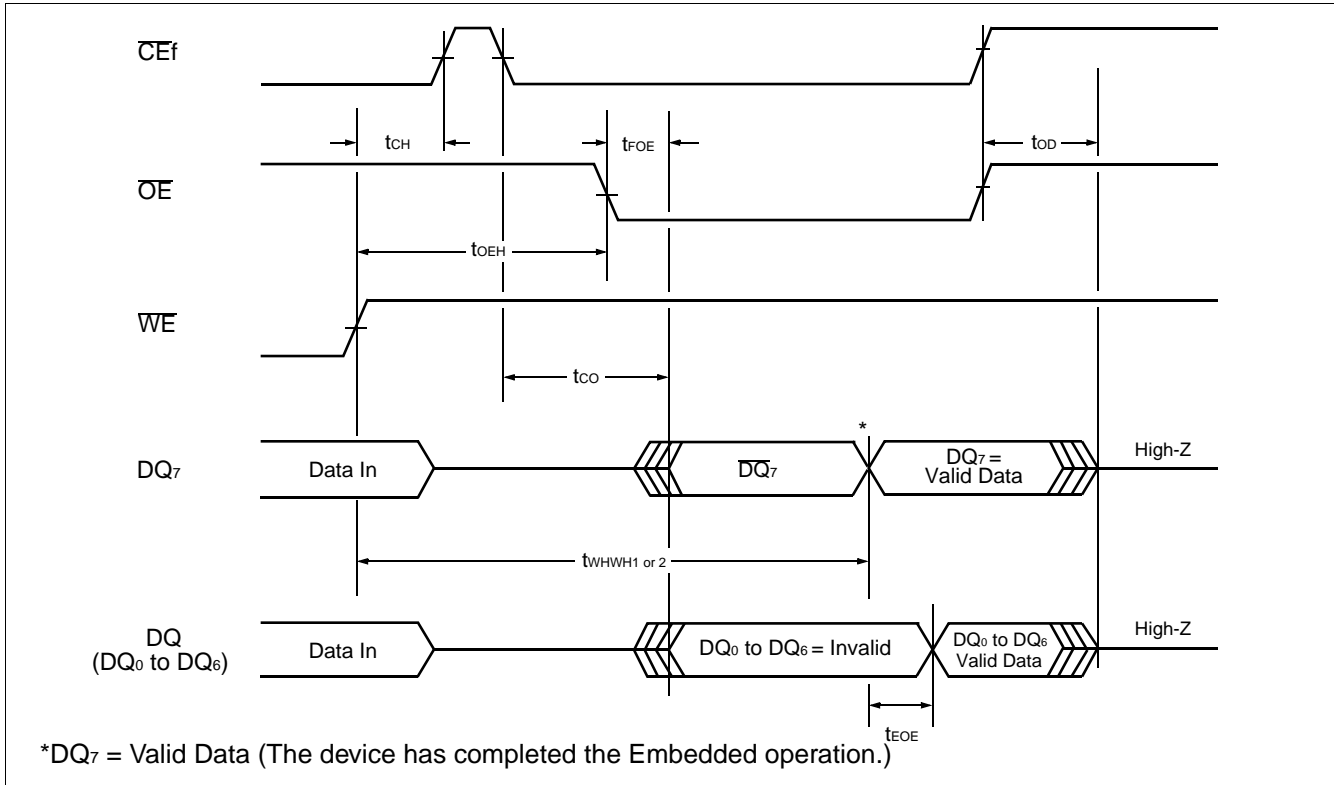
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• AC Waveforms Chip/Sector Erase Operations (Flash)

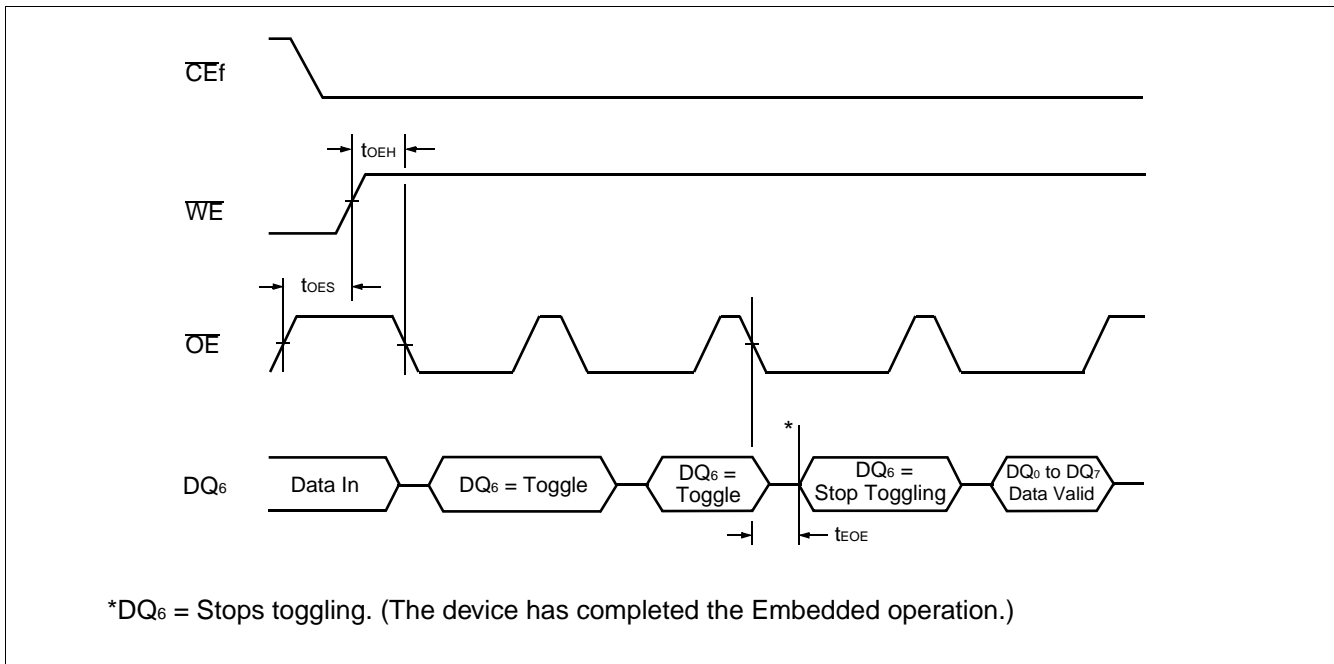


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• AC Waveforms for Data Polling during Embedded Algorithm Operations (Flash)

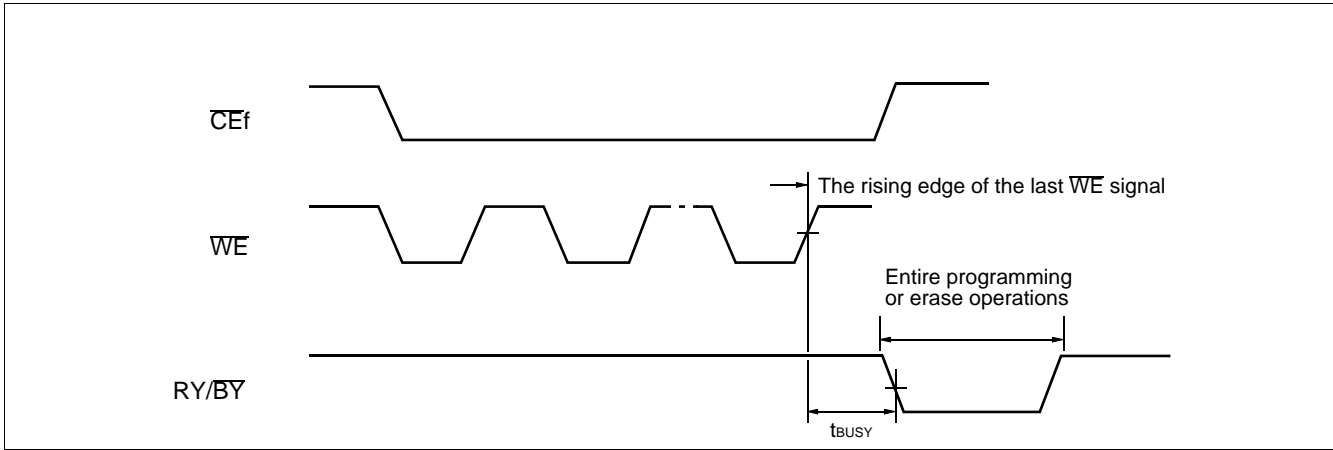


• AC Waveforms for Toggle Bit during Embedded Algorithm Operations (Flash)

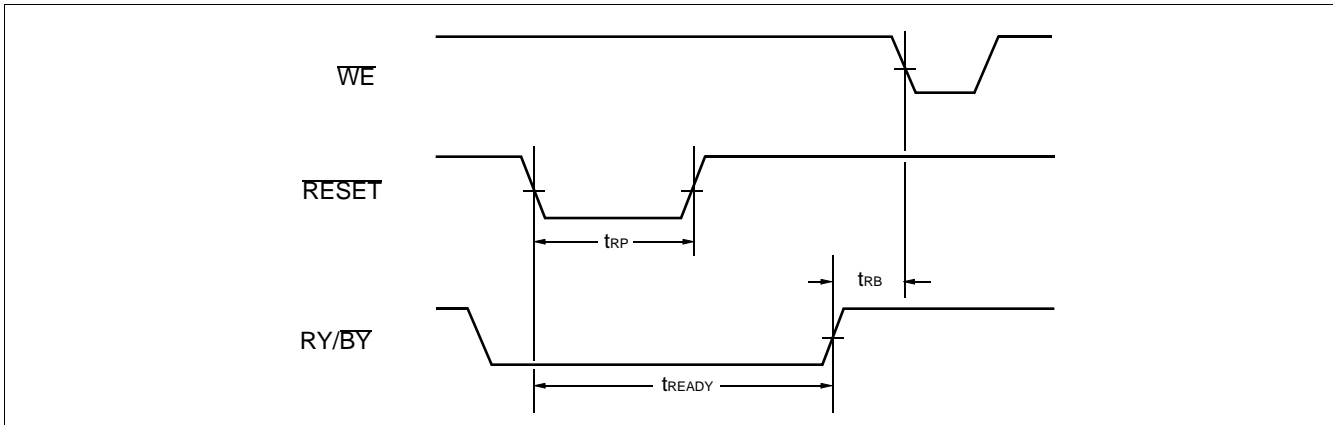


MB84VA2000-10/MB84VA2001-10

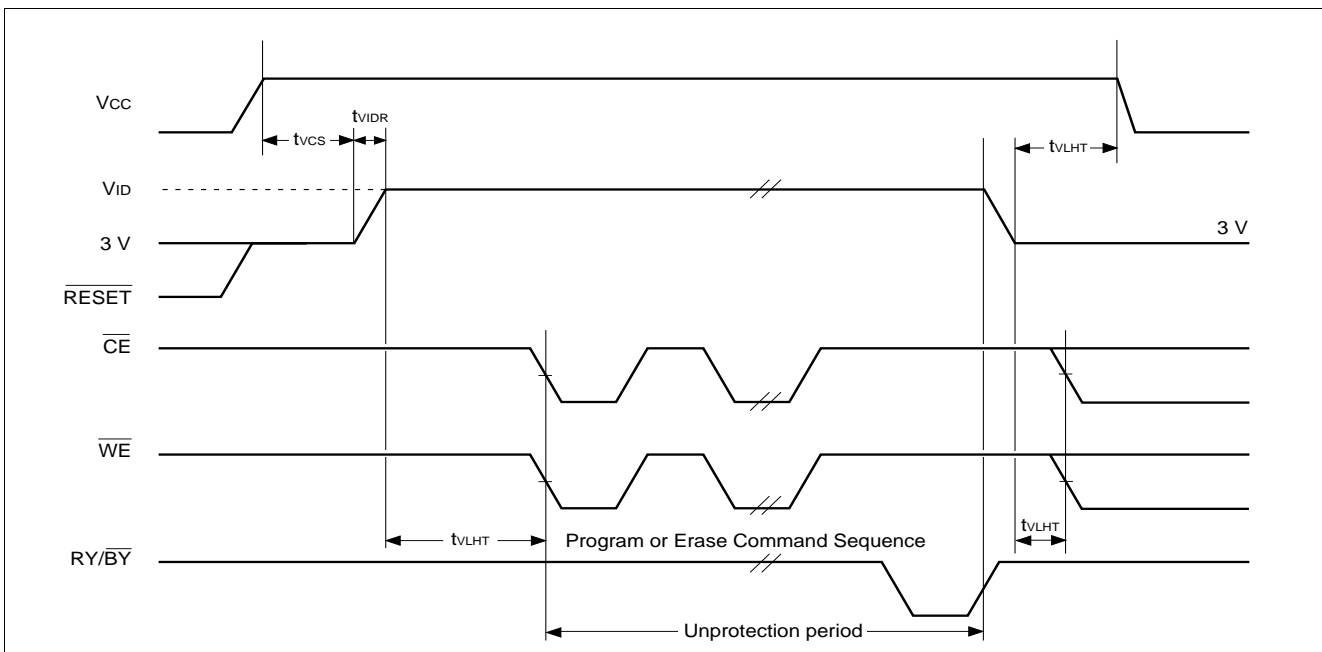
• RY/BY Timing Diagram during Write/Erase Operations (Flash)



• RESET, RY/BY Timing Diagram (Flash)

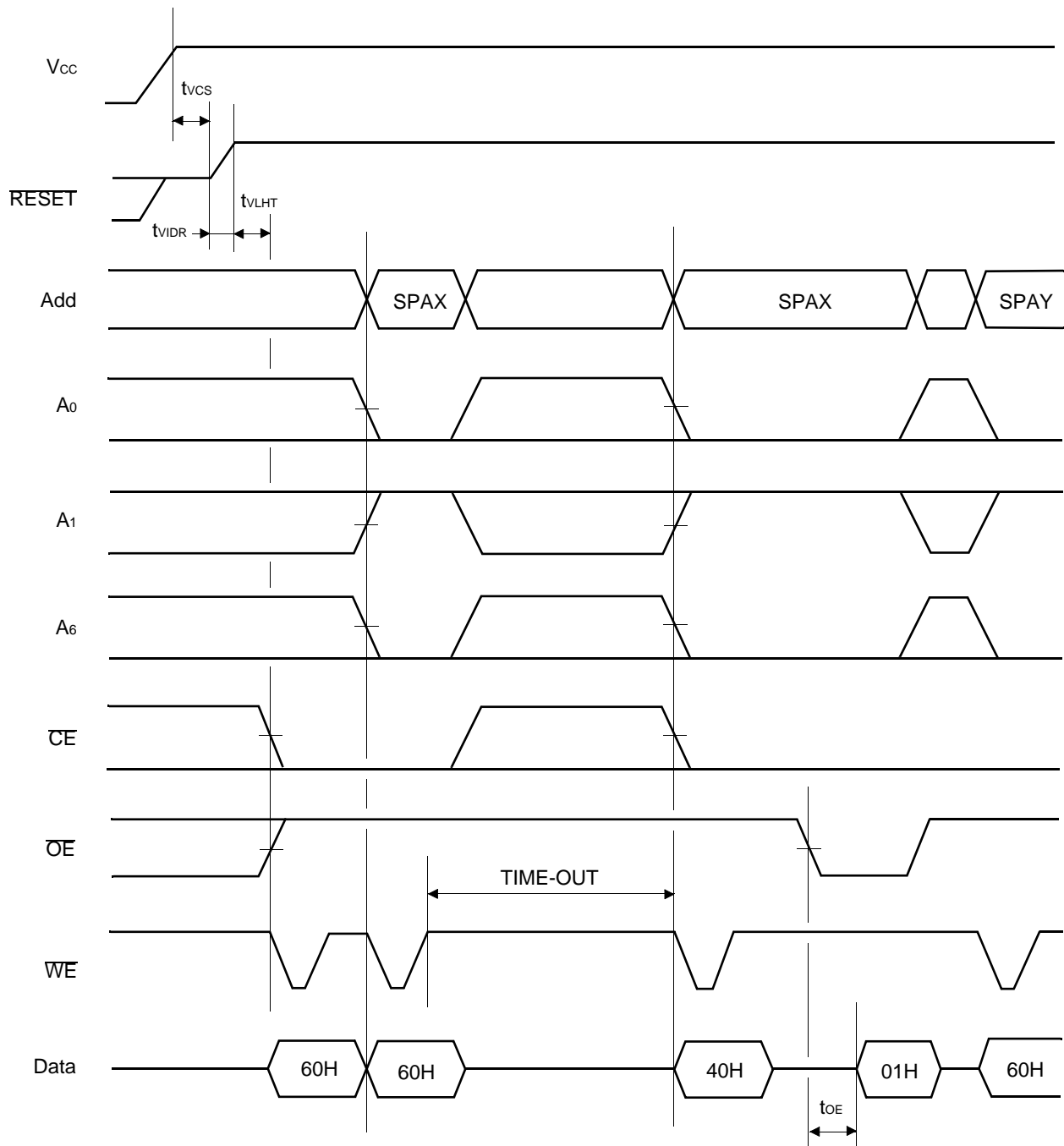


• Temporary Sector Unprotection (Flash)



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• Extended Sector Protection (Flash)



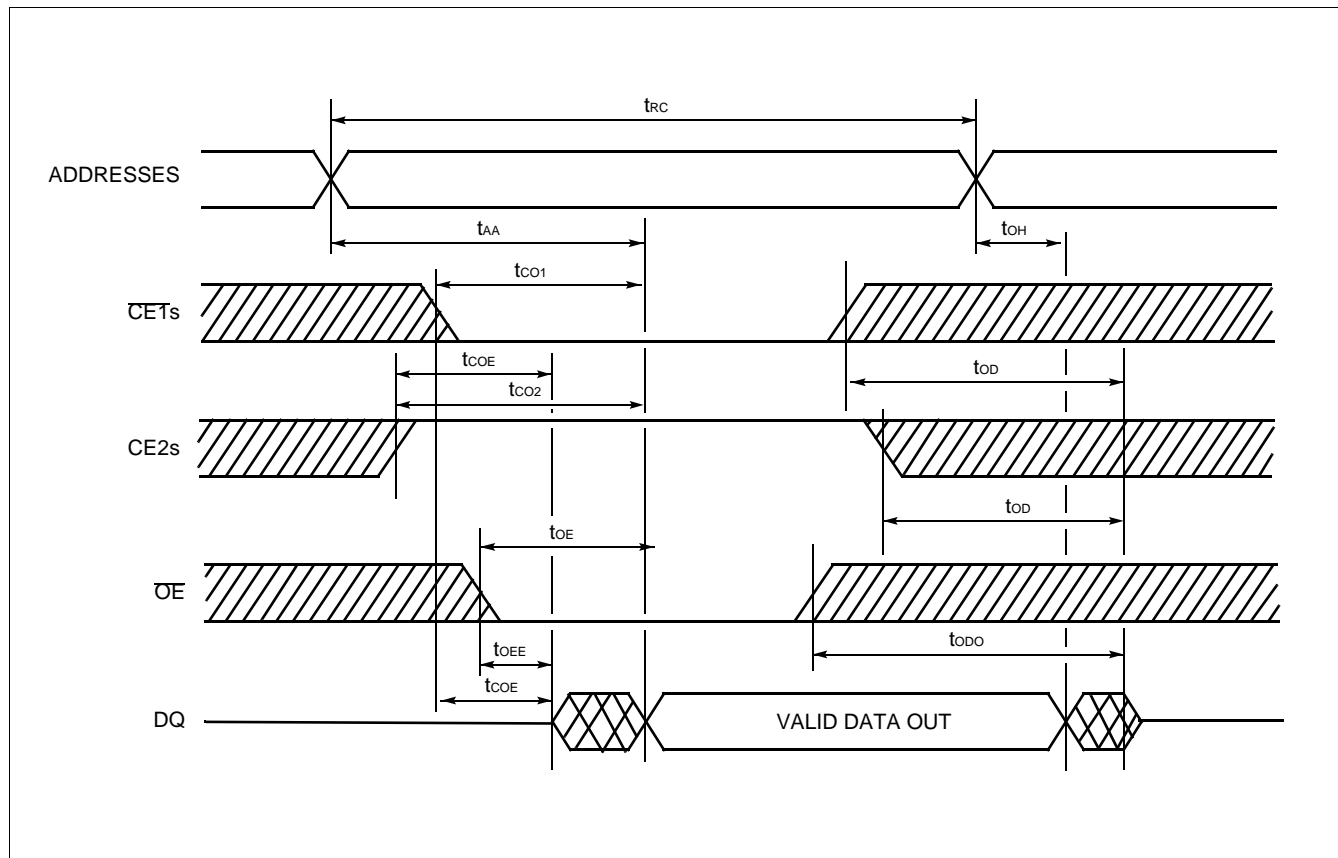
SPAX : Sector Address to be protected
 SPAY : Next Sector Address to be protected
 TIME-OUT : Time-Out window = 150 μ s (min)

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• Read Cycle (SRAM)

Parameter Symbol	Parameter Description	Min.	Max.	Unit
t_{RC}	Read Cycle Time	100	—	ns
t_{AA}	Address Access Time	—	100	ns
t_{CO1}	Chip Enable ($\overline{CE1}$ s) Access Time	—	100	ns
t_{CO2}	Chip Enable (CE2s) Access Time	—	100	ns
t_{OE}	Output Enable Access Time	—	50	ns
t_{COE}	Chip Enable ($\overline{CE1}$ s Low and CE2s High) to Output Active	5	—	ns
t_{OEE}	Output Enable Low to Output Active	0	—	ns
t_{OD}	Chip Enable ($\overline{CE1}$ s High or CE2s Low) to Output High-Z	—	40	ns
t_{ODO}	Output Enable High to Output High-Z	—	40	ns
t_{OH}	Output Data Hold Time	10	—	ns

• Read Cycle (Note 1) (SRAM)



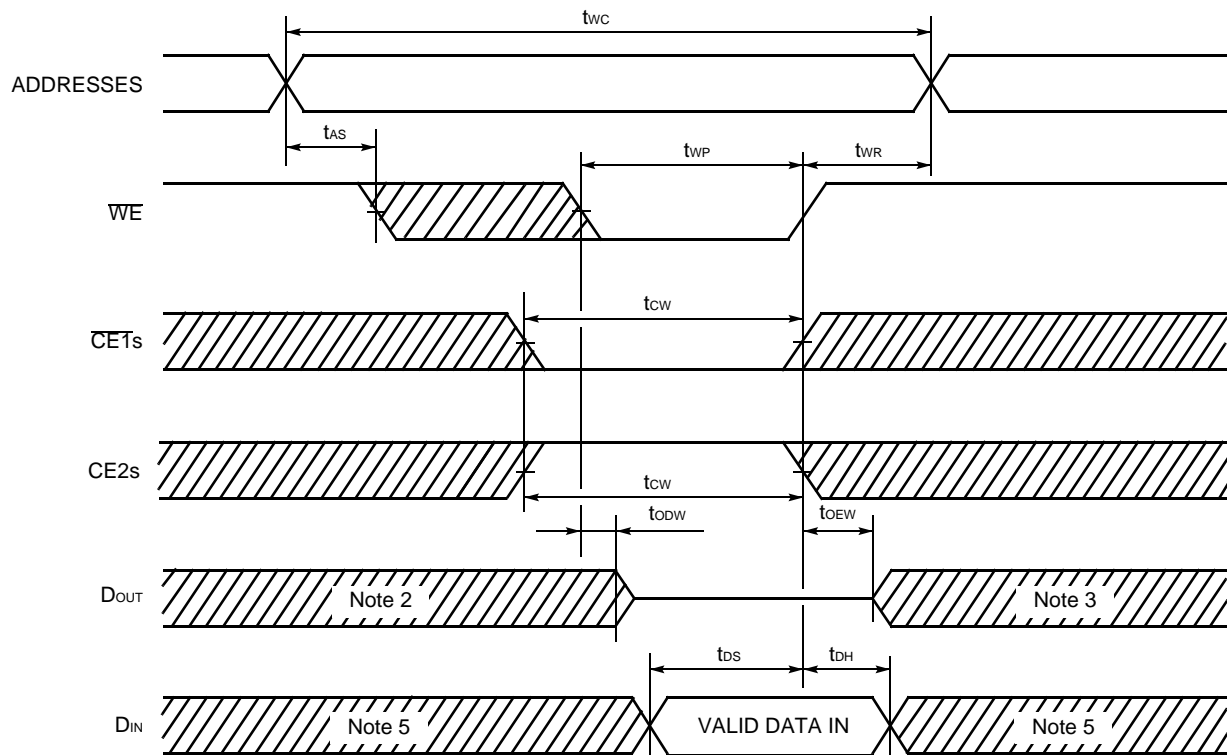
Note: 1. \overline{WE} remains HIGH for the read cycle.

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• Write Cycle (SRAM)

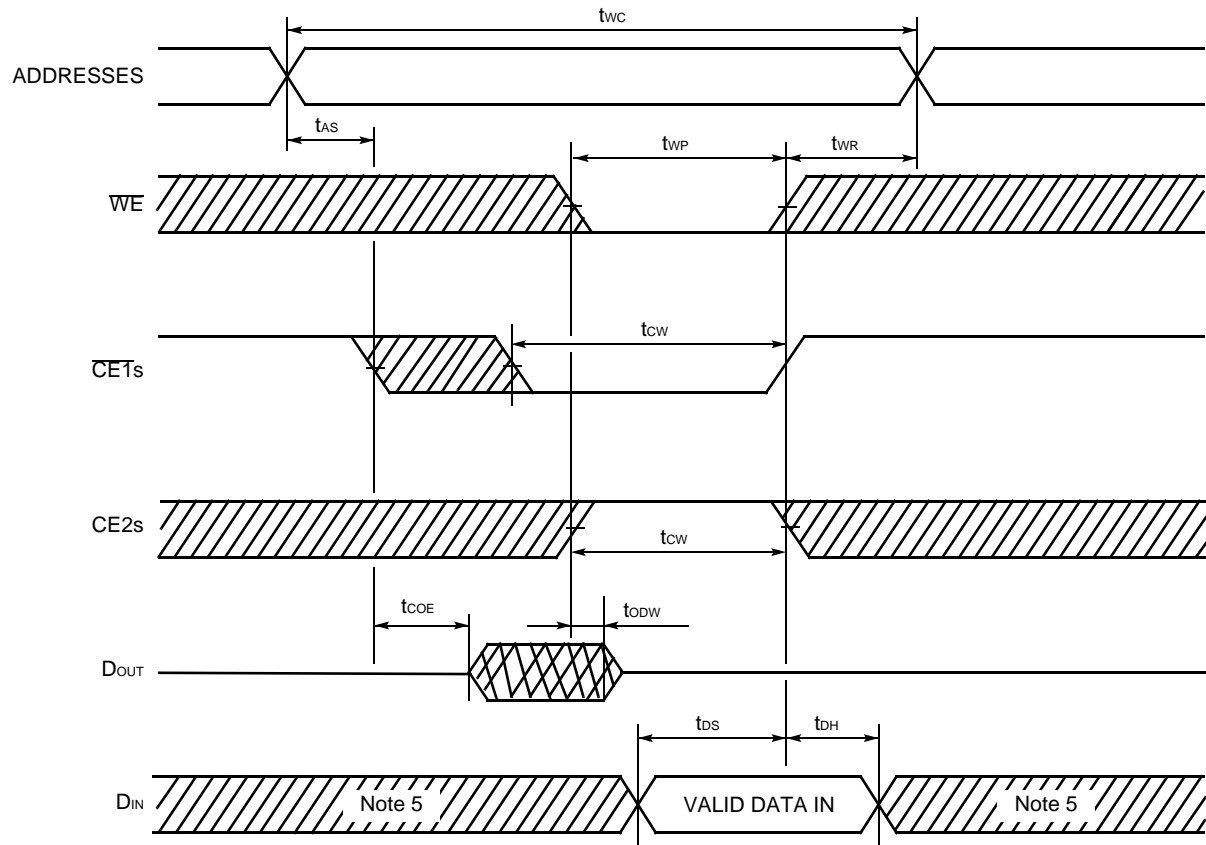
Parameter Symbol	Parameter Description	Min.	Max.	Unit
t_{WC}	Write Cycle Time	100	—	ns
t_{WP}	Write Pulse Width	60	—	ns
t_{CW}	Chip Enable to End of Write	80	—	ns
t_{AS}	Address Setup Time	0	—	ns
t_{WR}	Write Recovery Time	0	—	ns
t_{ODW}	WE Low to Output High-Z	—	40	ns
t_{OEW}	WE High to Output Active	0	—	ns
t_{DS}	Data Setup Time	40	—	ns
t_{DH}	Data Hold Time	0	—	ns

• Write Cycle (Note 4) (WE control) (SRAM)



- Notes:**
2. If $\overline{CE1s}$ goes LOW (or $\overline{CE2s}$ goes HIGH) coincident with or after \overline{WE} goes LOW, the output will remain at high impedance.
 3. If $\overline{CE1s}$ goes HIGH (or $\overline{CE2s}$ goes LOW) coincident with or before \overline{WE} goes HIGH, the output will remain at high impedance.
 4. If \overline{OE} is HIGH during the write cycle, the outputs will remain at high impedance.
 5. Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

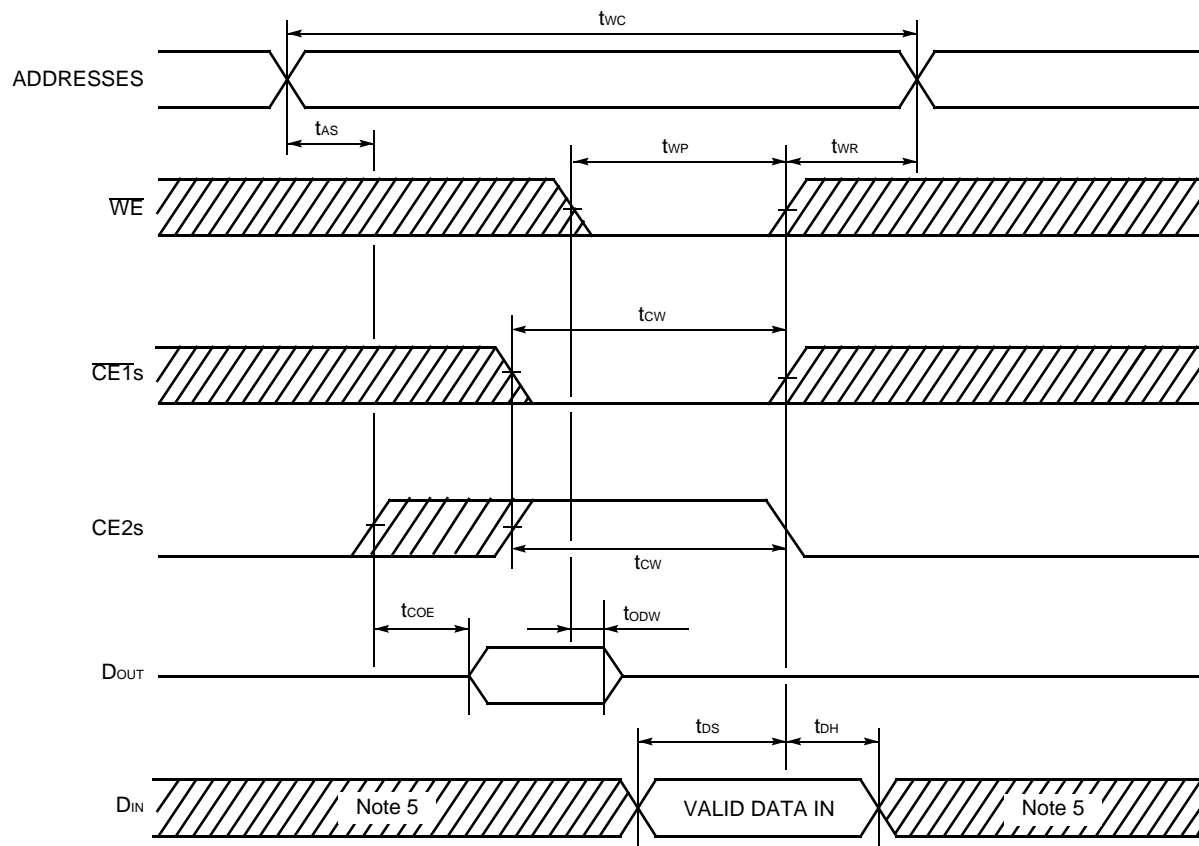
MB84VA2000-10/MB84VA2001-10

• Write Cycle (Note 4) ($\overline{CE1s}$ control) (SRAM)

- Notes:**
2. If $\overline{CE1s}$ goes LOW (or CE2s goes HIGH) coincident with or after \overline{WE} goes LOW, the output will remain at high impedance.
 3. If $\overline{CE1s}$ goes HIGH (or CE2s goes LOW) coincident with or before \overline{WE} goes HIGH, the output will remain at high impedance.
 4. If \overline{OE} is HIGH during the write cycle, the outputs will remain at high impedance.
 5. Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

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• Write Cycle (Note 4) (CE2s Control) (SRAM)



- Notes:**
2. If $\overline{CE1s}$ goes LOW (or $\overline{CE2s}$ goes HIGH) coincident with or after \overline{WE} goes LOW, the output will remain at high impedance.
 3. If $\overline{CE1s}$ goes HIGH (or $\overline{CE2s}$ goes LOW) coincident with or before \overline{WE} goes HIGH, the output will remain at high impedance.
 4. If \overline{OE} is HIGH during the write cycle, the outputs will remain at high impedance.
 5. Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

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■ ERASE AND PROGRAMMING PERFORMANCE (Flash)

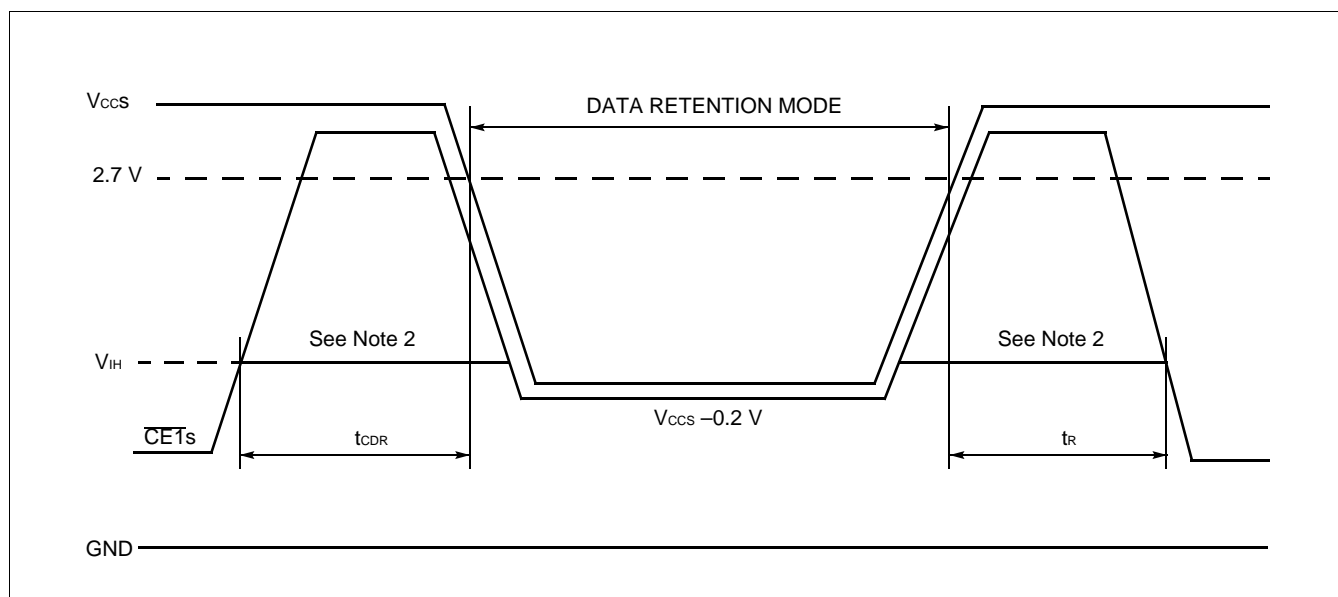
Parameter	Limits			Unit	Comment
	Min.	Typ.	Max.		
Sector Erase Time	—	1	15	sec	Excludes programming time prior to erasure
Byte Programming Time	—	8	3,600	μs	Excludes system-level overhead
Chip Programming Time	—	12	50	sec	Excludes system-level overhead
Erase/Program Cycle	100,000	—	—	cycles	

■ DATA RETENTION CHARACTERISTICS (SRAM)

Parameter Symbol	Parameter Description	Min.	Typ.	Max.	Unit
V_{DH}	Data Retention Supply Voltage	2.0	—	3.6	V
I_{DDs2}	Standby Current	$V_{DH} = 3.0\text{ V}$	—	50*	μA
		$V_{DH} = 3.6\text{ V}$	—	60	μA
t_{CDR}	Chip Deselect to Data Retention Mode Time	0	—	—	ns
t_R	Recovery Time	5	—	—	ms

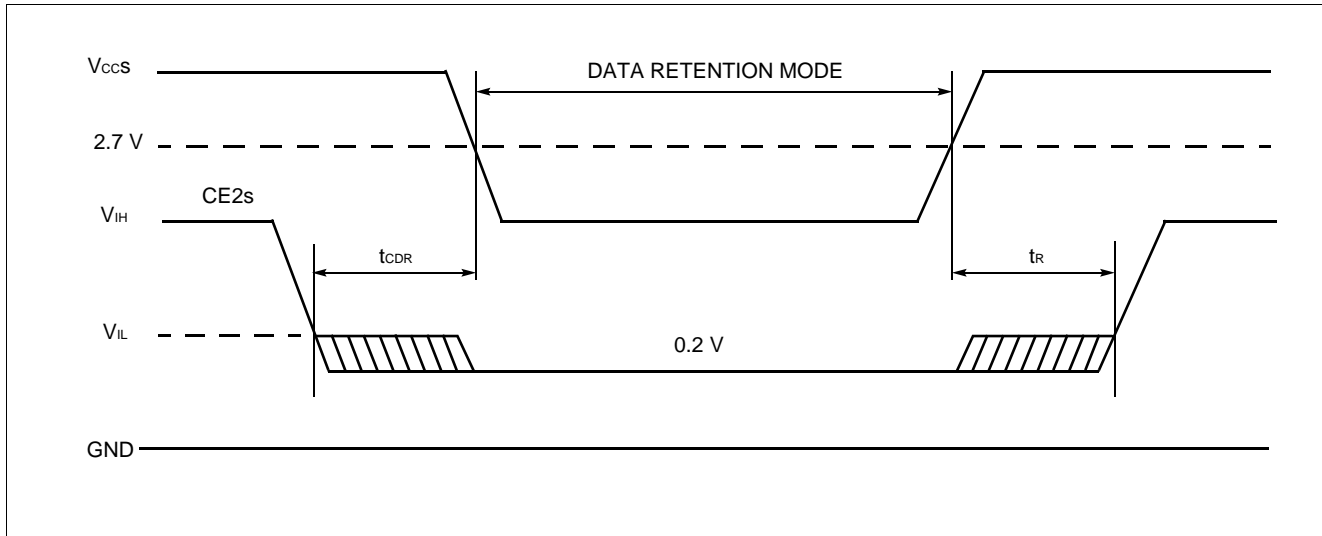
* : 5 μA (Max.) at $T_A = -20^\circ\text{C}$ to $+40^\circ\text{C}$

• $\overline{\text{CE}}\text{T}s$ Controlled Data Retention Mode (Note 1)



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• CE2s Controlled Data Retention Mode (Note 3)



- Notes:**
1. In $\overline{CE1}$ s controlled data retention mode, input level of CE2s should be fixed V_{ccs} to $V_{ccs}-0.2V$ or V_{ss} to $0.2V$ during data retention mode. Other input and input/output pins can be used between $-0.3V$ to $V_{ccs}+0.3V$.
 2. When $\overline{CE1}$ s is operating at the V_{IH} min. level ($2.2V$), the standby current is given by I_{SB1S} during the transition of V_{CCS} from 3.6 to $2.2V$.
 3. In CE2s controlled data retention mode, input and input/output pins can be used between $-0.3V$ to $V_{ccs}+0.3V$.

■ PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	T.B.D	T.B.D	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	T.B.D	T.B.D	pF
C_{IN2}	Control Pin Capacitance	$V_{IN} = 0$	T.B.D	T.B.D	pF

Note: Test conditions $T_A = 25^\circ C$, $f = 1.0$ MHz

■ HANDRING OF PACKAGE

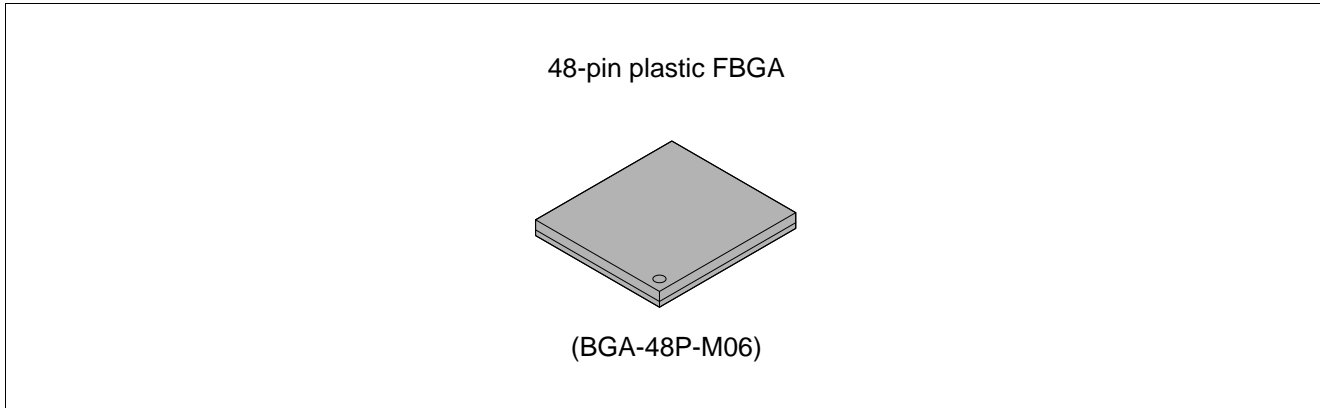
Please handle this package carefully since the sides of packages are right angle.

■ CAUTION

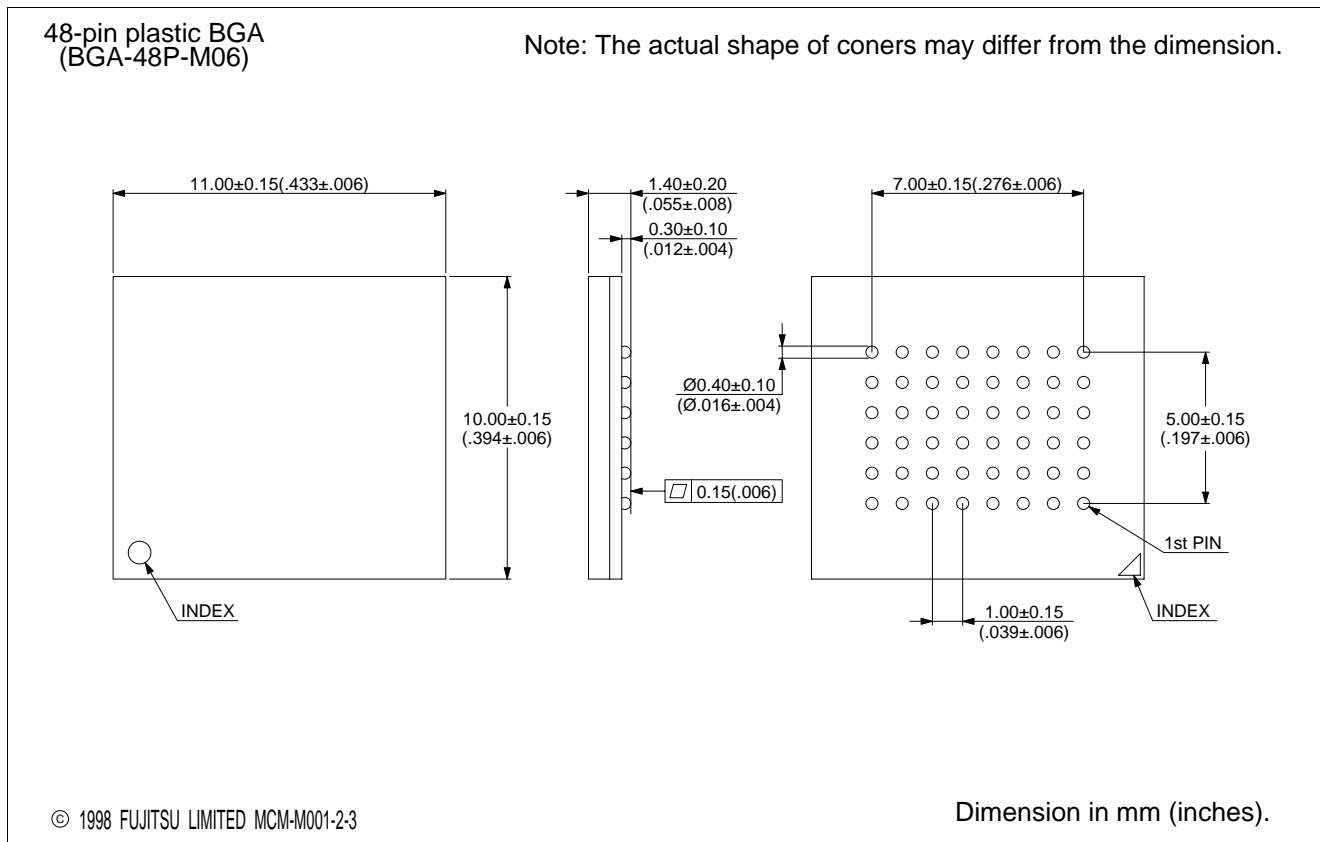
- 1.) The high voltage (VID) can not apply to address pins and control pins except **RESET**. Therefore, it can not use autoselect and sector protect function by applying the high voltage (VID) to specific pins.
- 2.) For the sector protection, since the high voltage (VID) can be applied to the **RESET**, it can be protected the sector using "Extended sector protect" command.

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■ PACKAGE



■ PACKAGE DIMENSIONS



MB84VA2000-10/MB84VA2001-10

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