Ordering number : EN5651B

Bi-CMOS IC

LV2700V

Spread Spectrum Communications IC

Overview

The LV2700V provides the reception and transmission functions necessary for half-duplex communication in spread-spectrum communications systems.

Features

- Can be used in weak radio wave band without frequency conversion (direct signal processing at 236 MHz)
- Can also be used in the ISM band (900MHz, 2.4GHz) with frequency conversion
- Wide spread-spectrum bandwidth (20 MHz)
- Sanyo developed system for PN code synchronization
- Allows direct primary modulation (FSK and FM) by data and analog signals.
- Data transfer at a maximum rate of 256kbps can be made (when the built-in LPF is used)
- Low-voltage operation (2.7 to 5.5 V)
- Low power dissipation (36 mW in RX mode)
- Small package: SSOP30

Functions

[TX Block]

- Spectrum spreader
- Crystal oscillator circuit
- PN code generator (M sequence)
- M sequence code length (511, 255, 127, 63, 31, or 15 chips)
- 9.83 MHz PLL
- Band limiting filter (LPF) for data transmission

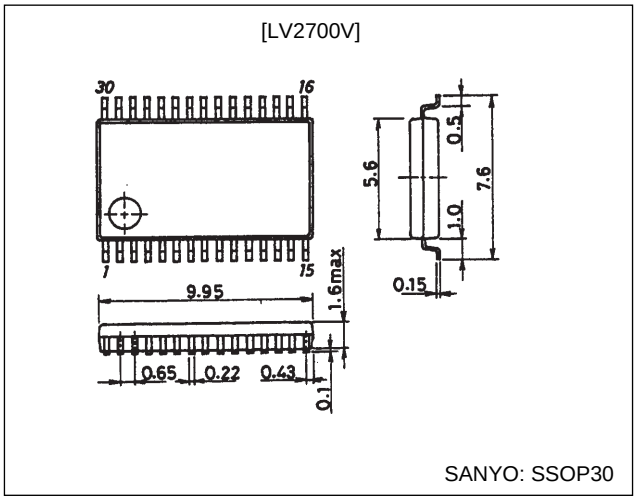
[RX Block]

- Spectrum despreader
- Synchronization supplementation and protection
- 236 MHz PLL
- PN code generator (M sequence)
- M sequence code length (511, 255, 127, 63, 31, or 15 chips)
- FM demodulation
- Lock detector
- 150k LPF through SW

Package Dimensions

unit: mm

4182-SSOP30



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TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		6	V
Allowable power dissipation	Pd max		150	mW
Operating temperature	Topr		–20 to +75	°C
Storage temperature	Tstg		–40 to +125	°C

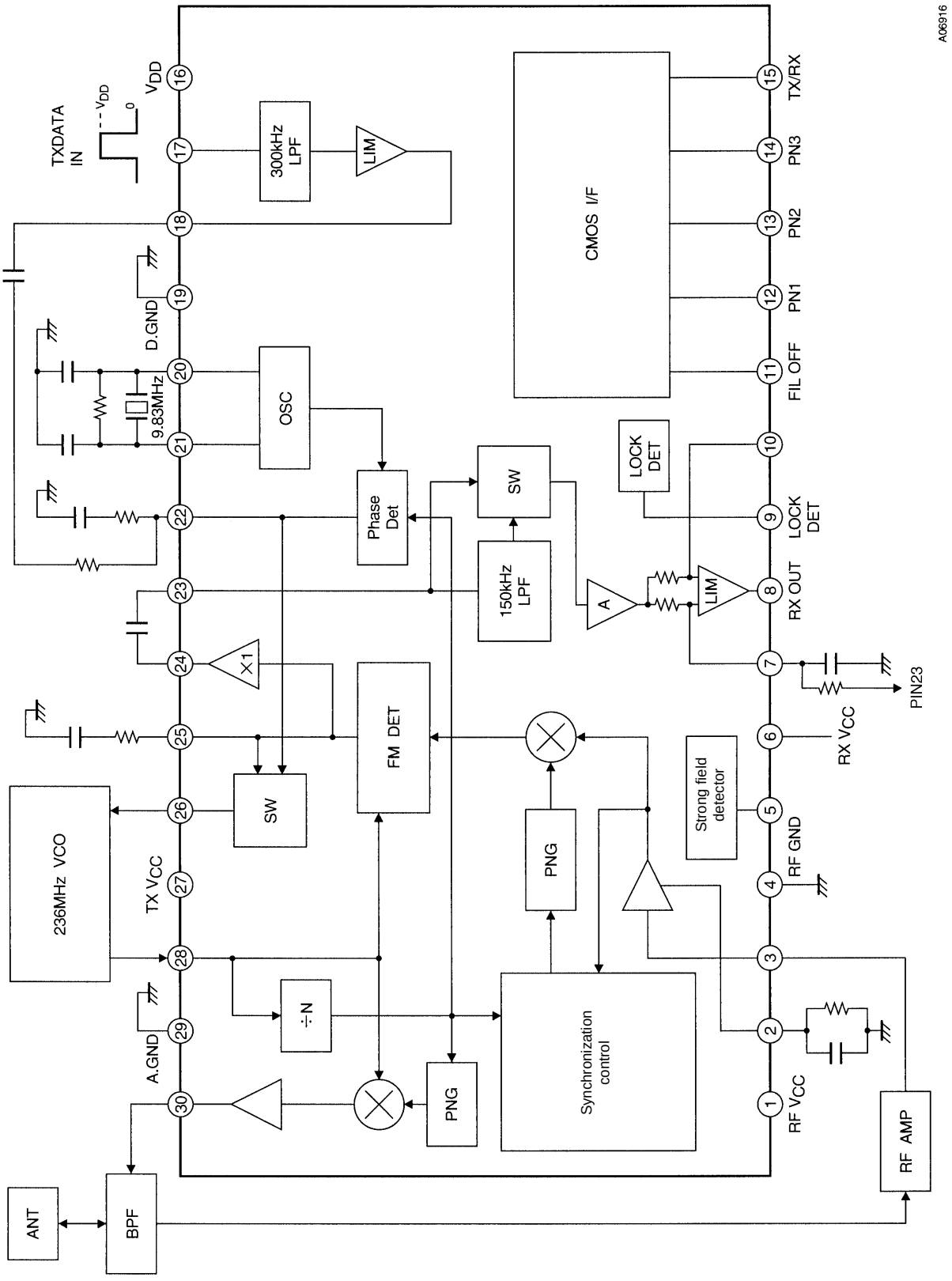
Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		3	V
Allowable voltage range	V_{CC}op		2.7 to 5.5	V
Operating frequency range	Fin		200 to 280	MHz

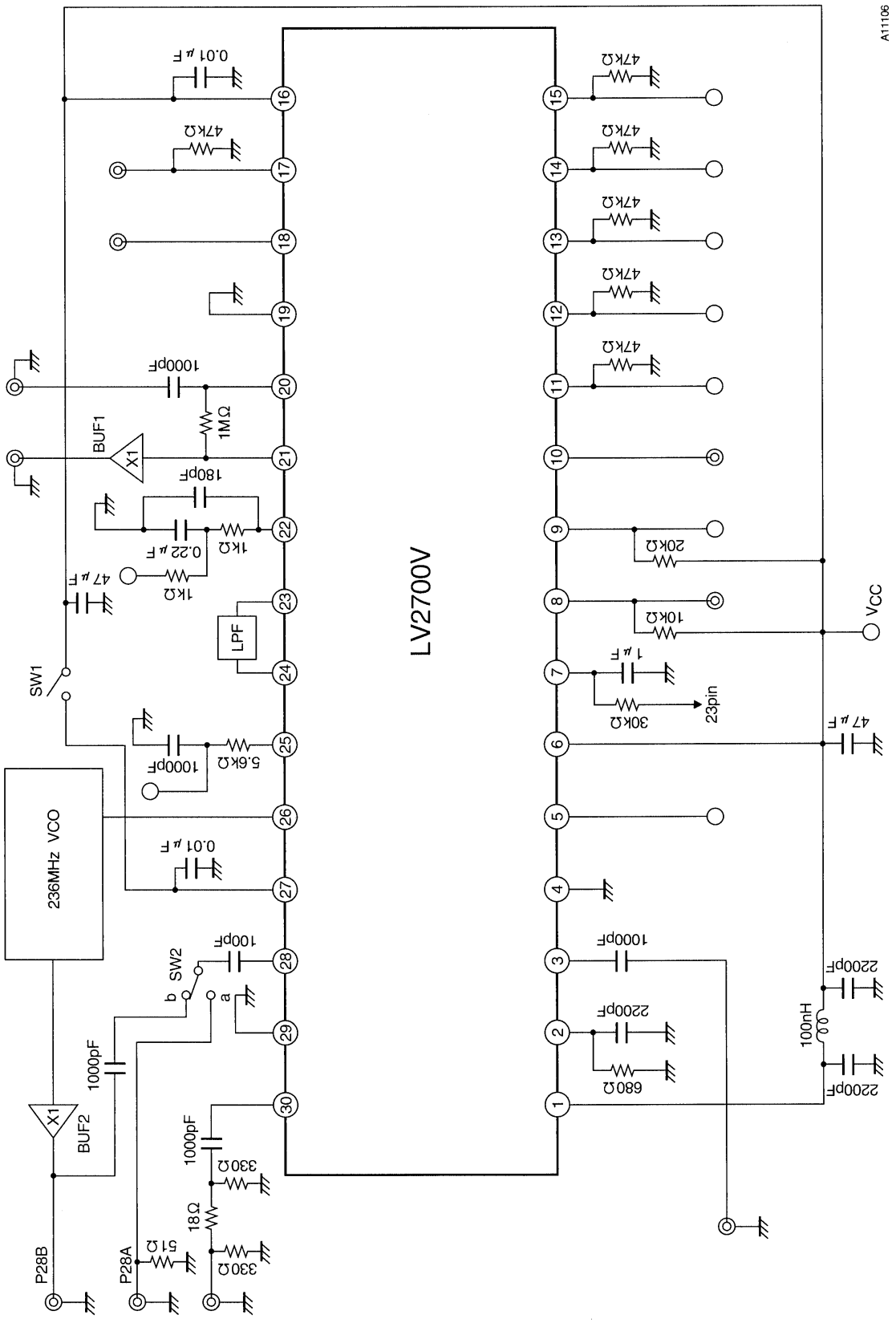
Electrical Characteristics at Ta = 25°C, V_{CC} = 3 V, fc = 236 MHz, fm = 10 kHz, Vm = 0.2 Vp-p

Parameter		Symbol	Conditions	Ratings			Unit
				min	typ	max	
Quiescent current		I_{CCO}TX	TXV_{CC} + V_{DD}		8	11	mA
		I_{CCO}RX	RFV_{CC} + RXV_{CC} + V_{DD}		12	16	mA
[TX Block]							
Modulated signal voltage		V_OTX	Applied to Pin 22 via a 20kΩ resistor		0.2	2	Vp-p
RF output voltage		V_OTX	SW2: a, V28 = 236 MHz, –10 dBm	–38	–35	–32	dBm
Spread bandwidth		WS	SW2: a, V28 = 236 MHz, –10 dBm		19.7		MHz
[RX Block]							
Input sensitivity		V_SRX	THD = 5% in the output at Pin 10		–80	–75	dBm
Demodulated output 1	High level	V_ORX1H	Pin 9 output	2.5			V
	Low level	V_ORX1L				0.4	V
Demodulated output 2		V_ORX2	Pin 10 output	240	300		mVrms
Total harmonic distortion		THD RX	Pin 10 output		0.5	2	%
Signal-to-noise ratio		S/N	Pin 10 output, IHF filter	45	55		dB
[CMOS-Level Interface]							
Input high-level voltage		V_IH	Pins 11 to 15, 17	2.1			V
Input low-level voltage		V_IL	Pins 11 to 15, 17			0.6	V
Output high-level voltage		V_OH	Pins 8, 9	2.5			V
Output low-level voltage		V_OL	Pins 8, 9			0.4	V
Input high-level current		I_IH	Pins 11 to 15, 17			5	µA
Input low-level current		IIL	Pins 11 to 15, 17			5	µA
Input amplitude		V_{IN}	VCOIN	–16			dBm
Crystal oscillator frequency conditions		X_{OSC}	XIN, XOUT	5		13	MHz
Input capacitance		C_{IN}	RFIN, XIN, VCOIN		2.5		pF

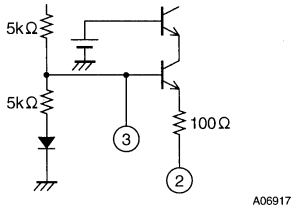
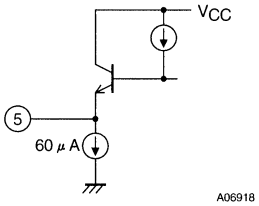
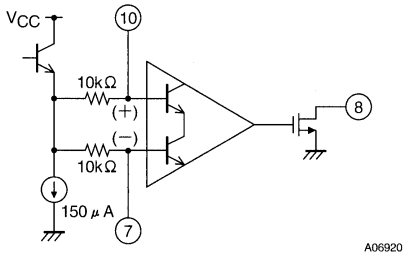
Block Diagram



AC Test Circuit



Pin Functions

Pin No.	Pin	Pin voltage(V)	Pin function	Equivalent circuit
1	RFV_{CC}		RF block power supply	
2	REXT	0.2	Connection for the external capacitor and resistor used by the internal RF amplifier	
3	RFIN	1	RF input	
4	RFGND		RF block ground	
5	ANTDUMP	1.2	Output for the DC voltage used under strong reception conditions to prevent saturation of the RF amplifier. Voltage variability range: about 0.5 V	
6	RXV_{CC}		Reception block power supply	
7	CEXT		Connect a capacitor between the limiter reference terminal for demodulated data waveshaping and the GND terminal.	
8	RXOUT		Demodulated data output (CMOS output.)	
9	LOCK DET		Outputs a high level when PN code synchronization is established. (This is a CMOS-level output.)	
10	RXAOUT		Demodulated analog output	

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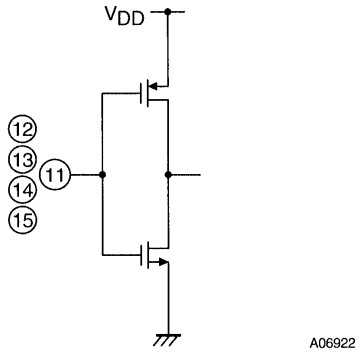
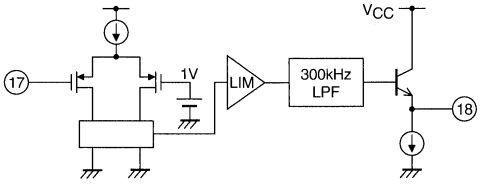
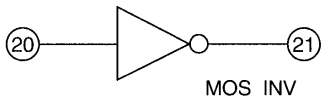
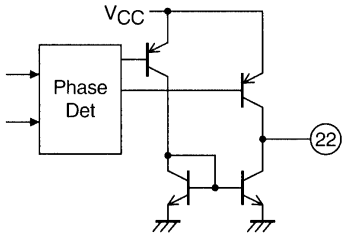
<table>
<tr><th>Pin No.</th><th>Pin</th><th>Pin voltage(V)</th><th>Pin function</th><th>Equivalent circuit</th></tr>
<tr><td>11</td><td>FILOFF</td><td></td><td>Through SW selection of 150kHz LPF. The through SW becomes ON when this input is HIGH, but is normally OFF (Low).</td><td rowspan="5"> 

A06922</td></tr>
<tr><td>12</td><td>PN1</td><td></td><td rowspan="3">PN code selection

These pins select one of six code-length types.

<table>
<tr><th>PN1</th><th>PN2</th><th>PN3</th><th>PN code length</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>15</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>15</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>31</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>63</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>127</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>255</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>511</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>PN reset</td></tr>
</table>
0 = Low 1 = High</td></tr>
<tr><td>13</td><td>PN2</td><td></td></tr>
<tr><td>14</td><td>PN3</td><td></td></tr>
<tr><td>15</td><td>TX/RX</td><td></td><td>Send/receive mode selection.
High: Transmission
Low: Reception</td></tr>
<tr><td>16</td><td>V_{DD}</td><td></td><td>CMOS block power supply</td><td></td></tr>
<tr><td>17</td><td>TX DATAIN</td><td></td><td>Transmission data input (CMOS levels). Do not apply analog signals to this pin.</td><td rowspan="2"> 

A06923</td></tr>
<tr><td>18</td><td>TX DATAOUT</td><td> 
</td><td>Transmission data output. The output signal is band limited to 300kHz and voltage limited to 1 Vp-p.</td></tr>
<tr><td>19</td><td>DGND</td><td></td><td>CMOS block ground</td><td></td></tr>
<tr><td>20</td><td>XIN</td><td>1/2V_{CC}</td><td>Input for the 9.8304MHz reference oscillator inverter.</td><td rowspan="2"> 

A06924</td></tr>
<tr><td>21</td><td>XOUT</td><td>1/2V_{CC}</td><td>Output for the 9.8304MHz reference oscillator inverter.
Add a resistor of about 1MΩ between XIN and XOUT.</td></tr>
<tr><td>22</td><td>TXLPF</td><td>1.5</td><td>Connection for the 9.8MHz PLL loop filter used in transmission.</td><td> 

A06925</td></tr>
</table>

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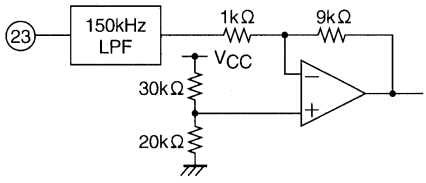
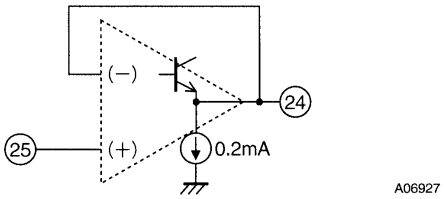
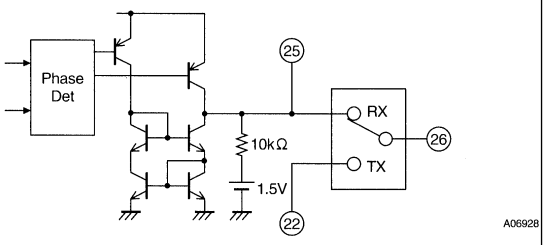
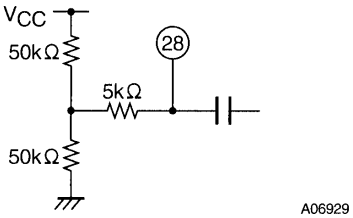
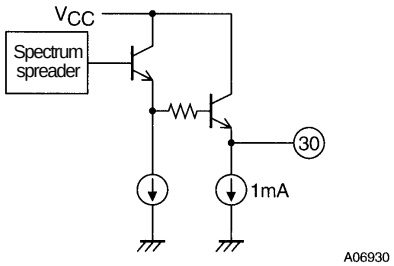
Pin No.	Pin	Pin voltage(V)	Pin function	Equivalent circuit
23	LPFIN	V7	Demodulated signal input (loop filter output) used in reception. Connect an external bias resistor.	
24	RXPDOUT	V25	Pin 25 buffer output. Connect an external low-pass filter between pins 23 and 24 if required.	
25	RXLPF	1.5	Connection for the 236MHz PLL loop filter used in reception.	
26	LPFOUT	1.5	Control input for the 236MHz VCO. The LV2700V includes a switch for selecting the loop filter depending on the mode (transmission or reception).	
27	TX V_{CC}		Transmission power supply	
28	VCOIN	1/2 V_{CC}	Input for the output from the 236MHz VCO. Minimum input level: about –20 dBm	
29	AGND		Analog system ground	
30	TX RFOUT	1.3	Spread-spectrum RF output (in transmission mode)	

Description of Operation and Application Information

1. Principle of Operation
   The LV2700V has all the transmission and reception functions necessary for carrying out half-duplex communication using spread spectrum communication. The spectrum spreading is being done using the direct sequence (DS) method in which the carrier wave is multiplied by the PN code. The PN code used for spectrum spreading at this time is the typical M sequence code, and it is possible to select six types of code lengths from 15 chips to 511 chips. Further, since the clock for generating the PN code is derived from the carrier wave by frequency division, a system is realized in which the carrier wave and the PN code are synchronized in phase thereby obtaining a configuration with simplified PN synchronization system.

2. Transmission Mode
   The transmission block is shown in Fig. 1.

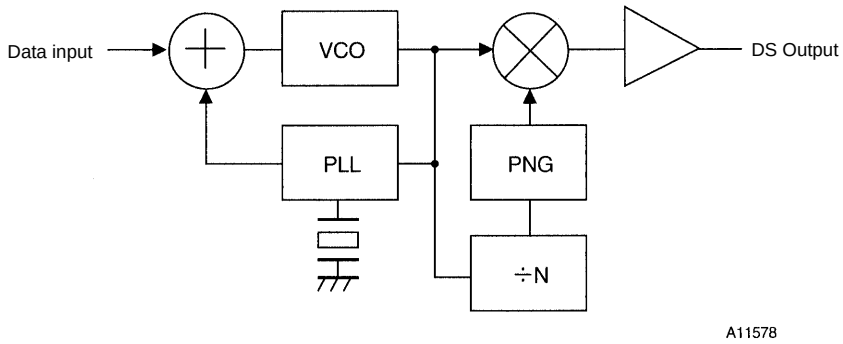


Fig. 1 The transmission block

• PN Code generation method
The PN (Pseudo-random Noise) code is, as its name suggests, a pulse train in which the occurrence probabilities of 1's and 0's are pseudo-random in nature, and is required for spectrum spreading in the direct spreading method. Although there are many types of PN code series, the most typical among them, the M sequence PN code (maximum-length sequence) is being used in the LV2700V. The generator of the M sequence PN code is configured using a shift register and feedback circuit. Fig. 2 shows the configuration of a PN code generator of the 15-chip type. In the LV2700V, it is possible to select among six types of PN codes from 15 chips to 511 chips. Although there are several shift register feedback methods (called feedback taps) in the case of M sequence of code length more than 15 chips, in the LV2700V, only one type of feedback tap is used for each code length. The actual positions of the feedback taps are shown in Table 1.

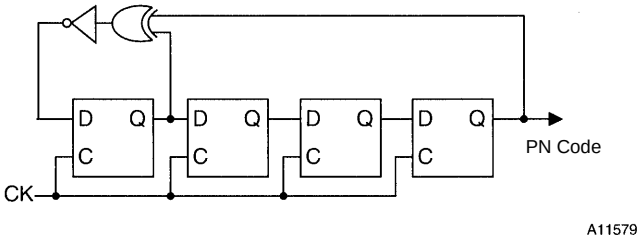


Fig. 2 PN Code generator

Table 1 Feedback tap position

PN Code length	Tap position
15	(1, 4)
31	(2, 5)
63	(1, 6)
127	(1, 7)
255	(2, 3, 4, 8)
511	(4, 9)

- Modulation method (FM, FSK)
  The modulation method using the information signal is that of direct frequency modulation (FM) of the VCO. Specifically, frequency modulation is carried out by adding the signal to the loop filter of the PLL. This is the same in the case of analog signals and digital data. Consequently, the lower limit frequency in frequency modulation gets limited by the loop band width of the PLL. That is, the lower limit frequency becomes lower as the loop bandwidth of PLL becomes narrower. In the case of FSK by data, although it is necessary to make the lower limit frequency lower than that in the case of FM using analog signals, it is possible to sufficiently lower the lower limit frequency by adding a circuit that modulates the reference oscillator frequency.

3. Reception Mode
   The reception block is shown in Fig. 3.

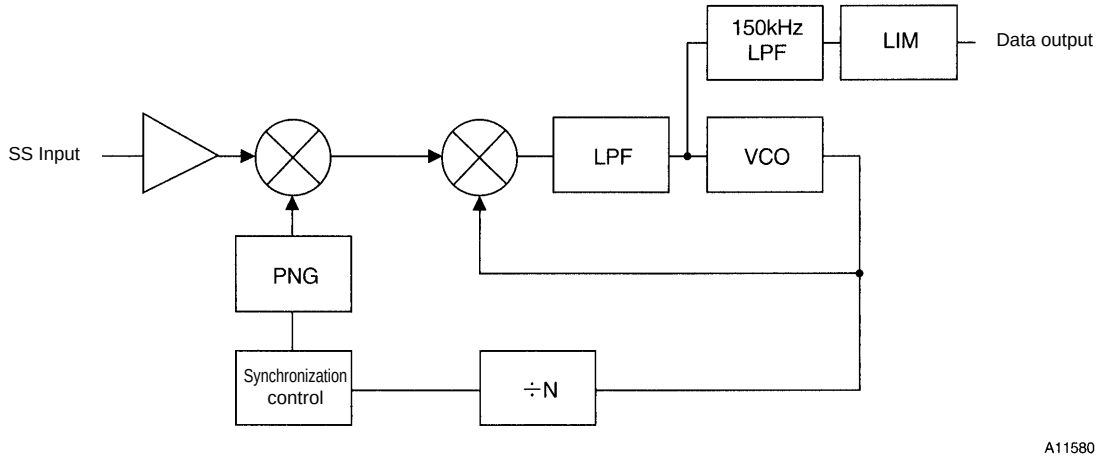


Fig. 3 The reception block

- PN Code synchronization

  In order to obtain data by demodulating the signal that has been spread spectrum modulated, it is necessary first to unspread the signal and convert it into a narrow band signal. This unspreading operation is made by multiplying the input high frequency signal with the PN code in a manner similar to the spreading operation made in the transmitting side. The PN code used at this time should be the same PN code that was used at the transmitting side. However, it is not possible to recover the narrow band signal before spreading by merely using the same code. It is necessary for the phases of the PN codes on the transmitting and receiving sides be matched to within ±1 chip.

  Let us consider this from the autocorrelation function. Fig. 4 shows the autocorrelation function of the PN code. Two identical PN codes are taken, and the autocorrelation function is obtained by evaluating the sum of products with one code kept fixed as the reference and the other code shifted by one chip at a time relative to the reference code, that is, each of the chips is multiplied with the corresponding chip at the same position and the sum of the products is obtained. As shown in the figure, the autocorrelation function is highly characteristic in that it shows meaningful output values only within a limited range. Therefore, in other words, the correlation value will always be –1 when there is a phase difference of more than ±1 chip, and the value becomes a maximum when the two PN codes have the same phase. Consequently, the process of PN synchronization consists of making the phase of the receiving side PN code to the phase of the transmitting side PN code so that the correlation value between the two transmitting side and receiving side PN codes becomes a maximum.

  In general, the process of establishing PN code synchronization can be considered to consist of the two stages of firstly the initial process in which the phase of the receiving side PN code is made to be within ±1 chip of the transmitting side PN code at which the autocorrelation output appears, and thereafter the process of obtaining the best synchronization point while maintaining the level of synchronization obtained earlier so that the autocorrelation function value becomes a maximum. The first of these two process stages is called initial acquisition and the second stage process is called synchronization maintenance and tracking control.

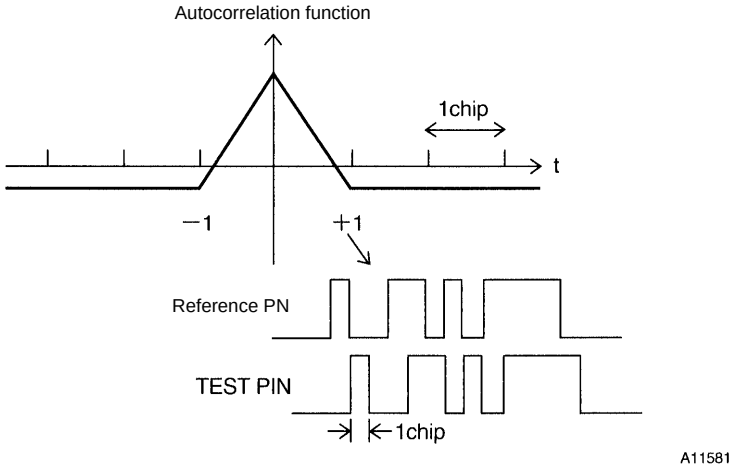
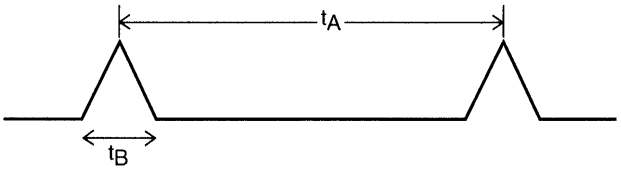


Fig. 4 Autocorrelation function

• Initial acquisition

In the LV2700V, initial acquisition is done by sliding correlation. Sliding correlation is the method of obtaining the correlation by shifting, by small amounts at a time, the phase of the receiving side PN code relative to the transmitting side PN code. The clock of the receiving side PN code generator is being generated by frequency division of the VCO output similar to the transmitting side. Therefore, a frequency difference is caused between the PN clocks of the sending and receiving side by slightly shifting the free running frequency from the carrier wave frequency, thereby carrying out the required sliding. In this case, since the speed of sliding is proportional to the amount of this frequency shift, making the amount of frequency shift smaller causes the time required for initial capture to become longer. Fig. 5 shows the time between peaks of the autocorrelation function value, etc., during the sliding process.



$$t_A = \frac{24 \bullet \text{PN code length}}{\Delta F} = 3.6 \text{ msec @15 chip}$$

ΔF = 100 kHz

$$t_B = \frac{24 \bullet 2}{\Delta F} = 480 \text{ µsec @15 chip}$$

ΔF = 100 kHz

Here,
ΔF: VCO Frequency – Carrier frequency
24: Frequency division factor from the VCO output to the PNG clock.

Fig. 5 The sliding time

Next, let us consider the process up to achieving the initial acquisition. In the sliding process, the output of the unspreading unit will still be the spread spectrum signal during the period in which the correlation output is zero. Further, since the carrier wave component is suppressed in the spread wave, the PLL does not operate effectively and does not get locked, and hence the sliding is continued with the VCO remaining in the free running frequency condition. Next, in the timing at which a valid autocorrelation output appears, since the continuous carrier wave component appears in the unspread output, the PLL operates correctly thereby achieving phase synchronization with the carrier wave. As a result, the VCO output changes from the free running frequency to the carrier wave frequency thereby making the difference in the transmitting side and receiving side PN clock frequencies zero, and the sliding stop at the point and the initial acquisition process gets completed.

- Optimal control (tracking control)

  After the initial acquisition is completed, the PN code synchronization condition is maintained by the PLL. This is because, in the LV2700V, since a system configuration is adopted that maintains phase synchronization between the carrier wave and the PN clock, the PN code synchronization is maintained as long as the PLL is locked to the carrier wave. However, since the position of the synchronization point within the ±1 chip range is not definite, a control circuit is provided to track to the best synchronization point. Fig. 6 shows the block diagram of the optimal control circuit. In this optimal control circuit, three PN codes delayed successively by 1/4 chip are used as the PN code for unspreading successively. In other words, these correspond to the reference phase P, the early phase E, and the late phase L. Next, the correlation output is obtained for each PN code by the envelope detector circuit. These correlation outputs are successively compared and the phase of the PN code is controlled so that the correlation output at the reference phase P is larger than the correlation values at the other PN codes. For example, when the PN codes at E, P, and L are at the positions shown in Fig. 7, since the correlation value at L is larger than that at the reference P, the phase of the PN code is controlled by gradually delaying until finally the position of P is at the point at which the value of the autocorrelation function becomes a maximum.

  Since this optimal control operation is being carried out continuously, the PN synchronization condition is maintained always at the best position even when the reception condition varies by large amounts.

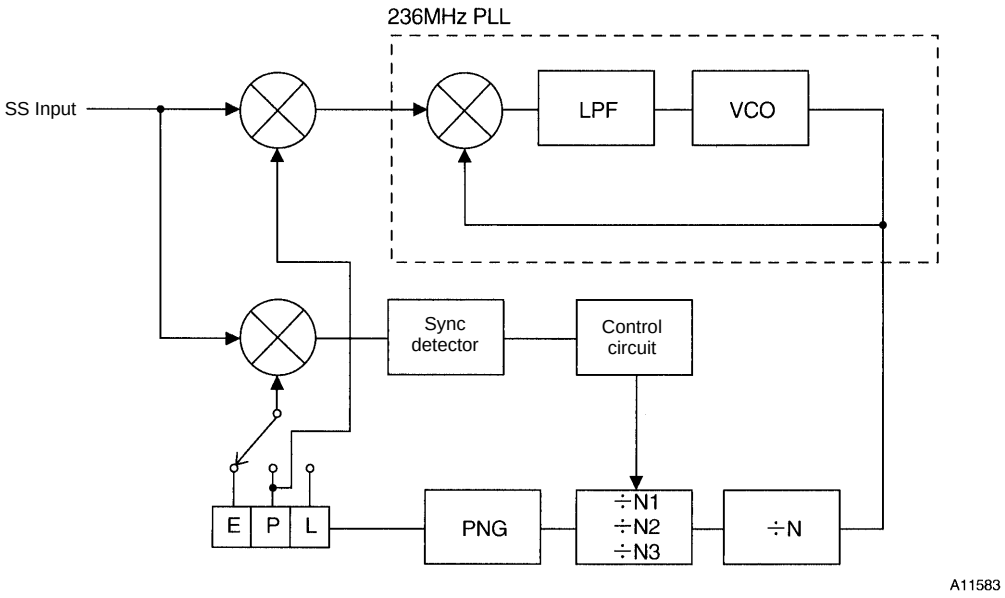


Fig. 6 Optimal control circuit

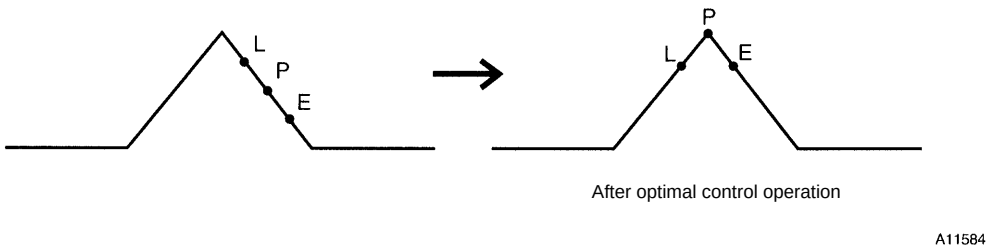


Fig. 7

• FM Demodulation

The PN code of the reference phase described above is used in the unspreading unit for the signals. Further, the PLL in the last stage of the unspreading unit carries out the operation of not only the above PN synchronization maintenance but also functions as an FM demodulator so that the data signal is obtained at the end of the loop filter. However, since it is not possible to set the loop bandwidth to be sufficiently narrow because of the setting of the initial acquisition time response characteristics, the PN component cannot be sufficiently suppressed at the end of the loop filter. Therefore, a 150kHz LPF is provided at the demodulator output thereby removing the leakage components of the PN code thus improving the S/N ratio. If the S/N ratio is to be further improved by limiting the demodulation bandwidth, it is necessary to add another LPF.

Application Information

1. Operating Mode Selection

The selection of the transmission mode and the reception mode is set as follows by the input at pin 15 and the method of applying the voltage at the power supply terminal. Note that the power supply to the bias circuit of the circuit block dedicated to the RX mode is automatically made OFF by pin 15 during the TX mode thereby saving power dissipation.

Mode	Pin 15	Power supply terminal setting method
TX	High	Voltages are applied to all the power supply terminals.
RX	Low	The voltage is applied to all power supply terminals except pin 27.

2. RF Block

Since the LV2700V carries out direct signal processing at 236 MHz without converting to an IF frequency, it is possible to configure a transmitting and receiving system with a minimum of external components. The standard operating frequency of 236 MHz has been selected so that it can be used as such in systems using weak radio waves. In addition, by combining with an up-converter or a down-converter so that the IF frequency becomes 236 MHz, it is possible to use this IC even in ISM bands such as 2.4 GHz, etc.

The LV2700V has a 15 dB RF amplifier in the input block, and hence is it possible to obtain an input sensitivity of about –100dBm by using an external RF amplifier of about 25 dB. Further, it is necessary to place a BPF in the latter stage of the antenna thereby removing components outside the band of interest and thus improving the interference characteristics and the input sensitivity.

3. VCO

• TX Mode

The VCO output is adjusted by the PLL circuit to a frequency that is 24 times the reference oscillator frequency, that is, 236 MHz. The reference oscillator circuit is configured by an inverter using a quartz oscillator element of 9.8304 MHz. Also, the phase comparator uses an EX-OR gate and carries out the comparison operation at the reference frequency. Further, since the clock of the PN code generator is generated by frequency division of the VCO output by 24, its frequency becomes equal to the reference frequency.

• RX Mode

In the reception mode, the input signal will be the reference signal for the PLL. Therefore, under the no-signal condition, the VCO will be in the free running state. The phase comparator carries out phase comparison at 236 MHz using an analog mixer circuit. By using a circuit configuration in which there is no frequency divider between the VCO and the phase comparator, the PLL loop gain is made large thereby increasing the input sensitivity of the PLL itself. The PN clock is generated by frequency dividing the VCO output by 24 similar to that in the transmission mode.

4. FM, FSK Modulation

When the input signal is an analog signal, the modulation is FM and the modulation is FSK when the input signal is a digital signal. However, the modulation method is common to both, and the modulating signal is applied as the analog signal to the control terminal of the VCO in the PLL.

Data Input

The data is input to pin 17. Pin 17 is a dedicated data input terminal. This signal is passed through a 1 Vpp limiter amplifier and a 300 kHz LPF and is output at pin 18. The output at pin 18 is connected via an RC series circuit to pin 22 which is the loop filter terminal.

Analog Input

Since the input pin 17 is dedicated to data, it cannot be used for analog inputs. Connect analog input signals via an RC series circuit to pin 22.

5. FM, FSK Demodulation

In the reception mode, the FM demodulated signal is obtained from the loop filter terminal of pin 25. An output after passing through a buffer amplifier is output at pin 24 in order to take out the demodulated signal without affecting the loop filter constants. However, as explained earlier, since it is not possible to make the loop bandwidth sufficiently narrow due to the setting of the time response characteristics of the PN synchronization initial acquisition process, it is not possible to sufficiently suppress the PN component in the output at the loop filter terminal. Therefore, a 150 kHz LPF is incorporated to remove the PN component included in the demodulated signal. However, since the fundamental PN frequency becomes less than 150 kHz when the PN code length becomes longer than 127 chips, it is not possible to sufficiently suppress the PN components by the built-in filter. Hence, when using PN code lengths of more than 127 chips, add an LPF between pin 23 and pin 24. The fundamental PN frequency at each PN code length is given in the table below. Since these frequencies become the fundamental frequencies of the PN leakage component, use an LPF that has sufficient attenuation at this frequency. Further, these values also become the maximum data transfer rates during data transmission. However, when the built-in 150 kHz LPF is used, the maximum rate will be limited to less than 256 kbps.

PN Code length	Fundamental PN frequency
15	655 kHz
31	317 k
63	156 k
127	77 k
255	38 k
511	19 k

Note: Fundamental PN frequency = $\frac{\text{PN Clock frequency}}{\text{PN code length}}$

Analog Output

The analog output can be obtained at pin 10.

Data Output

The data is output at pin 8 which is an open drain output. In order to suppress the output of noise under the no-modulation conditions, hysteresis is provided by connecting a feedback resistor of about 510 kΩ between pin 8 and pin 10. Care should be taken because the effective sensitivity becomes lower if the feedback resistor for hysteresis is made lower than 200 kΩ.

• Method of biasing pin 23

It is necessary to set the DC bias at pin 23 to a value equal to the reference bias of the amplifier through the built-in LPF. The reference bias of the built-in amplifier is provided by a resistance divider consisting of a 30 k and a 20 k resistors, and the bias will be about 1.2 V when the power supply voltage is 3 V. As a result, although it is possible to set the bias of pin 23 using the 30k and 20 k bias resistors, it is recommended to connect a 30 k feedback resistor between pin 7 and pin 23 (see Fig. 8). Using this biasing method, it is possible to apply the same DC bias as the internal bias voltage at pin 23 at all times without being affected by variations in the power supply voltage or the resistance values.

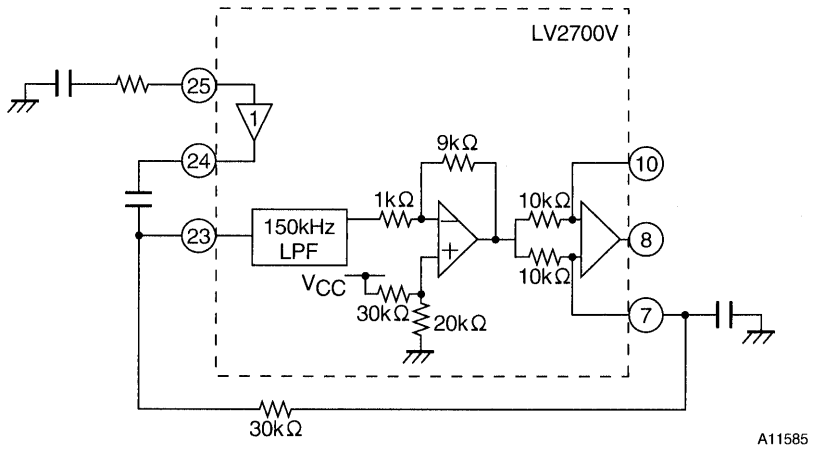


Fig. 8

7. Miscellaneous information

• On LOCKDET

This output goes to the high level when the PN code synchronization is achieved. However, since the LOCKDET sensitivity is lower than the PN synchronization sensitivity, near the input sensitivity limit, even when the demodulated output is being made, the LOCKDET output may sometimes remain in the low level. Treat this as merely a simple carrier detection signal.

• On ANTDUMP

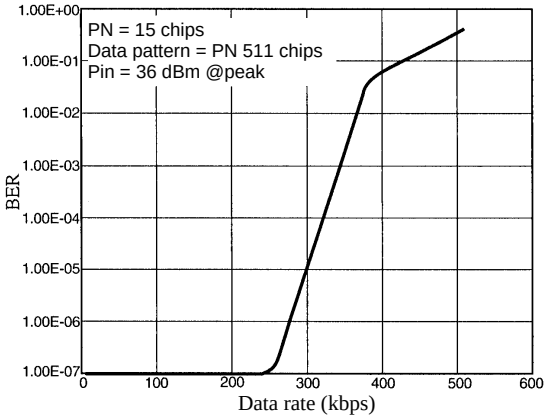
This is a DC output proportional to the RF input level. However, since the input dynamic range of about 20 dB and the output range of variation of about 0.5 V are narrow, this output is not suitable for a signal meter. Its major application is for the saturation prevention circuit of the RF amplifier under strong radio signal inputs.

• The lock up time of the reception PLL is about 2 ms to 10 ms at the time of switching on the power, and about 500 µs to 1ms when there is a change from the no-signal condition to the signal input condition.

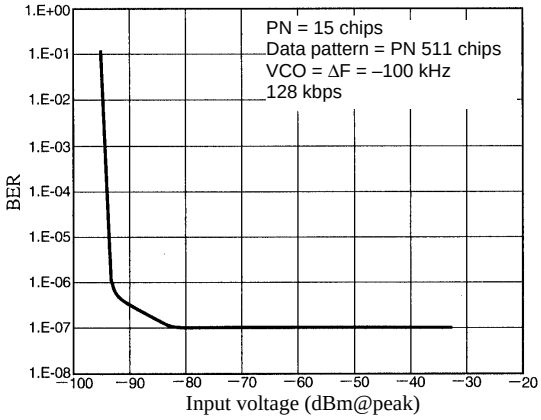
8. Recommended Components

Recommended component	Type No.	Manufacturer
SAW Resonator	SAR 234.74MF10T115	Murata Mfg. Co., Ltd.
236 MHz BPF	LFB30N12B0236B024	Murata Mfg. Co., Ltd.
Variable coil	CS-5N (SA-1100)	Sumida Electric

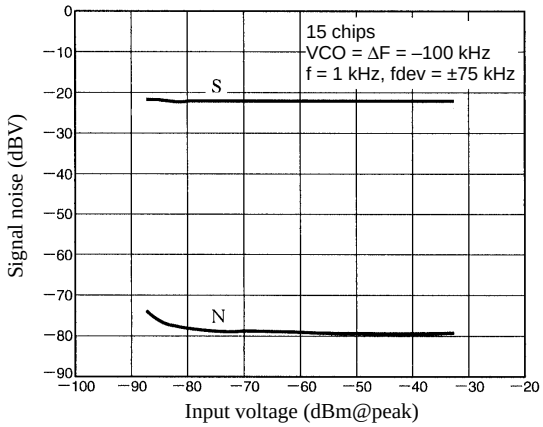
BER



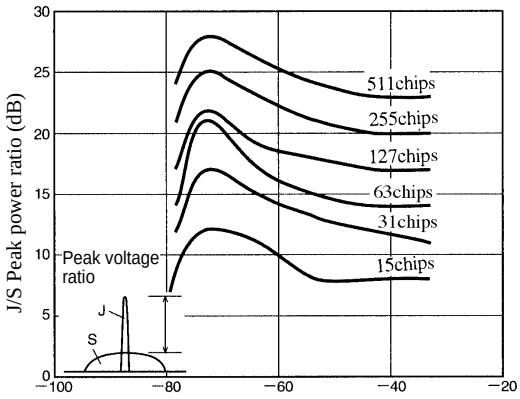
Input sensitivity



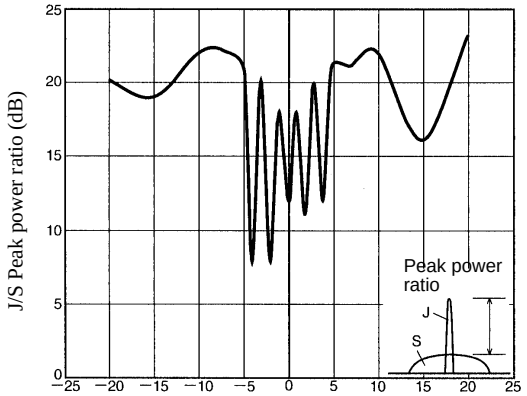
S/N characteristics pin 10 output



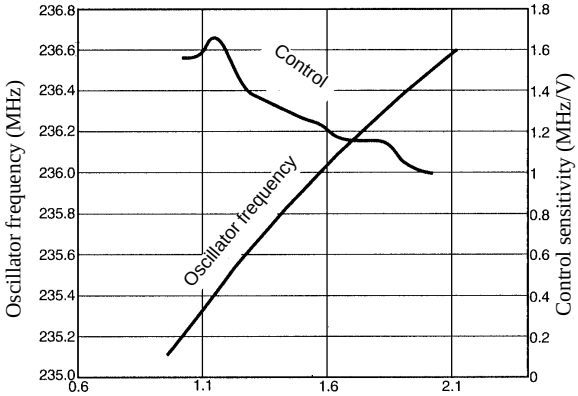
Anti-interference characteristics



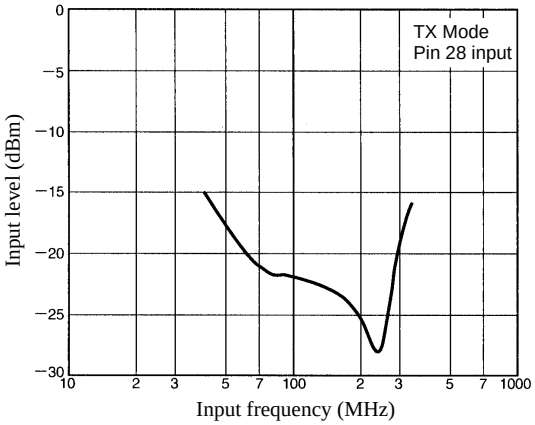
Frequency dependence of anti-interference characteristics



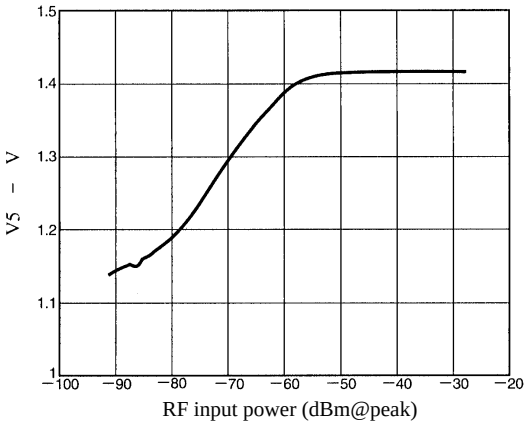
RX VCO control characteristics



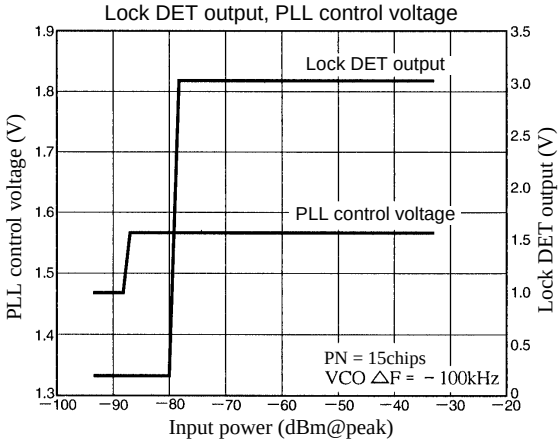
ECL frequency divider input sensitivity



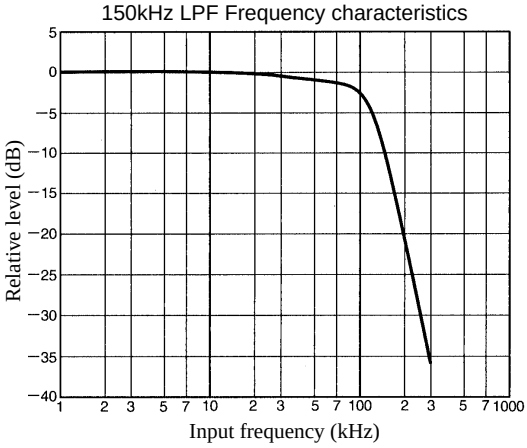
AGC output



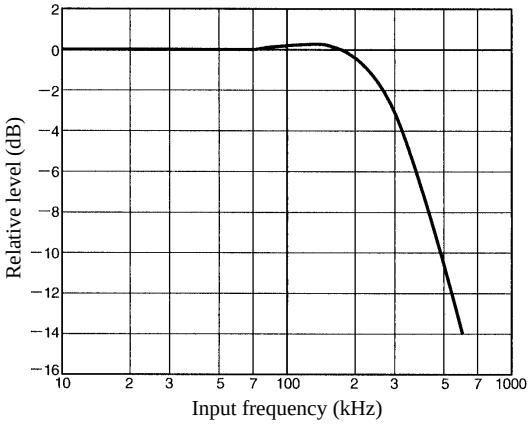
Lock DET output, PLL control voltage



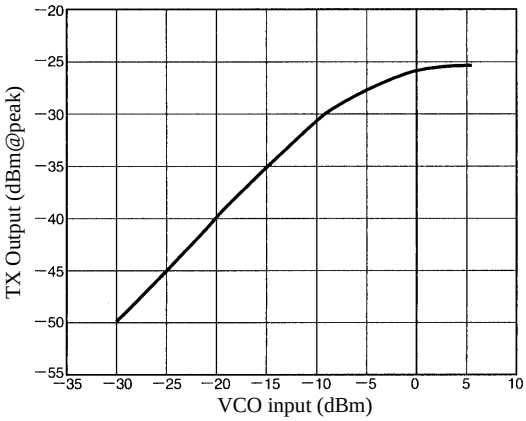
150kHz LPF Frequency characteristics



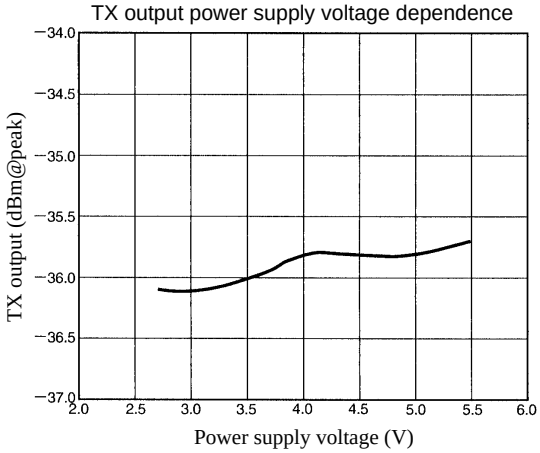
TX 300kHz LPF frequency characteristics



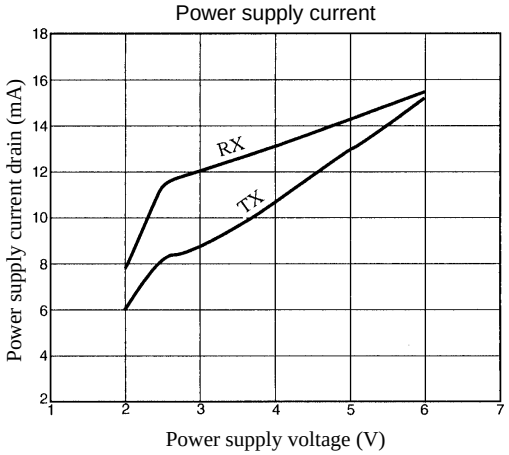
TX output vs VCO input



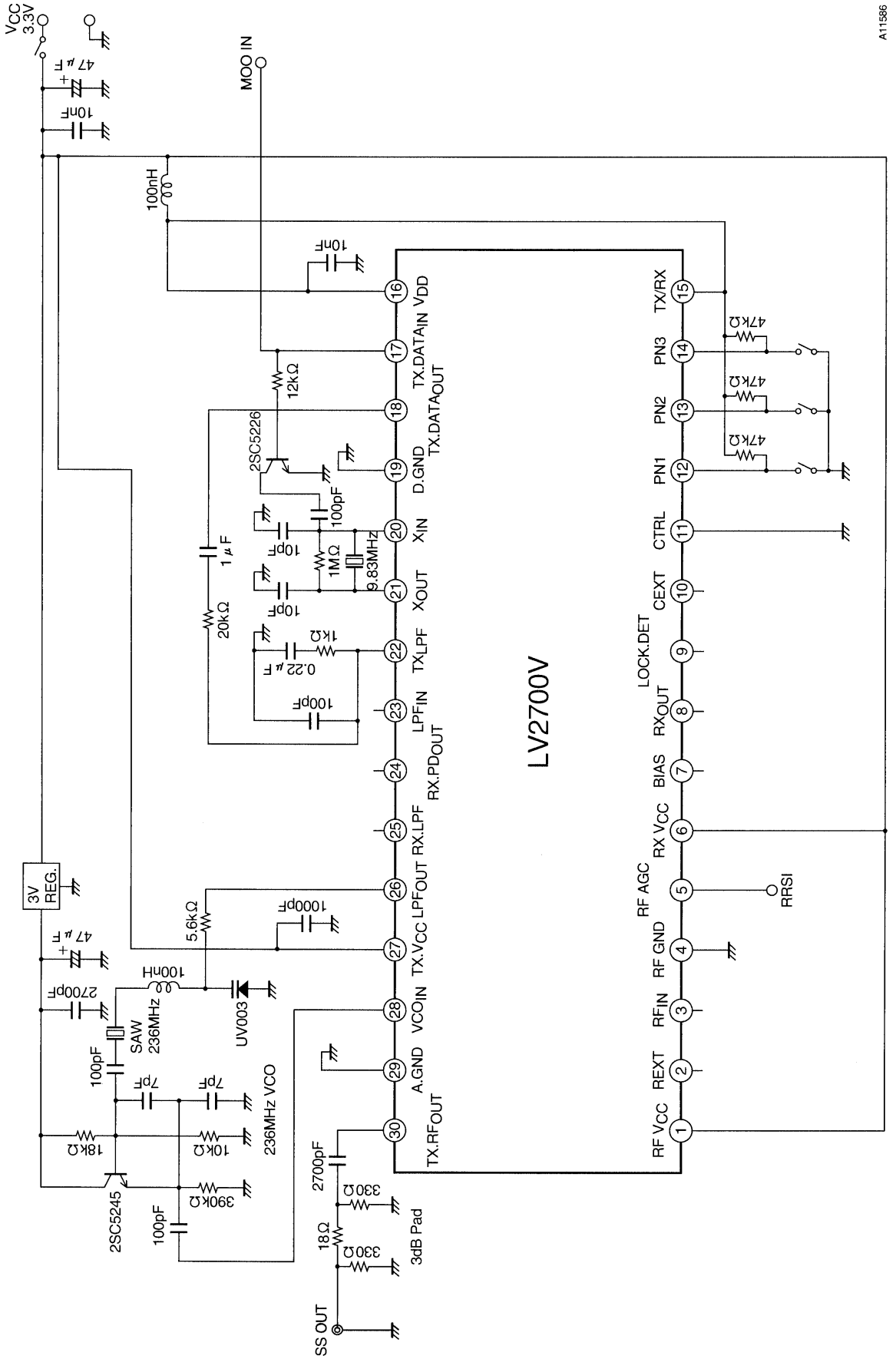
TX output power supply voltage dependence



Power supply current



Sample Application Circuit (Transmission side)



Sample Application Circuit (Reception side)