Ordering number : EN*4435A

CMOS LSI

LC587008, 587006, 587004

Single-Chip 4-Bit Microprocessors with LCD Driver, 2 Kb RAM, and 8, 12, or 16 KB ROM on chip

Preliminary

Overview

The LC587004, LC587006 and LC587008 are 80-pin low-voltage CMOS 4-bit microprocessors that include LCD drivers, 2 Kb RAM and 8, 12, or 16 KB ROM on chip. These microprocessors correspond to the earlier LC5870 series with the 256 by 4-bit on-chip RAM expanded to a 512 by 4-bit capacity.

Applications

- System control and LCD display in CD players, cameras and radio tuners
- System control and LCD display in miniature test equipment and consumer health care products
- These microprocessors are optimal for products that include LCD displays and, in particular, battery operated products.
- Remote controllers for VCRs and audio equipment

Functions

- Program ROM: 8064 × 16 bits (LC587008), 6144 × 16 bits (LC587006) and 4096 × 16 bits (LC587004)
- RAM: 512 × 4 bits on chip
- All instructions execute in a single cycle
- Cycle time and operating voltage ranges
  - — 2 µs cycle time: V_{DD} = 2.8 to 6.0 V
    10 µs cycle time: V_{DD} = 2.2 to 6.0 V
    122 µs cycle time: V_{DD} = 2.0 to 6.0 V
- Rich set of HALT/HOLD mode clearing and interrupt functions
  - — Eight HALT mode clearing functions
  - — Seven HOLD mode clearing functions
  - — Seven interrupt functions (all of which can be used as external interrupts)
  - — Subroutines can be nested up to eight levels (including interrupt handling)
  - — Built-in watchdog timer function
- Powerful hardware for improved processing capacity
  - — Built-in segment PLA and segment decoder: LCD panel segments can be handled with no software processing of the LCD driver outputs. Also, the LCD drive pins can be switched to function as output ports.
  - — Built-in 8-bit synchronous serial I/O circuit
  - — One 8-bit programmable timer (that can be used as an event counter)
  - — One 8-bit programmable reload timer (that can be used to generate a remote control carrier signal)
  - — The whole RAM area can be used as working area (by using the RAM bank register)
  - — Built-in RAM data pointer
  - — Built-in clock oscillator and 15-bit divider (also used to generate the LCD alternating frequency)
- Highly flexible LCD panel drive output pins (35 pins)

  LCD panel .....Number of .....Required
  drive type.....segments .....common pins
  1/3 bias 1/4 duty .....140 segments .....Four pins
  1/3 bias 1/3 duty .....105 segments .....Three pins
  1/2 bias 1/4 duty .....140 segments .....Four pins
  1/2 bias 1/3 duty .....105 segments .....Three pins
  1/2 bias 1/2 duty .....70 segments .....Two pins
  Static.....35 segments .....One pin

  The LCD output pins can be switched to function as general-purpose outputs.
  - — C-MOS type: Up to 35 pins
  - — P-channel type: Up to 35 pins
  - — N-channel type: Up to 35 pins
- These microprocessors allow the use of an oscillator appropriate to the application system specifications.
  - — Crystal oscillator: 32 kHz, 65 kHz or 38 kHz (for the time base, system clock or LCD alternating frequency)
  - — Ceramic oscillator: 400 kHz to 4 Mhz (for the system clock and the timers and serial counter)
  - — RC oscillator: 200 kHz to 1 MHz (for the system clock and the timers and serial counter)
  - — External clock (for the system clock and the timers and serial counter)

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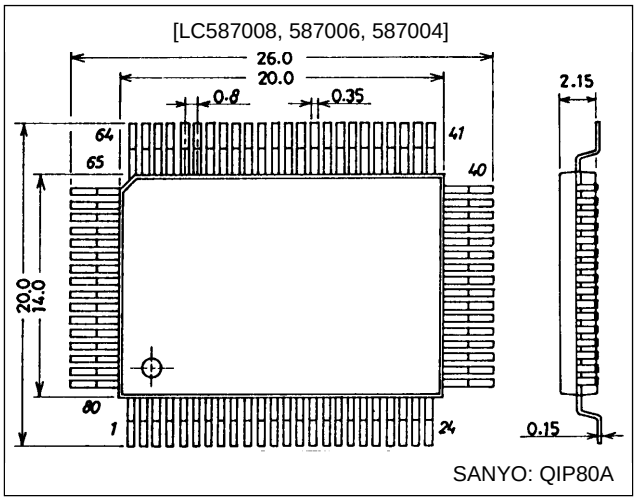
Features

- These microprocessors are the top end of the LC5870 series and have the following features.
  Faster cycle times
  — Cycle time: 2 µs for V_{DD} between 4.5 and 6.0 V
  — Cycle time: 10 µs for V_{DD} between 2.2 and 6.0 V
  Low power dissipation HALT mode (typical) Continuous operation (typical)
  — Ceramic filter (CF) 4 MHz (5.0 V) 600 µA 1.7 mA (cycle time = 2 µs)
  — Crystal oscillator 32 kHz (3.0 V, CF stopped) 4.0 µA 20 µA (cycle time = 122 µs)
  Improved timer functions
  — One 8-bit programmable timer (that can be used as an event counter)
  — One 8-bit programmable reload timer (that can be used to generate a remote control carrier signal)
  — Time base timer (for use as a clock)
  — Watchdog timer
  Improved standby functions
  — Clock standby function (HALT mode), software switching between low speed mode (low current) and high speed mode
  — Full standby mode (HOLD mode)
  — HALT and HOLD modes can be cleared by external interrupt pins, input ports (up to nine pins) and serial I/O interrupts
  Improved I/O functions
  — External interrupt pins
  — Up to 9 input and I/O pins that can clear HALT and HOLD modes
  — Up to 24 input ports with built-in software controllable input resistors (either pull-up or pull-down specified as mask options)
  — Up to 25 input port pins with a built-in floating prevention circuit
  — LCD driver: four common pins and 35 segment pins
  — General-purpose I/O ports: 20 pins (of which 12 are p-channel open drain and 4 are n-channel open drain)
  — General-purpose inputs: five pins
  — General-purpose outputs (type 1): four pins (LED direct drive pins, one internal alarm signal output pin and one carrier output pin)
  — General-purpose outputs (type 2): 35 pins (when all 35 LCD segment port pins are switched over to function as general-purpose outputs)
  — Eight-bit serial I/O port: one set (three pins: input, output and clock)
- Delivery formats: QFP80 (QIP80) and chip

Package Dimensions

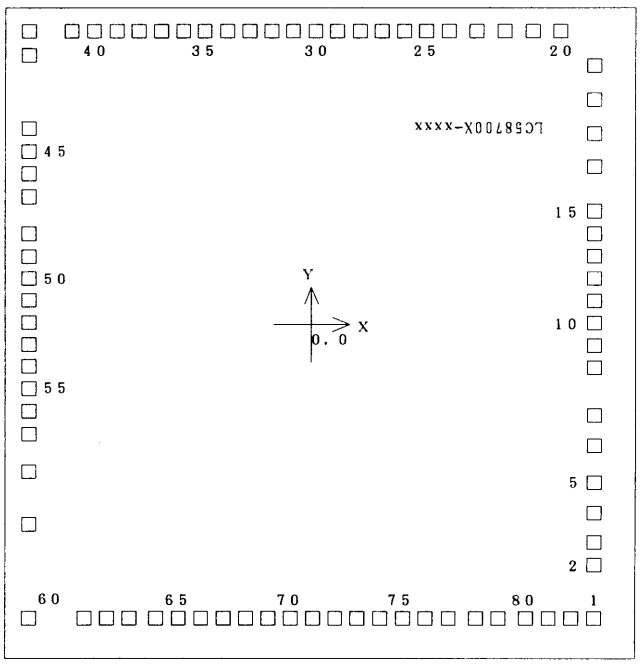
unit: mm

3044B-QFP80A



Pad Layout

Chip size: 5.12 mm × 5.29 mm
Pad size: 120 µm × 120 µm
Chip thickness: 480 µm (chip products)

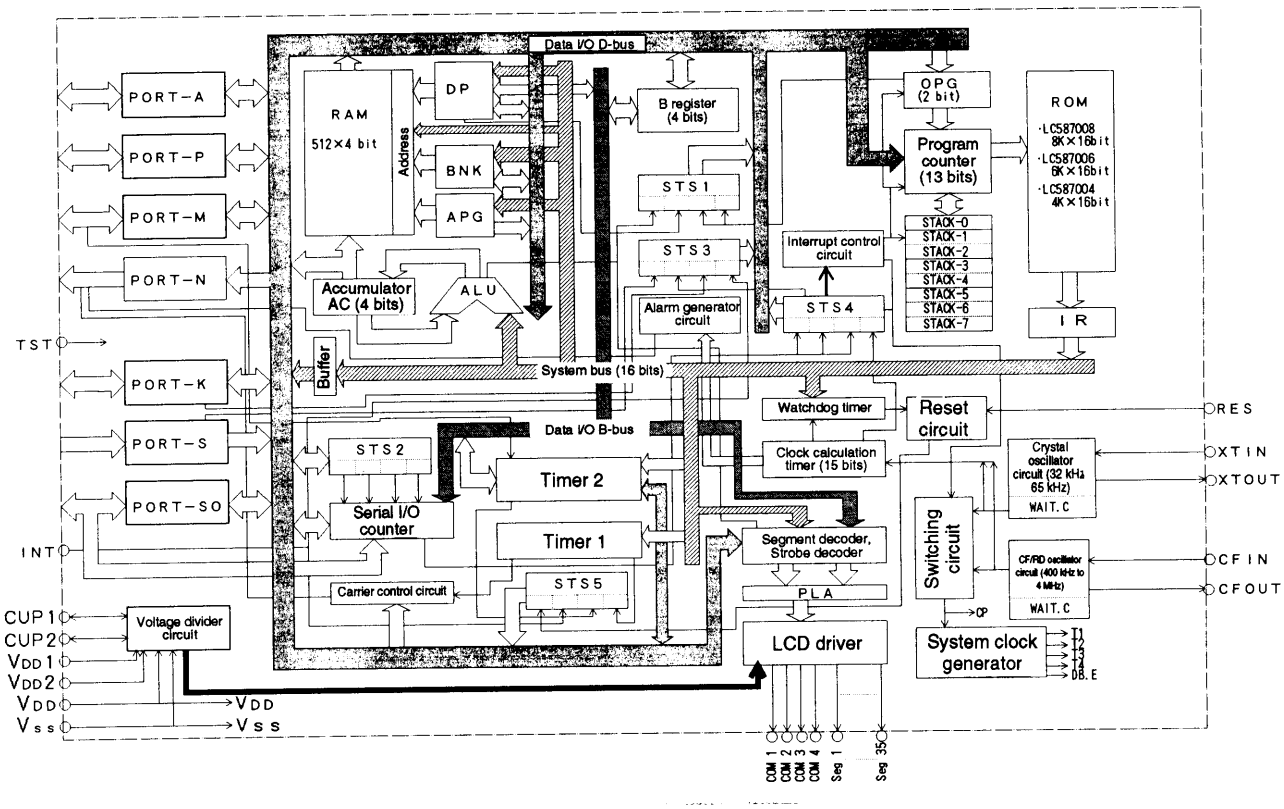


Pin Assignments/Pad Names and Coordinates

Pin No.	Pad No.	Symbol	Coordinates Xµm	Coordinates Yµm
24	1	V_{DD}	2234	–2319
25	2	CFIN	2234	–1883
26	3	CFOUT	2234	–1701
27	4	S1 (Input port)	2234	–1458
28	5	S2 (Input port)	2234	–1212
29	6	S3 (Input port)	2234	–915
30	7	S4 (Input port)	2234	–669
31	8	K1 (I/O port)	2234	–284
32	9	K2 (I/O port)	2234	–101
33	10	K3 (I/O port)	2234	81
34	11	K4 (I/O port)	2234	264
35	12	M1 (I/O port)	2234	448
36	13	M2 (I/O port)	2234	631
37	14	M3 (I/O port)	2234	814
38	15	M4 (I/O port)	2234	997
39	16	N1 (Output port)	2234	1352
40	17	N2 (Output port)	2234	1624
41	18	N3 (Output port)	2234	1895
42	19	N4 (Output port)	2234	2173
43	20	TST	1958	2449
44	21	Seg 1	1732	2449
45	22	Seg 2	1506	2449
46	23	Seg 3	1280	2449
47	24	Seg 4	1054	2449
48	25	Seg 5	874	2449
49	26	Seg 6	694	2449
50	27	Seg 7	514	2449
51	28	Seg 8	335	2449
52	29	Seg 9	155	2449
53	30	Seg 10	–24	2449
54	31	Seg 11	–204	2449
55	32	Seg 12	–384	2449
56	33	Seg 13	–564	2449
57	34	Seg 14	–744	2449
58	35	Seg 15	–923	2449
59	36	Seg 16	–1103	2449
60	37	Seg 17	–1283	2449
61	38	Seg 18	–1463	2449
62	39	Seg 19	–1643	2449
—	40	Test	–1821	2449
—	41	Test	–2001	2449
63	42	Seg 20	–2362	2449
64	43	Seg 21	–2362	2248
65	44	Seg 22	–2362	1649
66	45	Seg 23	–2362	1468
67	46	Seg 24	–2362	1288
68	47	Seg 25	–2362	1107
69	48	Seg 26	–2362	799
70	49	Seg 27	–2362	618
71	50	Seg 28	–2362	438
72	51	Seg 29	–2362	257
73	52	Seg 30	–2362	77
74	53	Seg 31	–2362	–103
75	54	Seg 32	–2362	–283
76	55	Seg 33	–2362	–464
77	56	Seg 34	–2362	–664
78	57	Seg 35	–2362	–824
79	58	COM4	–2362	–1139
80	59	COM3	–2362	–1564
1	60	COM2	–2362	–2319
2	61	COM1	–1912	–2319
3	62	CUP1	–1730	–2319
4	63	CUP2	–1549	–2319
5	64	RES	–1327	–2319
6	65	INT	–1145	–2319
7	66	SO1 (I/O port, SIO port)	–963	–2319
8	67	SO2 (I/O port, SIO port)	–780	–2319
9	68	SO3 (I/O port, SIO port)	–597	–2319
10	69	SO4 (I/O port, SIO port)	–414	–2319
11	70	A1 (I/O port)	–231	–2319
12	71	A2 (I/O port)	–48	–2319
13	72	A3 (I/O port)	134	–2319
14	73	A4 (I/O port)	317	–2319
15	74	P1 (I/O port)	504	–2319
16	75	P2 (I/O port)	687	–2319
17	76	P3 (I/O port)	870	–2319
18	77	P4 (I/O port)	1053	–2319
19	78	XTOUT	1279	–2319
20	79	XTIN	1462	–2319
21	80	$V_{DD}2$	1685	–2319
22	81	$V_{DD}1$	1868	–2319
23	82	V_{SS}	2050	–2319

Note: 1. Pin numbers are for QIP80 package products.
2. Connect the test pins (TST) to V_{SS}.
3. Pad numbers 40 and 41 must be left open in the chip specification product.
4. Do not use dip-soldering techniques to mount the QIP80 package versions.
5. For chip products either connect the substrate to V_{SS} or leave it open.

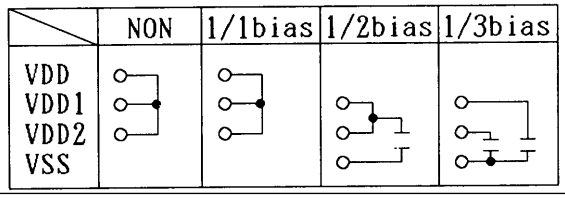
System Block Diagram



System Block Diagram for the LC587008, LC587006 and LC587004

RAM:	Data memory
ROM:	Program memory
DP:	Data pointer register
BNK:	Bank register
APG:	RAM page flags
AC:	Accumulator
ALU:	Arithmetic and logic unit
B:	B register
OPG:	ROM page flag
PC:	Program counter
IR:	Instruction register
STS1:	Status register 1
STS2:	Status register 2
STS3:	Status register 3
STS4:	Status register 4
STS5:	Status register 5
PLA:	Segment data and strobe programmable logic array
WAIT.C:	Waiting time counter

Pin Functions

Pin	I/O	QIP-80 Pin No.	Function	Option	At reset
V_{DD} V_{SS}	— —	24 23	Power supply		
$V_{DD}1$ $V_{DD}2$	— —	22 21	LCD drive power supply 		
CUP1 CUP2	— —	3 4	Switching pin used to supply the LCD drive voltage to the $V_{DD}1$ and $V_{DD}2$ pins • Connect a nonpolarized capacitor between CUP1 and CUP2 when 1/2 or 1/3 bias is used. • Leave open when a bias other than 1/2 or 1/3 is used.		
CFIN	Input	25	System clock oscillator connections • Ceramic resonator connection (CF specifications) • RC component connection (RC specifications) • External signal input pin (CFOUT is left open) This oscillator is stopped by the execution of a STOP or SLOW instruction.	• CF specifications • RC specifications • External specifications • Not used	
CFOUT	Output	26			
XTIN	Input	20	Reference calculation (clock specifications, LCD alternating frequency), system clock oscillator • 32 kHz crystal resonator connection • 65 kHz crystal resonator connection This oscillator is stopped by the execution of a STOP instruction.	• 32k specifications • 65k specifications • 38k specifications • Not used	
XTOUT	Output	19			
S1 S2 S3 S4	Input	27 28 29 30	Input-only ports • Input pins used to read data into RAM • Built-in 7.8 ms and 1.95 ms chatter rejection circuits • Built-in pull-up/pull-down resistors Note: The 7.8 ms and 1.95 ms times are the times when ø0 is 32.768 kHz.	• Transistors to hold a low or high level • Selection of either pull-up or pull-down resistors	• The pull-up or pull-down resistors are on. Note: These pins go to the floating state when reset is cleared.
K1 K2 K3 K4	I/O	31 32 33 34	I/O ports • Input pins used to read data into RAM • Output pins used to output data from RAM • Built-in 7.8 ms and 1.95 ms input-mode chatter rejection circuits. The selection of 7.8 or 1.95 ms is linked to that for the S ports. Note: The 7.8 ms and 1.95 ms times are the times when ø0 is 32.768 kHz.	• Transistors to hold a low or high level • Selection of either pull-up or pull-down resistors	• The pull-up or pull-down resistors are on. Note: These pins go to the floating state when reset is cleared. • Input mode • Output latch data is set high.
M1 M2 M3 M4	I/O	35 36 37 38	I/O ports • Input pins used to read data into RAM • Output pins used to output data from RAM • M4 is used as the external clock input pin in TM2 mode 3. * The minimum period for the external clock is twice the cycle time. • Built-in pull-up/pull-down resistors	The same as K1 to K4	The same as K1 to K4
A1 A2 A3 A4	I/O	11 12 13 14	I/O ports • Input pins used to read data into RAM • Output pins used to output data from RAM • Built-in pull-up/pull-down resistors	The same as K1 to K4	The same as K1 to K4
P1 P2 P3 P4	I/O	15 16 17 18	I/O ports Function: The same as pins A1 to A4	The same as K1 to K4	The same as K1 to K4

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Pin	I/O	QIP-80 Pin No.	Function	Option	At reset
SO1 SO2 SO3 SO4	I/O	7 8 9 10	I/O ports Function: The same as for pins A1 to A4 Pins SO1 to SO3 area also used for the serial interface. • Use of these pins in serial mode can be selected under program control. • Pin functions: SO1: Serial input pin SO2: Serial output pin SO3: Serial clock pin The serial clock pin can be switched between internal and external, and between rising edge output and falling edge output.	• Transistors to hold a low or high level • Selection of either pull-up or pull-down resistors • Internal serial clock divisor selection I 1/1 II 1/2 III 1/4	The same as for K1 to K4
N1 N2 N3 N4	Output	39 40 41 42	Output-only ports • Output pins used to output data from RAM • An alarm signal can be output from pin N4. (Note that this is only when the N4 output latch is low.) • An alarm signal modulated at 1, 2 or 4 kHz can be output. (These frequencies are output when ø0 is 32.768 kHz.) • A carrier signal can be output from N3. (Note that this is only when the N3 output latch is low.)	• Pins N1 to N4 output circuit type: I CMOS II N-channel open drain • Pins N1 to N4 output level I High level II Low level	The output levels on pins N1 to N4 can be specified as an option.
INT	Input	6	Input ports • External interrupt request inputs • Input pins used to read data into RAM • Input detection can be performed on either rising or falling edges. • Built-in pull-up/pull-down resistors	• Transistors to hold a low or high level • Selection of either pull-up or pull-down resistors • Signal conversion (rising/falling) selection	
RES	Input	5	LSI internal reset input • The reset input level can be selected to be either high or low. • Built-in pull-up/pull-down resistors • Note: The reset pulse must be at least 500 µs.	* Only when the input resistor open specification is selected	
TST	Input	43	Test input • QIP80 products: Connect to V_{SS}. • Chip products: Leave open or connect to V_{SS}.		
Seg1, Seg2 to Seg35	Output	44, 45 to 78	• LCD panel drive/general-purpose output — LCD panel drive I STATIC II 1/2 bias – 1/2 duty III 1/2 bias – 1/3 duty IV 1/2 bias – 1/4 duty V 1/3 bias – 1/3 duty VI 1/3 bias – 1/4 duty Types I to V can be specified as mask options. — General-purpose output mode I CMOS II P-channel open drain III N-channel open drain Types I to III can be specified as mask options. • LCD/general-purpose output control is handled by the segment PLA, and thus program control is not required. • These pins support output latch control on reset and in standby states when the oscillators are stopped. • Arbitrary combinations of LCD drive and general-purpose outputs can be used.	• LCD driver/general-purpose output switching • LCD drive type switching — STATIC — 1/2 bias – 1/2 duty — 1/2 bias – 1/3 duty — 1/2 bias – 1/4 duty — 1/3 bias – 1/3 duty — 1/3 bias – 1/4 duty • General-purpose output circuit switching — CMOS — P-channel open drain — N-channel open drain • Output latch control in standby modes	• LCD drive — All segments on — All segments off *: Determined by mask options • General purpose outputs — High level — Low level *: Determined by mask options Note: When a combination of LCD drive and general-purpose outputs, the output state is either: — All lit/high level — All off/low level. • These pins go to the static drive mode during the reset period.

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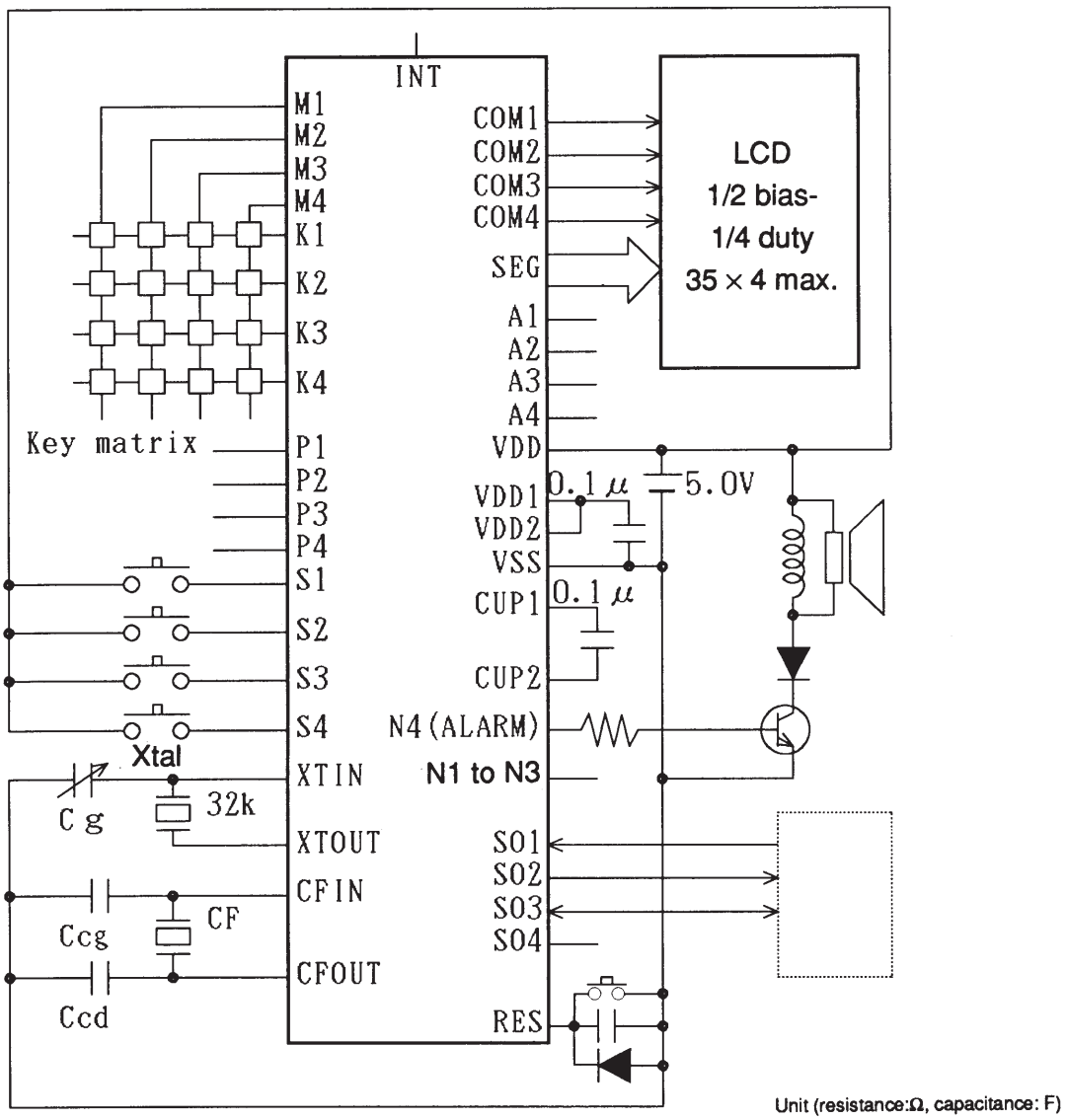
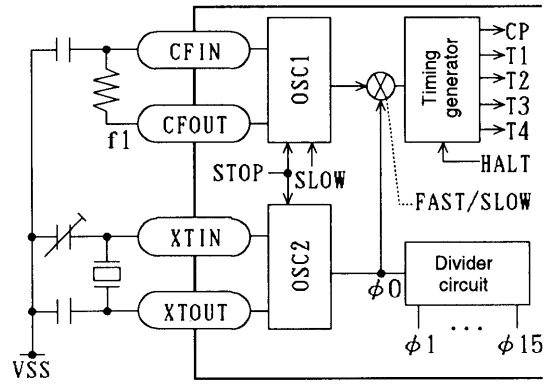
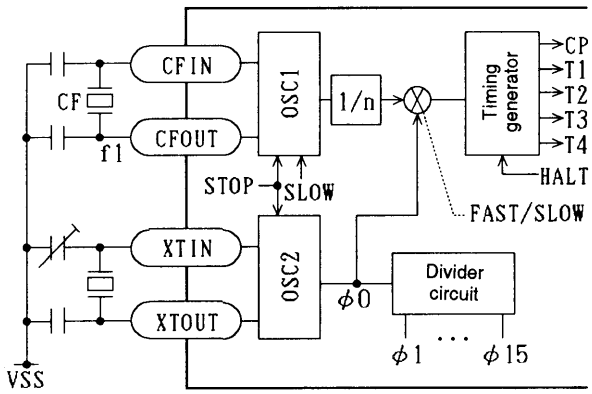
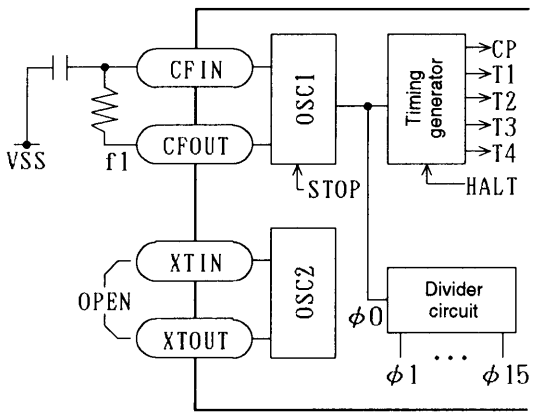
<table>
<tr><th>Pin</th><th>I/O</th><th>QIP-80
Pin No.</th><th>Function</th><th>Option</th><th>At reset</th></tr>
<tr>
<td>COM1
COM2
COM3
COM4</td>
<td>Output</td>
<td>2
1
80
79</td>
<td>LCD panel drive common polarity outputs
The table below shows how these pins are used depending on the duty used. (Values for alternating frequency reflect a typical specification of 32.768 MHz for ø0.)
<table>
<tr><th></th><th>Static duty</th><th>1/2 duty</th><th>1/3 duty</th><th>1/4 duty</th></tr>
<tr><td>COM1
COM2
COM3
COM4</td><td>○
×
×
×</td><td>○
○
×
×</td><td>○
○
○
×</td><td>○
○
○
○</td></tr>
<tr><td>Alternation frequency</td><td>32 Hz</td><td>32 Hz</td><td>42.7 Hz</td><td>32 Hz</td></tr>
</table>
Note: A cross (×) indicates that the pin is not used with that duty type.</td>
<td></td>
<td>The static drive waveform is output during the reset period.
* There are cases where the alternating frequency stops for the CF, RC and external clock specifications. (These cases differ depending on option specifications.)</td>
</tr>
</table>

Sample Application Circuit

LCD: 1/2 bias – 1/4 duty



Oscillator Circuit Options

Option	Circuit configuration	Note
RC and Xtal		• The cycle time is four times the f1 period. • The divider outputs (ø1 to ø15) are used as the time base, the LCD drive waveform generation clock, the S and K port chattering rejection clock and for other functions. • OSC1 is stopped when a SLOW instruction is executed.
CF and Xtal • 400 kHz (CF) • 4 MHz (CF)		• The cycle time is four times n times the f1 period. (Note: n is 2.) • The divider outputs (ø1 to ø15) are used as the time base, the LCD drive waveform generation clock, the S and K port chattering rejection clock and for other functions. • OSC1 is stopped when a SLOW instruction is executed.
RC		• The cycle time is four times the f1 period. • The divider outputs (ø1 to ø15) are used as the LCD drive waveform generation clock, the S and K port chattering rejection clock and for other functions.

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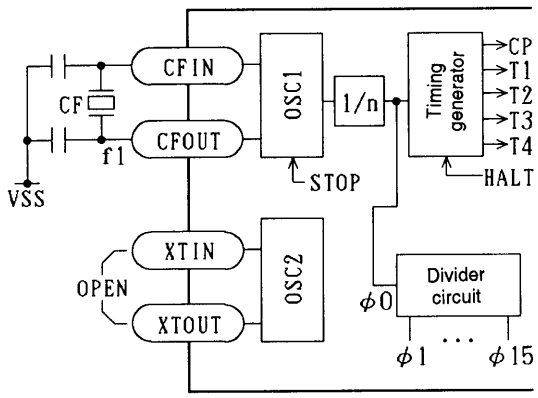
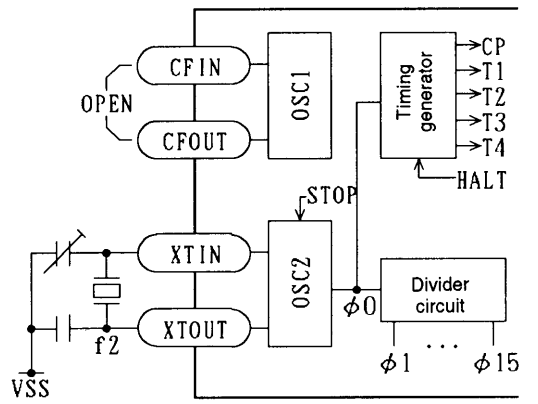
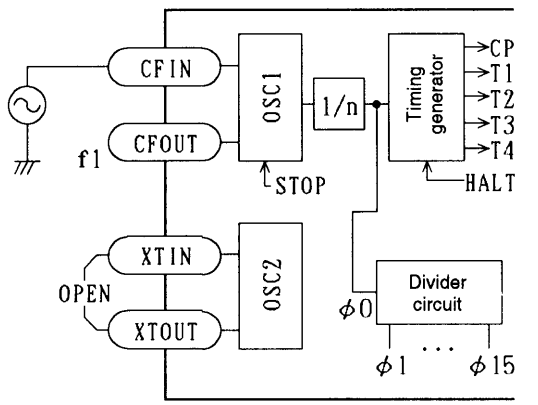
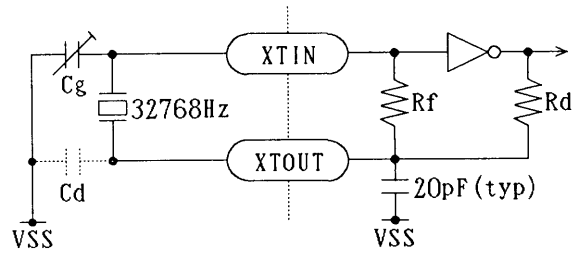
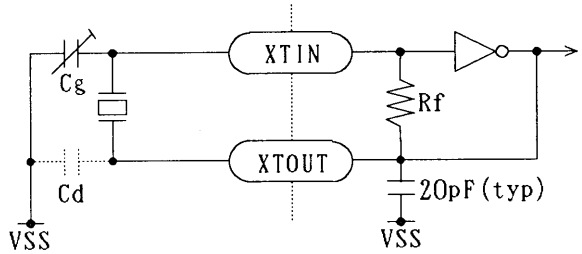
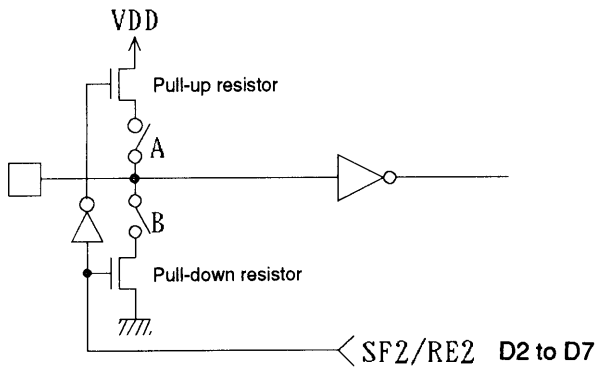
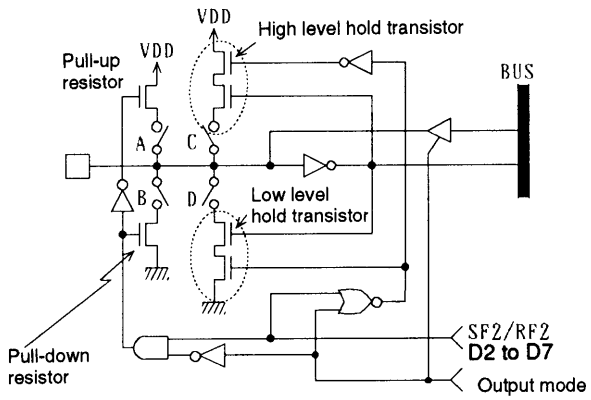
Option	Circuit configuration	Note
CF • 400 kHz • 4 MHz		• The cycle time is four times n times the f1 period. (Note: n is 2.) • The divider outputs (ø1 to ø15) are used as the LCD drive waveform generation clock, the S and K port chattering rejection clock and for other functions.
Xtal		• The cycle time is four times the f2 period. • The divider outputs (ø1 to ø15) are used as the time base, the LCD drive waveform generation clock, the S and K port chattering rejection clock and for other functions.
External input		• The cycle time is four times n times the f1 period. (Note: n is 2.) • The divider outputs (ø1 to ø15) are used as the LCD drive waveform generation clock, the S and K port chattering rejection clock and for other functions.

Crystal Oscillator Circuit Options

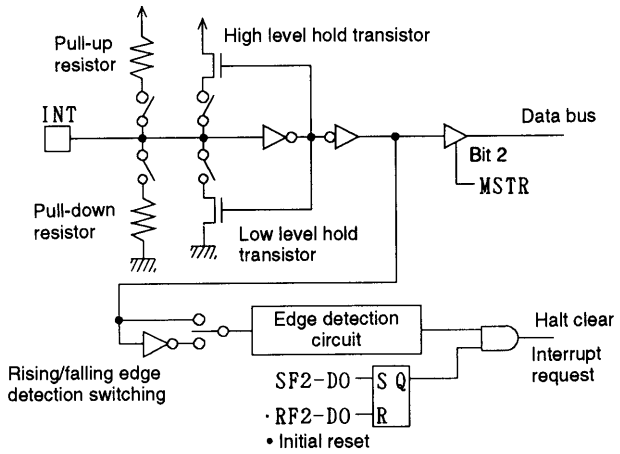
Option	Circuit configuration	Note
32 kHz oscillator		The resistor Rd (200 kΩ typical) for use with a 32 kHz oscillator is built in.
5 kHz oscillator 38 kHz oscillator		• The cycle time is four times n times the f1 period. (Note: n is 2.) • The divider outputs (ø1 to ø15) are used as the time base, the LCD drive waveform generation clock, the S and K port chattering rejection clock and for other functions. • OSC1 is stopped when a SLOW instruction is executed.

Input Port Options

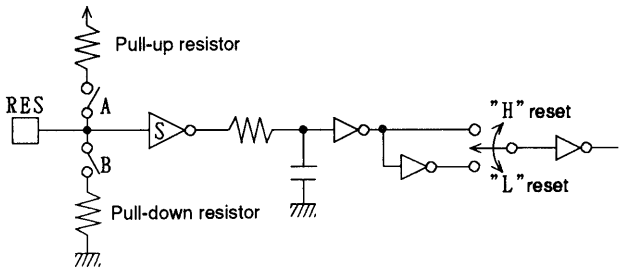
Option	Circuit configuration	Note
Selection of either the • Built-in pull-up resistor, or the • Built-in pull-down resistor option		The following ports are switched at the same time • S1 to S4, K1 to K4, M1 to M4, P1 to P4 SO1 to SO4 and A1 to A4 At reset: The resistors are on during the reset period. The resistors are turned off when reset is cleared. Options: Either A or B can be selected. One of A and B must be selected.
Selection of high or low level hold transistor	 Combination examples	When the hold transistors used option is selected: • Used to reduce the current flowing in the pull-up or pull-down resistors when, for example, a push switch is used for S1 or a slide switch is used for S2. • For input open specification versions, the resistors are turned on before the input is read, the input state is read and then the resistors are turned off. If the input is floating at this point the high or low level hold transistor operates to hold the value read. When the hold transistors unused option is selected: • Use with the pull-up or pull-down resistor in the on state. • Select hold transistors unused when connecting to external control signals and the connections will never be floating

Type	1	2	3	4
Pull-up resistor (A)	On	On		
Pull-down resistor (B)			On	On
High level hold transistor (C)	On			
Low level hold transistor (D)			On	

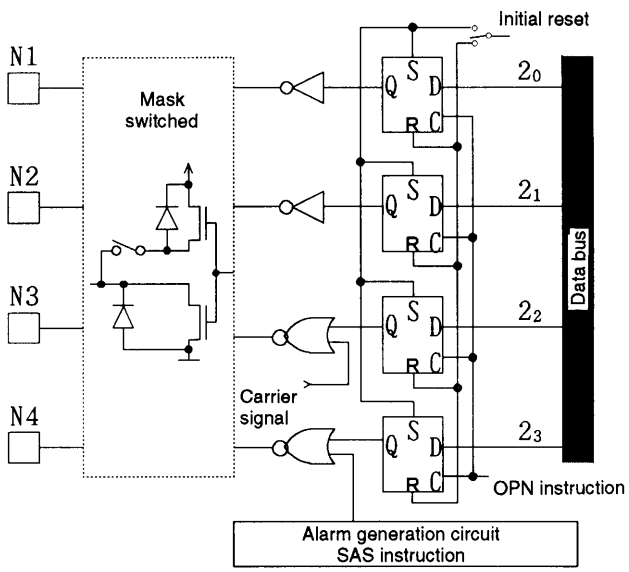
INT Pins

Option	Circuit configuration	Note
Pull-up resistor, pull-down resistor or resistor open selection		Built-in resistor selection • Pull-up resistor used • Pull-down resistor used • Used open
High or low level hold transistor selection		Input signal level hold transistor selection • High level hold transistor used • Low level hold transistor used • Level hold transistors unused
Rising edge or falling edge detection selection		Signal change edge detection switching • Change on rising signal • Change on falling signal

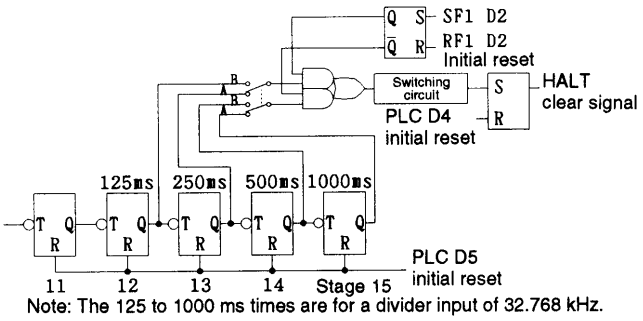
RES Pin

Option	Circuit configuration	Note
Pull-up resistor, pull-down resistor or resistor open and reset level selection		Built-in resistor and polarity selection • Pull-up resistor connected, low level reset • Pull-down resistor connected, high level reset • Resistors open, low level reset • Resistors open, high level reset

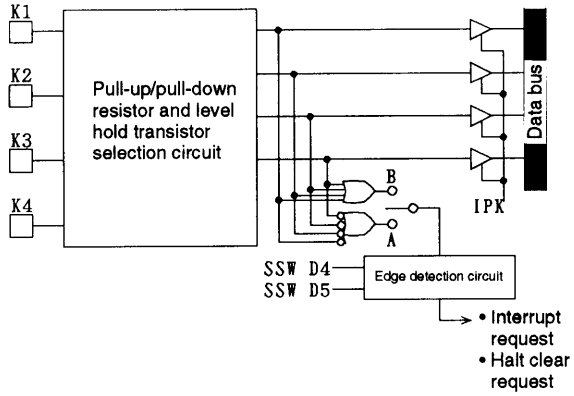
Pins N1 to N4

Option	Circuit configuration	Note
N-channel/CMOS selection		• Selection of CMOS or n-channel open drain circuit type • Pins N1 to N4 can be specified independently • The output level during reset can be specified. — High level — Low level

Fifteen-Stage Divider Overflow Time

Option	Circuit configuration	Note
• 1000 ms/250 ms • 500 ms/125 ms	 Note: The 125 to 1000 ms times are for a divider input of 32.768 kHz.	A 15-stage (15-bit) divider is provided on chip to count the reference time. One of two types of divider overflow detection can be selected as a mask option and a further selection of two types can be made under program control. One of these mask options must be specified.

K Input Port Options

Option	Circuit configuration	Note
Pull-up/pull-down resistor selection		When the pull-up/pull-down resistor selection is made, the K port input detection switching gate is switched accordingly. A: When all of K1 to K4 are high and even one pin goes low a signal is applied to the edge detection circuit. (Applies to the pull-up specifications.) Note: When even one of the K1 to K4 pins is low, the edge detection circuit will not operate for any combination of high or low values on the other pins. B: The opposite of item A

Mask Option Overview

1. Port resistor selection (ports S, K, P, M, A and SO)
   - Pull-up resistor specification
   - Pull-down resistor specification

2. S port high or low level hold transistors
   - Level hold transistors used
   - No level hold transistors

3. K port high or low level hold transistors
   - Level hold transistors used
   - No level hold transistors

4. M port high or low level hold transistors
   - Level hold transistors used
   - No level hold transistors

5. P port high or low level hold transistors
   - Level hold transistors used
   - No level hold transistors

6. A port high or low level hold transistors
   - Level hold transistors used
   - No level hold transistors

7. SO port high or low level hold transistors
   - Level hold transistors used
   - No level hold transistors

8. INT pin resistor selection and signal edge selection
   - Pull-up resistor (negative edge)
   - Pull-down resistor (positive edge)
   - Open (negative edge)
   - Open (positive edge)

9. INT pin level hold transistor selection
   - Low or high level hold transistors used
   - No low or high level hold transistors

10. RES pin
    - Pull-up resistor (low level reset)
    - Pull-down resistor (high level reset)
    - Open (low level reset)
    - Open (high level reset)

11. N1 pin
    - N-channel open drain type
    - CMOS type

12. N2 pin
    - N-channel open drain type
    - CMOS type

13. N3 pin
    - N-channel open drain type
    - CMOS type

14. N4 pin
    - N-channel open drain type
    - CMOS type

15. N port initial level
    - High level
    - Low level

16. OSC specifications
    - CF only (ceramic filter)
    - RC only (resistor and capacitor oscillator)
    - Crystal only (32 to 65 kHz crystal oscillator)
    - CF + crystal
    - RC + crystal
    - External + crystal

17. CF/External
    - 400 kHz or 800 kHz
    - 1 MHz, 2 MHz or 4 MHz

18. Crystal oscillator
    - 32 kHz
    - 65 kHz
    - 38 kHz

19. Fifteen-bit counter overflow
    - ø0/2048 or ø/8192
    - ø0/4096 or ø0/16384

20. Serial I/O internal clock period
    - Cycle time × 1 × 2
    - Cycle time × 2 × 2
    - Cycle time × 4 × 2

21. LCD driver
    - Static
    - 1/2 bias – 1/2 duty
    - 1/2 bias – 1/3 duty
    - 1/2 bias – 1/4 duty
    - 1/3 bias – 1/3 duty
    - 1/3 bias – 1/4 duty

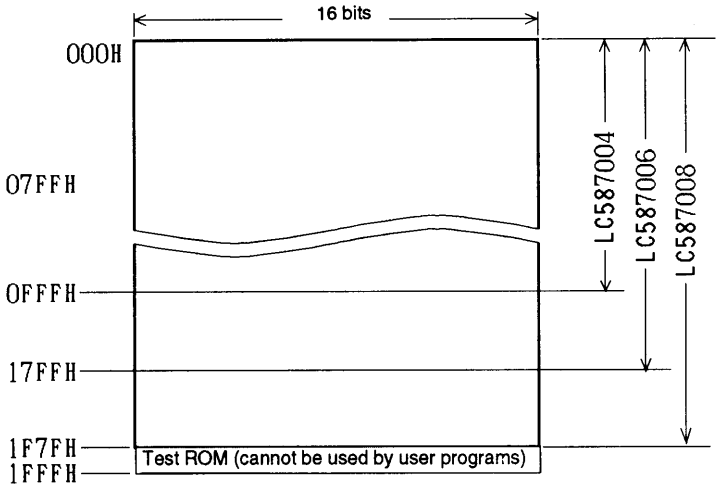
22. LCD alternating frequency
    - Slow
    - Typical
    - Fast

23. Internal reset circuit
    - Selection
    - Disabled

24. Segment ports at reset
    LCD drive pins
    - All on
    - All off

    CMOS, p/n-channel type pins
    - High level

Internal Register Functions

<table>
<tr><th>Symbol</th><th>R/W</th><th>Function</th><th>Initialization value at reset</th></tr>
<tr><td>PC</td><td>—</td><td>
Program counter
The PC is a 13-bit counter that indicates the address in program memory (ROM) of the next instruction to execute. Normally the PC is incremented on every instruction cycle in the range 000H to 1F7FH. (Addresses in the range 1F80 to 1FFF are reserved for testing and cannot be used by user programs.) However, data values are loaded into the PC by the execution of branch and subroutine instructions and on the occurrence of interrupts or an initial reset. The table below describes the data loaded for these operations.
<table>
<tr><th>Operation \ PC</th><th>PC12</th><th>PC11</th><th>PC10</th><th>PC9</th><th>PC8</th><th>PC7</th><th>PC6</th><th>PC5</th><th>PC4</th><th>PC3</th><th>PC2</th><th>PC1</th><th>PC0</th></tr>
<tr><td>Initializing reset</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>INT pin external interrupt</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>S/K pin external interrupt</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Timer 1 or timer 2 internal interrupt</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Serial counter internal interrupt or SO4 pin external interrupt</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Unconditional jump (JMP)</td><td colspan="2">Page</td><td>P10</td><td>P9</td><td>P8</td><td>P7</td><td>P6</td><td>P5</td><td>P4</td><td>P3</td><td>P2</td><td>P1</td><td>P0</td></tr>
<tr><td>Conditional jump (BAB0, BAB1, BAB2, BAB3, BAZ, BANZ, BCH, BCNH)</td><td colspan="2">Page</td><td>P10</td><td>P9</td><td>P8</td><td>P7</td><td>P6</td><td>P5</td><td>P4</td><td>P3</td><td>P2</td><td>P1</td><td>P0</td></tr>
<tr><td>Call instruction (CALL)</td><td colspan="2">Page</td><td>P10</td><td>P9</td><td>P8</td><td>P7</td><td>P6</td><td>P5</td><td>P4</td><td>P3</td><td>P2</td><td>P1</td><td>P0</td></tr>
<tr><td>Return instruction (RTS, RTSR)</td><td colspan="12">CALL address + 1</td></tr>
</table>
Page: the ROM page flags, which take 2048 locations as a single page
The page is specified with the MROPF and SROPF instructions.
P00 to P10: Bits in the instruction code (i.e., immediate data)
</td><td></td></tr>
<tr><td>ROM</td><td>R/O</td><td>
Program memory
The ROM memory consists of 4096 x 16 bits (4 kwords or 8 kbytes) in the LC587004, 6144 x 16 bits (6 kwords or 12 kbytes) in the LC587006 and 8064 x 16 bits (8 kwords or 16 kbytes) in the LC587008. ROM hold user programs to be executed.


</td><td></td></tr>
<tr><td>RAM</td><td>R/W</td><td>
Data memory
These microprocessors provide an on-chip RAM that consists of 512 × 4 bits (2 Kb). This RAM is accessed as two 256 × 4-bit pages.
RAM addresses can be specified in four ways as listed below.
• Directly specified at 00H to FFH (immediate addressing)
• Indirect specification using the 8-bit data pointer.
• Indirect specification by the 4-bit RAM bank register multiplied by 10H plus immediate data in the range 0 to FH.
• Indirect specification by the 4-bit RAM bank register multiplied by 10H plus 8H plus immediate data in the range 0 to FH.
Writing to RAM is always performed through the accumulator.
</td><td>Undefined</td></tr>
</table>

Continued on next page.

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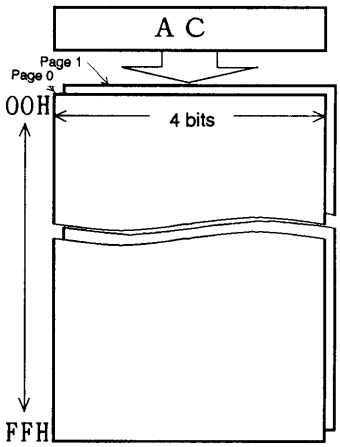
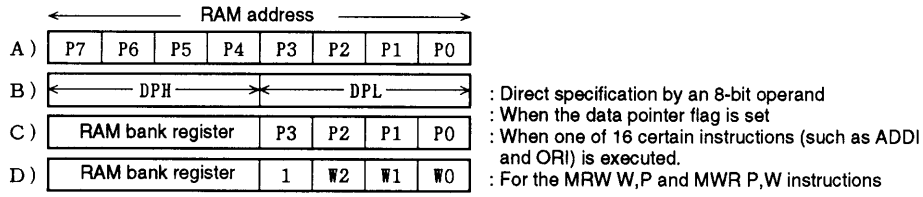
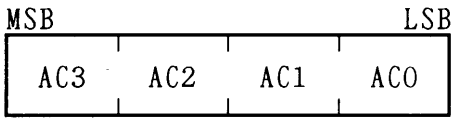
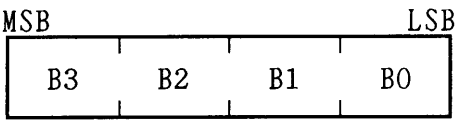
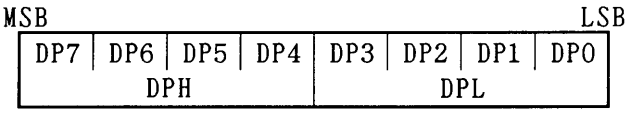
<table>
<tr><th>Symbol</th><th>R/W</th><th>Function</th><th>Initialization value at reset</th></tr>
<tr><td>RAM</td><td>R/W</td><td>




: Direct specification by an 8-bit operand
: When the data pointer flag is set
: When one of 16 certain instructions (such as ADDI and ORI) is executed.
: For the MRW W,P and MWR P,W instructions

Note: In case B, data pointer RAM address specification is illegal if the RAM address specification (the DPH immediate data) has the same value as the RAM bank register (BNK). In this case immediate specification is allowed.
Example: If an IPS 10H instruction is executed when the data pointer flag is set, DPH is 5H, DPL is 3 H and the RAM bank register (BNK) is 1H, then the contents of the S port will be written to RAM location 10H.
Example: If BNK and DPH differ, then the following operation will be performed.
If an IPS 10H instruction is executed when DPF is 1, DPH is 5, DPL is 3 and BNK is 4, then the contents of the S port will be written to RAM location 53H.
</td><td>Undefined</td></tr>
<tr><td>AC</td><td>R/W</td><td>Accumulator


</td><td>Undefined</td></tr>
<tr><td>B</td><td>R/W</td><td>B register


This register is used in combination with RAM as a pair for output to the LCD ports and for timer 2, serial counter and data pointer I/O.
</td><td>Undefined</td></tr>
<tr><td>DP</td><td>R/W</td><td>Data pointer


The data pointer register functions as a data pointer when the data pointer flag (DPF) is set, allowing control of the on-chip RAM.
</td><td>Undefined</td></tr>
</table>

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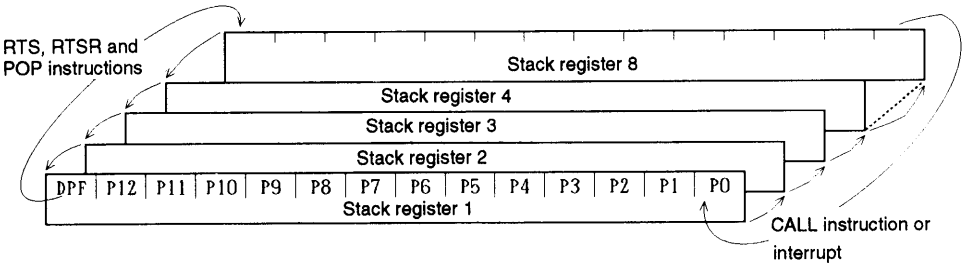
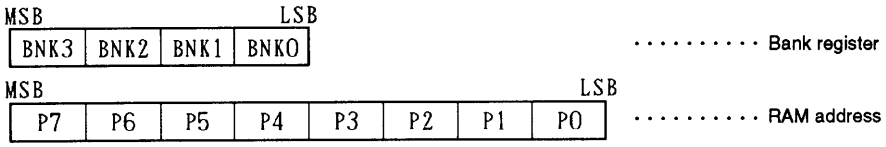
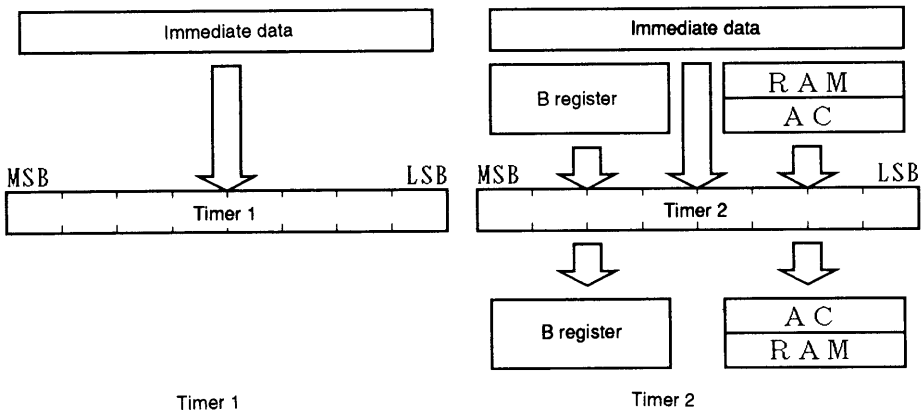
Symbol	R/W	Function	Initialization value at reset
STACK	R/W	Stack pointer The stack consists of eight 14-bit registers and thus can be set to a depth of up to eight levels. The stack pointer is incremented by CALL instructions and interrupts, and decremented by RTS, RTSR and POP instructions.  P0 to P11: Program counter (PC) DPF: Data pointer flag	01H
BNK	R/W	Bank register The bank register is a 4-bit register that divides RAM (from 00H to FFH) into 16 sections and is used in moving RAM data, immediate operations and setting the data pointer.  Example: ADD*_5,10.....If BNK is 6 then the operation performed will be: RAM(65H) + 10 → AC → RAM(65H).	00H
APG	R/W	RAM page flags The RAM page flags consist of 2 bits that allow RAM to be expanded in 256 4-bit pages to a total of 1024 4-bit locations. Note: Pages 2 and 3 cannot be used by the LC587004, LC587006 and LC587008.	00H
TIM TIM1 TIM2	R/W	Timer counters The timers consist of 8-bit down counters. (timer 1 and timer 2) Timer setting is performed in 8-bit units for immediate data. (timer 1 and timer 2) Reading and writing the lower 4 bits of a timer counter is performed through a RAM location. (timer 2 only) Reading and writing the upper 4 bits of a timer counter is performed using the B register. (timer 2 only)  	Undefined

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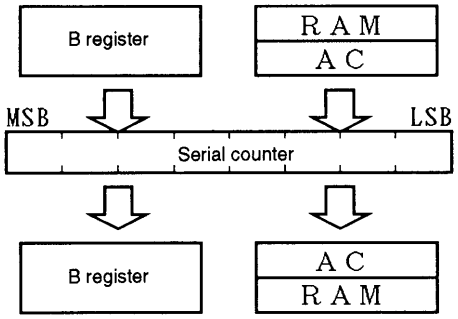
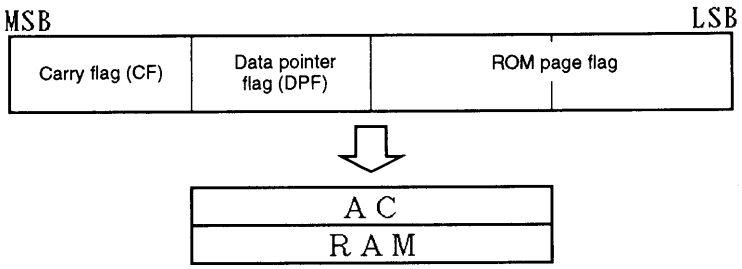
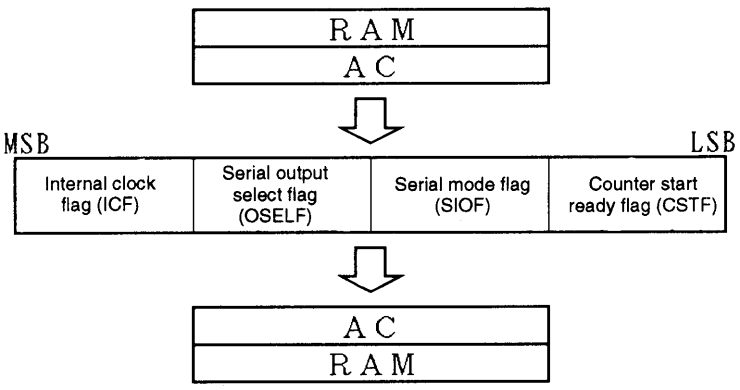
<table>
<tr><th>Symbol</th><th>R/W</th><th>Function</th><th>Initialization value at reset</th></tr>
<tr><td>SIO</td><td>R/W</td><td>Serial counter
The serial counter is an 8-bit shift register.
Reading and writing the lower 4 bits of the serial counter is performed through a RAM location.
Reading and writing the upper 4 bits of the serial counter is performed using the B register.
 
</td><td>Undefined</td></tr>
<tr><td>OPG</td><td>R/W</td><td>ROM page flags
The ROM page flags consist of 2 bits that allow ROM to be expanded in 2048 16-bit pages to a total of 8063 16-bit locations.
In the LC587004 the legal values are 0 and 1, in the LC587006 the legal values are 0 to 2 and in the LC587008 the legal values are 0 to 3.
(The operation when an illegal value is used is undefined.)</td><td>00H</td></tr>
<tr><td>STS1</td><td>R/O</td><td>Status register 1 (STS1)
Status register 1 is a 4-bit register whose bits are used as shown below.
 
</td><td>00H</td></tr>
<tr><td>STS2</td><td>R/W</td><td>Status register 2 (STS2)
Status register 2 is a 4-bit register that is used for serial counter control and state confirmation.
 

ICF: High when the internal clock is used
OSELF: High when the SO2 pin is set to the high impedance state (Z).
Low when SO2 is set to the CMOS or n-channel open drain state.
SIOF: High when used as serial I/O
CSTF: High on serial counter start
Low during serial counter operation</td><td>00H</td></tr>
</table>

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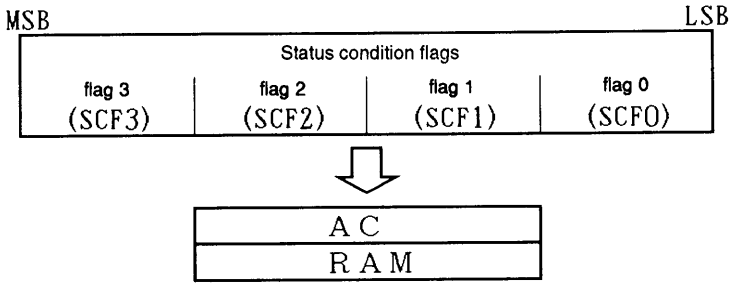
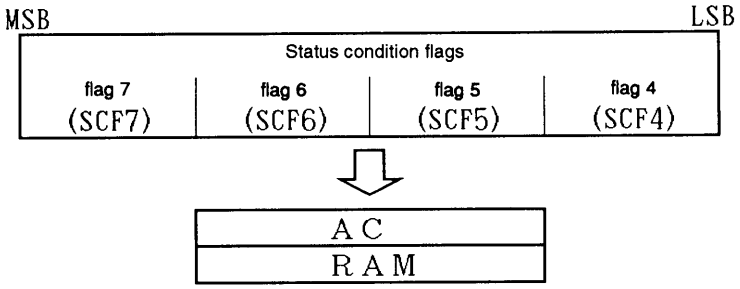
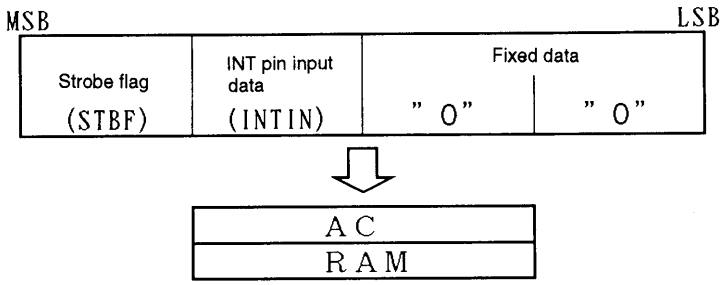
Symbol	R/W	Function	Initialization value at reset
STS3	R/O	Status register 3 (STS3) Status register 3 is a 4-bit register that is used to confirm the HALT and STOP clear conditions.  SCF0: Set to 1 if there was a signal change on the INT pin. SCF1: Set to 1 if there was a signal change on the K port. SCF2: Set to 1 if any of the flags in STS4 is set. SCF3: Set to 1 if there was a signal change on the S port. Note: SCF0 is used when enabled by an SF2-1 instruction. SCF1 and SCF3 are used when enabled by an SSW instruction.	00H
STS4	R/O	Status register 4 (STS4) Status register 4 is a 4-bit register that is used to confirm the HALT and STOP clear conditions.  SCF4: Divider overflow SCF5: Timer 1 underflow SCF6: Timer 2 underflow SCF7: Serial counter overflow or signal change on SO4	00H
STS5	R/O	Status register 5 (STS5) Status register 5 is a 4-bit register whose bits are used as shown below.  Bits 0 and 1: These bits are always 0 and cannot be used. INTIN: Reflects in the input data on the INT pin. STBF: Strobe flag for the segment port (Set to 1 for 00 to 0F and to 0 for 10 to 1E.)	00H

Specifications

The electrical characteristics specified here are provisional and subject to change.

Absolute Maximum Ratings at V_{SS} = 0 V, Ta = 25°C

Parameter	Symbol	Conditions	min	typ	max	Unit
Maximum supply voltage	V_{DD}		–0.3		+7.0	V
	$V_{DD}1$		–0.3		V_{DD}	V
	$V_{DD}2$		–0.3		V_{DD}	V
Maximum input voltage	V_I (1)	Allowed in the specified circuit (Figure 1), XTIN, CFIN	Allowed up to the generated voltage			
	V_I (2)	S1 to S4, K1 to K4, P1 to P4, SO1 to SO4, A1to A4,RES, INT, TST, (With the K, P, M, SO and ports in input mode)	–0.3		V_{DD} + 0.3	V
Maximum output voltage	V_O (1)	Allowed in the specified circuit (Figure 1), XTOUT, CFOUT	Allowed up to the generated voltage			
	V_O (2)	K1 to K4, P1 to P4, SO1 to SO4, A1 to A4, N1 to N4, CUP1, CUP2, Seg1 to Seg35, COM1 to COM4 (With the K, P, M, SO and A ports in output mode)	–0.3		V_{DD} + 0.3	V
	V_O (3)	Open drain specifications, N1 to N4 (N ch)	–0.3		+13	V
Output pin current	I_O (1)	Per pin: N1 to N4	0		+15	mA
	I_O (2)		–10		0	mA
	I_O (3)	Per pin: K1 to K4, P1 to P4, M1 to M4, SO1 to SO4, A1 to A4	0		5	mA
	I_O (4)		–5		0	mA
	ΣI_O (1)	Total current for all pins: K1 to K4, P1 to P4, M1 to M4, SO1 to SO4, A1 to A4, N1 to N4, Seg1 to Seg35			70	mA
	ΣI_O (2)		–70			mA
Allowable power dissipation	Pd max	QIP80 flat package			500	mW
Operating temperature	Topg		–30		+70	°C
Storage temperature	Tstg		–55		+125	°C

Allowable Operating Ranges at V_{SS} = 0 V, Ta = –30 to +70°C

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}	LCD unused specifications: $V_{DD}1 = V_{DD}2 = V_{DD}$	2.0		6.0	V
		Static specifications: $V_{DD}1 = V_{DD}2 = V_{DD}$	2.0		6.0	V
		1/2 bias specifications: $V_{DD}1 = V_{DD}2 \approx 2 \times 1/2\ V_{DD}$	2.8		6.0	V
		1/3 bias specifications: $V_{DD}1 \approx 2 \times 1/3\ V_{DD}$, $V_{DD}2 \approx 1/3\ V_{DD}$	2.8		6.0	V
Hold supply voltage	V_{HD}	Voltage required to hold the contents of RAM and the registers*	2.0		V_{DD}	V
Input high level voltage	$V_{IH}1$	S1 to S4, K1 to K4, P1 to P4, M1 to M4, SO1 to SO4, A1 to A4, INT, (With the K, P, M, SO and ports in input mode)	0.7 V_{DD}		V_{DD}	V
Input low level voltage	$V_{IL}1$		0		0.3 V_{DD}	V
Input high level voltage	$V_{IH}2$	RES pin	0.75 V_{DD}		V_{DD}	V
Input low level voltage	$V_{IL}2$		0		0.25 V_{DD}	V
Input high level voltage	$V_{IH}3$	CFIN pin	0.75 V_{DD}		V_{DD}	V
Input low level voltage	$V_{IL}3$		0		0.25 V_{DD}	V
Operating frequency 1	fopg1	V_{DD} = 2.0 to 6.0 V, 32 kHz; XTIN/XTOUT crystal oscillator	32		33	kHz
Operating frequency 2	fopg2	V_{DD} = 2.2 to 6.0 V. 38 kHz; XTIN/XTOUT crystal oscillator	37		39	kHz
Operating frequency 3	fopg3	V_{DD} = 2.2 to 6.0 V, 65 kHz; XTIN/XTOUT crystal oscillator	60		70	kHz
Operating frequency 4	fopg4	V_{DD} = 2.2 to 6.0 V; CFIN/CFOUT CF specifications	190		810	kHz
Operating frequency 5	fopg5	V_{DD} = 2.5 to 6.0 V; CFIN/CFOUT CF specifications	190		1200	kHz
Operating frequency 6	fopg6	V_{DD} = 2.5 to 6.0 V; CFIN/CFOUT CF specifications	190		2300	kHz
Operating frequency 7	fopg7	V_{DD} = 2.8 to 6.0 V; CFIN/CFOUT CF specifications	190		4200	kHz
Operating frequency 8	fopg8	V_{DD} = 4.0 to 6.0 V, CFIN/CFOUT RC specifications	100		1500	kHz
Operating frequency 9	fopg9	V_{DD} = 2.0 to 6.0 V, CFIN/CFOUT EXT specifications	190		800	kHz
Operating frequency 10	fopg10	V_{DD} = 3.0 to 6.0 V, O1/SO3 pins (in serial mode), Rising and falling edges on the input signals and clock waveform of the SO1/SO3 pins (in serial mode) must be 10 µs or less.	DC		200	kHz

Note: In the state where the CF/RC oscillator and/or the crystal oscillator are completely stopped and the internal circuits are completely stopped.

Electrical Characteristics at V_{DD} = 2.5 to 3.2 V, V_{SS} = 0 V, Ta = –30 to +70°C

Parameter	Symbol	Conditions		min	typ	max	Unit
Input resistance	R_{IN}1 A	V_{IN} = 0.2 V_{DD}, low level hold transistor* Figure 2		60	300	1200	kΩ
	R_{IN}1 B	V_{IN} = V_{DD}, pull-down resistor* Figure 2		30	150	500	kΩ
	R_{IN}1 C	V_{IN} = 0.8 V_{DD}, high level hold transistor* Figure 2		60	300	1200	kΩ
	R_{IN}1 D	V_{IN} = V_{SS}, pull-up resistor* Figure 2		30	150	500	kΩ
	R_{IN}2 A	V_{IN} = 0.2 V_{DD}, the INT pin low level hold transistor		60	300	1200	kΩ
	R_{IN}2 B	V_{IN} = V_{DD}, The INT pin pull-down resistor		300	1500	5000	kΩ
	R_{IN}2 C	V_{IN} = 0.8 V_{DD}, the INT pin high level hold transistor		60	300	1200	kΩ
	R_{IN}2 D	V_{IN} = V_{SS}, the INT pin pull-up resistor		300	1500	5000	kΩ
	R_{IN}3	V_{IN} = V_{DD}, the RES pin pull-down resistor		10	30	50	kΩ
	R_{IN}4	V_{IN} = V_{SS}, the RES pin pull-up resistor		10	30	50	kΩ
	R_{IN}5	V_{IN} = V_{DD}, the TST pin pull-down resistor		60	250	1000	kΩ
	R_{IN}1 A	V_{IN} = 0.2 V_{DD}, low level hold transistor* Figure 2	V_{DD} = 2.5 V	80	300	1200	kΩ
	R_{IN}1 B	V_{IN} = V_{DD}, pull-down resistor* Figure 2		40	150	500	kΩ
	R_{IN}1 C	V_{IN} = 0.8 V_{DD}, high level hold transistor* Figure 2		80	300	1200	kΩ
	R_{IN}1 D	V_{IN} = V_{SS}, pull-up resistor* Figure 2		40	150	500	kΩ
	R_{IN}2 A	V_{IN} = 0.2 V_{DD}, the INT pin low level hold transistor		80	300	1200	kΩ
	R_{IN}2 B	V_{IN} = V_{DD}, the INT pin pull-down resistor		400	1500	5000	kΩ
	R_{IN}2 C	V_{IN} = 0.8 V_{DD}, the INT pin high level hold transistor		80	300	1200	kΩ
	R_{IN}2 D	V_{IN} = V_{SS}, the INT pin pull-up resistor		400	1500	5000	kΩ
	R_{IN}3	V_{IN} = V_{DD}, the RES pin pull-down resistor		10	30	50	kΩ
	R_{IN}4	V_{IN} = V_{SS}, the RES pin pull-up resistor		10	30	50	kΩ
	R_{IN}5	V_{IN} = V_{DD}, the TST pin pull-down resistor		80	250	1000	kΩ
Output high level voltage	V_{OH} (1)	I_{OH} = –500 µA	N1 to N4	V_{DD} – 0.5			V
Output low level voltage	V_{OL} (1)	I_{OL} = 1.0 mA				0.5	V
Output high level voltage	V_{OH} (2)	I_{OH} = –400 µA	K1 to K4, P1 to P4, M1 to M4, SO1 to SO4, A1 to A4 (with the K, P, M, SO and A ports in output mode)	V_{DD} – 0.5			V
Output low level voltage	V_{OL} (2)	I_{OL} = 400 µA				0.5	V
Output off leakage current	$\lvert I_{OFF} \rvert$	V_{OH} = 10.5 V	N1 to 4 (open specifications), Figure 10			1.0	µA
Segment port output impedances [In CMOS output port mode]							
Output high level voltage	V_{OH} (3)	I_{OH} = –100 µA	Seg1 to Seg35	V_{DD} – 0.5			V
Output low level voltage	V_{OL} (3)	I_{OL} = 100 µA				0.5	V
[In p-channel open-drain output port mode (See Figure 11.)]							
Output high level voltage	V_{OH} (3)	I_{OH} = –100 µA	Seg1 to Seg35	V_{DD} – 0.5			V
Output off leakage current	$\lvert I_{OFF} \rvert$	V_{OL} = V_{SS}				1.0	µA
[In n-channel open-drain output port mode (See Figure 11.)]							
Output low level voltage	V_{OL} (3)	I_{OL} = 100 µA	Seg1 to Seg35			0.5	V
Output off leakage current	$\lvert I_{OFF} \rvert$	V_{OH} = V_{DD}				1.0	µA
[Static drive]							
Output high level voltage	V_{OH} (4)	I_{OH} = –20 µA, Seg1 to Seg35		V_{DD} – 0.2			V
Output low level voltage	V_{OL} (4)	I_{OL} = 20 µA				0.2	V
Output high level voltage	V_{OH} (5)	I_{OH} = –100 µA, COM1		V_{DD} – 0.2			V
Output low level voltage	V_{OL} (5)	I_{OL} = 100 µA				0.2	V

Note: For the 24 pins S1 to S4, K1 to K4, P1 to P4, M1 to M4, SO1 to SO4 and A1 to A4.

Electrical Characteristics at V_{DD} = 3.0 to 4.5 V, V_{SS} = 0 V, Ta = –30 to +70°C

Parameter	Symbol	Conditions		min	typ	max	Unit
Input resistance	R_{IN}1 A	V_{IN} = 0.2 V_{DD}, low level hold transistor* Figure 2		35	200	800	kΩ
	R_{IN}1 B	V_{IN} = V_{DD}, pull-down resistor* Figure 2		15	80	300	kΩ
	R_{IN}1 C	V_{IN} = 0.8 V_{DD}, high level hold transistor* Figure 2		35	200	800	kΩ
	R_{IN}1 D	V_{IN} = V_{SS}, pull-up resistor* Figure 2		15	80	300	kΩ
	R_{IN}2 A	V_{IN} = 0.2 V_{DD}, the INT pin low level hold transistor		35	200	800	kΩ
	R_{IN}2 B	V_{IN} = V_{DD}, The INT pin pull-down resistor		150	800	3000	kΩ
	R_{IN}2 C	V_{IN} = 0.8 V_{DD}, the INT pin high level hold transistor		35	200	800	kΩ
	R_{IN}2 D	V_{IN} = V_{SS}, the INT pin pull-up resistor		150	800	3000	kΩ
	R_{IN}3	V_{IN} = V_{DD}, the RES pin pull-down resistor		10	30	50	kΩ
	R_{IN}4	V_{IN} = V_{SS}, the RES pin pull-up resistor		10	30	50	kΩ
	R_{IN}5	V_{IN} = V_{DD}, the TST pin pull-down resistor		25	130	500	kΩ
	R_{IN}1 A	V_{IN} = 0.2 V_{DD}, low level hold transistor* Figure 2	V_{DD} = 3.0 to 4.0 V	40	200	800	kΩ
	R_{IN}1 B	V_{IN} = V_{DD}, pull-down resistor* Figure 2		20	80	300	kΩ
	R_{IN}1 C	V_{IN} = 0.8 V_{DD}, high level hold transistor* Figure 2		40	200	800	kΩ
	R_{IN}1 D	V_{IN} = V_{SS}, pull-up resistor* Figure 2		20	80	300	kΩ
	R_{IN}2 A	V_{IN} = 0.2 V_{DD}, the INT pin low level hold transistor		40	300	800	kΩ
	R_{IN}2 B	V_{IN} = V_{DD}, the INT pin pull-down resistor		200	800	3000	kΩ
	R_{IN}2 C	V_{IN} = 0.8 V_{DD}, the INT pin high level hold transistor		40	200	1200	kΩ
	R_{IN}2 D	V_{IN} = V_{SS}, the INT pin pull-up resistor		200	800	3000	kΩ
	R_{IN}3	V_{IN} = V_{DD}, the RES pin pull-down resistor		10	30	50	kΩ
	R_{IN}4	V_{IN} = V_{SS}, the RES pin pull-up resistor		10	30	50	kΩ
	R_{IN}5	V_{IN} = V_{DD}, the TST pin pull-down resistor		30	130	500	kΩ
Output high level voltage	V_{OH} (1)	I_{OH} = –500 µA	N1 to N4	V_{DD} – 0.5			V
Output low level voltage	V_{OL} (1)	I_{OL} = 1.0 mA				0.5	V
Output high level voltage	V_{OH} (2)	I_{OH} = –400 µA	K1 to K4, P1 to P4, M1 to M4, SO1 to SO4, A1 to A4 (with the K, P, M, SO and A ports in output mode)	V_{DD} – 0.5			V
Output low level voltage	V_{OL} (2)	I_{OL} = 400 µA				0.5	V
Output off leakage current	$\lvert I_{OFF} \rvert$	V_{OH} = 10.5 V	N1 to 4 (open specifications), Figure 10			1.0	µA
Segment port output impedances [In CMOS output port mode]							
Output high level voltage	V_{OH} (3)	I_{OH} = –100 µA	Seg1 to Seg35	V_{DD} – 0.5			V
Output low level voltage	V_{OL} (3)	I_{OL} = 100 µA				0.5	V
[In p-channel open-drain output port mode (See Figure 11.)]							
Output high level voltage	V_{OH} (3)	I_{OH} = –100 µA	Seg1 to Seg35	V_{DD} – 0.5			V
Output off leakage current	$\lvert I_{OFF} \rvert$	V_{OL} = V_{SS}				1.0	µA
[In n-channel open-drain output port mode (See Figure 11.)]							
Output low level voltage	V_{OL} (3)	I_{OL} = 100 µA	Seg1 to Seg35			0.5	V
Output off leakage current	$\lvert I_{OFF} \rvert$	V_{OH} = V_{DD}				1.0	µA
[Static drive]							
Output high level voltage	V_{OH} (4)	I_{OH} = –20 µA, Seg1 to Seg35		V_{DD} – 0.2			V
Output low level voltage	V_{OL} (4)	I_{OL} = 20 µA				0.2	V
Output high level voltage	V_{OH} (5)	I_{OH} = –100 µA, COM1		V_{DD} – 0.2			V
Output low level voltage	V_{OL} (5)	I_{OL} = 100 µA				0.2	V
[1/2 bias drive]							
Output high level voltage	V_{OH} (4)	I_{OH} = –20 µA	Seg1 to Seg35	V_{DD} – 0.2		0.2	V
Output low level voltage	V_{OL} (4)	I_{OL} = 20 µA					
Output high level voltage	V_{OH} (5)	I_{OH} = –100 µA	COM1 to COM4	V_{DD} – 0.2			V
Output middle level voltage	V_{OM}	I_{OH} = –100 µA I_{OL} = 100 µA		V_{DD}/2 – 0.2		V_{DD}/2 + 0.2	V
Output low level voltage	V_{OL} (5)	I_{OL} = 100 µA				0.2	V

Note: For the 24 pins S1 to S4, K1 to K4, P1 to P4, M1 to M4, SO1 to SO4 and A1 to A4.

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Parameter	Symbol	Conditions		min	typ	max	Unit
[1/3 bias drive: About 1/10 of the rating for V_{DD} = 4.5 to 6.0 V]							
Supply leakage current	I_{LEK} (1)	V_{DD} = 3.0 V, Ta = 25°C, Figure 3			0.2	1.0	µA
Supply leakage current	I_{LEK} (2)	V_{DD} = 3.0 V, Ta = 50°C, Figure 3			1.0	5.0	µA
Input leakage current	I_{OFF}	V_{DD} = 3.0 V	S1 to S4, K1 to K4, P1 to P4, M1 to M4, SO1 to SO4, A1 to A4, INT, RES (with the K, P, M, SO and A ports in input mode, and with open specifications for the INT and RES pins)				
		V_{IN} = V_{DD}				1.0	µA
		V_{IN} = V_{SS}		–1.0			µA
Output voltage 1	V_{DD}1-(1)	V_{DD} = 3.0 V, C1 = C2 = 0.1 µF, V_{DD}1 = V_O, 1/2 bias, fopg = 32.768 kHz, Figure 4		1.3	1.5	1.7	V
Supply current 1	$\lvert I_{DD} \rvert$ 1-1	V_{DD} = 3.0 V, Ta = 25°C	Crystal oscillator specifications, crystal: 32 kHz, Cg = 20 pF, CI = 25 kΩ, HALT mode, Figure 6, LCD = 1/3 bias		4.0	8.0	µA
	$\lvert I_{DD} \rvert$ 1-2	V_{DD} = 3.0 V, Ta = 50°C				20	µA
Supply current 2	$\lvert I_{DD} \rvert$ 2-1	V_{DD} = 3.0 V, Ta = 25°C	Crystal oscillator specifications, crystal: 38 or 65 kHz, Cg = 10 pF, CI = 25 kΩ, HALT mode, Figure 6, LCD = 1/3 bias		6.0	10	V
	$\lvert I_{DD} \rvert$ 2-2	V_{DD} = 3.0 V, Ta = 50°C				30	µA
Supply current 3	$\lvert I_{DD} \rvert$ 3-1	V_{DD} = 3.0 V, Ta = 25°C	CF oscillator specifications, CF: 400 kHz, Ccg = Ccd = 330 pF, HALT mode, Figure 7		150	300	µA
	$\lvert I_{DD} \rvert$ 3-2	V_{DD} = 3.0 V, Ta = 50°C				500	µA
Oscillator start voltage	$\lvert V_{STT} \rvert$	T_{STT} ≤ 5 s	Crystal oscillator specifications, using a 32 kHz crystal, Cg = 20 pF, CI ≤ 25 kΩ, Figure 6			2.2	V
Oscillator hold voltage	$\lvert V_{HOLD} \rvert$			2.0		6.0	V
Oscillator start time	$\lvert T_{STT} \rvert$	V_{DD} = 2.2 V				5	s
Oscillator stability	Δf	V_{DD} = 2.95 to 3.05 V				3	ppm
Oscillator start voltage	$\lvert V_{STT} \rvert$	T_{STT} ≤ 5 s	Crystal oscillator specifications, using a 38 or 65 kHz crystal, XCg = 10 pF, CI ≤ 25 kΩ, Figure 6			2.4	V
Oscillator hold voltage	$\lvert V_{HOLD} \rvert$			2.2		6.0	V
Oscillator start time	$\lvert T_{STT} \rvert$	V_{DD} = 2.4 V				5	s
Oscillator start voltage	$\lvert V_{STT} \rvert$	T_{STT} ≤ 30 ms	CF oscillator specifications, using a 400 kHz ceramic filter, Ccg = Ccd = 330 pF, Figure 7			2.4	V
Oscillator hold voltage	$\lvert V_{HOLD} \rvert$			2.2		6.0	V
Oscillator start time	$\lvert T_{STT} \rvert$	V_{DD} = 2.4 V				30	ms
Oscillator start voltage	$\lvert V_{STT} \rvert$	T_{STT} ≤ 30 ms	CF oscillator specifications, using an 800 kHz ceramic filter, Ccg = Ccd = 220 pF or 100 pF, Figure 7			2.4	V
Oscillator hold voltage	$\lvert V_{HOLD} \rvert$			2.2		6.0	V
Oscillator start time	$\lvert T_{STT} \rvert$	V_{DD} = 2.4 V				30	ms
Oscillator correction capacitance	Cd	V_{DD} = 3.0 V, XTOUT pin (built-in)		16	20	24	pF

Electrical Characteristics at V_{DD} = 4.5 to 6.0 V, V_{SS} = 0 V, Ta = –30 to +70°C

Parameter	Symbol	Conditions		min	typ	max	Unit
Input resistance	R_{IN}1 A	V_{IN} = 0.2 V_{DD}, low level hold transistor* Figure 2		30	120	500	kΩ
	R_{IN}1 B	V_{IN} = V_{DD}, pull-down resistor* Figure 2		10	50	200	kΩ
	R_{IN}1 C	V_{IN} = 0.8 V_{DD}, high level hold transistor* Figure 2		30	120	500	kΩ
	R_{IN}1 D	V_{IN} = V_{SS}, pull-up resistor* Figure 2		10	50	200	kΩ
	R_{IN}2 A	V_{IN} = 0.2 V_{DD}, the INT pin low level hold transistor		30	120	500	kΩ
	R_{IN}2 B	V_{IN} = V_{DD}, The INT pin pull-down resistor		100	500	2000	kΩ
	R_{IN}2 C	V_{IN} = 0.8 V_{DD}, the INT pin high level hold transistor		30	120	500	kΩ
	R_{IN}2 D	V_{IN} = V_{SS}, the INT pin pull-up resistor		100	500	2000	kΩ
	R_{IN}3	V_{IN} = V_{DD}, the RES pin pull-down resistor		10	30	50	kΩ
	R_{IN}4	V_{IN} = V_{SS}, the RES pin pull-up resistor		10	30	50	kΩ
	R_{IN}5	V_{IN} = V_{DD}, the TST pin pull-down resistor		20	70	300	kΩ
Output high level voltage	V_{OH} (1)	I_{OH} = –5.0 mA	N1 to N4	V_{DD} – 0.5			V
Output low level voltage	V_{OL} (1)	I_{OL} = 10.0 mA				0.5	V
Output high level voltage	V_{OH} (2)	I_{OH} = –1.0 mA	K1 to K4, P1 to P4, M1 to M4, SO1 to SO4, A1 to A4 (with the K, P, M, SO and A ports in output mode), N1 to N4 (open specifications) Figure 10	V_{DD} – 0.5	V_{DD} – 0.2		V
Output low level voltage	V_{OL} (2)	I_{OL} = 2.0 mA			0.2	0.5	V
Output off leakage current	$\lvert I_{OFF} \rvert$	V_{OH} = 10.5 V				1.0	µA
Segment port output impedances [In CMOS output port mode]							
Output high level voltage	V_{OH} (3)	I_{OH} = –500 µA	Seg1 to Seg35	V_{DD} – 0.5	V_{DD} – 0.2		V
Output low level voltage	V_{OL} (3)	I_{OL} = 500 µA				0.5	V
[In p-channel open-drain output port mode (See Figure 11.)]							
Output high level voltage	V_{OH} (4)	I_{OH} = –500 µA	Seg1 to Seg35	V_{DD} – 0.5	V_{DD} – 0.2		V
Output off leakage current	$\lvert I_{OFF} \rvert$	V_{OL} = V_{SS}				1.0	µA
[In N-channel open-drain output port mode (See Figure 11.)]							
Output low level voltage	V_{OL} (4)	I_{OL} = 500 µA	Seg1 to Seg35		0.2	0.5	V
Output off leakage current	$\lvert I_{OFF} \rvert$	V_{OH} = V_{DD}				1.0	µA
[Static drive]							
Output high level voltage	V_{OH} (4)	I_{OH} = –40 µA	Seg1 to Seg35	V_{DD} – 0.2			V
Output low level voltage	V_{OL} (4)	I_{OL} = 40 µA				0.2	V
Output high level voltage	V_{OH} (6)	I_{OH} = –400 µA	COM1	V_{DD} – 0.2			V
Output low level voltage	V_{OL} (6)	I_{OL} = 400 µA				0.2	V
[1/2 bias drive]							
Output high level voltage	V_{OH} (4)	I_{OH} = –40 µA	Seg1 to Seg35	V_{DD} – 0.2			V
Output low level voltage	V_{OL} (4)	I_{OL} = 40 µA				0.2	V
Output high level voltage	V_{OH} (6)	I_{OH} = –400 µA	COM1 to COM4	V_{DD} – 0.2			V
Output middle level voltage	V_{OM}2-1	I_{OH} = –400 µA I_{OL} = 400 µA		V_{DD}/2 – 0.2		V_{DD}/2 + 0.2	V
Output low level voltage	V_{OL} (6)	I_{OL} = 400 µA				0.2	V
[1/3 bias drive]							
Output high level voltage	V_{OH} (4)	I_{OH} = –40 µA	Seg1 to Seg35	V_{DD} – 0.2			V
Output middle level voltage	V_{OM}1-1	I_{OH} = –40 µA		2 V_{DD}/3 – 0.2		2 V_{DD}/3 + 0.2	V
	V_{OM}1-2	I_{OL} = 40 µA		V_{DD}/3 – 0.2		V_{DD}/3 + 0.2	V
Output low level voltage	V_{OL} (4)	I_{OL} = 40 µA				0.2	V
Output high level voltage	V_{OH} (6)	I_{OH} = –400 µA	COM1 to COM4	V_{DD} – 0.2			V
Output middle level voltage	V_{OM}2-1	I_{OH} = –400 µA		2 V_{DD}/3 – 0.2		2 V_{DD}/3 + 0.2	V
	V_{OM}2-2	I_{OL} = 400 µA		V_{DD}/3 – 0.2		V_{DD}/3 + 0.2	V
Output low level voltage	V_{OL} (6)	I_{OL} = 400 µA				0.2	V

Note: For the 24 pins S1 to S4, K1 to K4, P1 to P4, M1 to M4, SO1 to SO4 and A1 to A4.

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Parameter	Symbol	Conditions			min	typ	max	Unit
Operating current	I_{OP}-1	V_{DD} = 3 V, Ta = 25°C, 32 kHz crystal oscillator, LCD = 1/3 bias, Figure 6				20	30	µA
	I_{OP}-2	V_{DD} = 5 V, Ta = 25°C, 32 kHz crystal oscillator, LCD = 1/3 bias, Figure 6				40	60	µA
	I_{OP}-3	V_{DD} = 3 V, Ta = 25°C, 400 kHz, CF oscillator, Figure 6				240	300	µA
	I_{OP}-4	V_{DD} = 5 V, Ta = 25°C, 400 kHz, CF oscillator, Figure 6				620	780	µA
	I_{OP}-5	V_{DD} = 3 V, Ta = 25°C, 1 MHz, CF oscillator, Figure 6				350	480	µA
	I_{OP}-6	V_{DD} = 5 V, Ta = 25°C, 1 MHz, CF oscillator, Figure 6				850	1200	µA
	I_{OP}-7	V_{DD} = 5 V, Ta = 25°C, 4 MHz, CF oscillator, Figure 6				1700	2500	µA
Supply leakage current	I_{LEK} (1)	V_{DD} = 6.0 V, Ta = 25°C, Figure 3				0.2	1.0	µA
Supply leakage current	I_{LEK} (2)	V_{DD} = 6.0 V, Ta = 50°C, Figure 3				1.0	5.0	µA
Input leakage current	I_{OFF}	V_{DD} = 6.0 V	S1 to S4, K1 to K4, M1 to M4, SO1 to SO4, A1 to A4, INT, RES (with the K, P, M, SO and A ports in input mode and with open specifications for the INT and RES pins)					µA
		V_{IN} = V_{DD}					1.0	µA
		V_{IN} = V_{SS}			–1.0			µA
Output voltage 2	V_{DD}1-(2)	V_{DD} = 5.0 V, C1 = C2 = 0.1 µF, Figure 4, 1/2 bias, fopg = 32.768 kHz		V_{DD}1 = V_O	2.4	2.5	2.6	V
Output voltage 3	V_{DD}1-(3)	V_{DD} = 5.0 V, C1 = C2 = 0.1 µF, Figure 4, 1/3 bias, fopg = 32.768 kHz		V_{DD}1 = V_O,	1.4	1.67	1.8	V
	V_{DD}2-(3)			V_{DD}2 = V_O	3.1	3.33	3.5	V
Supply current 1	| I_{DD} | 1-1	V_{DD} = 5.0 V, Ta = 25°C	Crystal oscillator specifications, crystal: 32 kHz Cg = 20 pF, C1 = 25 kΩ, HALT mode, Figure 6, LCD = 1/3 bias			15	30	µA
	| I_{DD} | 1-2	V_{DD} = 5.0 V, Ta = 50°C					50	µA
Supply current 2	| I_{DD} | 2-1	V_{DD} = 5.0 V, Ta = 25°C	Crystal oscillator specifications, crystal: 38 or 65 kHz, Cg = 10 pF, C1 = 25 kΩ, HALT mode, Figure 6, LCD = 1/3 bias			15	30	µA
	| I_{DD} | 2-2	V_{DD} = 5.0 V, Ta = 50°C					50	µA
Supply current 3	| I_{DD} | 3-1	V_{DD} = 5.0 V, Ta = 25°C	CF oscillator specifications, CF: 400 kHz, Ccg = Ccd = 330 pF, HALT mode, Figure 7			400	600	µA
	| I_{DD} | 3-2	V_{DD} = 5.0 V, Ta = 50°C					600	µA
Supply current 4	| I_{DD} | 4-1	V_{DD} = 5.0 V, Ta = 25°C	CF oscillator specifications, CF: 1000 kHz, Ccg = Ccd = 100 pF, HALT mode, Figure 8 or 220 pF			450	650	µA
	| I_{DD} | 4-2	V_{DD} = 5.0 V, Ta = 50°C					700	µA
Supply current 5	| I_{DD} | 5-1	V_{DD} = 5.0 V, Ta = 25°C	CF oscillator specifications, CF: 2000 kHz, Ccg = Ccd = 33 pF, HALT mode, Figure 8			500	700	µA
	| I_{DD} | 5-2	V_{DD} = 5.0 V, Ta = 50°C					750	µA
Supply current 6	| I_{DD} | 6-1	V_{DD} = 5.0 V, Ta = 25°C	CF oscillator specifications, CF: 4000 kHz, Ccg = Ccd = 33 pF, HALT mode, Figure 8			700	900	µA
	| I_{DD} | 6-2	V_{DD} = 5.0 V, Ta = 50°C					1000	µA
Oscillator correction capacitance	Cd	V_{DD} = 5.0 V, XTOUT pin (built-in)			16	20	24	pF

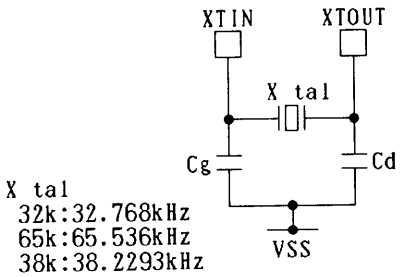


Figure 1-1 Oscillator Circuit (XT pins)

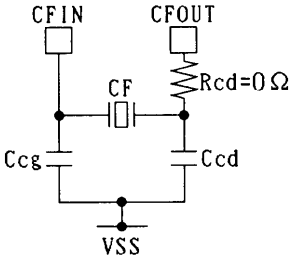


Figure 1-2 Oscillator Circuit (CF pins)

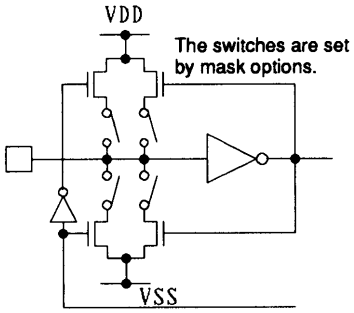


Figure 2 S, K, P, M, SO and A Port Input Circuit Configuration

Recommended Ceramic Filters

Manufacturer	Murata Mfg. Co., Ltd.			Kyocera Corporation		
Item / Frequency	Catalog No.	Ccg (pF)	Ccd (pF)	Catalog No.	Ccg (pF)	Ccd (pF)
400 kHz	CSB400P	330	330	KBR-400B	330	330
800 kHz	CSB800J	220	220	KBR-800H	100	100
1 MHz	CSB1000J	220	220	KBR-1000H/Y	100	100
2 MHz	CSA2.00MG, CST2.00MG	33 (built-in)	33 (built-in)	KBR-2.0MS	33	33
4 MHz	CSA4.00MG, CSA4.00MGW	33 (built-in)	33 (built-in)	KBR-4.0MSA/MCA, KBR-4.0MKS/MWS	33 (built-in)	33 (built-in)

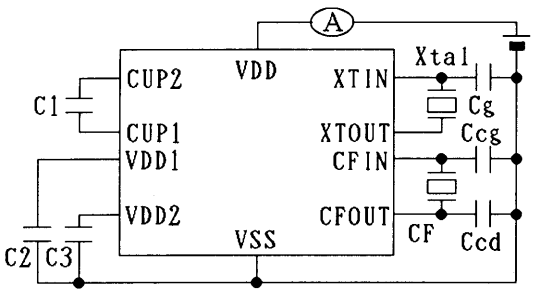


Figure 3 Supply Leakage Test Circuit

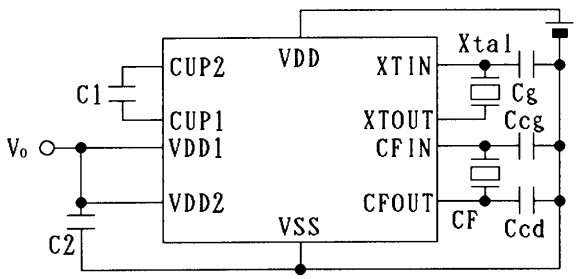


Figure 4 Output Voltage Test Circuit

- Stopped state
- S-port input resistors: on state
- I/O ports: output mode, all data values high
- RES and INT pins: built-in resistor specifications, open state
- Currents due to external components connected to the LCD ports are not included.
- Crystal frequency: between 32 and 65 kHz
- CF frequency: 200 kHz to 4 MHz

- Crystal frequency: 32 kHz
- C1, C2 and C3: 0.1 µF
- LCD ports: open
- CF frequency: 200 kHz to 4 MHz

Figures 4 and 5

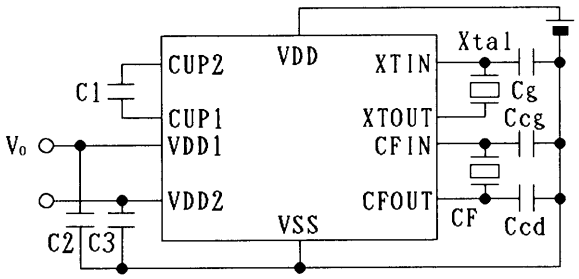


Figure 5 Output Voltage Test Circuit

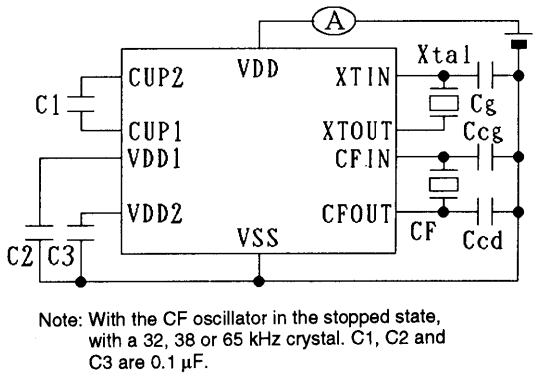


Figure 6 Supply Current Test Circuit

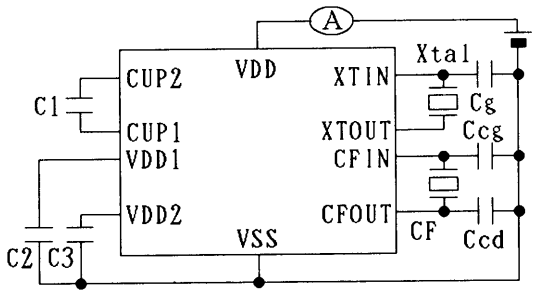


Figure 7 Supply Current Test Circuit

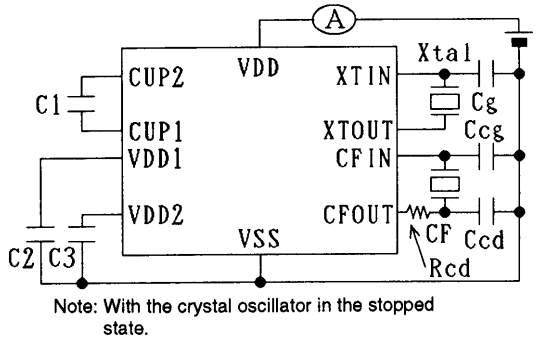


Figure 8 Supply Current Test Circuit

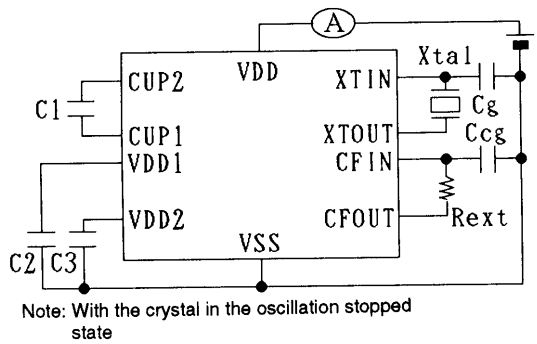


Figure 9 Supply Current Test Circuit

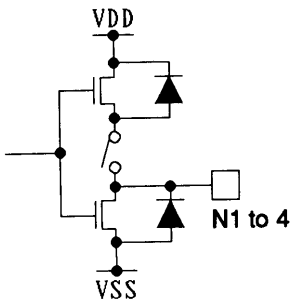


Figure 10 Supply Current Test Circuit

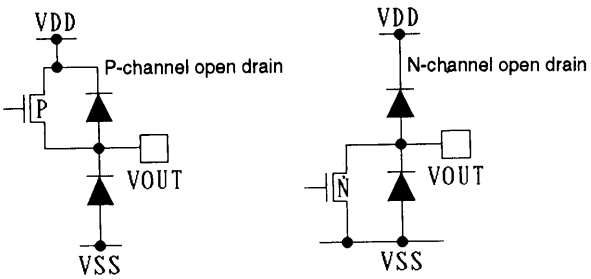
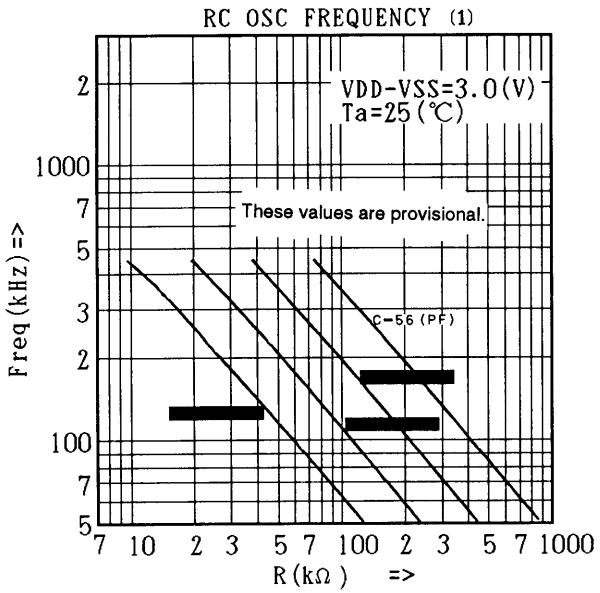


Figure 11 Segment Pin Open Drain Circuit Configurations



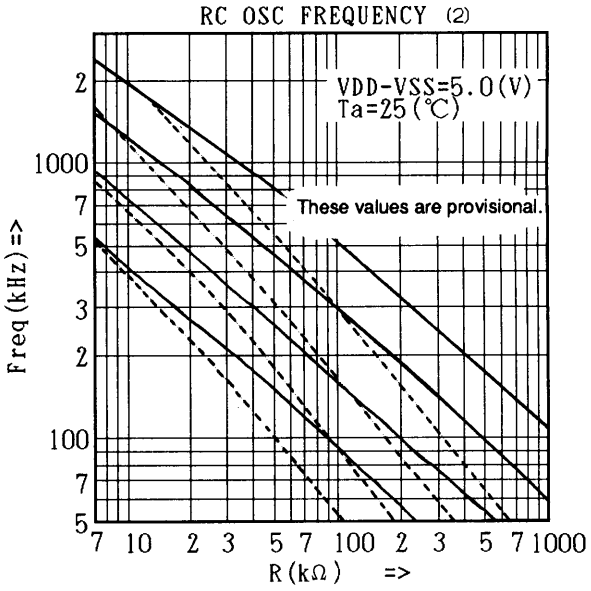
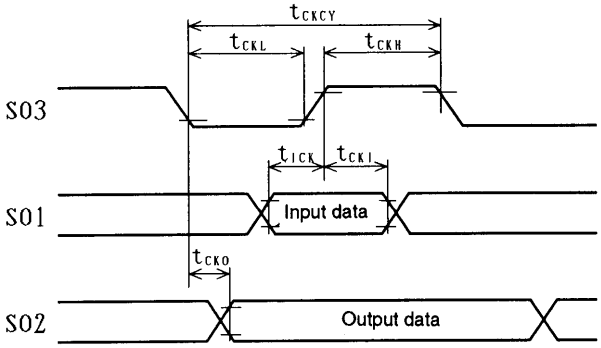


Figure 12 Sample RC Oscillator Frequency Characteristics



t_{CKCY} ····· 5 μs MIN
t_{CKL} = t_{CKH} ····· 2.4 μs MIN
t_{ICK} ····· 1 μs MIN
t_{CKI} ····· 1 μs MIN
t_{CKO} ····· 1 μs MAX
V_{DD} = 3.0 to 6.0 V

Figure 13 Serial I/O Timing (in external clock mode)

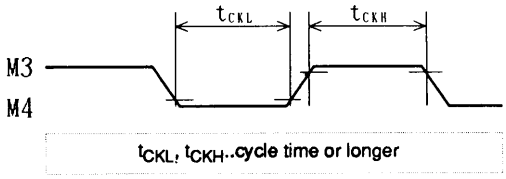


Figure 14 Timer 1 and Timer 2 External Clock Input Timing (external clock mode, pins M3 and M4)

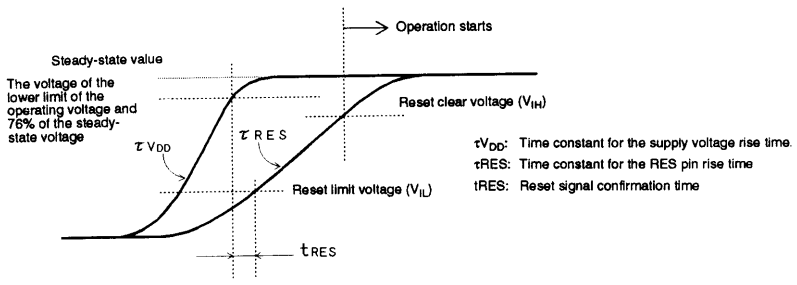


Figure Initial Reset Timing