

Preliminary

Overview

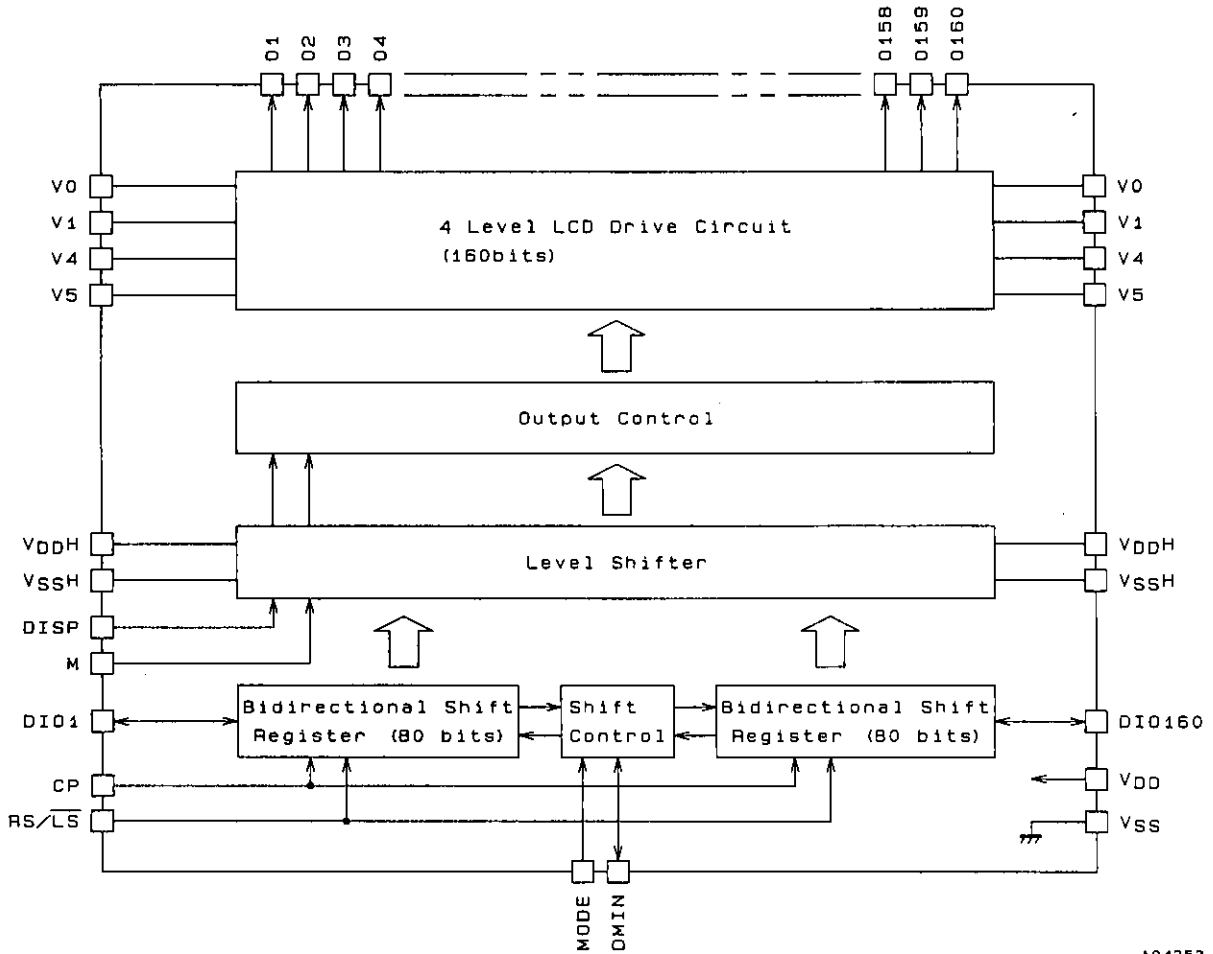
The LC4103 is a common driver LSI for large-scale dot matrix LCD displays. It includes a 160-bit bidirectional shift register and 4-level LCD drivers. The number of bits can be increased by using the I/O pins provided for cascode connection. In conjunction with the LC4104 segment driver, the LC4103 forms a chip set that can drive large-screen LCD panels.

Features

- High-voltage CMOS (P-sub) process
- LCD drive voltage: 42 V
- Logic system power-supply voltage: 2.7 to 5.5 V
- Maximum fcp: 2.5 MHz ($V_{DD} = 5\text{ V} \pm 10\%$),
200 kHz ($V_{DD} = 2.7\text{ to }4.5\text{ V}$)
- Bidirectional shift register
- The shift register can be divided into two 80-bit registers (thus allowing two-screen drive)
- DISPOFF function (Holds the LCD drive voltage at a fixed level.)
- Slim TAB (160 outputs)
- Display duty ratios: 1/160 to 1/480
- Package lineup

Type No.	Package
LC4103TAB-01	TAB: 250 μm outer lead pitch
LC4103TAB-02	TAB: 180 μm outer lead pitch
LC4103C	Chip product

Block Diagram



A04353

Specifications

The following electrical characteristics apply when sealed in a Sanyo standard PGA-208 package.

Absolute Maximum Ratings at $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	min	typ	max	Unit
Maximum supply voltage	$V_{DD\text{ max}}$	V_{DD}	-0.3		7	V
Maximum supply voltage	$V_{DDH\text{ max}}$	V_{DDH}	-0.3		45	V
Maximum supply voltage	$V_{SSH\text{ max}}$	V_{SSH}	-0.3		+0.3	V
Input voltage	V_{IN}	CP, RS/LS, DISP, M, DIO0, DIO160, DMIN	-0.3		$V_{DD} + 0.3$	V
Input voltage	V0, V1	*, V0, V1	$V_{DDH} - 7$		$V_{DDH} + 0.3$	V
Input voltage	V4	*, V4	-0.3		$V_{SS} + 7$	V
Input voltage	V5	*, V5	-0.3		+0.3	V
Operating temperature	T_{opr}		-20		+75	°C
Storage temperature	T_{stg}		-55		+125	°C

Note: * V0, V1, V4, and V5 must obey the following inequalities: $V_{DDH} \geq V0 \geq V1 \geq V_{DDH} - 7\text{ V}$, and $7\text{ V} \geq V4 \geq V5 \geq V_{SS}$.

LC4103TAB-01, 4103TAB-02, 4103C

Allowable Operating Ranges at $T_a = -20$ to $+75^\circ\text{C}$, $V_{SS} = 0$ V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}	V_{DD}	2.7		5.5	V
Supply voltage	V_{DDH}	V_{DDH}	20		42	V
Supply voltage	V_{SSH}	V_{SSH}		0		V
Input high-level voltage	V_{IH}	RS/LS, DISP, M, DIO1, DIO160, CP, DMIN, MODE	$0.8 V_{DD}$		V_{DD}	V
Input low-level voltage	V_{IL}	RS/LS, DISP, M, DIO1, DIO160, CP, DMIN, MODE	0		$0.2 V_{DD}$	V
Input voltage	V_0, V_1	*, V_0, V_1	$V_{DDH} - 7$		V_{DDH}	V
Input voltage	V_4	*, V_4	0		$V_{SSH} + 7$	V
Input voltage	V_5	*, V_5		0		V

Note: V_0, V_1, V_4 , and V_5 must obey the following inequalities: $V_{DDH} \geq V_0 \geq V_1 \geq V_{DDH} - 7$ V, and 7 V $\geq V_4 \geq V_5 \geq V_{SSH}$.
 At power on: First turn on the logic system power supply and then turn on the high-voltage system power supply.
 At power off: First turn off the high-voltage system power supply and then turn off the logic system power supply.

Allowable Operating Ranges at $V_{DD} = 5$ V \pm 10%

Parameter	Symbol	Conditions	min	typ	max	Unit
Clock frequency	fcp	CP			2.5	MHz
High-level clock pulse width	t _{wc}	CP	30			ns
Input setup time	t _{su}	CP, DIO0, DIO160, DMIN	100			ns
Input hold time	t _h	CP, DIO0, DIO160, DMIN	30			ns
CP rise time	t _r	CP			30	ns
CP fall time	t _f	CP			30	ns

Allowable Operating Ranges at $V_{DD} = 2.7$ to 4.5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Clock frequency	fcp	CP			200	kHz
High-level clock pulse width	t _{wc}	CP	100			ns
Input setup time	t _{su}	CP, DIO0, DIO160, DMIN	100			ns
Input hold time	t _h	CP, DIO0, DIO160, DMIN	30			ns
CP rise time	t _r	CP			30	ns
CP fall time	t _f	CP			30	ns

Electrical Characteristics at $T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 2.7$ to 5.5 V, $V_{SS} = 0$ V

Parameter	Symbol	Conditions	min	typ	max	Unit
Input high-level current	I_{IH}	$V_{IN} = V_{DD}$: CP, RS/LS, DISP, M, DIO0, DIO160, DMIN, MODE			1	μA
Input low-level current	I_{IL}	$V_{IN} = V_{SS}$: CP, RS/LS, DISP, M, DIO0, DIO160, DMIN, MODE	-1			μA
Output high-level voltage	V_{OH}	$I_O = -0.4$ mA: DIO1, DIO160	$0.8 V_{DD}$		V_{DD}	V
Output low-level voltage	V_{OL}	$I_O = 0.4$ mA: DIO1, DIO160	V_{SS}		$0.2 V_{DD}$	V
Output on resistance	R_{OUT}	$V_{DDH} = 40$ V, *, $V_0 - V_O = 0.5$ V, $V_1 - V_O = 0.5$ V, $V_0 - V_4 = 0.5$ V, $V_0 - V_5 = 0.5$ V, $V_{DD} = 2.7$ V: O1 to O160			1.0	k Ω
Current drain 1	I_{DD}	$V_{DD} = 2.7$ to 5.5 V, fcp = 50 kHz			200	μA
Current drain 2	I_{DDH}	fM = 100 Hz, no output load, $V_{DDH} = 42$ V, 1 data shift			500	μA

Note: * V_O is the voltage applied for an on output, $V_0 = V_{DDH}$, $V_1 = 19/20 (V_{DDH} - V_{SSH})$, $V_4 = 1/20 (V_{DDH} - V_{SSH})$, $V_5 = V_{SSH}$, $V_{SSH} = V_{SS}$

LC4103TAB-01, 4103TAB-02, 4103C

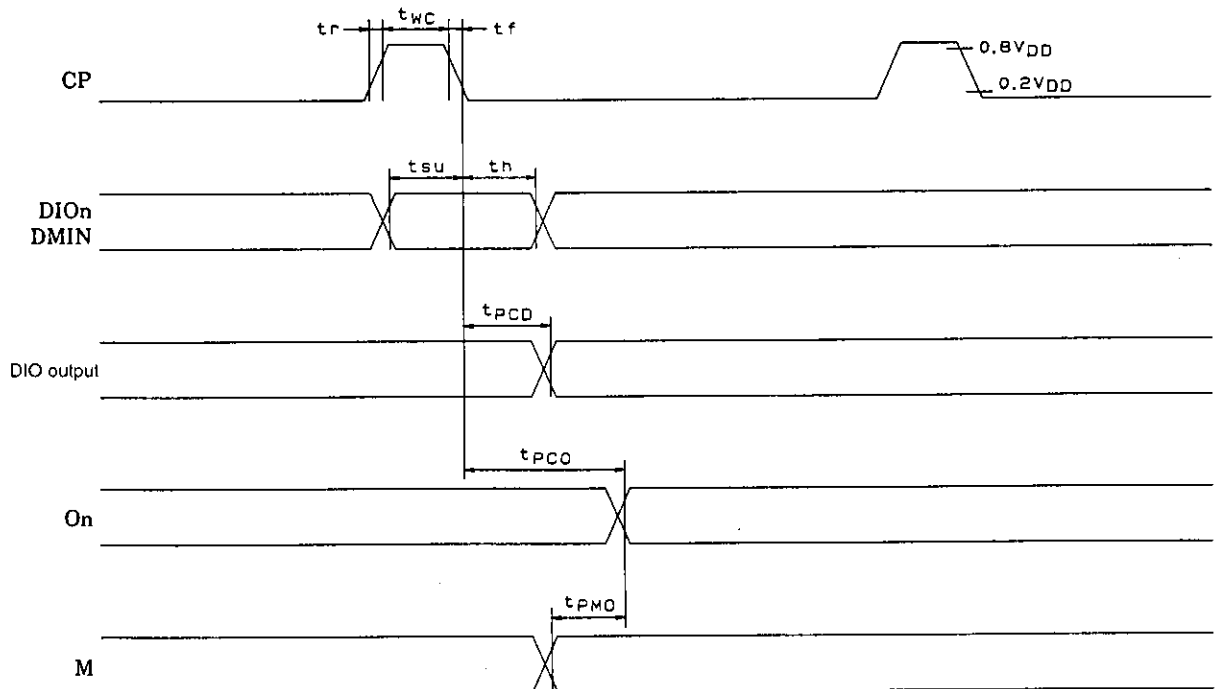
Switching Characteristics at $T_a = -20$ to $+75^\circ\text{C}$, $V_{SS} = 0\text{ V}$, $V_{DD} = 5\text{ V} \pm 10\%$

Parameter	Symbol	Conditions	min	typ	max	Unit
DIO output delay time	t_{PCD}	30 pF capacitive load			90	ns
CP/On delay time	t_{PCO}	100 pF capacitive load			700	ns
M/On delay time	t_{PMO}	100 pF capacitive load			700	ns

Switching Characteristics at $T_a = -20$ to $+75^\circ\text{C}$, $V_{SS} = 0\text{ V}$, $V_{DD} = 2.7$ to 4.5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
DIO output delay time	t_{PCD}	30 pF capacitive load			350	ns
CP/On delay time	t_{PCO}	100 pF capacitive load			3	μs
M/On delay time	t_{PMO}	100 pF capacitive load			3	μs

Timing Chart

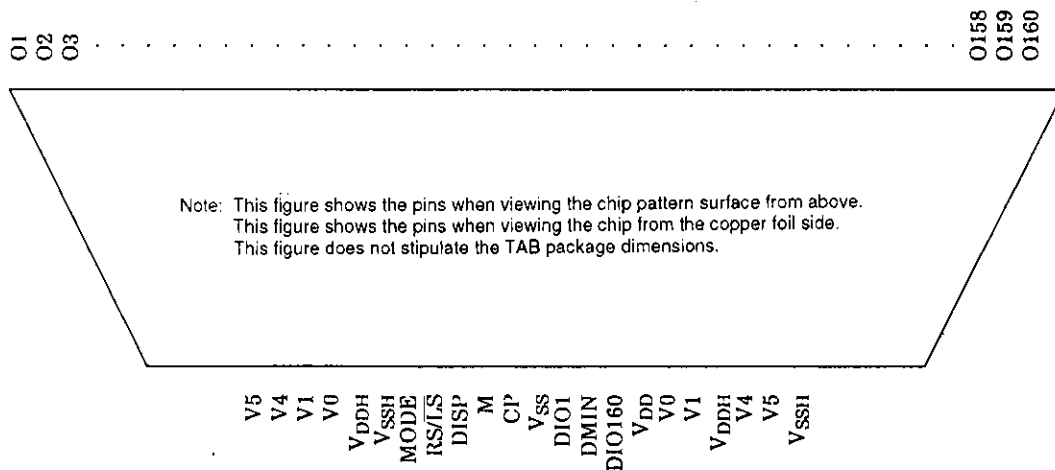


A04354

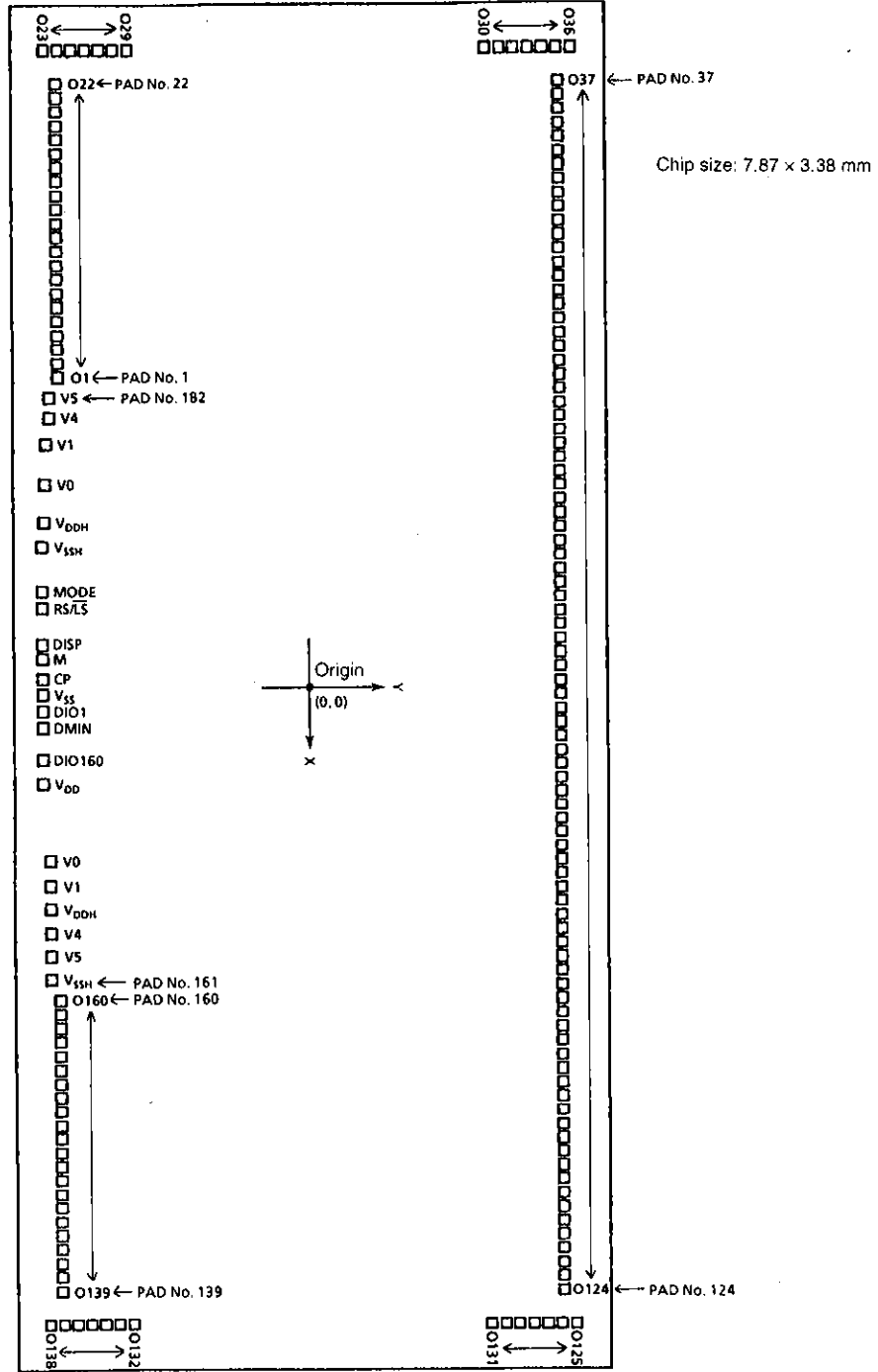
Pin Functions

Symbol	I/O	Function																												
O1 to O160	O	LCD drive outputs																												
		<table border="1"> <thead> <tr> <th>M</th> <th>Data</th> <th>DISP</th> <th>On</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>H</td> <td>H</td> <td>V0</td> </tr> <tr> <td>H</td> <td>L</td> <td>H</td> <td>V1</td> </tr> <tr> <td>L</td> <td>L</td> <td>H</td> <td>V4</td> </tr> <tr> <td>H</td> <td>H</td> <td>H</td> <td>V5</td> </tr> <tr> <td>*</td> <td>*</td> <td>L</td> <td>V5</td> </tr> </tbody> </table>	M	Data	DISP	On	L	H	H	V0	H	L	H	V1	L	L	H	V4	H	H	H	V5	*	*	L	V5				
		M	Data	DISP	On																									
		L	H	H	V0																									
		H	L	H	V1																									
		L	L	H	V4																									
H	H	H	V5																											
*	*	L	V5																											
*: Don't care. (Must be held either high or low.)																														
V0	I	V0 level drive voltage supply (selected level) } Pins with the same name must be set to the same potential. V1 level drive voltage supply (unselected level) V4 level drive voltage supply (unselected level) V5 level drive voltage supply (selected level)																												
V1	I																													
V4	I																													
V5	I																													
V _{DDH}	—	High-voltage system power supply. Pins with the same name must be set to the same potential.																												
V _{SSH}	—	High-voltage system ground. Pins with the same name must be set to the same potential.																												
DISP	I	LCD off function. All outputs go to the V5 level when this pin is low.																												
M	I	Alternation signal input																												
CP	I	Data shift pulse input (falling edge)																												
MODE	I	<table border="1"> <thead> <tr> <th>MODE</th> <th>RS/LS</th> <th>Data transfer direction</th> <th>DIO1</th> <th>DIO160</th> <th>DMIN</th> </tr> </thead> <tbody> <tr> <td rowspan="2">L</td> <td>L</td> <td>O160 → O1</td> <td>Out</td> <td>In</td> <td>*</td> </tr> <tr> <td>H</td> <td>O1 → O160</td> <td>In</td> <td>Out</td> <td>*</td> </tr> <tr> <td rowspan="2">H</td> <td>L</td> <td>O160 → O81 O80 → O1</td> <td>Out</td> <td>In</td> <td>In</td> </tr> <tr> <td>H</td> <td>O1 → O80 O81 → O160</td> <td>In</td> <td>Out</td> <td>In</td> </tr> </tbody> </table>	MODE	RS/LS	Data transfer direction	DIO1	DIO160	DMIN	L	L	O160 → O1	Out	In	*	H	O1 → O160	In	Out	*	H	L	O160 → O81 O80 → O1	Out	In	In	H	O1 → O80 O81 → O160	In	Out	In
MODE	RS/LS		Data transfer direction	DIO1	DIO160	DMIN																								
L	L		O160 → O1	Out	In	*																								
	H		O1 → O160	In	Out	*																								
H	L		O160 → O81 O80 → O1	Out	In	In																								
	H		O1 → O80 O81 → O160	In	Out	In																								
RS/LS	I																													
DIO1	I/O																													
DMIN	I																													
DIO160	I/O																													
*: Don't care (Must be held either high or low.)																														
V _{DD}	—	Logic system power supply																												
V _{SS}	—	Logic system ground																												

Pin Assignment



Pad Assignment



LC4103TAB-01, 4103TAB-02, 4103C

Pad Coordinates

PAD No.	Signal	X coordinate	Y coordinate	PAD No.	Signal	X coordinate	Y coordinate
1	O1	-1800.0	-1425.2	41	O41	-3160.0	1429.2
2	O2	-1880.0	-1425.2	42	O42	-3080.0	1429.2
3	O3	1960.0	-1425.2	43	O43	-3000.0	1429.2
4	O4	-2040.0	-1425.2	44	O44	-2920.0	1429.2
5	O5	-2120.0	-1425.2	45	O45	-2840.0	1429.2
6	O6	-2200.0	-1425.2	46	O46	-2760.0	1429.2
7	O7	-2280.0	-1425.2	47	O47	-2680.0	1429.2
8	O8	-2360.0	-1425.2	48	O48	-2600.0	1429.2
9	O9	-2440.0	-1425.2	49	O49	-2520.0	1429.2
10	O10	-2520.0	-1425.2	50	O50	-2440.0	1429.2
11	O11	-2600.0	-1425.2	51	O51	-2360.0	1429.2
12	O12	-2680.0	-1425.2	52	O52	-2280.0	1429.2
13	O13	-2760.0	-1425.2	53	O53	-2200.0	1429.2
14	O14	-2840.0	-1425.2	54	O54	-2120.0	1429.2
15	O15	-2920.0	-1425.2	55	O55	-2040.0	1429.2
16	O16	-3000.0	-1425.2	56	O56	-1960.0	1429.2
17	O17	-3080.0	-1425.2	57	O57	-1880.0	1429.2
18	O18	-3160.0	-1425.2	58	O58	-1800.0	1429.2
19	O19	-3240.0	-1425.2	59	O59	-1720.0	1429.2
20	O20	-3320.0	-1425.2	60	O60	-1640.0	1429.2
21	O21	-3400.0	-1425.2	61	O61	-1560.0	1429.2
22	O22	-3480.0	-1425.2	62	O62	-1480.0	1429.2
23	O23	-3673.0	-1497.6	63	O63	-1400.0	1429.2
24	O24	-3673.0	-1417.6	64	O64	-1320.0	1429.2
25	O25	-3673.0	-1337.6	65	O65	-1240.0	1429.2
26	O26	-3673.0	-1257.6	66	O66	-1160.0	1429.2
27	O27	-3673.0	-1177.6	67	O67	-1080.0	1429.2
28	O28	-3673.0	-1097.6	68	O68	-1000.0	1429.2
29	O29	-3673.0	-1017.6	69	O69	-920.0	1429.2
30	O30	-3673.0	1017.6	70	O70	-840.0	1429.2
31	O31	-3673.0	1097.6	71	O71	-760.0	1429.2
32	O32	-3673.0	1177.6	72	O72	-680.0	1429.2
33	O33	-3673.0	1257.6	73	O73	-600.0	1429.2
34	O34	-3673.0	1337.6	74	O74	-520.0	1429.2
35	O35	-3673.0	1417.6	75	O75	-440.0	1429.2
36	O36	-3673.0	1497.6	76	O76	-360.0	1429.2
37	O37	-3480.0	1429.2	77	O77	-280.0	1429.2
38	O38	-3400.0	1429.2	78	O78	-200.0	1429.2
39	O39	-3320.0	1429.2	79	O79	-120.0	1429.2
40	O40	-3240.0	1429.2	80	O80	-40.0	1429.2

Continued on next page.

LC4103TAB-01, 4103TAB-02, 4103C

Continued from preceding page.

PAD No.	Signal	X coordinate	Y coordinate	PAD No.	Signal	X coordinate	Y coordinate
81	O81	40.0	1429.2	121	O121	3240.0	1429.2
82	O82	120.0	1429.2	122	O122	3320.0	1429.2
83	O83	200.0	1429.2	123	O123	3400.0	1429.2
84	O84	280.0	1429.2	124	O124	3480.0	1429.2
85	O85	360.0	1429.2	125	O125	3673.0	1497.6
86	O86	440.0	1429.2	126	O126	3673.0	1417.6
87	O87	520.0	1429.2	127	O127	3673.0	1337.6
88	O88	600.0	1429.2	128	O128	3673.0	1257.6
89	O89	680.0	1429.2	129	O129	3673.0	1177.6
90	O90	760.0	1429.2	130	O130	3673.0	1097.6
91	O91	840.0	1429.2	131	O131	3673.0	1017.6
92	O92	920.0	1429.2	132	O132	3673.0	-1017.6
93	O93	1000.0	1429.2	133	O133	3673.0	-1097.6
94	O94	1080.0	1429.2	134	O134	3673.0	-1177.6
95	O95	1160.0	1429.2	135	O135	3673.0	-1257.6
96	O96	1240.0	1429.2	136	O136	3673.0	-1337.6
97	O97	1320.0	1429.2	137	O137	3673.0	-1417.6
98	O98	1400.0	1429.2	138	O138	3673.0	-1497.6
99	O99	1480.0	1429.2	139	O139	3480.0	-1425.2
100	O100	1560.0	1429.2	140	O140	3400.0	-1425.2
101	O101	1640.0	1429.2	141	O141	3320.0	-1425.2
102	O102	1720.0	1429.2	142	O142	3240.0	-1425.2
103	O103	1800.0	1429.2	143	O143	3160.0	-1425.2
104	O104	1880.0	1429.2	144	O144	3080.0	-1425.2
105	O105	1960.0	1429.2	145	O145	3000.0	-1425.2
106	O106	2040.0	1429.2	146	O146	2920.0	-1425.2
107	O107	2120.0	1429.2	147	O147	2840.0	-1425.2
108	O108	2200.0	1429.2	148	O148	2760.0	-1425.2
109	O109	2280.0	1429.2	149	O149	2680.0	-1425.2
110	O110	2360.0	1429.2	150	O150	2600.0	-1425.2
111	O111	2440.0	1429.2	151	O151	2520.0	-1425.2
112	O112	2520.0	1429.2	152	O152	2440.0	-1425.2
113	O113	2600.0	1429.2	153	O153	2360.0	-1425.2
114	O114	2680.0	1429.2	154	O154	2280.0	-1425.2
115	O115	2760.0	1429.2	155	O155	2200.0	-1425.2
116	O116	2840.0	1429.2	156	O156	2120.0	-1425.2
117	O117	2920.0	1429.2	157	O157	2040.0	-1425.2
118	O118	3000.0	1429.2	158	O158	1960.0	-1425.2
119	O119	3080.0	1429.2	159	O159	1880.0	-1425.2
120	O120	3160.0	1429.2	160	O160	1800.0	-1425.2

Continued on next page.

Continued from preceding page.

PAD No.	Signal	X coordinate	Y coordinate
161	V _{SSH}	1682.0	-1473.7
162	V5	1547.0	-1473.7
163	V4	1412.0	-1473.7
164	V _{DDH}	1277.0	-1473.7
165	V1	1142.0	-1473.7
166	V0	993.0	-1473.7
167	V _{DD}	544.0	-1522.7
168	DIO160	403.6	-1522.7
169	DMIN	217.5	-1522.7
170	DIO1	122.5	-1522.7
171	V _{SS}	27.5	-1522.7
172	CP	-57.5	-1522.7
173	M	-172.5	-1522.7
174	DISP	-257.5	-1522.7
175	RS/ \overline{LS}	-468.6	-1522.7
176	MODE	-563.6	-1522.7
177	V _{SSH}	-821.6	-1523.7
178	V _{DDH}	-959.0	-1507.7
179	V0	-1178.0	-1503.7
180	V1	-1412.0	-1493.7
181	V4	-1567.0	-1473.7
182	V5	-1682.0	-1473.7

- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
 - ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use:
 - ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of December, 1995. Specifications and information herein are subject to change without notice.