



LC378000RP

Internally Synchronized Silicon Gate 8M (1,048,576-word × 8-bit, 524,288-word × 16-bit) Mask ROM

Preliminary



Overview

The LC378000RP is an 8-Mbit mask ROM that can be switched between byte mode, which provides an 8-bit × 1,048,576-word structure, and word mode, which provides a 16-bit × 524,288-word structure. Since this device operates over the wide supply voltage range of 2.6 to 5.5 V and achieves access times (t_{AA}) of 100 ns (at $V_{CC} = 4.5$ to 5.5 V) and 200 ns (at $V_{CC} = 2.6$ to 5.5 V), it can be used in a wide range of systems, from 5-V systems requiring high-speed access to 3-V battery operated systems.

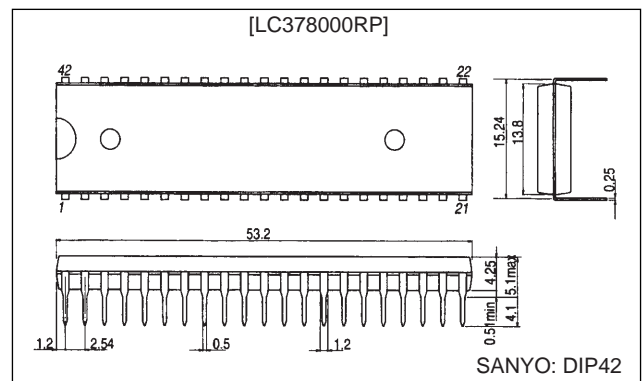
Features

- Supply voltage range: 2.6 to 5.5 V
- Access time (t_{AA}): 100 ns ($V_{CC} = 4.5$ to 5.5 V)
(t_{CA}): 110 ns ($V_{CC} = 4.5$ to 5.5 V)
200 ns ($V_{CC} = 2.6$ to 5.5 V)
- Switchable between 8-bit and 16-bit data path widths
Byte mode: 1,048,576 words × 8 bits
Word mode: 524,288 words × 16 bits
- Operating current drain: 90 mA (maximum)
- Standby current: 30 μ A (maximum)
- Fully static operation (internal synchronization)
- Three-state outputs
- Package: 42-pin DIP (600 mil) plastic package

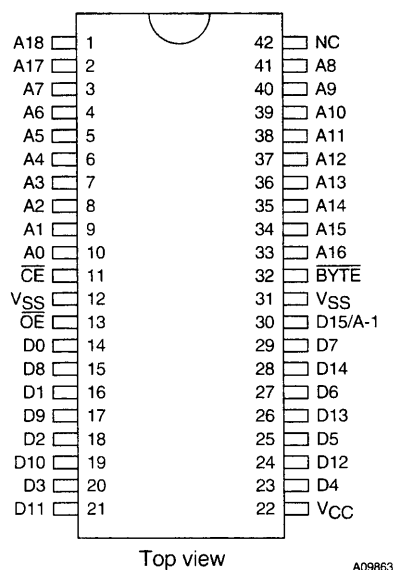
Package Dimensions

unit: mm

3014A-DIP42



Pin Assignment

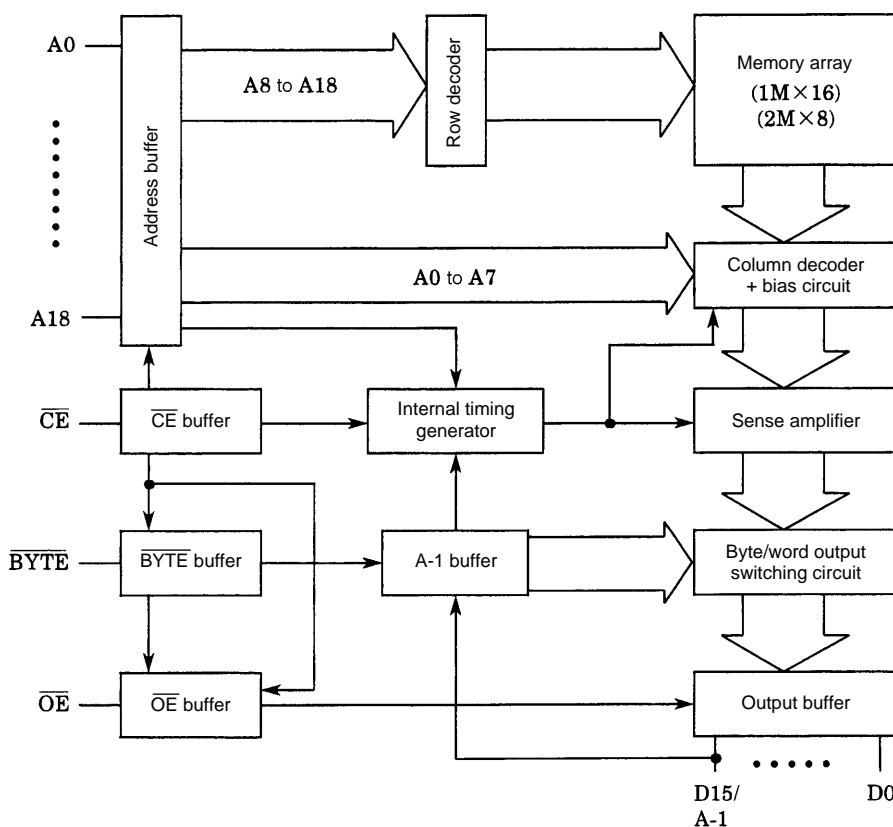


Pin Functions

| | |
|-------------------|--------------------------|
| A0 to A19 | Address inputs |
| D0 to D15/A-1 | Data outputs |
| \overline{CE} | Chip enable input |
| \overline{OE} | Output enable input |
| \overline{BYTE} | Byte/word mode switching |
| V _{CC} | Power |
| V _{SS} | Ground |

D15/A-1: In byte mode, this pin functions as the A-1 address input, and in word mode, it functions as the D15 data output pin.

Block Diagram



Function Logic Table

| \overline{CE} | \overline{OE} | \overline{BYTE} | Output pin state | Current drain |
|-----------------|-----------------|-------------------|-----------------------|----------------------|
| H | X | L | High impedance | Standby mode level |
| L | H | L | High impedance | Operating mode level |
| L | L | L | DOUT × 8 (BYTE MODE)* | Operating mode level |
| H | X | H | High impedance | Standby mode level |
| L | H | H | High impedance | Operating mode level |
| L | L | H | DOUT × 16 (WORD MODE) | Operating mode level |

Note: X: A high-level or low-level input
 D8 to 14 are high impedance and D15 functions as the A-1 address input.

Specifications

Absolute Maximum Ratings*

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|-------------------|--------------------------|-------------------------|------------------|
| Supply voltage | V_{CC} | | -0.3 to +7.0 | V |
| Input pin voltage | V_{IN} | | -0.3* to $V_{CC} + 0.3$ | V |
| Output pin voltage | V_{OUT} | | -0.3 to $V_{CC} + 0.3$ | V |
| Allowable power dissipation | $P_d \text{ max}$ | $T_a = 25^\circ\text{C}$ | 1.0 | W |
| Operating temperature | T_{opr} | | -10 to +70 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | | -55 to +125 | $^\circ\text{C}$ |

Note: Application of stresses greater than or equal to the maximum ratings may lead to device destruction.

*: Minimum value minus 3.0 V for pulses with widths of 30 ns or less.

Capacitance Characteristics* at $T_a = 25^\circ\text{C}$, $f = 1.0 \text{ MHz}$

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|------------------------|-----------|--|---------|-----|-----|------|
| | | | min | typ | max | |
| Input pin capacitance | C_{IN} | $V_{IN} = 0 \text{ V}$. Reference value using the Sanyo DIP. | | | 8 | pF |
| Output pin capacitance | C_{OUT} | $V_{OUT} = 0 \text{ V}$. Reference value using the Sanyo DIP. | | | 10 | pF |

Note: These parameters are not tested in all units, but rather are sampled in a subset of units produced.

DC Allowable Operating Ranges at $T_a = -10 \text{ to } +70^\circ\text{C}$

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|--------------------------|----------------------|------------|---------|-----|----------------|------|
| | | | min | typ | max | |
| Supply voltage | $V_{CC \text{ max}}$ | | 2.6 | 5.0 | 5.5 | V |
| Input high-level voltage | V_{IH} | | 2.2 | | $V_{CC} + 0.3$ | V |
| Input low-level voltage | V_{IL} | | -0.3 | | 0.6 | V |

DC Electrical Characteristics at $T_a = -10 \text{ to } +70^\circ\text{C}$, $V_{CC} = 2.6 \text{ to } 5.5 \text{ V}$

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---------------------------|------------|--|--------------|-----|-----------|---------------|
| | | | min | typ | max | |
| Operating current drain | I_{CCA1} | $\overline{CE} = 0.2 \text{ V}$, $V_I = V_{CC} - 0.2 \text{ V}/0.2 \text{ V}$ | | | 30 | mA |
| | I_{CCA2} | $\overline{CE} = V_{IL}$, $I_O = 0 \text{ mA}$, $V_I = V_{IH}/V_{IL}$, $f = 10 \text{ MHz}$ | | | 90 | mA |
| Standby current drain | I_{CCS1} | $\overline{CE} = V_{CC} - 0.2 \text{ V}$ | | | 30 (1.0) | μA |
| | I_{CCS2} | $\overline{CE} = V_{IH}$ | | | 1.0 (0.3) | mA |
| Input leakage current | I_{LI} | $V_{IN} = 0 \text{ to } V_{CC}$ | | | ± 1.0 | μA |
| Output leakage current | I_{LO} | \overline{CE} or $\overline{OE} = V_{IH}$, $V_{OUT} = 0 \text{ to } V_{CC}$ | | | ± 1.0 | μA |
| Output high-level voltage | V_{OH} | $I_{OH} = -0.5 \text{ mA}$ | $0.8 V_{CC}$ | | | V |
| Output low-level voltage | V_{OL} | $I_{OL} = 0.5 \text{ mA}$ | | | 0.2 | V |

Note: Values in parentheses are guaranteed at $T_a = 25^\circ\text{C}$.

AC Characteristics at $T_a = -10 \text{ to } +70^\circ\text{C}$, $V_{CC} = 2.6 \text{ to } 5.5 \text{ V}$

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|-----------------------------|------------|------------|-----------|-----|-----------|------|
| | | | min | typ | max | |
| Cycle time | t_{CYC} | | 200 (100) | | | ns |
| Address access time | t_{AA} | | | | 200 (100) | ns |
| \overline{CE} enable time | t_{CEON} | | 200 (135) | | | ns |
| \overline{CE} access time | t_{CA} | | | | 200 (110) | ns |
| \overline{OE} access time | t_{OA} | | | | 100 (40) | ns |
| Output hold time | t_{OH} | | 20 | | | ns |
| Output disable time* | t_{OD} | | | | 100 | ns |

Note: t_{OD} is stipulated as the time from the rise of either \overline{CE} or \overline{OE} (whichever occurs first) to the point when the output goes to the high-impedance state.

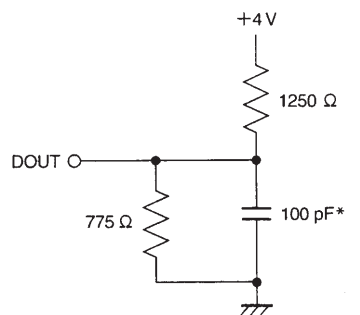
These parameters are not tested in all units, but rather are sampled in a subset of units produced.

Values in parentheses are for $V_{CC} = 4.5 \text{ to } 5.5 \text{ V}$.

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Test Conditions

| | |
|-----------------------------|----------------|
| Input voltage amplitude | 0.4 V to 2.8 V |
| Rise and fall times | 5 ns |
| Input discrimination level | 1.5 V |
| Output discrimination level | 1.5 V |
| Output load | See figure. |

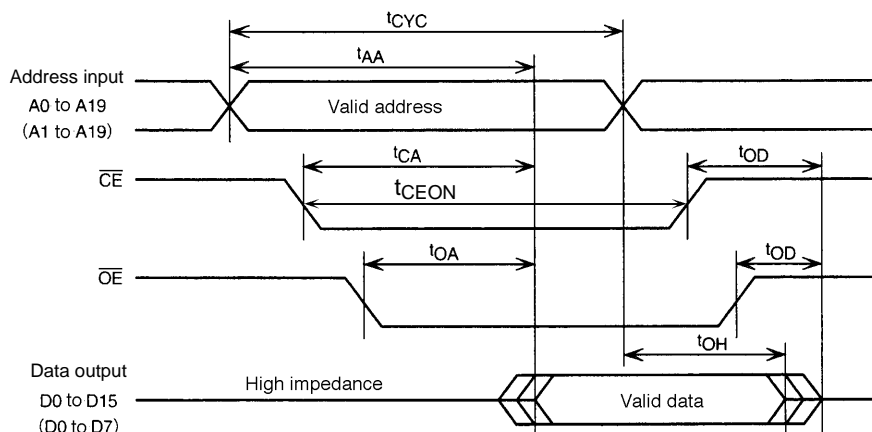


*: Includes the oscilloscope and jig capacitances.

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Output Load

Timing Waveforms



Note: Items in parentheses are for byte mode operation.

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Notes on System Design

This IC adopts the ATD technique, in which operation starts when a change in either the CE or address inputs is detected. This means that the output data immediately after power is applied is invalid. When using this IC as program memory for the Z80 and similar microprocessors, applications must take into account the fact that valid data will not be output after power is first applied unless the value of either the CE line or at least one of the address lines is changed after the power supply has stabilized.

Another point due to the use of the ATD technique is that this IC is sensitive to input noise. Do not apply voltages outside the allowable DC input levels for extended periods and do not apply input voltages with large noise components.

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