Ordering number : EN*5087C

CMOS LSI

LC371100SP, SM, ST-10/20LV

1 MEG (131072 words× 8 bits) Mask ROM
Internal Clocked Silicon Gate

Preliminary

Overview

The LC371100SP, LC371100SM and LC371100ST are 131,072-word × 8-bit organization (1,048,576-bit) mask programmable read only memories.

The LC371100SP-10, LC371100SM-10 and LC371100ST-10 feature an access time of 100 ns, an OE access time of 40 ns, and a standby current of 30 µA, and are optimal for use in 5-V systems that require high-speed access.

The LC371100SP-20LV, LC371100SM-20LV and LC371100ST-20LV feature an access time of 200 ns, an OE access time of 80 ns, and a standby current of 4 µA. Additionally, they provide high-speed access in 3.3-V systems (3.0 to 3.6 V) with a 150-ns access time and a 60-ns OE access time.

These ROMs adopt the JEDEC standard pin assignment which allows them to replace EPROM easily. To prevent bus line collisions in multi-bus microcontroller systems, pin 24 can be mask programmed to be either active high or active low.

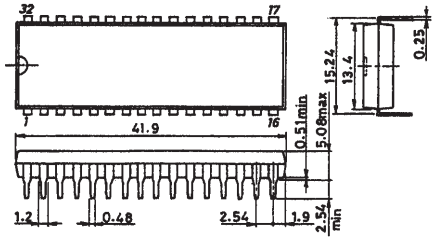
Features

- 131072 words × 8 bits organization
- Power supply
  LC371100SP, SM, ST-10: 5.0 V ± 10%
  LC371100SP, SM, ST-20LV: 2.7 to 3.6 V
- Fast access time (t_{AA}, t_{CA})
  LC371100SP, SM, ST-10: 100 ns (max.)
  LC371100SP, SM, ST-20LV: 200 ns (max.)
  150 ns (V_{CC} = 3.0 to 3.6 V)
- Operating current
  LC371100SP, SM, ST-10: 70 mA (max.)
  LC371100SP, SM, ST-20LV: 20 mA (max.)
- Standby current
  LC371100SP, SM, ST-10: 30 µA (max.)
  LC371100SP, SM, ST-20LV: 5 µA (max.)
- Full static operation (internal clocked type)
- Fully TTL compatible (5 V supply)
- 3 state outputs
- JEDEC standard pin configuration
- Package type
  LC371100SP-10/20LV: DIP32 (600 mil)
  LC371100SM-10/20LV:SOP32 (525 mil)
  LC371100ST-10/20LV: TSOP32 (8 mm × 20 mm)

Package Dimensions

unit: mm
3192-DIP32

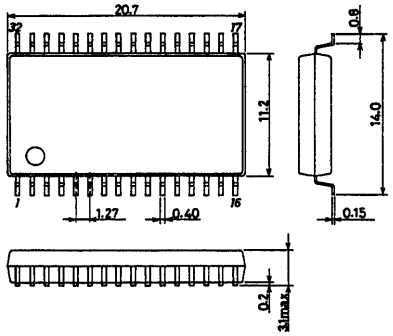
[LC371100SP]



SANYO: DIP32

unit: mm
3205-SOP32

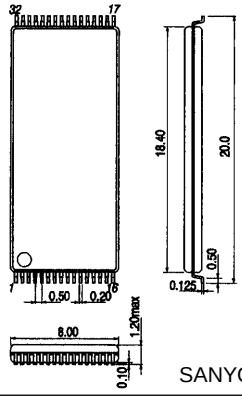
[LC371100SM]



SANYO: SOP32

unit: mm
3224-TSOP32

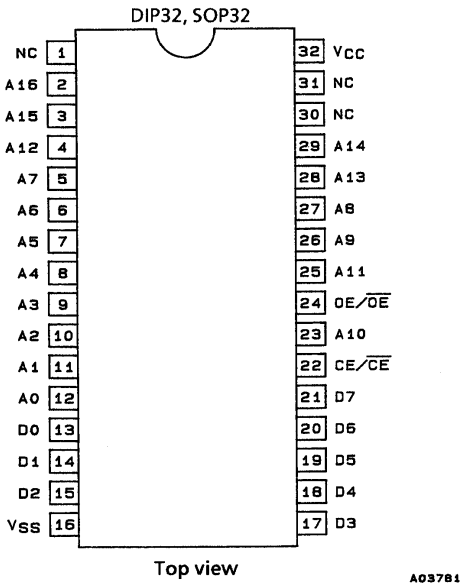
[LC371100ST]



SANYO: TSOP32 (type-I)

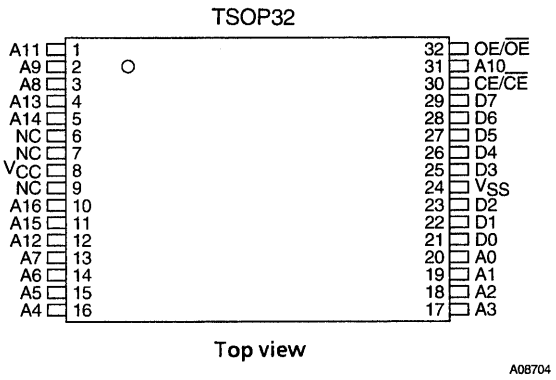
SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Pin Assignments

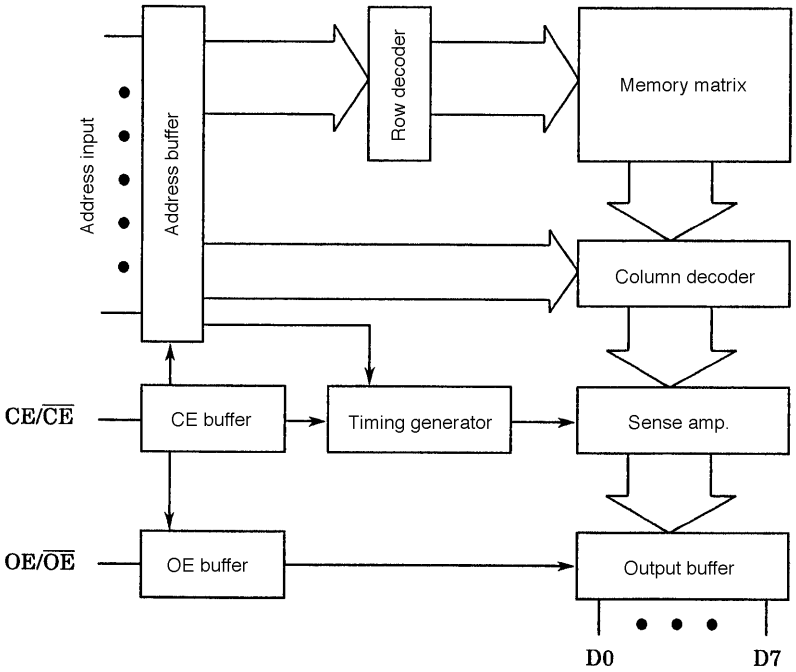


Pin Functions

A0 to A16	Address input
D0 to D7	Data output
CE/$\overline{CE}$	Chip enable input
OE/$\overline{OE}$	Output enable input
V_{CC}	Power supply
V_{SS}	Ground



Block Diagram



Truth Table

CE/$\overline{CE}$	OE/$\overline{OE}$	Output	Current drain
L/H	X	High-impedance	Standby mode
H/L	L/H	High-impedance	Operating mode
H/L	H/L	DOUT	Operating mode

X: H or L level should be offered.

Specifications

Absolute Maximum Ratings *1

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		–0.3 to +7.0	V
Supply input voltage	V_{IN}		–0.3*2 to V_{CC} + 0.3	V
Supply output voltage	V_{OUT}		–0.3 to V_{CC} + 0.3	V
Allowable power dissipation	Pd max	Ta = 25°C; Reference values for the SANYO DIP package	1.0	W
Operating temperature	Topr		0 to +70	°C
Storage temperature	Tstg		–55 to +125	°C

Note: 1. Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to Recommended Operating Conditions.
2. V_{IN} (min) = –3.0 V (pulse width ≤ 30 ns)

Input/Output Capacitance* at Ta = 25°C, f = 1.0 MHz

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input capacitance	C_{IN}	V_{IN} = 0 V; Reference values for the SANYO DIP package			8	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V; Reference values for the SANYO DIP package			10	pF

Note: * This parameter is periodically sampled and not 100% tested.

3 V Operation

DC Recommended Operating Ranges at Ta = 0 to +70°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{CC} max		2.7	3.0	3.6	V
Input high level voltage	V_{IH}		0.8 V_{CC}		V_{CC} + 0.3	V
Input low level voltage	V_{IL}		–0.3		+0.4	V

DC Electrical Characteristics at Ta = 0 to +70°C, V_{CC} = 2.7 to 3.6 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Operating supply current	I_{CCA1}	$\overline{CE}$ = 0.2 V (CE = V_{CC} – 0.2 V), V_I = V_{CC} – 0.2 V/0.2 V			15	mA
	I_{CCA2}	$\overline{CE}$ = V_{IL} (CE = V_{IH}), I_O = 0 mA, V_I = V_{IH}/V_{IL}, f = 5 MHz			20	mA
Standby supply current	I_{CCS1}	$\overline{CE}$ = V_{CC} – 0.2 V (CE = 0.2 V)			5 (0.5*)	µA
	I_{CCS2}	$\overline{CE}$ = V_{IH} (CE = V_{IL})			50 (10*)	µA
Input leakage current	I_{LI}	V_{IN} = 0 to V_{CC}			±1.0	µA
Output leakage current	I_{LO}	$\overline{CE}$ or $\overline{OE}$ = V_{IH} (CE or OE = V_{IL}), V_{OUT} = 0 to V_{CC}			±1.0	µA
Output high level voltage	V_{OH}	I_{OH} = –0.5 mA	V_{CC} – 0.2			V
Output low level voltage	V_{OL}	I_{OL} = 0.5 mA			0.2	V

Note: * Guaranteed at Ta = 25°C

AC Characteristics at Ta = 0 to +70°C, V_{CC} = 2.7 to 3.6 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Cycle time	t_{CYC}		200 (150*2)			ns
Address access time	t_{AA}				200 (150*2)	ns
$\overline{CE}$ access time	t_{CA}				200 (150*2)	ns
$\overline{OE}$ access time	t_{OA}				80 (60*2)	ns
Output hold time	t_{OH}		25			ns
Output disable time*1	t_{OD}				50	ns

Note: 1. t_{OD} is measured from the earlier edge of the $\overline{CE}$ (CE) or $\overline{OE}$(OE)'s going high impedance. This parameter is periodically sampled and not 100% tested.
2. Guaranteed at V_{CC} = 3.0 to 3.6 V

5 V Operation

DC Recommended Operating Ranges at Ta = 0 to +70°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{CC} max		4.5	5.0	5.5	V
Input high level voltage	V_{IH}		2.2		V_{CC} + 0.3	V
Input low level voltage	V_{IL}		–0.3		+0.6	V

DC Characteristics at Ta = 0 to +70°C, V_{CC} = 5.0 V ±10%

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Operating supply current	I_{CCA1}	$\overline{CE}$ = 0.2 V (CE = V_{CC} – 0.2 V), V_I = V_{CC} – 0.2 V/0.2 V			30	mA
	I_{CCA2}	$\overline{CE}$ = V_{IL} (CE = V_{IH}), I_O = 0 mA, V_I = V_{IH}/V_{IL}, f = 10 MHz			70	mA
Standby supply current	I_{CCS1}	$\overline{CE}$ = V_{CC} – 0.2 V (CE = 0.2 V)			30 (1.0*)	µA
	I_{CCS2}	$\overline{CE}$ = V_{IH} (CE = V_{IL})			1.0 (300*)	mA (µA)
Input leakage current	I_{LI}	V_{IN} = 0 to V_{CC}			±1.0	µA
Output leakage current	I_{LO}	$\overline{CE}$ or $\overline{OE}$ = V_{IH} (CE or OE = V_{IL}), V_{OUT} = 0 to V_{CC}			±1.0	µA
Output high level voltage	V_{OH}	I_{OH} = –1.0 mA	2.4			V
Output low level voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V

Note: * Guaranteed at Ta = 25°C

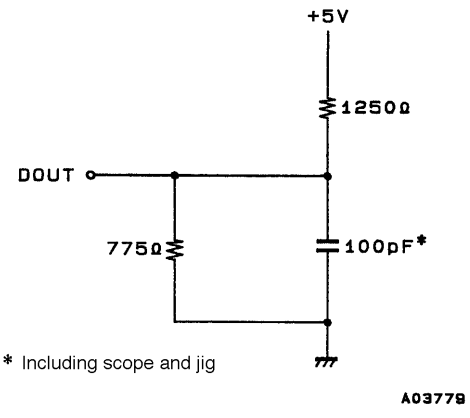
AC Characteristics at Ta = 0 to +70°C, V_{CC} = 5.0 V ±10%

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Cycle time	t_{CYC}		100			ns
Address access time	t_{AA}				100	ns
$\overline{CE}$ access time	t_{CA}				100	ns
$\overline{OE}$ access time	t_{OA}				40	ns
Output hold time	t_{OH}		20			ns
Output disable time*	t_{OD}				30	ns

Note: * t_{OD} is measured from the earlier edge of the $\overline{CE}$ (CE) or $\overline{OE}$(OE)'s going high impedance.
This parameter is periodically sampled and not 100% tested.

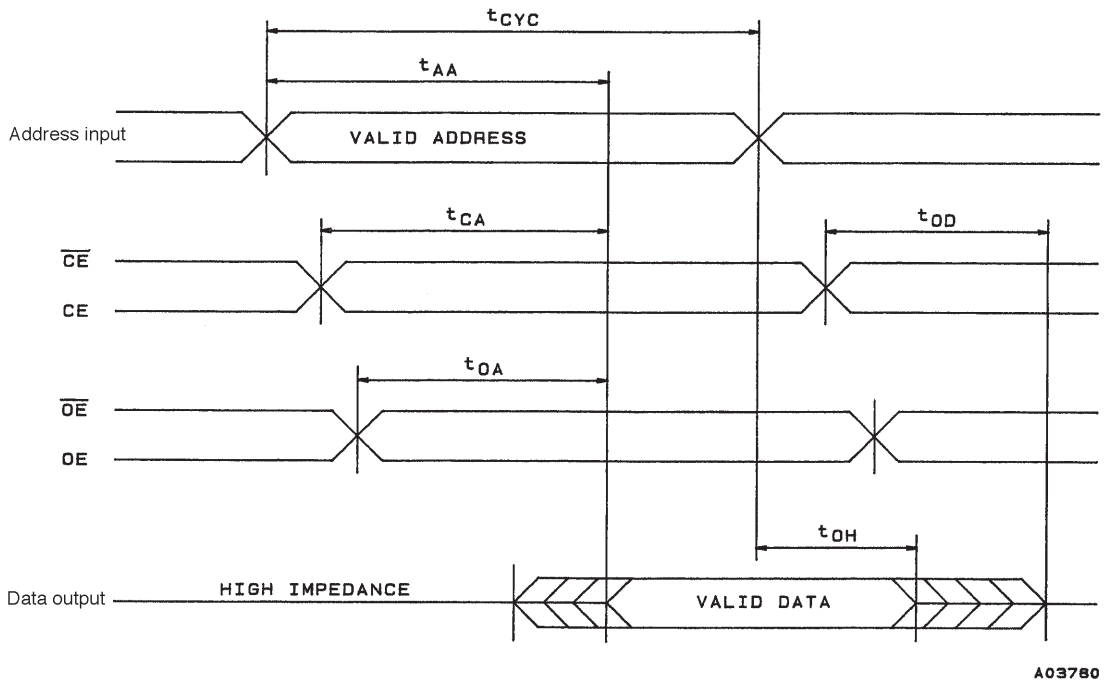
AC Test Conditions

Input pulse levels	0.4 V to 0.8 V_{CC} (3 V measurement), 0.6 V to 2.4 V (5 V measurement)
Input rise/fall time	5 ns
Input timing level	1.5 V
Output timing level	1.5 V
Output load	70 pF (3 V measurement) See figure (5 V measurement)



Output Load (5 V measurement)

Timing Chart



System Design Notes

These LSIs adopt an internal synchronization technique in which operation is started by detecting changes in either the CE input or the address inputs. As a result, the output data immediately after power on is invalid. Once power has been applied, valid data is output after the application changes the value of either the CE input or at least one of the address inputs.

Another point due to the use of the ATD technique is that these LSIs are extremely sensitive to input noise. Applications must take precautions to provide stable input signals, both for the CE input and the address inputs, to prevent incorrect operation.