



# LC371100SP, SM, ST-10/20LV

## 1 MEG (131072 words × 8 bits) Mask ROM Internal Clocked Silicon Gate

### Preliminary

### Overview

The LC371100SP, LC371100SM and LC371100ST are 131,072-word × 8-bit organization (1,048,576-bit) mask programmable read only memories.

The LC371100SP-10, LC371100SM-10 and LC371100ST-10 feature an access time of 100 ns, an OE access time of 40 ns, and a standby current of 30 μA, and are optimal for use in 5-V systems that require high-speed access.

The LC371100SP-20LV, LC371100SM-20LV and LC371100ST-20LV feature an access time of 200 ns, an OE access time of 80 ns, and a standby current of 4 μA. Additionally, they provide high-speed access in 3.3-V systems (3.0 to 3.6 V) with a 150-ns access time and a 60-ns OE access time.

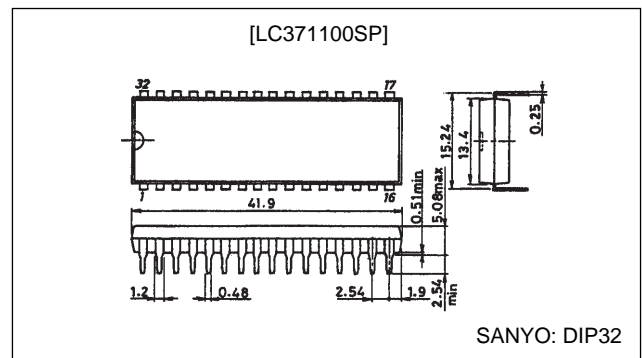
These ROMs adopt the JEDEC standard pin assignment which allows them to replace EPROM easily. To prevent bus line collisions in multi-bus microcontroller systems, pin 24 can be mask programmed to be either active high or active low.

### Features

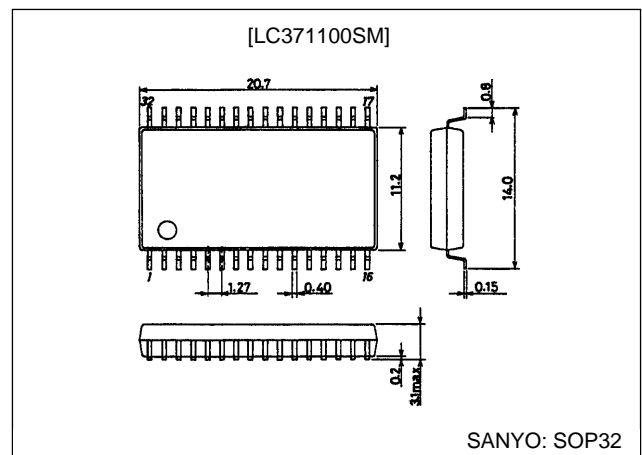
- 131072 words × 8 bits organization
- Power supply
  - LC371100SP, SM, ST-10: 5.0 V ± 10%
  - LC371100SP, SM, ST-20LV: 2.7 to 3.6 V
- Fast access time ( $t_{AA}$ ,  $t_{CA}$ )
  - LC371100SP, SM, ST-10: 100 ns (max.)
  - LC371100SP, SM, ST-20LV: 200 ns (max.)
  - 150 ns ( $V_{CC} = 3.0$  to 3.6 V)
- Operating current
  - LC371100SP, SM, ST-10: 70 mA (max.)
  - LC371100SP, SM, ST-20LV: 20 mA (max.)
- Standby current
  - LC371100SP, SM, ST-10: 30 μA (max.)
  - LC371100SP, SM, ST-20LV: 5 μA (max.)
- Full static operation (internal clocked type)
- Fully TTL compatible (5 V supply)
- 3 state outputs
- JEDEC standard pin configuration
- Package type
  - LC371100SP-10/20LV: DIP32 (600 mil)
  - LC371100SM-10/20LV: SOP32 (525 mil)
  - LC371100ST-10/20LV: TSOP32 (8 mm × 20 mm)

### Package Dimensions

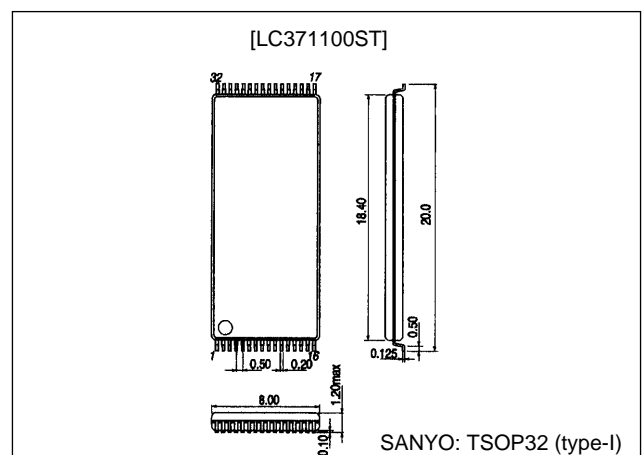
unit: mm  
3192-DIP32



unit: mm  
3205-SOP32



unit: mm  
3224-TSOP32

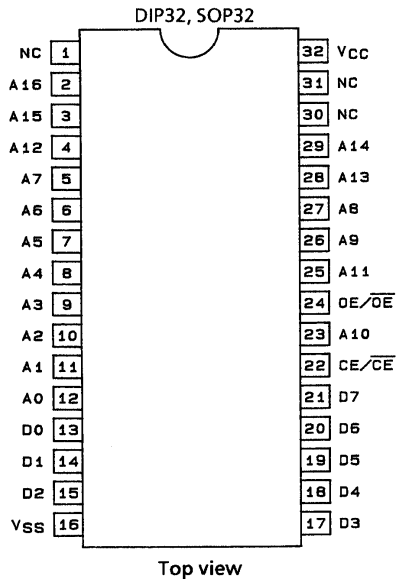


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## Pin Assignments

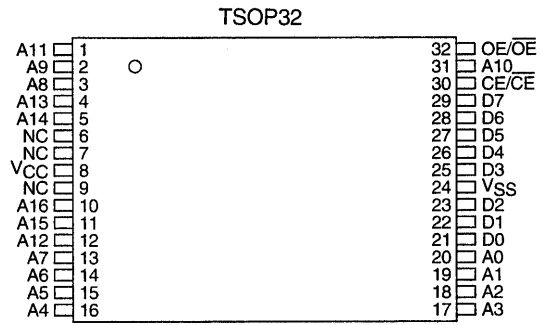


Top view

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## Pin Functions

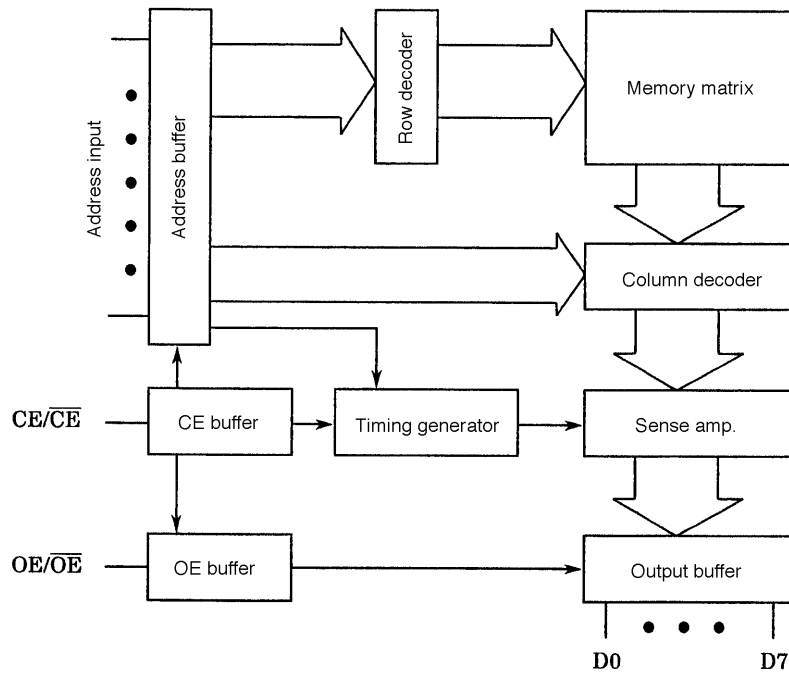
A0 to A16	Address input
D0 to D7	Data output
CE/CE-bar	Chip enable input
OE/OE-bar	Output enable input
VCC	Power supply
VSS	Ground



Top view

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## Block Diagram



## Truth Table

CE/CE-bar	OE/OE-bar	Output	Current drain
L/H	X	High-impedance	Standby mode
H/L	L/H	High-impedance	Operating mode
H/L	H/L	DOUT	Operating mode

X: H or L level should be offered.

## Specifications

### Absolute Maximum Ratings \*1

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC}$ max		-0.3 to +7.0	V
Supply input voltage	$V_{IN}$		-0.3*2 to $V_{CC} + 0.3$	V
Supply output voltage	$V_{OUT}$		-0.3 to $V_{CC} + 0.3$	V
Allowable power dissipation	$P_d$ max	$T_a = 25^\circ\text{C}$ ; Reference values for the SANYO DIP package	1.0	W
Operating temperature	$T_{opr}$		0 to +70	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-55 to +125	$^\circ\text{C}$

Note: 1. Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to Recommended Operating Conditions.

2.  $V_{IN}$  (min) = -3.0 V (pulse width  $\leq 30$  ns)

### Input/Output Capacitance\* at $T_a = 25^\circ\text{C}$ , $f = 1.0$ MHz

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input capacitance	$C_{IN}$	$V_{IN} = 0$ V; Reference values for the SANYO DIP package			8	pF
Output capacitance	$C_{OUT}$	$V_{OUT} = 0$ V; Reference values for the SANYO DIP package			10	pF

Note: \* This parameter is periodically sampled and not 100% tested.

## 3 V Operation

### DC Recommended Operating Ranges at $T_a = 0$ to $+70^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{CC}$ max		2.7	3.0	3.6	V
Input high level voltage	$V_{IH}$		$0.8 V_{CC}$		$V_{CC} + 0.3$	V
Input low level voltage	$V_{IL}$		-0.3		+0.4	V

### DC Electrical Characteristics at $T_a = 0$ to $+70^\circ\text{C}$ , $V_{CC} = 2.7$ to $3.6$ V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Operating supply current	$I_{CCA1}$	$\overline{CE} = 0.2$ V ( $CE = V_{CC} - 0.2$ V), $V_I = V_{CC} - 0.2$ V/0.2 V			15	mA
	$I_{CCA2}$	$\overline{CE} = V_{IL}$ ( $CE = V_{IH}$ ), $I_O = 0$ mA, $V_I = V_{IH}/V_{IL}$ , $f = 5$ MHz			20	mA
Standby supply current	$I_{CCS1}$	$\overline{CE} = V_{CC} - 0.2$ V ( $CE = 0.2$ V)			5 (0.5*)	$\mu\text{A}$
	$I_{CCS2}$	$\overline{CE} = V_{IH}$ ( $CE = V_{IL}$ )			50 (10*)	$\mu\text{A}$
Input leakage current	$I_{LI}$	$V_{IN} = 0$ to $V_{CC}$			$\pm 1.0$	$\mu\text{A}$
Output leakage current	$I_{LO}$	$\overline{CE}$ or $\overline{OE} = V_{IH}$ ( $CE$ or $OE = V_{IL}$ ), $V_{OUT} = 0$ to $V_{CC}$			$\pm 1.0$	$\mu\text{A}$
Output high level voltage	$V_{OH}$	$I_{OH} = -0.5$ mA	$V_{CC} - 0.2$			V
Output low level voltage	$V_{OL}$	$I_{OL} = 0.5$ mA			0.2	V

Note: \* Guaranteed at  $T_a = 25^\circ\text{C}$

### AC Characteristics at $T_a = 0$ to $+70^\circ\text{C}$ , $V_{CC} = 2.7$ to $3.6$ V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Cycle time	$t_{CYC}$		200 (150*2)			ns
Address access time	$t_{AA}$				200 (150*2)	ns
$\overline{CE}$ access time	$t_{CA}$				200 (150*2)	ns
$\overline{OE}$ access time	$t_{OA}$				80 (60*2)	ns
Output hold time	$t_{OH}$		25			ns
Output disable time*1	$t_{OD}$				50	ns

Note: 1.  $t_{OD}$  is measured from the earlier edge of the  $\overline{CE}$  ( $CE$ ) or  $\overline{OE}$  ( $OE$ )'s going high impedance.

This parameter is periodically sampled and not 100% tested.

2. Guaranteed at  $V_{CC} = 3.0$  to  $3.6$  V

5 V Operation

DC Recommended Operating Ranges at Ta = 0 to +70°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V <sub>CC</sub> max		4.5	5.0	5.5	V
Input high level voltage	V <sub>IH</sub>		2.2		V <sub>CC</sub> + 0.3	V
Input low level voltage	V <sub>IL</sub>		-0.3		+0.6	V

DC Characteristics at Ta = 0 to +70°C, V<sub>CC</sub> = 5.0 V ±10%

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Operating supply current	I <sub>CCA1</sub>	$\overline{CE} = 0.2\text{ V}$ (CE = V <sub>CC</sub> - 0.2 V), V <sub>I</sub> = V <sub>CC</sub> - 0.2 V/0.2 V			30	mA
	I <sub>CCA2</sub>	$\overline{CE} = V_{IL}$ (CE = V <sub>IH</sub> ), I <sub>O</sub> = 0 mA, V <sub>I</sub> = V <sub>IH</sub> /V <sub>IL</sub> , f = 10 MHz			70	mA
Standby supply current	I <sub>CCS1</sub>	$\overline{CE} = V_{CC} - 0.2\text{ V}$ (CE = 0.2 V)			30 (1.0*)	μA
	I <sub>CCS2</sub>	$\overline{CE} = V_{IH}$ (CE = V <sub>IL</sub> )			1.0 (300*)	mA (μA)
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = 0 to V <sub>CC</sub>			±1.0	μA
Output leakage current	I <sub>LO</sub>	$\overline{CE}$ or $\overline{OE} = V_{IH}$ (CE or OE = V <sub>IL</sub> ), V <sub>OUT</sub> = 0 to V <sub>CC</sub>			±1.0	μA
Output high level voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1.0 mA	2.4			V
Output low level voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.0 mA			0.4	V

Note: \* Guaranteed at Ta = 25°C

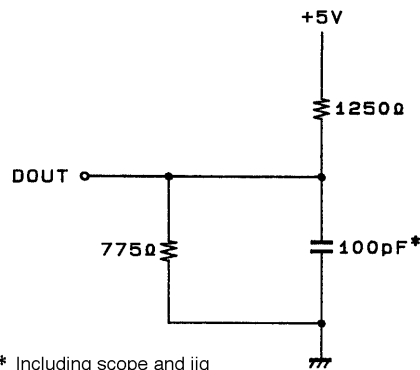
AC Characteristics at Ta = 0 to +70°C, V<sub>CC</sub> = 5.0 V ±10%

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Cycle time	t <sub>CYC</sub>		100			ns
Address access time	t <sub>AA</sub>				100	ns
$\overline{CE}$ access time	t <sub>CA</sub>				100	ns
$\overline{OE}$ access time	t <sub>OA</sub>				40	ns
Output hold time	t <sub>OH</sub>		20			ns
Output disable time*	t <sub>OD</sub>				30	ns

Note: \* t<sub>OD</sub> is measured from the earlier edge of the  $\overline{CE}$  (CE) or  $\overline{OE}$  (OE)'s going high impedance. This parameter is periodically sampled and not 100% tested.

AC Test Conditions

Input pulse levels	0.4 V to 0.8 V <sub>CC</sub> (3 V measurement), 0.6 V to 2.4 V (5 V measurement)
Input rise/fall time	5 ns
Input timing level	1.5 V
Output timing level	1.5 V
Output load	70 pF (3 V measurement) See figure (5 V measurement)

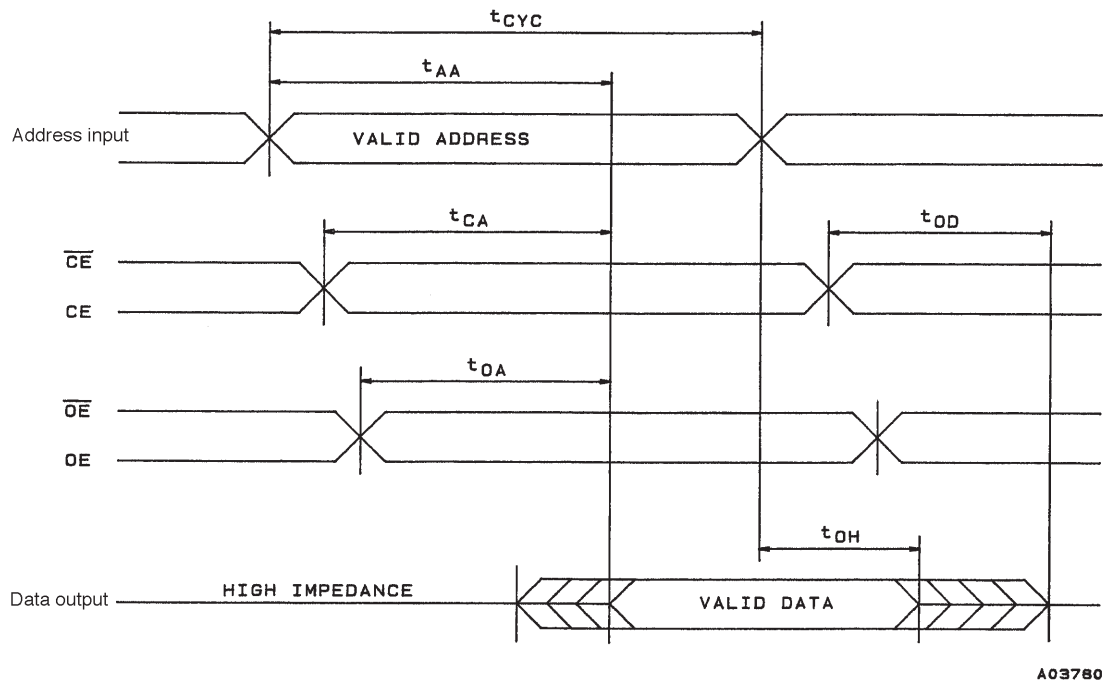


\* Including scope and jig

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Output Load (5 V measurement)

Timing Chart



System Design Notes

These LSIs adopt an internal synchronization technique in which operation is started by detecting changes in either the CE input or the address inputs. As a result, the output data immediately after power on is invalid. Once power has been applied, valid data is output after the application changes the value of either the CE input or at least one of the address inputs.

Another point due to the use of the ATD technique is that these LSIs are extremely sensitive to input noise. Applications must take precautions to provide stable input signals, both for the CE input and the address inputs, to prevent incorrect operation.

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