Asynchronous Silicon Gate CMOS LSI

SANYO

LC36256AL, AML-70/85/10/12

256 K (32768 words × 8 bits) SRAM

Overview

The LC36256AL, AML are fully asynchronous silicon gate CMOS static RAMs with an 32768 words × 8 bits configuration.

This series have $\overline{CE}$ chip enable pin for device select/nonselect control and an $\overline{OE}$ output enable pin for output control, and features high speed as well as low power dissipation.

For these reasons, the series is especially suited for use in systems requiring high speed, low power, and battery backup, and it is easy to expand memory capacity.

Features

• Access time
   70 ns (max.) : LC36256AL-70, LC36256AML-70
   85 ns (max.) : LC36256AL-85, LC36256AML-85
   100 ns (max.) : LC36256AL-10, LC36256AML-10
   120 ns (max.) : LC36256AL-12, LC36256AML-12

• Low current dissipation
   During standby
      2 μA (max.) / Ta = 25°C
      5 μA (max.) / Ta = 0 to +40°C
      25 μA (max.) / Ta = 0 to +70°C

   During data retention
      1 μA (max.) / Ta = 25°C
      2 μA (max.) / Ta = 0 to +40°C
      10 μA (max.) / Ta = 0 to +70°C

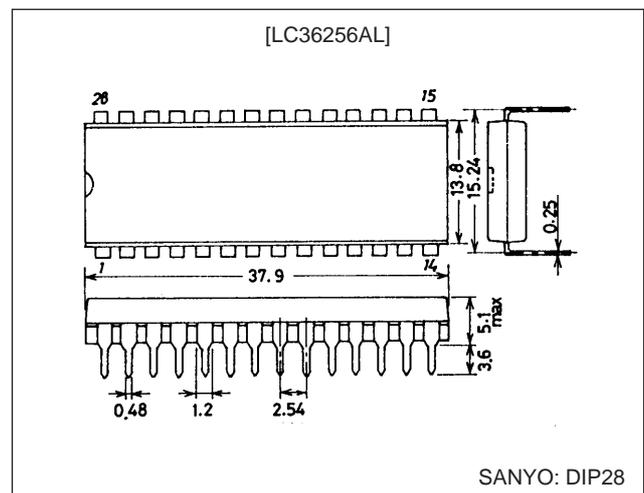   During operation (DC)
      10 mA (max.)

• Single 5 V power supply: 5 V ±10%

• Data retention power supply voltage: 2.0 to 5.5 V

• No clock required (Fully static memory)

• All input/output levels are TTL compatible

• Common input/output pins, with three output states

• Packages
   DIP 28 -pin (600 mil) plastic package : LC36256AL
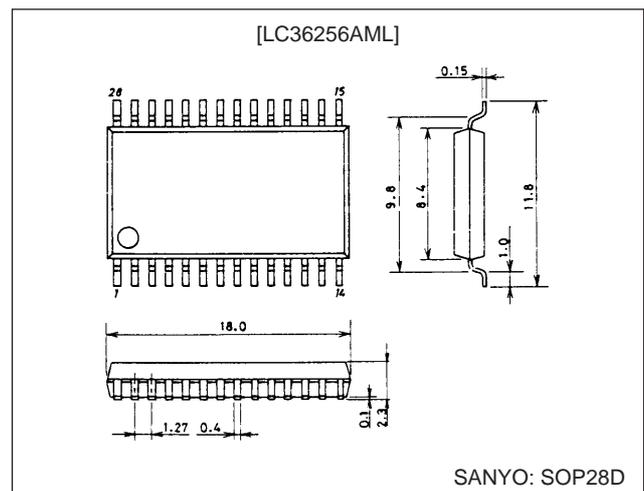   SOP 28-pin (450 mil) plastic package : LC36256AML

Package Dimensions
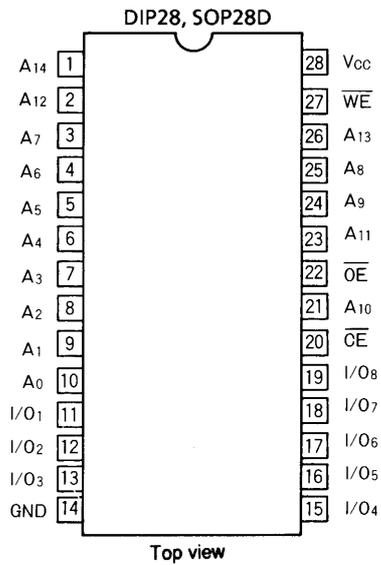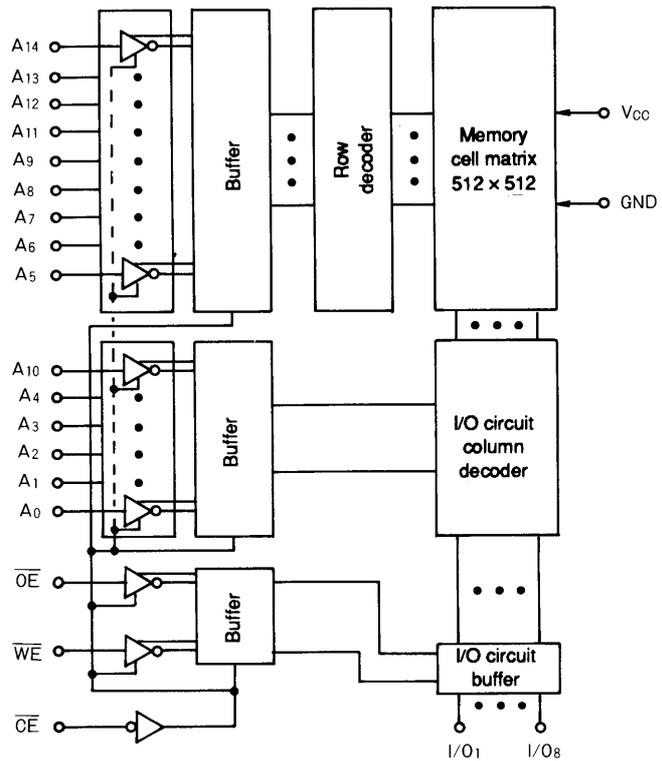
unit: mm
3012A - DIP28

[LC36256AL]

SANYO: DIP28

unit : mm
3187 - SOP28D

[LC36256AML]

SANYO: SOP28D

Pin Assignment

DIP28, SOP28D

A_{14}	1	28	V_{CC}
A_{12}	2	27	$\overline{WE}$
A_7	3	26	A_{13}
A_6	4	25	A_8
A_5	5	24	A_9
A_4	6	23	A_{11}
A_3	7	22	$\overline{OE}$
A_2	8	21	A_{10}
A_1	9	20	$\overline{CE}$
A_0	10	19	I/O_8
I/O_1	11	18	I/O_7
I/O_2	12	17	I/O_6
I/O_3	13	16	I/O_5
GND	14	15	I/O_4

Top view

Block Diagram

Pin Functions

A0 to A14	Address input
$\overline{WE}$	Read/write control input
$\overline{OE}$	Output enable input
$\overline{CE}$	Chip enable input
I/O1 to I/O8	Data input/output
VCC, GND	Power supply pins

Functions

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	Supply current
Read cycle	L	L	H	Data output	I_{CCA}
Write cycle	L	X	L	Data input	I_{CCA}
Output disable	L	H	H	High impedance	I_{CCA}
Nonselect	H	X	X	High impedance	I_{CCS}

X : H or L

Specifications

Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	Vcc max		7.0	V
Input pin voltage	VIN		−0.5* to Vcc+0.5	V
I/O pin voltage	VI/O		−0.5* to Vcc+0.5	V
Allowable power dissipation	Pd max	LC36256AL	1.0	W
		LC36256AML	0.7	W
Operating temperature range	Topr		0 to +70	°C
Storage temperature range	Tstg		−55 to +150	°C

* −3.0 V when pulse width is less than 50 ns

DC Recommended Operating Ranges at Ta = 0 to +70°C

Parameter	Symbol	min	typ	max	Unit
Power supply voltage	Vcc	4.5	5.0	5.5	V
Input high level voltage	VIH	2.2		Vcc+0.3	V
Input low level voltage	VIL	−0.3*		+0.8	V

* −3.0 V when pulse width is less than 50 ns

DC Electrical Characteristics at Ta = 0 to +70°C, Vcc = 5 V ±10%

Parameter	Symbol	Conditions			min	typ*	max	Unit
Input leakage current	ILI	VIN = 0 to Vcc			−0.5		+0.5	µA
I/O leakage current	ILO	V$\overline{CE}$ = VIH or V$\overline{OE}$ = VIH, VI/O = 0 to Vcc			−0.5		+0.5	µA
Output high level voltage	VOH	IOH = −1.0mA			2.4			V
Output low level voltage	VOL	IOL = 2.1mA					0.4	V
Operating supply current (DC)	ICCA1	V$\overline{CE}$ ≤ 0.2V, VIN ≤ 0.2V or VIN ≥ Vcc−0.2V				1	5	mA
	ICCA2	V$\overline{CE}$ = VIL, II/O=0mA				3	10	mA
Average operating supply current	ICCA3	min cycle Duty = 100% I I/O = 0mA	Access time	70ns		30	50	mA
				85ns		25	50	
				100ns		23	50	
				120ns		20	50	
Standby supply current	ICCS1	V$\overline{CE}$ ≥V$_{CC}$-0.2V		0 to +70°C			25	µA
				0 to +40°C			5	
				25°C		0.5	2	
	ICCS2	V$\overline{CE}$ = VIH				0.4	2	mA

* Reference values at Vcc = 5 V, Ta = 25°C

Input/Output Capacitance at Ta = 25°C, f = 1 MHz

Parameter	Symbol	Conditions	min	typ	max	Unit
Input/output capacitance	C$_{I/O}$	V$_{I/O}$ = 0V			8	pF
Input capacitance	C$_{IN}$	V$_{IN}$ = 0V			6	pF

Note: These parameters were obtained through sampling, and not full-lot measurement.

AC Electrical Characteristics at Ta = 0 to +70°C, V$_{CC}$ = 5 V ±10%

AC testing conditions

Input pulse voltage level	:	0.8 V, 2.2 V
Input rise and fall time	:	5 ns
Input - output timing level	:	1.5 V
Output load	:	1 TTL gate + C$_L$ = 100 pF (85 ns/100 ns/120 ns)
		1 TTL gate + C$_L$ = 30 pF (70 ns)
		(including scope and jig capacitance)

Read Cycle

Parameter	Symbol	LC36256AL, AML								Unit
		-70		-85		-10		-12		
		min	max	min	max	min	max	min	max	
Read cycle time	t$_{RC}$	70		85		100		120		ns
Address access time	t$_{AA}$		70		85		100		120	ns
$\overline{CE}$ access time	t$_{CA}$		70		85		100		120	ns
$\overline{OE}$ access time	t$_{OA}$		35		45		50		60	ns
Output hold time	t$_{OH}$	20		20		20		20		ns
$\overline{CE}$ output enable time	t$_{COE}$	10		10		10		10		ns
$\overline{OE}$ output enable time	t$_{OOE}$	5		5		5		5		ns
$\overline{OE}$ output disable time	t$_{COD}$	0	30	0	30	0	30	0	30	ns
$\overline{OE}$ output disable time	t$_{OOD}$	0	30	0	30	0	30	0	30	ns

Write Cycle

Parameter		LC36256AL, AML								Unit
		-70		-85		-10		-12		
		min	max	min	max	min	max	min	max	
Write cycle time	t$_{WC}$	70		85		100		120		ns
Address valid to end of write	t$_{AW}$	65		75		80		100		ns
Address setup time	t$_{AS}$	0		0		0		0		ns
Write pulse width	t$_{WP}$	50		50		60		70		ns
$\overline{CE}$ setup time	t$_{CW}$	65		75		80		100		ns
Write recovery time ($\overline{WE}$)	t$_{WR}$	0		0		0		0		ns
Write recovery time ($\overline{CE}$)	t$_{WR}$1	0		0		0		0		ns
Data setup time	t$_{DS}$	30		30		35		40		ns
Data hold time	t$_{DH}$	0		0		0		0		ns
$\overline{WE}$ output enable time	t$_{WOE}$	10		10		10		10		ns
$\overline{WE}$ output disable time	t$_{WOD}$	0	25	0	25	0	25	0	25	ns

Timing Chart

• Read Cycle (1): $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$

• Read Cycle (2): $\overline{WE} = V_{IH}$

• Write Cycle (1): $\overline{WE}$ Control Note (6)

• Write Cycle (2): $\overline{CE}$ Control Note (6)
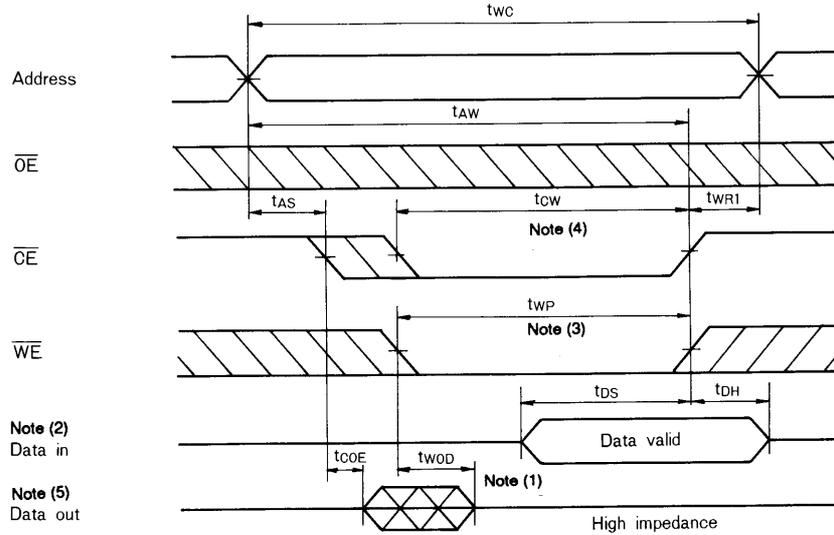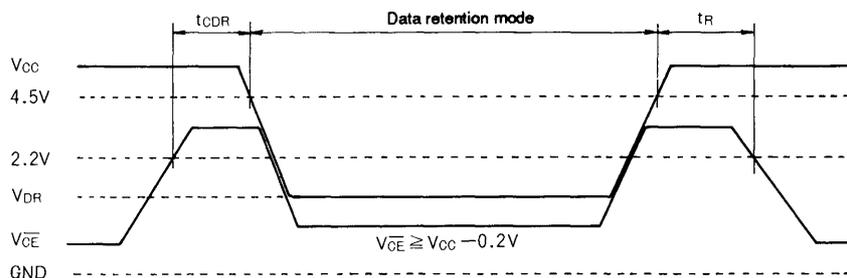

Notes   (1) t_{COD}, t_{OOD}, and t_{WOD} are defined as the time at which the outputs becomes the high impedance state and are not referred to output voltage levels.

(2) An external antiphase signal must not be applied when DOUT is in the output state.

(3) t_{WP} is the time interval that $\overline{CE}$ and $\overline{WE}$ are low-level and is defined as the interval from the falling of $\overline{WE}$ to the rising of $\overline{CE}$ or $\overline{WE}$ whichever is earlier.

(4) t_{CW} is the time interval that $\overline{CE}$ and $\overline{WE}$ are low-level and is defined as the time from the falling of $\overline{CE}$ to the rising of $\overline{CE}$ or $\overline{WE}$ whichever is earlier.

(5) DOUT goes to the high-impedance state when either $\overline{OE}$ is high-level, $\overline{CE}$ is high-level, or $\overline{WE}$ is low-level.

(6) When $\overline{OE}$ is high-level during the write cycle, DOUT goes to the high-impedance state.

Data Retention Characteristics at Ta = 0 to +70°C

Parameter	Symbol	Conditions		min	typ*	max	Unit
Data retention supply voltage	VDR	$V\overline{CE} \geq Vcc{-}0.2V$		2.0		5.5	V
Data retention supply current	ICCDR1	$Vcc = 3.0V$, $V\overline{CE} \geq 2.8V$	0 to +70°C			10	μA
			0 to +40°C			2	
			25°C		0.25	1	
	ICCDR2	$Vcc = 2.0$ to $5.5V$, $V\overline{CE} \geq Vcc{-}0.2V$			0.5	25	μA
$\overline{CE}$ setup time	t_{CDR}			0			ns
$\overline{CE}$ hold time	t_R			$t_{RC}{**}$			ns

*   Reference values at VCC = 5V, Ta = 25°C   ** t_{RC} = Read Cycle time

Data Retention Waveform

This catalog provides information as of February, 1996. Specifications and information herein are subject to change without notice.