Ordering number: EN 4484B

CMOS LSI

LC3564RM,RT-10LV/12LV/15LV

64K (8192 words × 8 bits) SRAM

Overview

The LC3564RM,RT are 8192-word × 8bit, asynchronous, silicon gate, low-voltage CMOS SRAM LSIs.They operate from a 2.0 to 3.6V supply, making them ideal for handheld, battery-operated equipment.

They are fully CMOS devices employing 2-layer A1 wiring to realize high-speed access, low operating current consumption and very low standby current. They incorporate control signal inputs; $\overline{OE}$ for high-speed memory access, and 2 chip enables $\overline{CE1}$ and CE2 for power-down and device selection.

They are ideal for systems requiring high speed, low power and battry backup or for easy mamory expansion. The very low standby current means that backup can also be achieved using a capacitor.

Features

■ Supply voltage range: 2.0 to 3.6V

- 3V operation: 2.7 to 3.6V
- Battery operation: 2.0 to 2.4V

■ High-speed access time

- 3V operation
  - LC3564RM,RT-10LV: 100ns (max)
  - LC3564RM,RT-12LV: 120ns (max)
  - LC3564RM,RT-15LV: 150ns (max)
- Battery operation
  - LC3564RM,RT-10LV: 200ns (max)
  - LC3564RM,RT-12LV: 250ns (max)
  - LC3564RM,RT-15LV: 300ns (max)

■Very-low standby current

- 3V operation
  - Ta ≤ 70°C: 1.0µA
  - Ta ≤ 85°C: 3.0µA
- Battery operation
  - Ta ≤ 70°C: 0.85µA
  - Ta ≤ 85°C: 2.5µA

■ Operating temperature range: –40 to +85°C

■ Data retention supply voltage: 2.0 to 3.6V

■ Input/output levels: CMOS Compatible (0.8Vcc/0.2Vcc)

■ 3 control inputs ($\overline{OE}$, $\overline{CE1}$, CE2)

■ Common-pin input/outputs, 3-state output

■ Clock not needed (fully-static RAM)

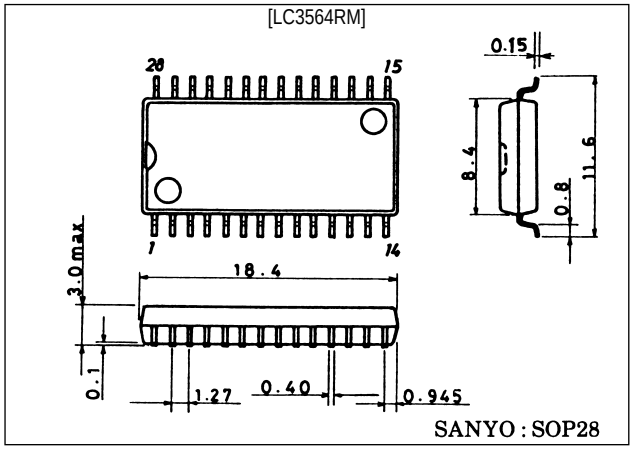
■ Package

- SOP 28-pin (450mil) plastic package: LC3564RM series
- TSOP 28-pin (8 × 13.4mm) plastic package: LC3564RT series

Package Dimensions

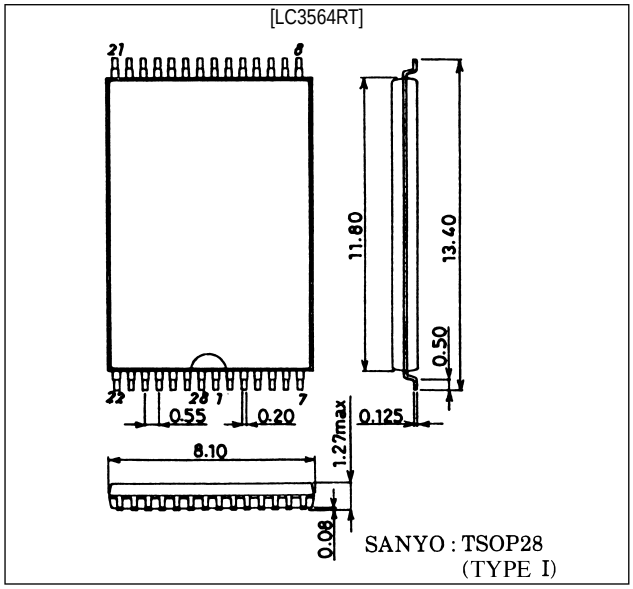
unit: mm

3158 - SOP28

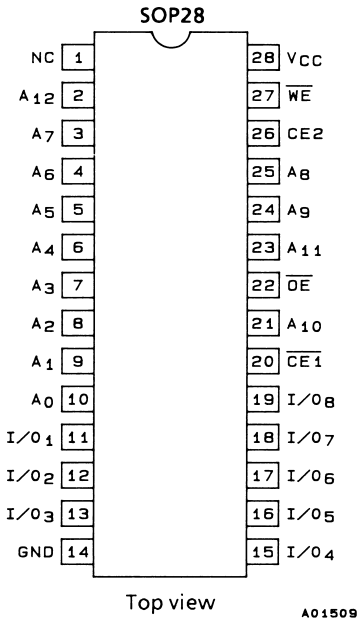


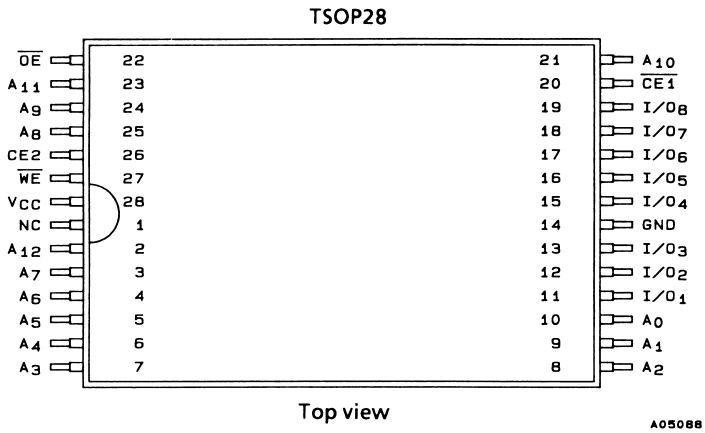
unit: mm

3221 - TSOP28

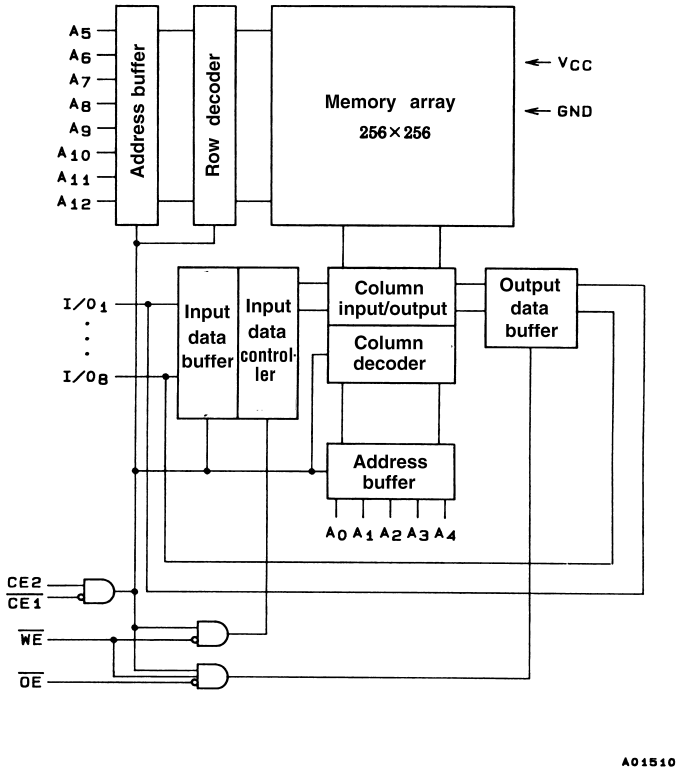


Pin Assignment





Block Diagram



Pin Functions

Number	Name	Function
1	NC	No connection
2 to 10, 21, 23 to 25	A0 to A12	Address inputs
27	$\overline{WE}$	Read/write control input
22	$\overline{OE}$	Output enable input
20, 26	$\overline{CE1}$, CE2	Chip enable inputs
11 to 13, 15 to 19	I/O1 to I/O8	Data input/outputs
28, 14	V_{CC}, GND	Supply and ground pins

Truth Table

Mode	$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE1}$	I/O	Supply current
Read cycle	L	H	L	H	Data output	I_{CCA}
Write cycle	L	H	X	L	Data input	I_{CCA}
Output disable	L	H	H	H	High impedance	I_{CCA}
No selection	H	X	X	X	High impedance	I_{CCS}
	X	L	X	X	High impedance	I_{CCS}

Note: X = H or L

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC\ max}$		4.6	V
Input voltage range	V_{IN}		–0.3 to V_{CC} + 0.3	V
Input/output voltage range	$V_{I/O}$		–0.3 to V_{CC} + 0.3	V
Operating temperature range	T_{opr}		–40 to +85	°C
Storage temperature range	T_{stg}		–55 to +125	°C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to Recommended operating conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

Inout/Output Capacitance at Ta = 25°C, f = 1 MHz

Parameter	Symbol	Conditions	Ratings			Unit
			min.	typ.	max.	
Input/output pin capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	-	6	10	pF
Input pin capacitance	C_I	V_I = 0V	-	6	10	pF

Note: Measured samples only.

3V Operation

DC Recommended Operating Ranges at Ta = –40 to +85°C, V_{CC} = 2.7 to 3.6V

Parameter	Symbol	Ratings			Unit
		min.	typ.	max.	
Supply voltage	V_{CC}	2.7	3.0	3.6	V
Input voltage	V_{IH}	$0.8V_{CC}$	-	V_{CC} + 0.3	V
	V_{IL}	–0.3*	-	$0.2V_{CC}$	V

* When pulsewidth is less than 30 ns, the minimum value is -2.0V.

DC Electrical Characteristics at Ta = –40 to +85°C, V_{CC} = 2.7 to 3.6V

Parameter		Symbol	Conditions		Ratings			Unit
					min.	typ.*	max.	
Input leakage current		I_{LI}	V_{IN} = 0V to V_{CC}		–1.0	-	+1.0	µA
I/O leakage current		I_{LO}	$V_{\overline{CE1}} = V_{IH}$ or $V_{CE2} = V_{IL}$ or $V_{\overline{OE}} = V_{IH}$ or $V_{\overline{WE}} = V_{IL}$, $V_{I/O}$ = 0V to V_{CC}		–1.0	-	+1.0	µA
Output high level voltage		V_{OH}	I_{OH} = –2.0mA		V_{CC} – 0.4	-	-	V
Output low level voltage		V_{OL}	I_{OL} = 2.0mA		-	-	0.4	V
Operating supply current	V_{CC} – 0.2V/0.2V input	I_{CCA1}	$V_{\overline{CE1}} \le 0.2V$, $V_{CE2} \ge V_{CC}$– 0.2V, $I_{I/O}$ = 0mA, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}$– 0.2V	Ta ≤ 70°C	-	0.01	1.0	µA
				Ta ≤ 85°C	-	-	3.0	µA
	CMOS input	I_{CCA2}	$V_{\overline{CE1}} = V_{IL}$, $V_{CE2} = V_{IH}$, $I_{I/O}$ = 0mA, $V_{IN} = V_{IH}$ or V_{IL}		-	-	4	mA
		I_{CCA3}	$V_{\overline{CE1}} = V_{IL}$, $V_{CE2} = V_{IH}$, $I_{I/O}$ = 0mA, duty = 100%	min. cycle	-	-	25	mA
				200 ns cycle	-	-	15	mA
				1 µs cycle	-	-	10	mA
Standby supply current	V_{CC} – 0.2V/0.2V input	I_{CCS1}	$V_{CE2} \le 0.2V$ or {$V_{\overline{CE1}} \ge V_{CC}$– 0.2V, $V_{CE2} \ge V_{CC}$– 0.2V}	Ta ≤ 70°C	-	0.01	1.0	µA
				Ta ≤ 85°C	-	-	3.0	µA
	CMOS input	I_{CCS2}	$V_{CE2} = V_{IL}$ or $V_{\overline{CE1}} = V_{IH}$, V_{IN} = 0V to V_{CC}		-	-	1	mA

* V_{CC} = 3.0V, Ta = 25°C

AC Electrical Characteristics at Ta = –40 to +85°C, V_{CC} = 2.7 to 3.6V

AC test conditions

Input pulse voltage level: $0.2V_{CC}$ to $0.8\ V_{CC}$

Input rise and fall times: 5 ns

Input/output timing level: $V_{CC}/2$

Output load: 30 pF (including jig capacitance)

Read Cycle

Parameter	Symbol	LC3564RM,RT						Unit
		-10LV		-12LV		-15LV		
		min.	max.	min.	max.	min.	max.	
Read cycle time	t_{RC}	100	-	120	-	150	-	ns
Address access time	t_{AA}	-	100	-	120	-	150	ns
$\overline{CE1}$ access time	t_{CA1}	-	100	-	120	-	150	ns
CE2 access time	t_{CA2}	-	100	-	120	-	150	ns
$\overline{OE}$ access time	t_{OA}	-	50	-	60	-	75	ns
Output hold time	t_{OH}	10	-	10	-	10	-	ns
$\overline{CE1}$ output enable time	t_{COE1}	10	-	10	-	10	-	ns
CE2 output enable time	t_{COE2}	10	-	10	-	10	-	ns
$\overline{OE}$ output enable time	t_{OOE}	5	-	5	-	5	-	ns
$\overline{CE1}$ output disable time	t_{COD1}	-	35	-	40	-	50	ns
CE2 output disable time	t_{COD2}	-	35	-	40	-	50	ns
$\overline{OE}$ output disable time	t_{OOD}	-	25	-	30	-	40	ns

Write Cycle

Parameter	Symbol	LC3564RM,RT						Unit
		-10LV		-12LV		-15LV		
		min.	max.	min.	max.	min.	max.	
Write cycle time	t_{WC}	100	-	120	-	150	-	ns
Address setup time	t_{AS}	0	-	0	-	0	-	ns
Write pulsewidth	t_{WP}	60	-	70	-	80	-	ns
$\overline{CE1}$ setup time	t_{CW1}	70	-	80	-	90	-	ns
CE2 setup time	t_{CW2}	70	-	80	-	90	-	ns
Write recovery time	t_{WR}	0	-	0	-	0	-	ns
$\overline{CE1}$ write recovery time	t_{WR1}	0	-	0	-	0	-	ns
CE2 write recovery time	t_{WR2}	0	-	0	-	0	-	ns
Data setup time	t_{DS}	50	-	55	-	60	-	ns
Data hold time	t_{DH}	0	-	0	-	0	-	ns
$\overline{CE1}$ data hold time	t_{DH1}	0	-	0	-	0	-	ns
CE2 data hold time	t_{DH2}	0	-	0	-	0	-	ns
WE output enable time	t_{WOE}	5	-	5	-	5	-	ns
WE output disable time	t_{WOD}	-	35	-	40	-	45	ns

Battery Operation

DC Recommended Operating Ranges at Ta = –40 to +85°C, V_{CC} = 2.0 to 2.4V

Parameter	Symbol	Ratings			Unit
		min.	typ.	max.	
Supply voltage	V_{CC}	2.0	2.2	2.4	V
Input voltage	V_{IH}	$0.8V_{CC}$	-	V_{CC} + 0.3	V
	V_{IL}	–0.3	-	$0.2V_{CC}$	V

DC Electrical Characteristics at Ta = –40 to +85°C, V_{CC} = 2.0 to 2.4V

Parameter		Symbol	Conditions		Ratings			Unit
					min.	typ.*	max.	
Input leakage current		I_{LI}	V_{IN} = 0V to V_{CC}		–1.0	-	+1.0	µA
I/O leakage current		I_{LO}	$V_{\overline{CE1}} = V_{IH}$ or $V_{CE2} = V_{IL}$ or $V_{\overline{OE}} = V_{IH}$ or $V_{\overline{WE}} = V_{IL}$, $V_{I/O}$ = 0V to V_{CC}		–1.0	-	+1.0	µA
Output high level voltage		V_{OH}	I_{OH} = –0.5mA		V_{CC} – 0.2	-	-	V
Output low level voltage		V_{OL}	I_{OL} = 0.5mA		-	-	0.2	V
Operating supply current	V_{CC} – 0.2V/0.2V input	I_{CCA1}	$V_{\overline{CE1}} \le 0.2V$, $V_{CE2} \ge V_{CC}$– 0.2V, $I_{I/O}$ = 0mA, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}$– 0.2V	Ta ≤ 70°C	-	0.01	0.85	µA
				Ta ≤ 85°C	-	-	2.5	µA
	CMOS input	I_{CCA2}	$V_{\overline{CE1}} = V_{IL}$, $V_{CE2} = V_{IH}$, $I_{I/O}$ = 0mA, $V_{IN} = V_{IH}$ or V_{IL}		-	-	2	mA
		I_{CCA3}	$V_{\overline{CE1}} = V_{IL}$, $V_{CE2} = V_{IH}$, $I_{I/O}$ = 0mA, duty = 100%	min. cycle	-	-	10	mA
				1 µs cycle	-	-	5	mA
Standby supply current	V_{CC} – 0.2V/0.2V input	I_{CCS1}	$V_{CE2} \le 0.2V$ or {$V_{\overline{CE1}} \ge V_{CC}$– 0.2V, $V_{CE2} \ge V_{CC}$– 0.2V}	Ta ≤ 70°C	-	0.01	0.85	µA
				Ta ≤ 85°C	-	-	2.5	µA
	CMOS input	I_{CCS2}	$V_{CE2} = V_{IL}$ or $V_{\overline{CE1}} = V_{IH}$, V_{IN} = 0V to V_{CC}		-	-	800	mA

* V_{CC} = 2.2V, Ta = 25°C

AC Electrical Characteristics at Ta = –40 to +85°C, V_{CC} = 2.0 to 2.4V

AC test conditions

Input pulse voltage level: $0.2V_{CC}$ to $0.8\ V_{CC}$

Input rise and fall times: 10 ns

Input/output timing level: $V_{CC}/2$

Output load: 30 pF (including jig capacitance)

Read Cycle

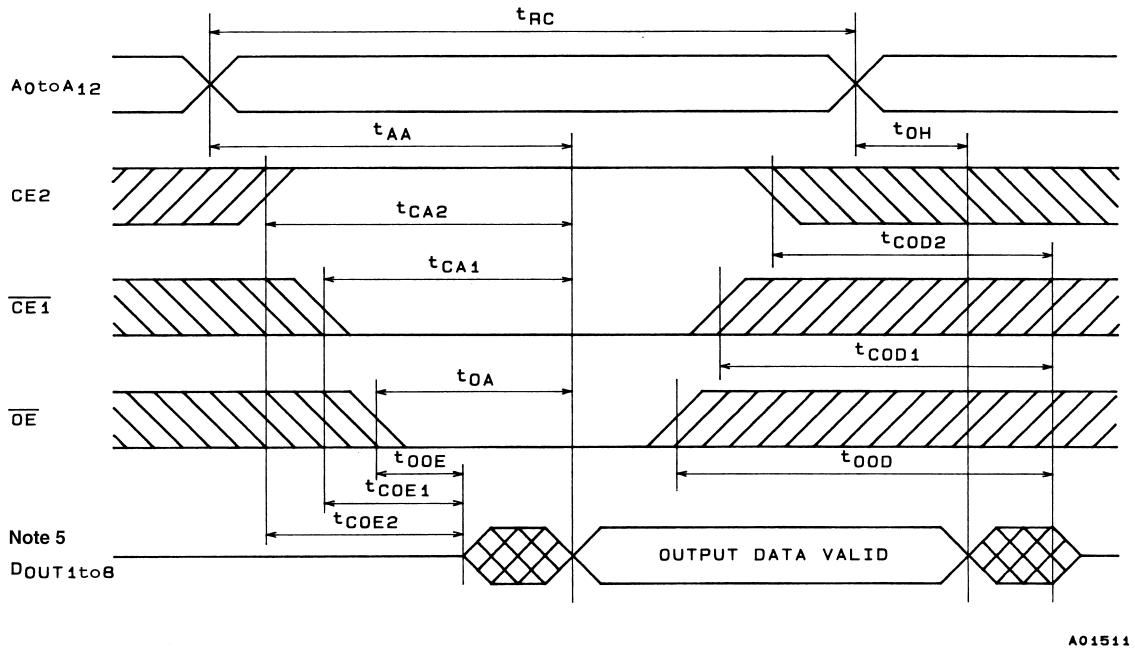
Parameter	Symbol	LC3564RM,RT						Unit
		-10LV		-12LV		-15LV		
		min.	max.	min.	max.	min.	max.	
Read cycle time	t_{RC}	200	-	250	-	300	-	ns
Address access time	t_{AA}	-	200	-	250	-	300	ns
$\overline{CE1}$ access time	t_{CA1}	-	200	-	250	-	300	ns
CE2 access time	t_{CA2}	-	200	-	250	-	300	ns
$\overline{OE}$ access time	t_{OA}	-	120	-	130	-	150	ns
Output hold time	t_{OH}	10	-	10	-	10	-	ns
$\overline{CE1}$ output enable time	t_{COE1}	10	-	10	-	10	-	ns
CE2 output enable time	t_{COE2}	10	-	10	-	10	-	ns
$\overline{OE}$ output enable time	t_{OOE}	5	-	5	-	5	-	ns
$\overline{CE1}$ output disable time	t_{COD1}	-	70	-	80	-	100	ns
CE2 output disable time	t_{COD2}	-	70	-	80	-	100	ns
$\overline{OE}$ output disable time	t_{OOD}	-	50	-	60	-	80	ns

Write Cycle

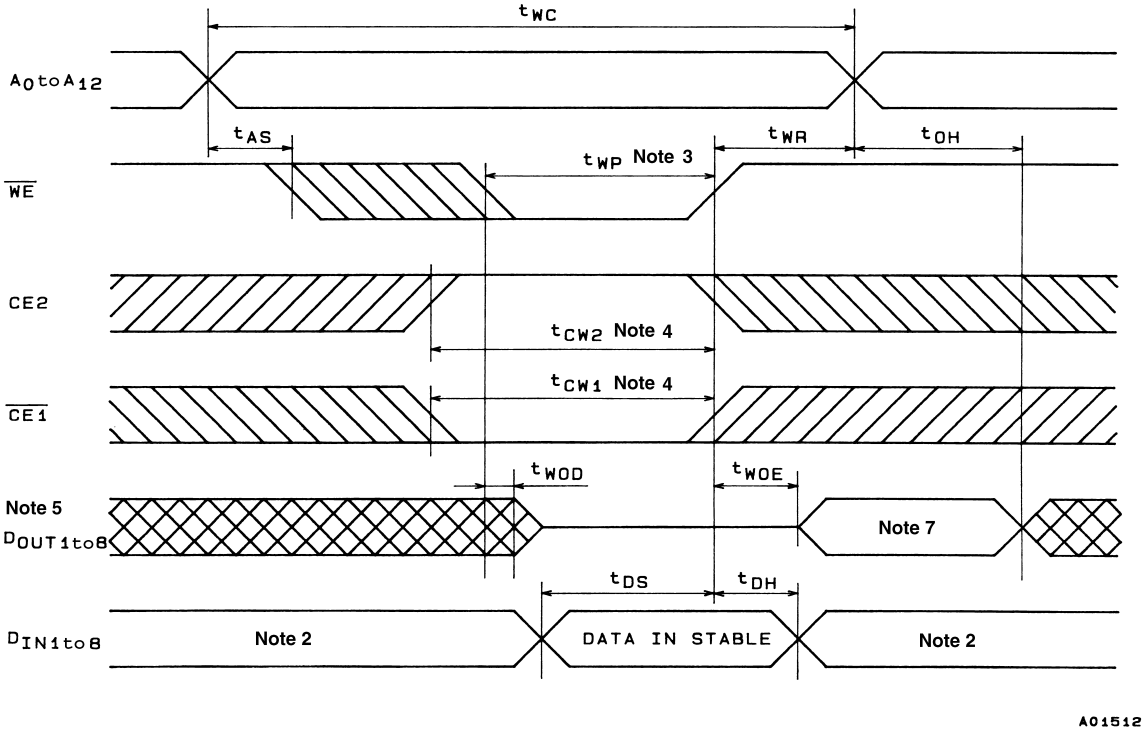
Parameter	Symbol	LC3564RM,RT						Unit
		-10LV		-12LV		-15LV		
		min.	max.	min.	max.	min.	max.	
Write cycle time	t_{WC}	200	-	250	-	300	-	ns
Address setup time	t_{AS}	0	-	0	-	0	-	ns
Write pulsewidth	t_{WP}	120	-	140	-	160	-	ns
$\overline{CE1}$ setup time	t_{CW1}	140	-	160	-	180	-	ns
CE2 setup time	t_{CW2}	140	-	160	-	180	-	ns
Write recovery time	t_{WR}	0	-	0	-	0	-	ns
$\overline{CE1}$ write recovery time	t_{WR1}	0	-	0	-	0	-	ns
CE2 write recovery time	t_{WR2}	0	-	0	-	0	-	ns
Data setup time	t_{DS}	120	-	130	-	150	-	ns
Data hold time	t_{DH}	0	-	0	-	0	-	ns
$\overline{CE1}$ data hold time	t_{DH1}	0	-	0	-	0	-	ns
CE2 data hold time	t_{DH2}	0	-	0	-	0	-	ns
WE output enable time	t_{WOE}	5	-	5	-	5	-	ns
WE output disable time	t_{WOD}	-	70	-	80	-	90	ns

Timing Chart

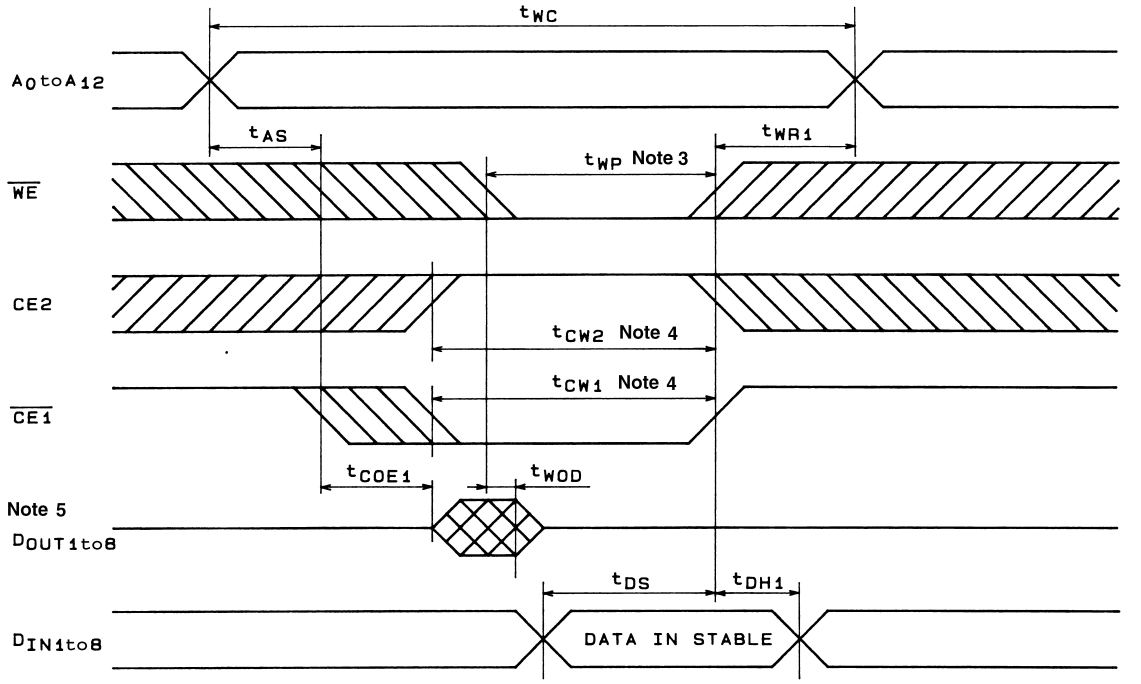
Read Cycle: Note 1



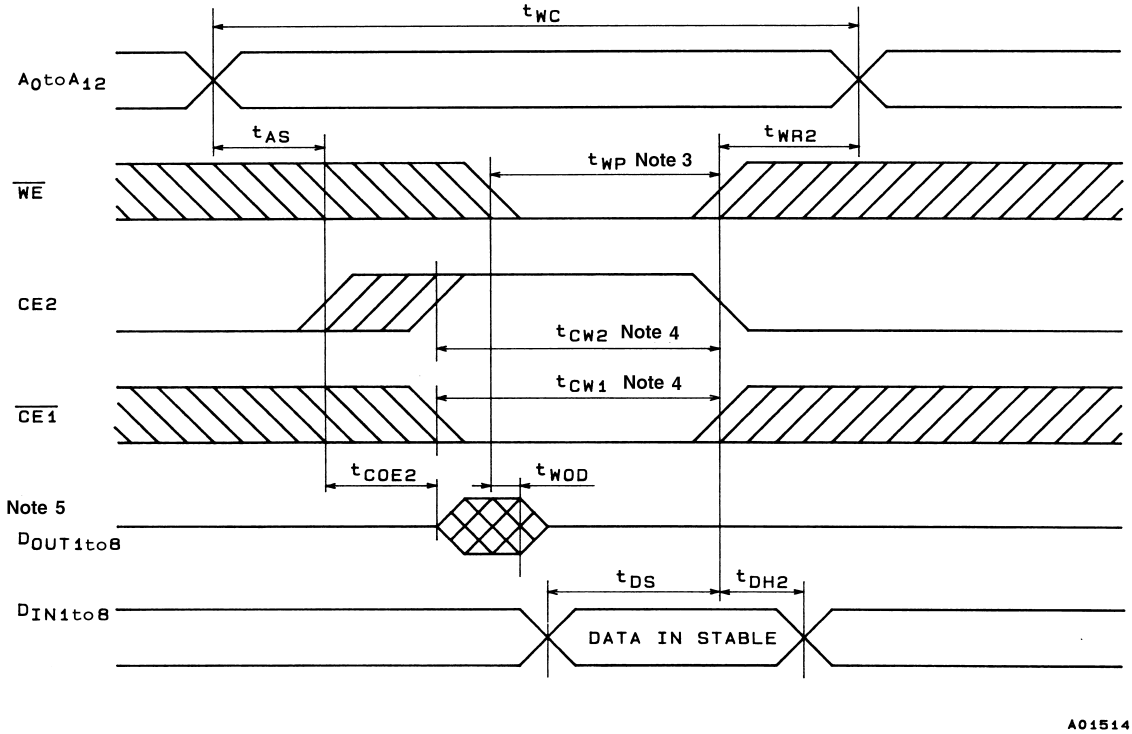
Write Cycle 1 ($\overline{WE}$ write): Note 6



Write Cycle 2 ($\overline{CE1}$ write): Note 6



Write Cycle 3 (CE2 write): Note 6



Note: 1. We should be held high level during the read cycle

2. Do not apply external signals that are out-of-phase with D_{OUT}
3. t_{WP} is a period when $\overline{CE1}$ and $\overline{WE}$ are LOW and CE2 is HIGH. It is measured from when $\overline{WE}$ goes low level to when either $\overline{CE1}$ and $\overline{WE}$ go HIGH or CE2 goes LOW, whichever occurs first.
4. t_{CW1} and t_{CW2} are periods when $\overline{CE1}$ and $\overline{WE}$ are LOW and CE2 is HIGH. They are measured from when $\overline{CE1}$ goes LOW and CE2 goes HIGH, respectively, to when either $\overline{CE1}$ and $\overline{WE}$ go HIGH or CE2 goes LOW, whichever occurs first.
5. The outputs D_{OUT1} to D_{OUT8} are in a high-impedance state when $\overline{OE}$ is HIGH, $\overline{CE1}$ is HIGH, CE2 is LOW and $\overline{WE}$ is LOW.
6. During the write cycle, $\overline{OE}$ is V_{IH} or V_{IL}.
7. D_{OUT} has the same phase as the write data.

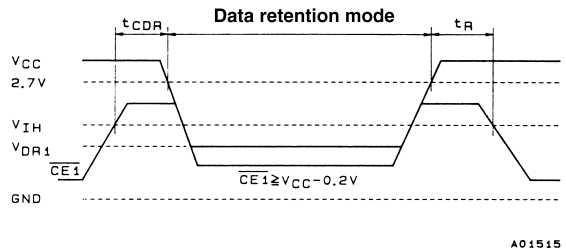
Data Retention Characteristics at Ta = –40 to +85°C

3V Operation

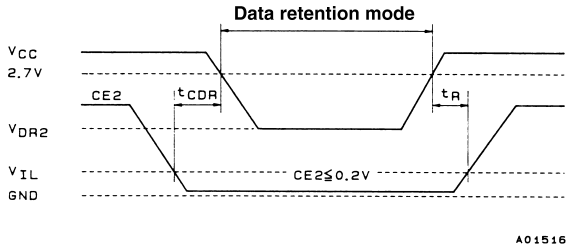
Parameter	Symbol	Conditions	Ratings			Unit
			min.	typ.	max.	
Data retention supply voltage	V_{DR}	$V_{\overline{CE1}} \geq V_{CC} - 0.2V$, $V_{CE2} \geq V_{CC} - 0.2V$ or $V_{CE2} \leq 0.2V$	2.0	-	3.6	V
Chip enable setup time	t_{CDR}		0	-	-	ns
Chip enable hold time	t_R		t_{RC}	-	-	ns

Note: t_{RC} is the read cycle time.

Data Retention Waveform 1 ($\overline{CE1}$ control)



Data Retention Waveform 2 (CE2 control)



Battery Operation

Parameter	Symbol	Conditions	Ratings			Unit
			min.	typ.	max.	
Data retention supply voltage	V_{DR}	$V_{\overline{CE1}} \geq V_{CC} - 0.2V$, $V_{CE2} \geq V_{CC} - 0.2V$ or $V_{CE2} \leq 0.2V$	2.0	-	3.6	V