



LC33832P, S, M, PL, SL, ML-70/80/10

256 K (32768 words × 8 bits) Pseudo-SRAM

Overview

The LC33832 series is composed of pseudo static RAM that operates on a single 5 V power supply and is organized as 32768 words × 8 bits. By using memory cells each composed of a single transistor and capacitor, together with peripheral CMOS circuitry, this series achieves ease of use with high density, high speed, and low power dissipation. The LC33832 series can easily accomplish auto-refresh and self-refresh by means of OE/RFSH input. As with asynchronous static RAM, WE input uses a system for incorporating input data at the WE rise, thereby facilitating interfacing with a microcomputer.

The LC33832 series features pin compatibility with 256 K static RAM (the LC36256A series), and available packages are the standard 28-pin DIP with widths of 600 mil or 300 mil, and the SOP with a width of 450 mil.

CE-only refresh can be accomplished by selecting address 256 (A0 to A7) within 4 ms.

Features

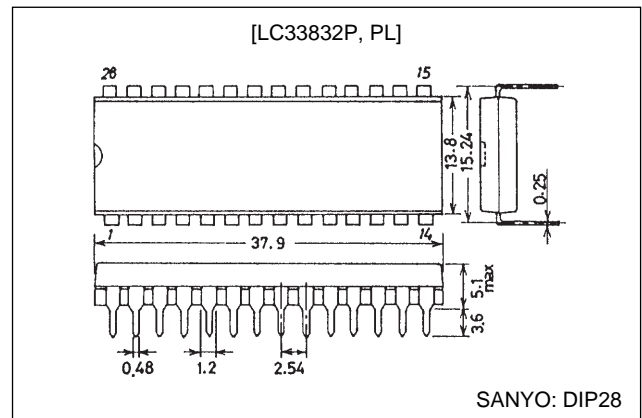
- 32768 words × 8 bits configuration
- Single 5 V ±10% power supply
- All input and output (I/O) TTL compatible
- Fast access times and low power dissipation
- 4 ms refresh using 256 refresh cycle
- CE-only refresh, auto-refresh, and self-refresh
- Low-power version: 100 µA self-refresh current
- Package

DIP28-pin (600 mil) plastic package: LC33832P, PL
 DIP28-pin (300 mil) plastic package: LC33832S, SL
 SOP28-pin (450 mil) plastic package: LC33832M, ML

Package Dimensions

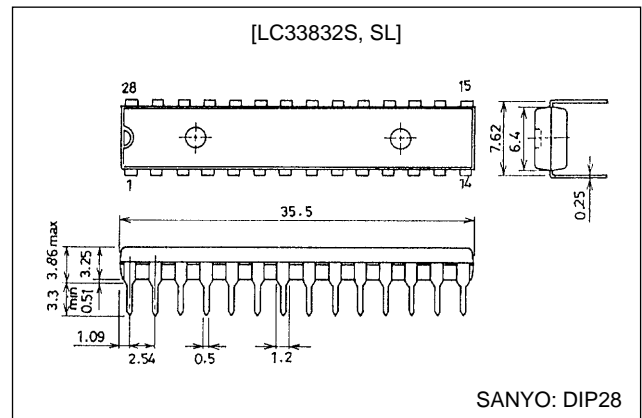
unit: mm

3012A-DIP28



unit: mm

3133-DIP28



- CE access time/OE access time/Cycle time/Current drain

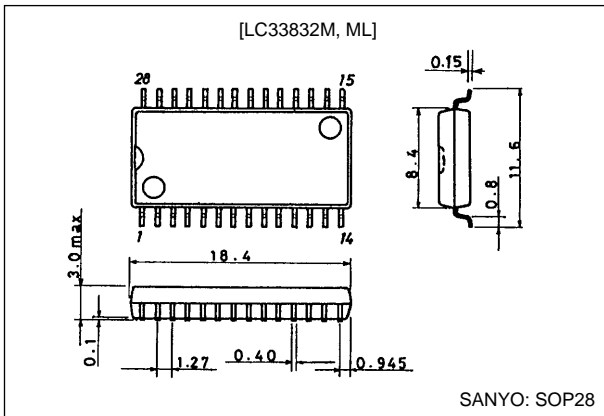
Parameter	LC33832P, S, M, PL, SL, ML		
	-70	-80	-10
CE access time	70 ns	80 ns	100 ns
OE access time	30 ns	35 ns	40 ns
Cycle time	115 ns	130 ns	160 ns
Current drain	Operating	65 mA	60 mA
	Standby	1 mA/100 µA (L version)	

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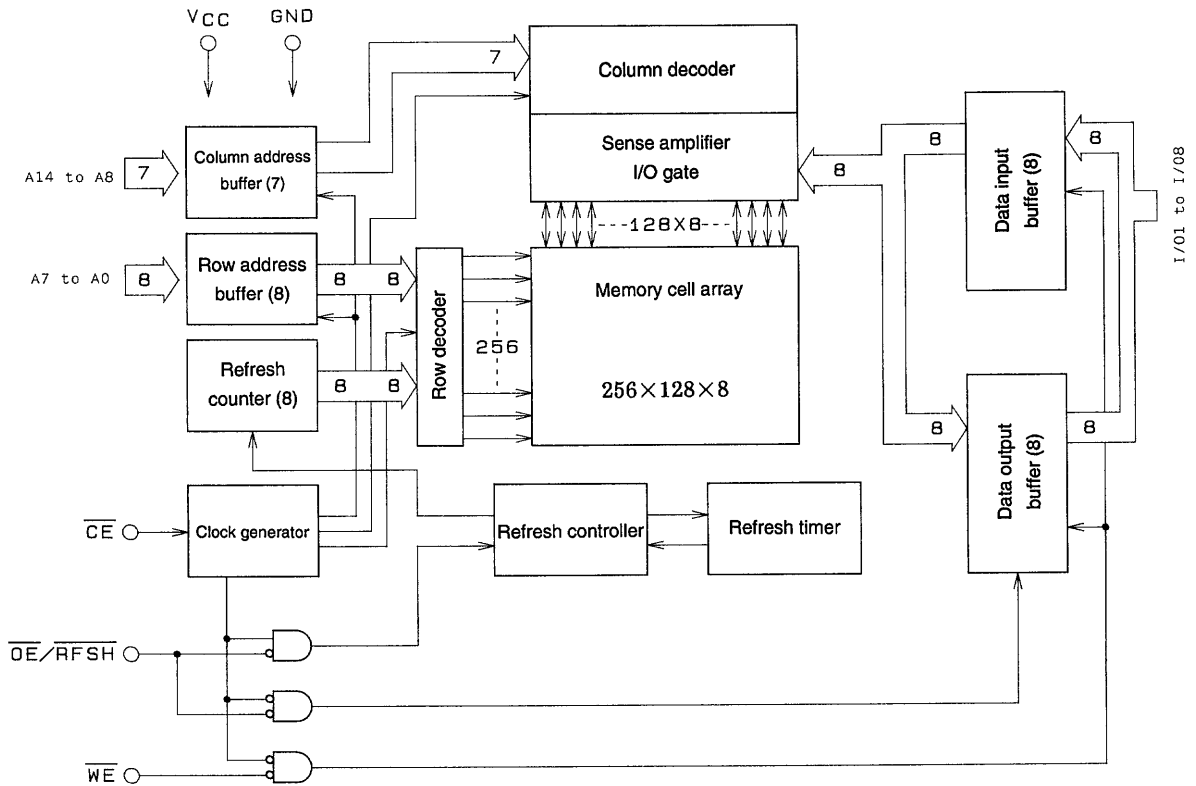
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unit : mm

3158-SOP28

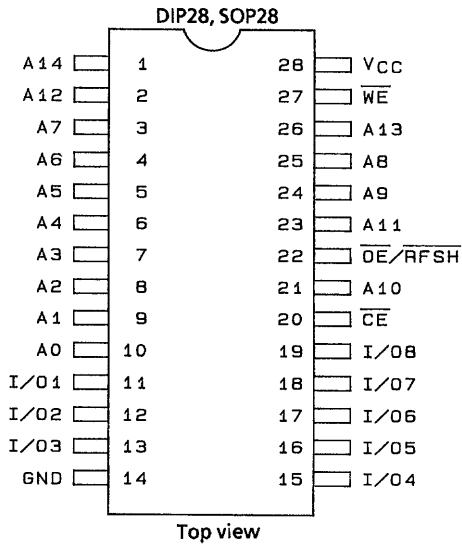


Block Diagram



A01120

Pin Assignment



Pin Functions

A0 to A14	Address input
\overline{WE}	Read/Write input
$\overline{OE/RFSH}$	Output-enable input/ refresh input
\overline{CE}	Chip-enable input
I/O1 to I/O8	Data input/output
V_{CC}	Power supply
GND	Ground

Functional Logic

\overline{CE}	$\overline{OE/RFSH}$	WE	A0 to A7	A8 to A14	I/O1 to I/O8	State
H	H	X	X	X	HZ	Standby
L	L	H	VX	VX	OUT	Read
L	H	L	VX	VX	IN	Write
L	H	H	VX	X	HZ	\overline{CE} -only refresh
H	L	X	X	X	HZ	Self-refresh
H	NP	X	X	X	HZ	Auto-refresh

- HHigh-level input of $V_{IN} = 6.5\text{ V}$ to V_{IH} (min)
- LLow-level input of $V_{IN} = V_{IL}$ (max) to -1.0 V
- XHigh- or low-level input
- NPNegative-polarity pulse input
- VX“IN” when $\overline{CE} = L$ is confirmed, then “X”
- HZHigh impedance
- INInput state
- OUTOutput state

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Maximum supply voltage	V_{CC} max	-1.0 to +7.0	V	1
Input voltage	V_{IN}	-1.0 to +7.0	V	1
Output voltage	V_{OUT}	-1.0 to +7.0	V	1
Allowable power dissipation	P_d max	600	mW	1
Output short-circuit current	I_{OUT}	50	mA	1
Operating temperature	T_{opr}	0 to +70	°C	1
Storage temperature	T_{stg}	-55 to +150	°C	1

Note: 1) Stresses greater than the above listed maximum values may result in damage to the device.

DC Recommended Operating Ranges at $T_a = 0$ to +70°C

Parameter	Symbol	min	typ	max	Unit	Note
Supply voltage	V_{CC}	4.5	5.0	5.5	V	2
Input high level voltage	V_{IH}	2.4		6.5	V	2
Input low level voltage	V_{IL}	-1.0		+0.8	V	2

Note: 2) All voltages are referenced to GND.

DC Electrical Characteristics at $T_a = 0$ to +70°C, $V_{CC} = 5V \pm 10\%$

Parameter	Symbol	Conditions	min	max	Unit	Note	
Operating current	I_{CCA}	Average current during operation	Access time	70ns	65	mA	3,4
				80ns	60		
				100ns	50		
Standby current 1	I_{CCS1}	$\overline{CE} = \overline{OE}/\overline{RFSH} = V_{IH}$		1	mA		
Standby current 2	I_{CCS2}	$\overline{CE} = \overline{OE}/\overline{RFSH} = V_{CC} - 0.2V$	LC33832P, S, M	1	mA		
			LC33832PL, SL, ML		100	μA	
Self-refresh current	I_{CCSR}	$\overline{CE} = V_{CC} - 0.2V, \overline{OE}/\overline{RFSH} = 0.2V$	LC33832P, S, M	1	mA		
			LC33832PL, SL, ML		100	μA	
Input leakage current	I_{IL}	$0V \leq V_{IN} \leq V_{CC}$, pins other than test pin = 0V	-10	+10	μA		
Output leakage current	I_{OL}	D_{OUT} disable, $0V \leq V_{OUT} \leq V_{CC}$	-10	+10	μA		
Output high level voltage	V_{OH}	$I_{OUT} = -5mA$	2.4		V		
Output low level voltage	V_{OL}	$I_{OUT} = 4.2mA$		0.4	V		

Note: 3) All current values are measured at minimal cycle rate. Since current flows immoderately, cycle times may become longer and shorter than shown here.

4) Dependent on output load. Maximum value is value during free state.

Input/Output Capacitance Characteristics at $T_a = 25^\circ C$, $f = 1MHz$, $V_{CC} = 5V \pm 10\%$

Parameter	Symbol	min	max	Unit	Test conditions
Input capacitance (A0 to A14)	C_{IN1}		5	pF	$V_{IN1} = 0V$
Input capacitance (CE, OE/RFSH, WE)	C_{IN2}		7	pF	$V_{IN2} = 0V$
Input/output capacitance	$C_{I/O}$		10	pF	$V_{I/O} = 0V$

Sampling inspections, and not full-lot inspections, are carried out for these parameters.

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AC Electrical Characteristics at Ta = 0 to +70°C, V_{CC} 5V±10% (Notes 5, 6, 7, 8, 9)

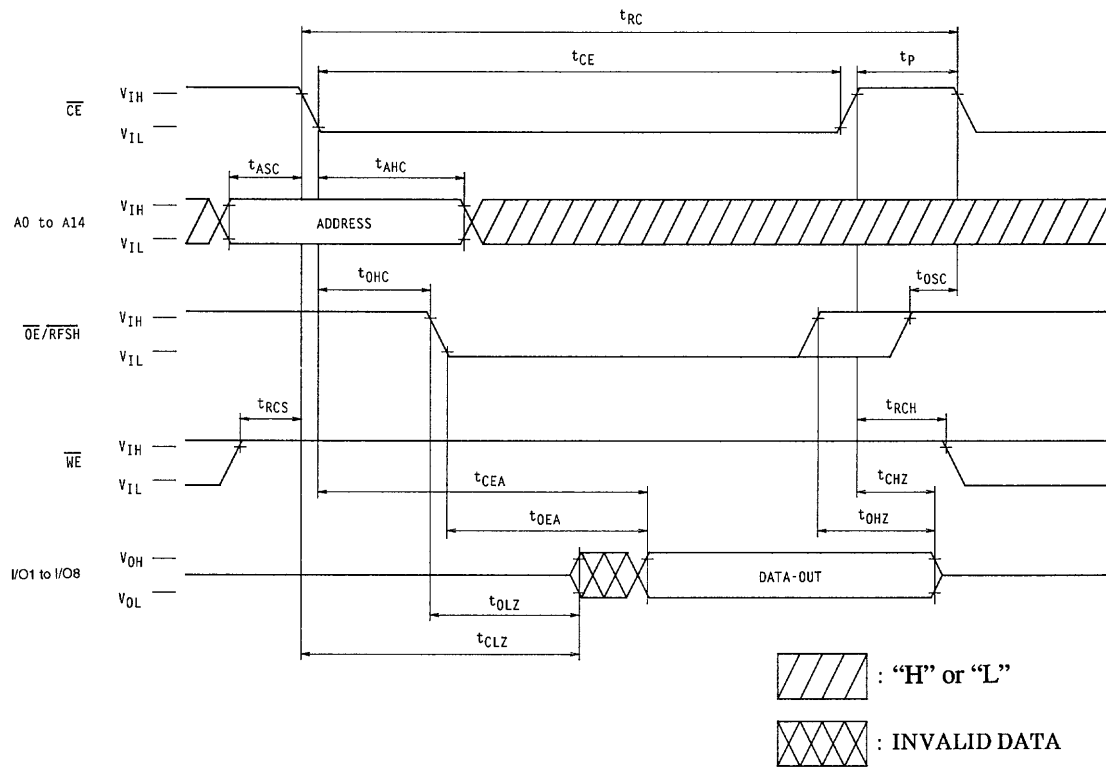
Parameter	Symbol	LC33832P, S, M, PL, SL, ML						Unit	Note
		-70		-80		-10			
		min	max	min	max	min	max		
Random read, write cycle time	t _{RC}	115		130		160		ns	
Read-write cycle time	t _{RMW}	165		195		240		ns	
$\overline{\text{CE}}$ pulse width	t _{CE}	70	10000	80	10000	100	10000	ns	
$\overline{\text{CE}}$ precharge time	t _P	35		40		50		ns	
$\overline{\text{CE}}$ access time	t _{CEA}		70		80		100	ns	
$\overline{\text{OE}}$ access time	t _{OEA}		30		35		40	ns	
$\overline{\text{CE}}$ output enable time	t _{CLZ}	10		10		10		ns	
$\overline{\text{OE}}$ output enable time	t _{OLZ}	0		0		0		ns	
$\overline{\text{WE}}$ output enable time	t _{WLZ}	0		0		0		ns	
$\overline{\text{CE}}$ output disable time	t _{CHZ}	0	20	0	25	0	30	ns	10
$\overline{\text{OE}}$ output disable time	t _{OHZ}	0	20	0	25	0	30	ns	10
$\overline{\text{WE}}$ output disable time	t _{WHZ}	0	20	0	25	0	30	ns	10
$\overline{\text{OE}}$ hold time for $\overline{\text{CE}}$	t _{OHC}	0		0		0		ns	
$\overline{\text{OE}}$ setup time for $\overline{\text{CE}}$	t _{OSC}	10		10		10		ns	
Read command setup time	t _{RCS}	0		0		0		ns	
Read command hold time	t _{RCH}	0		0		0		ns	
Write pulse width	t _{WP}	55		60		70		ns	
Write command hold time	t _{WCH}	55		60		70		ns	
Write command lead time	t _{CWL}	55		60		70		ns	
Input data setup time for $\overline{\text{WE}}$	t _{DSW}	30		35		40		ns	11
Input data setup time for $\overline{\text{CE}}$	t _{DSC}	30		35		40		ns	11
Input data hold time for $\overline{\text{WE}}$	t _{DHW}	0		0		0		ns	11
Input data hold time for $\overline{\text{CE}}$	t _{DHC}	0		0		0		ns	11
Address setup time for $\overline{\text{CE}}$	t _{ASC}	0		0		0		ns	12
Address hold time for $\overline{\text{CE}}$	t _{AHC}	15		20		25		ns	12
Auto-refresh cycle time	t _{FC}	115		130		160		ns	
$\overline{\text{RFSH}}$ delay time for $\overline{\text{CE}}$	t _{RFD}	35		40		50		ns	
$\overline{\text{RFSH}}$ pulse width (auto-refresh)	t _{FAP}	75	8000	80	8000	80	8000	ns	13
$\overline{\text{RFSH}}$ precharge time (auto-refresh)	t _{FP}	30		30		30		ns	13
$\overline{\text{RFSH}}$ active $\overline{\text{CE}}$ delay time (auto-refresh)	t _{FCE}	135		160		190		ns	13
$\overline{\text{RFSH}}$ pulse width (self-refresh)	t _{FAS}	8000		8000		8000		ns	13
$\overline{\text{RFSH}}$ precharge $\overline{\text{CE}}$ delay time (self-refresh)	t _{FRS}	135		160		190		ns	13
Refresh time	t _{REF}		4		4		4	ms	
Rise and fall time	t _T	3	50	3	50	3	50	ns	

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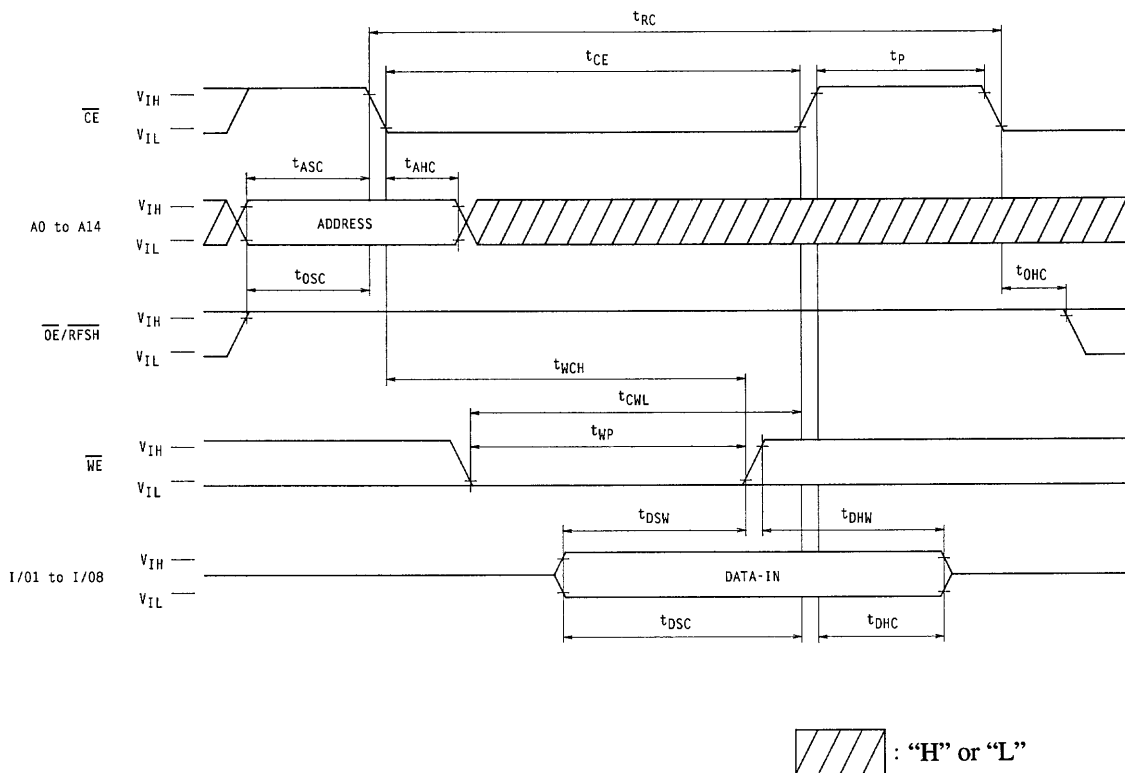
- Note :
- 5) To accomplish internal initialization, \overline{CE} and $\overline{OE}/\overline{RFSH}$ are fixed at V_{IH} for an interval of 1 ms when V_{CC} reaches the specified voltage after power is switched on.
 - 6) Measured at $t_T = 5$ ns.
 - 7) When measuring input signal timing, V_{IH} (min) and V_{IL} (max) are reference levels.
 - 8) Measured using an equivalent of 100 pF and two standard TTL loads.
 - 9) $\overline{OE}/\overline{RFSH}$ input functions as output-enable input (\overline{OE}) when $\overline{CE} = V_{IL}$, and as refresh input (\overline{RFSH}) when $\overline{CE} = V_{IH}$.
 - 10) t_{CHZ} , t_{OHZ} , and t_{WHZ} are defined as the time until output enters the open circuit state and the output voltage level becomes immeasurable.
 - 11) As with ordinary static RAM, write data is incorporated at the rise of \overline{WE} input or \overline{CE} input, whichever is earlier, and write data is therefore held during t_{DSW} , t_{DSC} , t_{DHW} , or t_{DHC} .
 - 12) Because address input is incorporated at the fall of \overline{CE} , the address is maintained during t_{ASC} or t_{AHC} .
 - 13) Auto-refresh and self-refresh are determined by $\overline{OE}/\overline{RFSH}$ pulse width when $\overline{CE} = V_{IH}$, and are defined as auto-refresh when below t_{FAP} (max), or as self-refresh when above t_{FAS} (min). In order to activate \overline{CE} after the completion of each refresh, t_{FCE} must be assured for auto-refresh, or t_{FRS} must be assured for self-refresh.

Timing Chart
Read Cycle



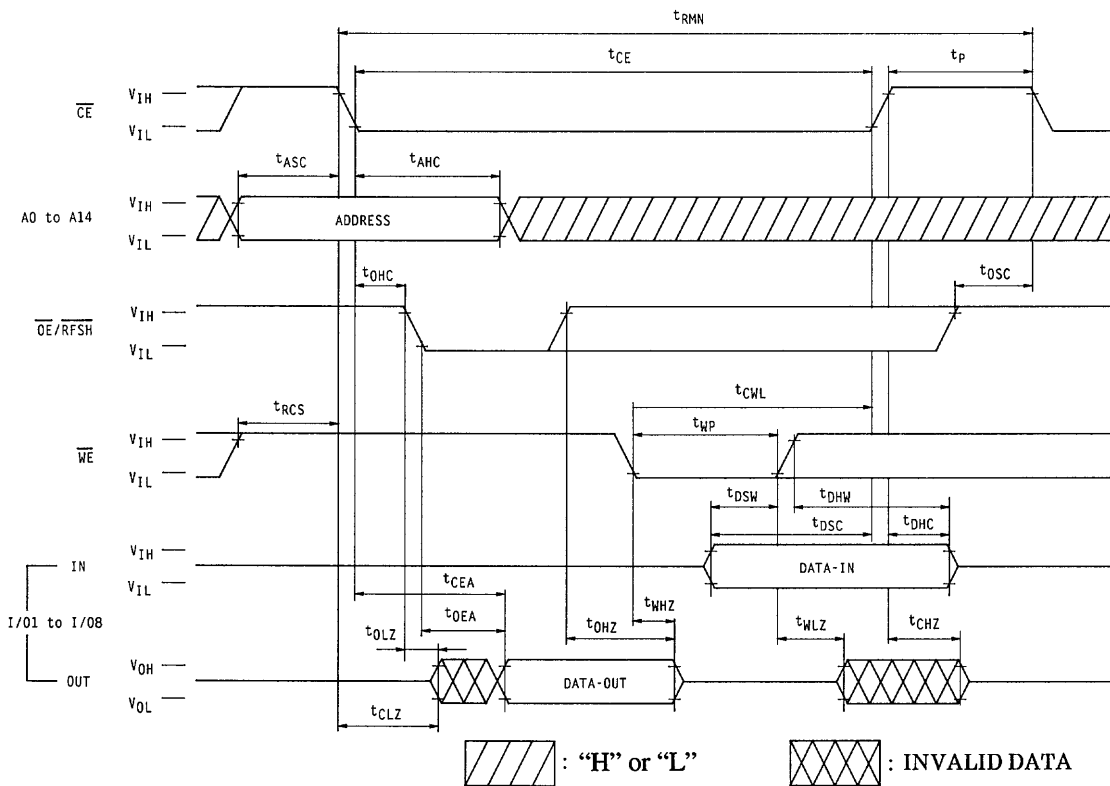
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Write Cycle



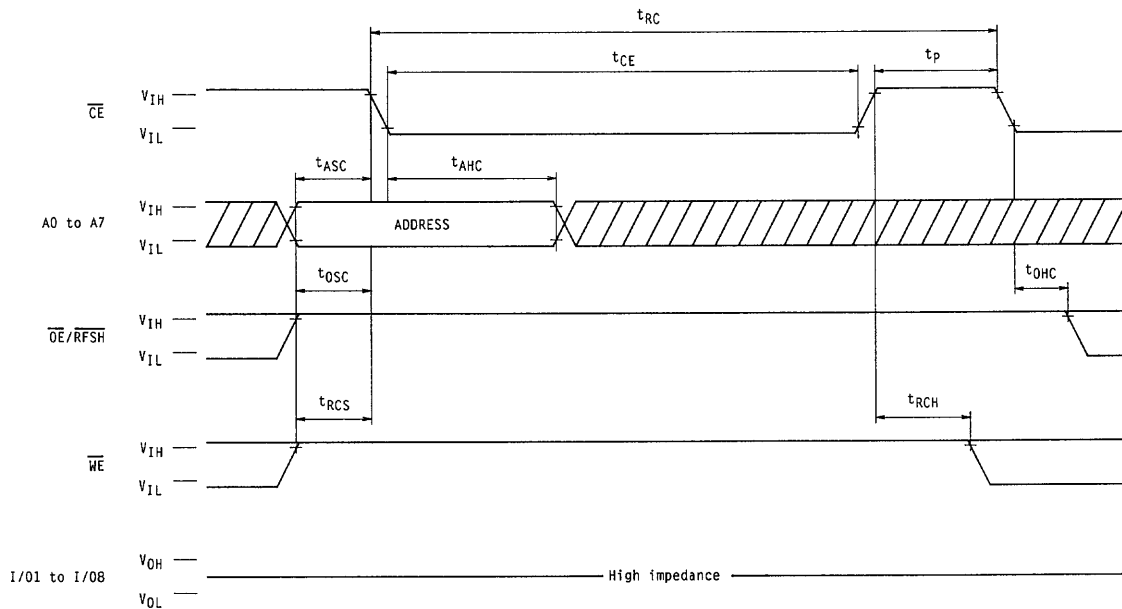
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Read-Write Cycle



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\overline{CE} -Only Refresh Cycle

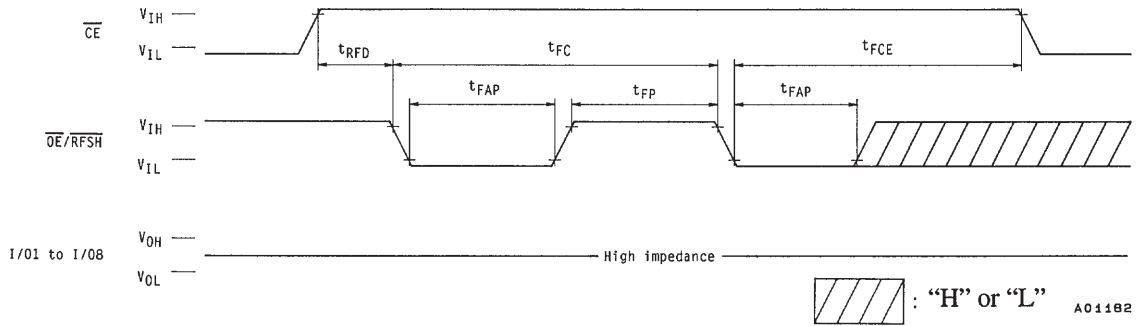


Note: A_8 to A_{14} : "H" or "L"

[Hatched Box]: "H" or "L"

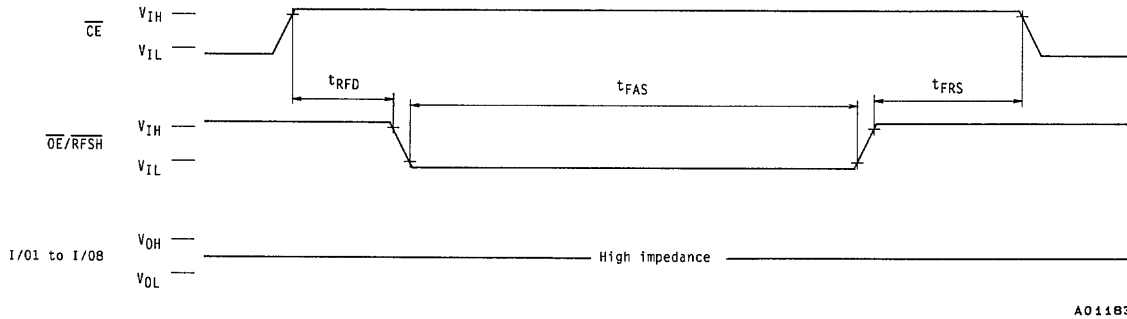
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Auto-Refresh Cycle



Note: A0 to A14, \overline{WE} : "H" or "L"

Self-Refresh Cycle



Note: A0 to A14, \overline{WE} : "H" or "L"

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