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|---|-------------|---|
|  | No. ※ 4711A | LC338128P, M, PL, ML-70/80/10 |
| | | 1 MEG (131072 words × 8 bits) Pseudo-SRAM |

Preliminary

Overview

The LC338128 series is composed of pseudo static RAM that operate on a single 5 V power supply and is organized as 65536 words × 16 bits. By using memory cells each composed of a single transistor and capacitor, together with peripheral CMOS circuitry, this series achieves ease of use with high density, high speed, and low power dissipation. Since the LC338128 series products provide refresh counter and timer on chip, this series can easily accomplish auto-refresh and self-refresh by means of $\overline{\text{RFSH}}$ input. The available packages are the 32-pin DIP with a width of 600 mil, and the 32-pin SOP with a width of 525 mil.

Features

- 131072 words × 8 bits configuration
- $\overline{\text{CE}}$ access time, $\overline{\text{OE}}$ access time, cycle time, operating supply current and self-refresh current 2.

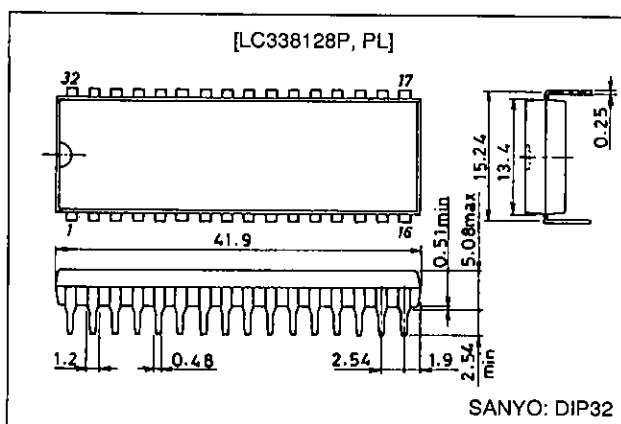
| Parameter | LC338128P, M, PL, ML | | |
|------------------------------------|------------------------------|--------|--------|
| | -70 | -80 | -10 |
| $\overline{\text{CE}}$ access time | 70 ns | 80 ns | 100 ns |
| $\overline{\text{OE}}$ access time | 25 ns | 30 ns | 40 ns |
| Cycle time | 115 ns | 130 ns | 160 ns |
| Operating supply current | 80 mA | 70 mA | 60 mA |
| Self-refresh current 2 | 1 mA/100 μ A (L version) | | |

- Single 5 V \pm 10% power supply
- All inputs and outputs (I/O) TTL compatible
- Fast access time and low power dissipation
- 8 ms refresh using 512 refresh cycles
- Supports auto-refresh, self-refresh and $\overline{\text{CE}}$ -only refresh
- Low-power version: 100 μ A standby current 2, $I_{\text{CCSR}2} = 100 \mu\text{A}$
- Packages
32-pin DIP (600mil) plastic package: LC338128P, PL
32-pin SOP (450mil) plastic package: LC338128M, ML

Package Dimensions

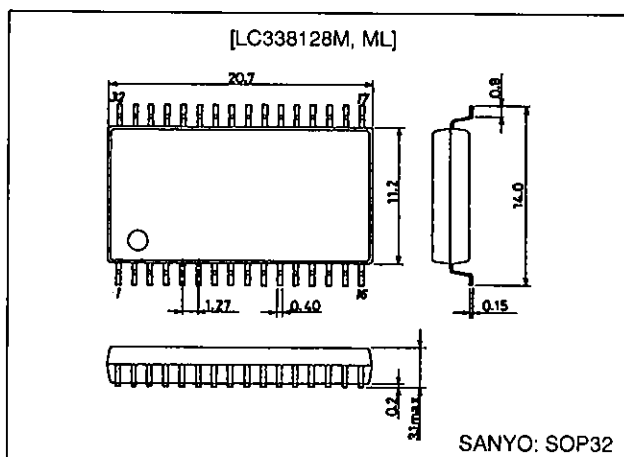
unit: mm

3192-DIP32

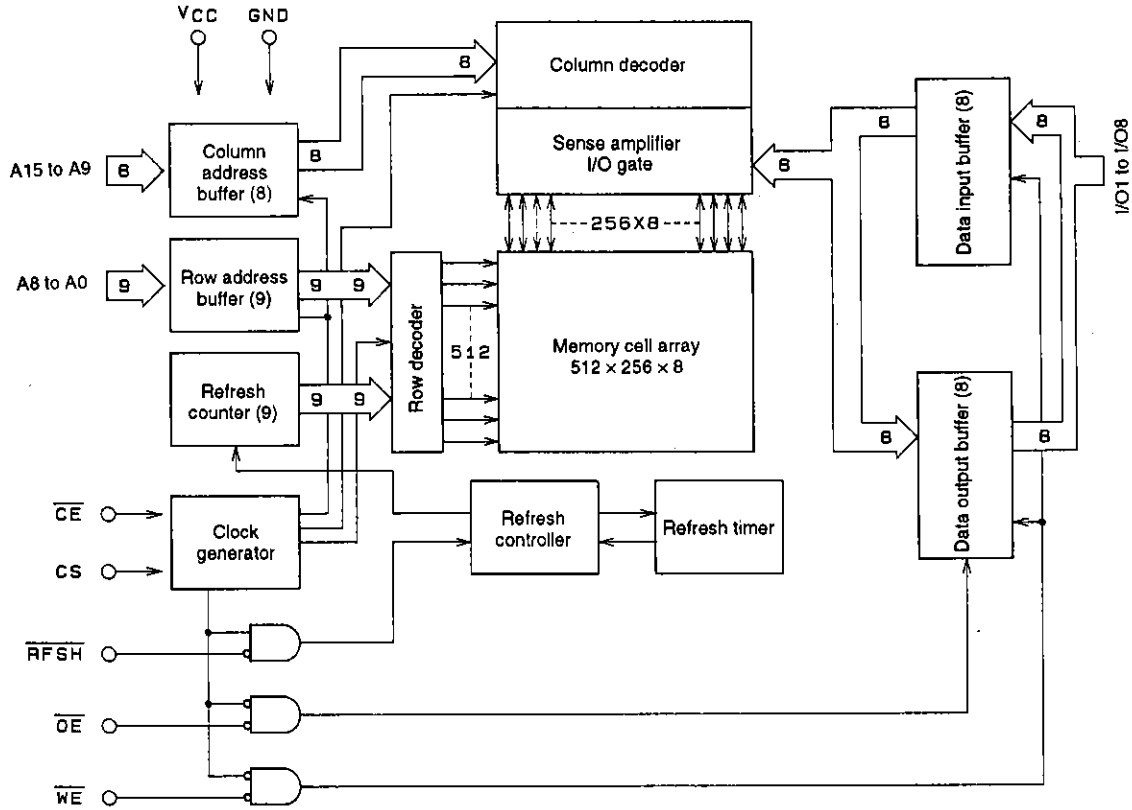


unit: mm

3205-SOP32

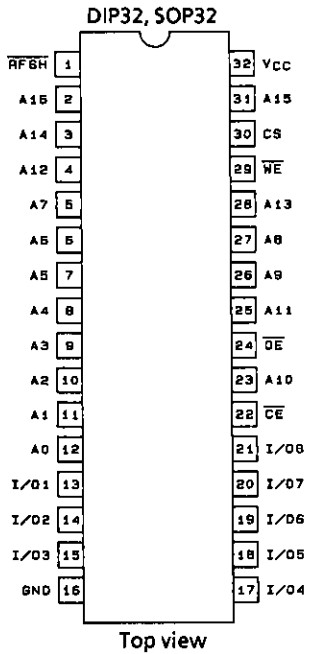


Block Diagram



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Pin Assignment



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Pin Functions

| | |
|--------------|---------------------|
| A0 to A16 | Address Input |
| WA | Read/write Input |
| OE | Output enable input |
| RFSH | Refresh Input |
| CE | Chip enable input |
| CS | Chip select input |
| I/O1 to I/O8 | Data Input/output |
| Vcc | Power supply |
| GND | Ground |

Function Logic

| CE | CS | OE | WE | RFSH | A0 to A8 | A9 to A15 | I/O1 to I/O8 | State |
|----|----|----|----|------|----------|-----------|--------------|-----------------|
| L | H | L | H | X | VX | VX | OUT | Read |
| L | H | X | L | X | VX | VX | IN | Write |
| L | H | H | H | X | VX | X | HZ | CE only refresh |
| L | L | X | X | X | X | X | HZ | CS standby |
| H | X | X | X | L | X | X | HZ | Self-refresh |
| H | X | X | X | NP | X | X | HZ | Auto-refresh |
| H | X | X | X | H | X | X | HZ | Standby |

H: High-level input of $V_{IN} = 6.5\text{ V}$ to V_{IH} (min)
 L: Low-level input of $V_{IN} = V_{IL}$ (max) to -1.0 V
 NP: Negative-polarity pulse input
 X: High- or low-level input
 VX: "IN" when $\overline{CE} = L$ is confirmed, then "X"
 HZ: High impedance
 IN: Input state
 OUT: Output state

Specifications

Absolute Maximum Ratings

| Parameter | Symbol | Ratings | Unit | Note |
|-----------------------------|---------------------|--------------|------|------|
| Maximum supply voltage | $V_{CC\text{ max}}$ | -1.0 to +7.0 | V | 1 |
| Input voltage | V_{IN} | -1.0 to +7.0 | V | 1 |
| Output voltage | V_{OUT} | -1.0 to +7.0 | V | 1 |
| Allowable power dissipation | $P_{d\text{ max}}$ | 600 | mW | 1 |
| Output short current | I_{OUT} | 50 | mA | 1 |
| Operating temperature range | T_{opr} | 0 to +70 | °C | 1 |
| Storage temperature range | T_{stg} | -55 to +150 | °C | 1 |

Note: 1. Stresses greater than the above listed maximum values may result in damage to the device.

DC Recommended Operating Ranges at $T_a = 0$ to $+70^\circ\text{C}$

| Parameter | Symbol | min | typ | max | Unit | Note |
|--------------------------|----------|------|-----|------|------|------|
| Supply voltage | V_{CC} | 4.5 | 5.0 | 5.5 | V | 2 |
| Input high level voltage | V_{IH} | 2.4 | | 6.5 | V | 2 |
| Input low level voltage | V_{IL} | -1.0 | | +0.8 | V | 2 |

Note: 2. All voltages are referenced to GND.

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DC Electrical Characteristics at Ta = 0 to +70°C, VCC = 5 V ± 10%

| Parameter | Symbol | Conditions | min | max | Unit | Note | |
|---|--------------------|---|--------------------------------|--------|--------|------|------|
| | | | | | | | |
| Operating current (average current during operation) | I _{CCA} | t _{RC} = t _{RC} (min) | Access time | 70 ns | 70 | mA | 3, 4 |
| | | | | 80 ns | 80 | | |
| | | | | 100 ns | 100 | | |
| Standby current 1 | I _{CCS1} | $\overline{CE} = \overline{RFSH} = V_{IH}$ | LC338128P, M LC338128PL, ML | | 2 1 | mA | |
| Standby current 2 | I _{CCS2} | $\overline{CE} = \overline{RFSH} = V_{CC} - 0.2 V$ | LC338128P, M | | 1 | mA | |
| | | | LC338128PL, ML | | 100 | µA | |
| Self-refresh current 1 (average current) | I _{CCSR1} | $\overline{CE} = V_{IH}, \overline{RFSH} = V_{IL}$ | LC338128P, M | | 2 | mA | |
| | | | LC338128PL, ML | | 1 | µA | |
| Self-refresh current 2 (average current) | I _{CCSR2} | $\overline{CE} = V_{CC} - 0.2 V, \overline{RFSH} = 0.2 V$ | LC338128P, M | | 1 | mA | |
| | | | LC338128PL, ML | | 100 | µA | |
| Input leakage current | I _{IL} | 0 V ≤ V _{IN} ≤ V _{CC} , pins other than measuring pin = 0 V | | -10 | +10 | µA | |
| Output leakage current | I _{OL} | Output disable, 0 V ≤ V _{OUT} ≤ V _{CC} | | -10 | +10 | µA | |
| Output high level voltage | V _{OH} | I _{OH} = -1 mA | | 2.4 | | V | |
| Output low level voltage | V _{OL} | I _{OL} = 2.1 mA | | | 0.4 | V | |

Note: 3. All current values are measured at minimum cycle rate. Since current flows immoderately, if cycle time is longer than shown here, current value becomes smaller. A bypass capacitor of 0.01 µF or larger should be inserted between V_{CC} and GND for each memory chip to suppress power supply noise (voltage drops) due to transient currents.

4. Dependent on output load. Maximum value is value during free state.

Input/Output Capacitance at Ta = 25°C, VCC = 5 V ± 10%, f = 1 MHz

| Parameter | Symbol | Measuring conditions | min | max | Unit |
|---|------------------|------------------------|-----|-----|------|
| Input capacitance (A0 to A16) | C _{IN1} | V _{IN1} = 0 V | | 5 | pF |
| Input capacitance (\overline{CE} , CS, \overline{OE} , \overline{RFSH} and \overline{WE}) | C _{IN2} | V _{IN2} = 0 V | | 7 | pF |
| I/O capacitance | C _{I/O} | V _{I/O} = 0 V | | 10 | pF |

Sampling inspections, and not full-lot inspections, are carried out for these parameters.

AC Electrical Characteristics at Ta = 0 to +70°C, VCC = 5 V ± 10% (Notes 5, 6, 7, 8)

| Parameter | Symbol | -70 | | -80 | | -100 | | Unit | Note |
|---|-------------------|-----|-------|-----|-------|------|-------|------|------|
| | | min | max | min | max | min | max | | |
| Random read or write cycle time | t _{RC} | 115 | | 130 | | 160 | | ns | |
| Read-modify-write cycle time | t _{RMW} | 165 | | 195 | | 235 | | ns | |
| \overline{CE} pulse width | t _{CE} | 70 | 10000 | 80 | 10000 | 100 | 10000 | ns | |
| \overline{CE} precharge time | t _p | 35 | | 40 | | 50 | | ns | |
| \overline{CE} access time | t _{CEA} | | 70 | | 80 | | 100 | ns | |
| \overline{OE} access time | t _{OE A} | | 25 | | 30 | | 40 | ns | |
| \overline{CE} output enable time | t _{CLZ} | 20 | | 25 | | 30 | | ns | |
| \overline{OE} output enable time | t _{OLZ} | 0 | | 0 | | 0 | | ns | |
| \overline{WE} output enable time | t _{WLZ} | 0 | | 0 | | 0 | | ns | |
| \overline{CE} output disable time | t _{CHZ} | 0 | 20 | 0 | 25 | 0 | 30 | ns | 9 |
| \overline{OE} output disable time | t _{OHZ} | 0 | 20 | 0 | 25 | 0 | 30 | ns | 9 |
| \overline{WE} output disable time | t _{WHZ} | 0 | 20 | 0 | 25 | 0 | 30 | ns | 9 |
| \overline{OE} disable setup time | t _{ODS} | 0 | | 0 | | 0 | | ns | |
| \overline{OE} disable hold time | t _{ODH} | 10 | | 10 | | 10 | | ns | |
| Read command setup time | t _{RCS} | 0 | | 0 | | 0 | | ns | |
| Read command hold time | t _{RCH} | 0 | | 0 | | 0 | | ns | |
| Chip select setup time | t _{CSS} | 0 | | 0 | | 0 | | ns | |
| Chip select hold time | t _{CSH} | 15 | | 20 | | 25 | | ns | |
| Write pulse width | t _{WP} | 30 | | 60 | | 70 | | ns | |
| Write command hold time | t _{WCH} | 55 | 10000 | 60 | 10000 | 70 | 10000 | ns | |
| Write command lead time | t _{CWL} | 40 | 10000 | 60 | 10000 | 70 | 10000 | ns | |
| Input data setup time for \overline{WE} | t _{DSW} | 30 | | 35 | | 40 | | ns | 10 |
| Input data setup time for \overline{CE} | t _{DSC} | 30 | | 35 | | 40 | | ns | 10 |

Continued on next page.

LC338128P, M, PL, ML-70/80/10

Continued from preceding page.

| Parameter | Symbol | -70 | | -80 | | -100 | | Unit | Note |
|---|-----------|------|------|------|------|------|------|------|------|
| | | min | max | min | max | min | max | | |
| Input data hold time for \overline{WE} | t_{DHW} | 0 | | 0 | | 0 | | ns | 10 |
| Input data hold time for \overline{CE} | t_{DHC} | 0 | | 0 | | 0 | | ns | 10 |
| Address setup time for \overline{CE} | t_{ASC} | 0 | | 0 | | 0 | | ns | 11 |
| Address hold time for \overline{CE} | t_{AHC} | 15 | | 20 | | 25 | | ns | 11 |
| Refresh command hold time | t_{RHC} | 15 | | 15 | | 15 | | ns | |
| Auto-refresh cycle time | t_{FC} | 115 | | 130 | | 160 | | ns | |
| \overline{RFSH} delay time for \overline{CE} | t_{RFD} | 35 | | 40 | | 50 | | ns | |
| \overline{RFSH} pulse width (auto-refresh) | t_{FAP} | 30 | 8000 | 30 | 8000 | 30 | 8000 | ns | 12 |
| \overline{RFSH} precharge time (auto-refresh) | t_{FP} | 30 | | 30 | | 30 | | ns | 12 |
| \overline{RFSH} pulse width (self-refresh) | t_{FAS} | 8000 | | 8000 | | 8000 | | ns | 12 |
| \overline{RFSH} precharge \overline{CE} delay time (self-refresh) | t_{FRS} | 135 | | 160 | | 190 | | ns | 12 |
| Refresh time (512 cycles, A0 to A8) | t_{REF} | | 8 | | 8 | | 8 | ms | |
| Rise or fall times | t_T | 3 | 50 | 3 | 50 | 3 | 50 | ns | |

Note: 5. To accomplish internal initialization, \overline{CE} is fixed at V_{IH} for an interval of 1 ms when V_{CC} reaches the specified voltage after power is switched on. At least eight cycles must be executed following that period.

6. Measured at $t_T = 5$ ns.

7. When measuring input signal timing, V_{IH} (min) and V_{IL} (max) are reference levels.

8. Measured using an equivalent of 100 pF and two standard TTL loads.

9. t_{CHZ} , t_{OHZ} and t_{WHZ} are defined as the time until output enters the open circuit state and the output voltage level becomes immeasurable.

10. As with ordinary static RAM, write data is incorporated at the rise of \overline{WE} input or \overline{CE} input, whichever is earlier, and write data is therefore held during t_{DSW} , t_{DSC} , t_{DHW} , or t_{DHC} .

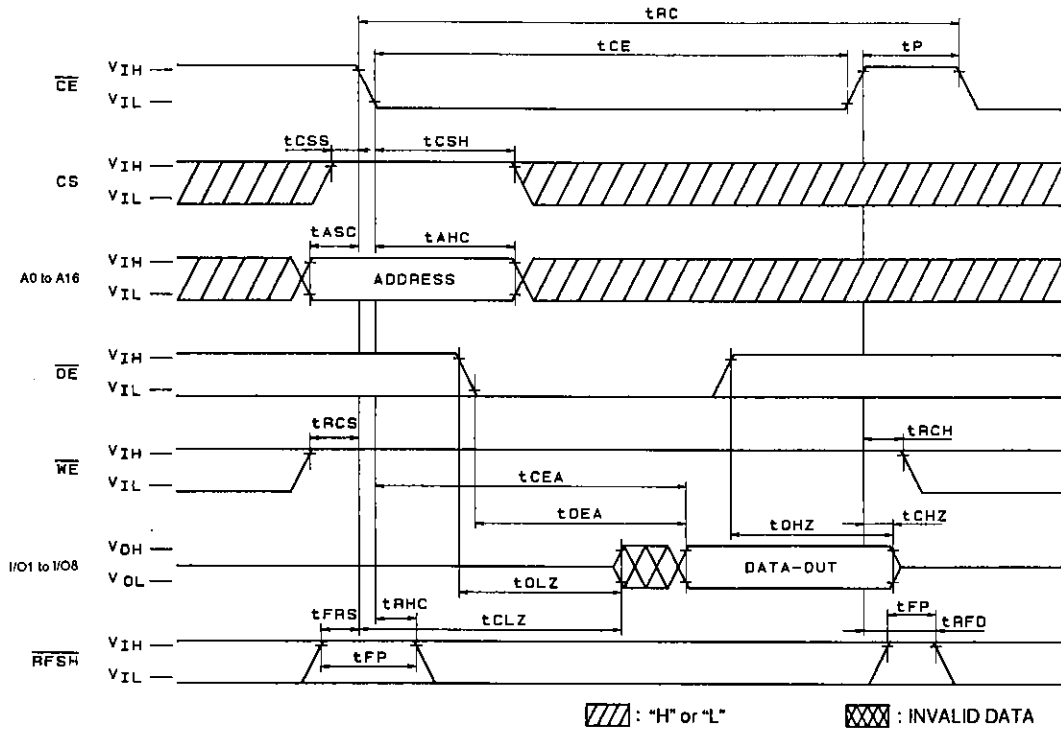
11. Because address input is incorporated at the fall of \overline{CE} , the address is maintained during t_{ASC} or t_{AHC} .

12. Auto-refresh and self-refresh are determined by \overline{RFSH} pulse width when $\overline{CE} = V_{IH}$, and are defined as auto-refresh when below t_{FAP} (max), or as self-refresh when above t_{FAS} (min). In order to activate \overline{CE} after the completion of each refresh, t_{FCE} must be assured for auto-refresh, or t_{FRS} must be assured for self-refresh.

Similarly, if self-refresh timing ($\overline{RFSH} = \text{Low}$) is used after power is switched on, t_{FRS} must be assured.

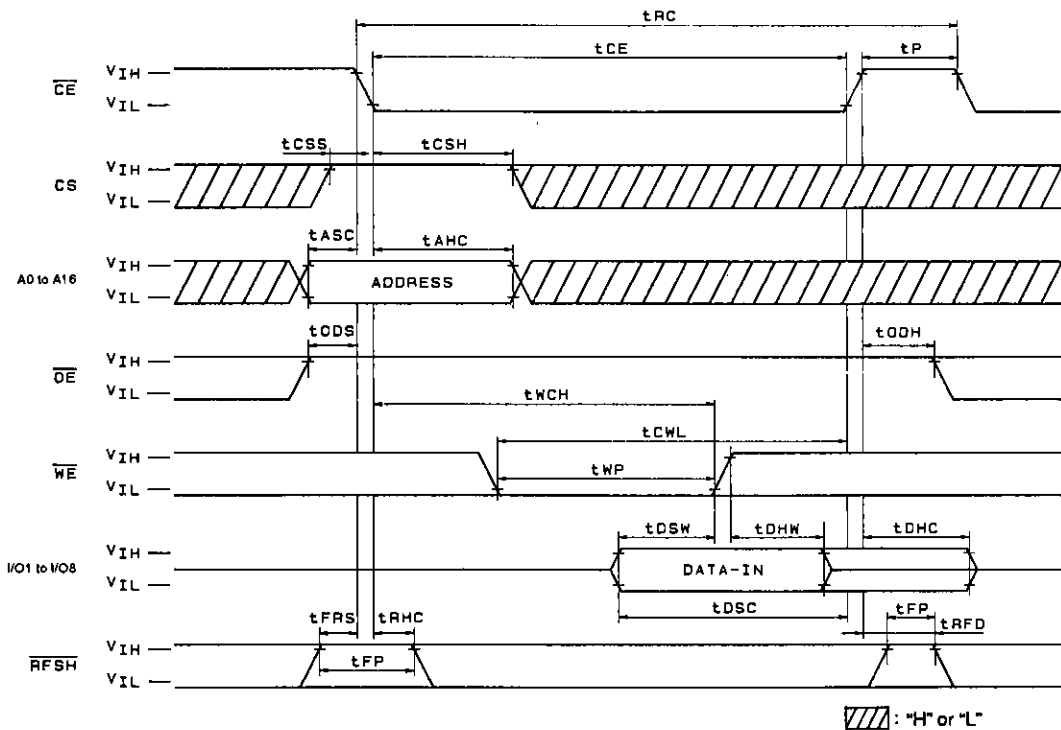
Timing Chart

Read Cycle



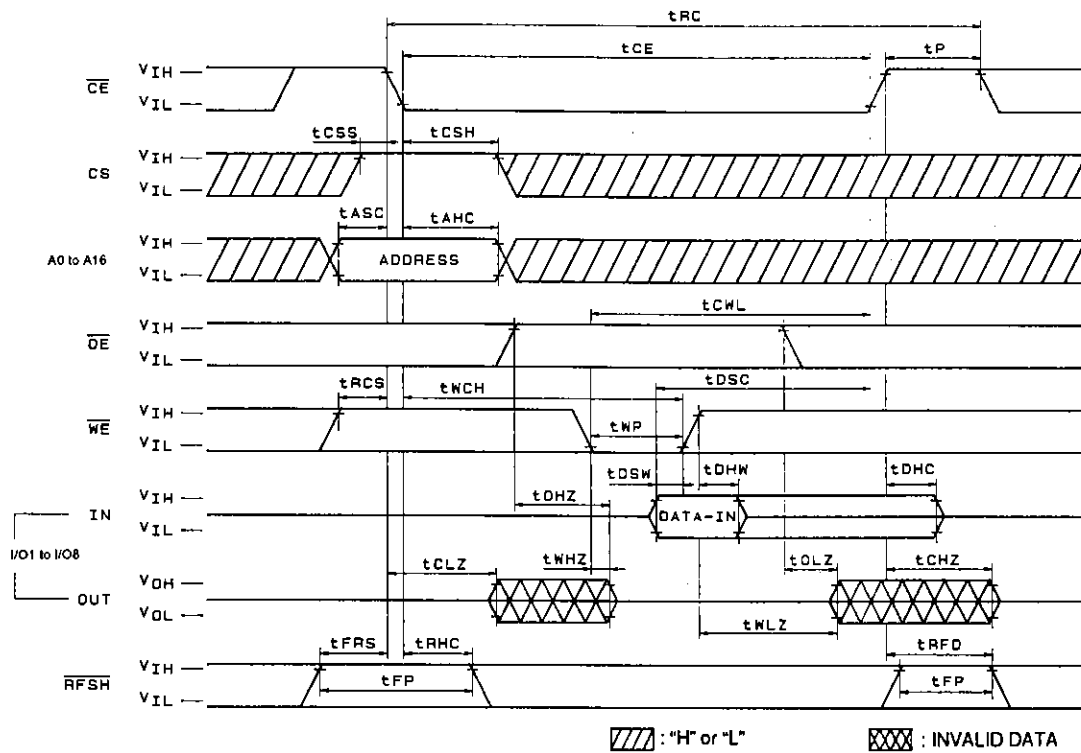
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Write Cycle 1 (\overline{OE} Fix High)



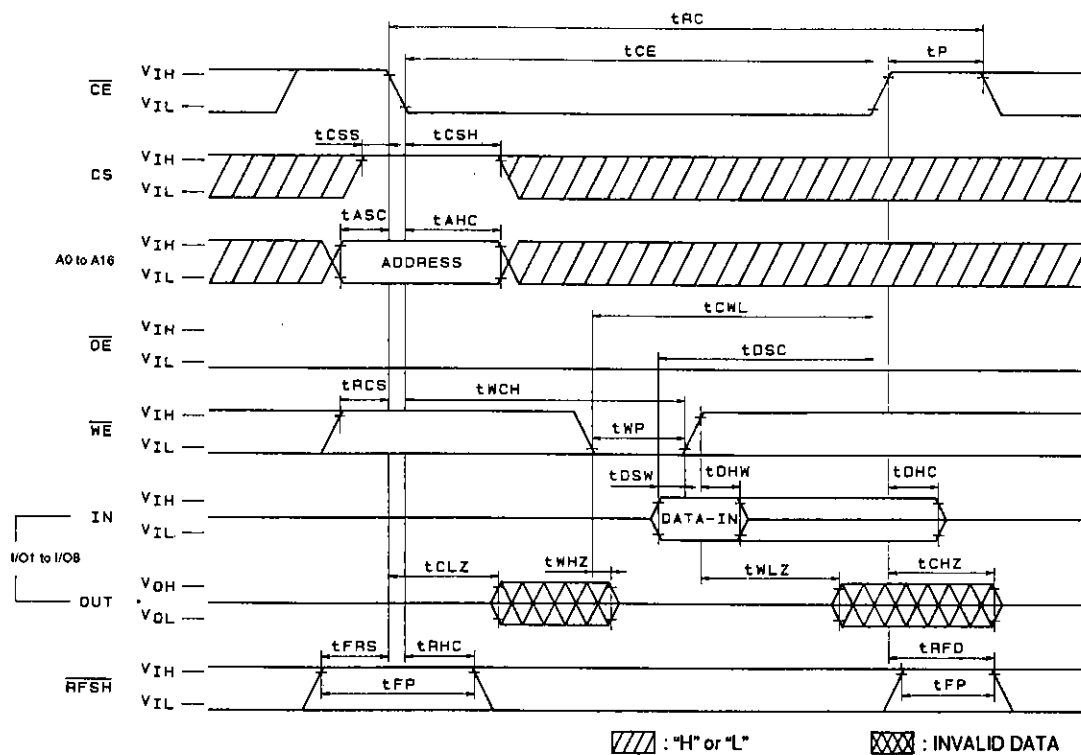
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Write Cycle 2 (\overline{OE} Clock)



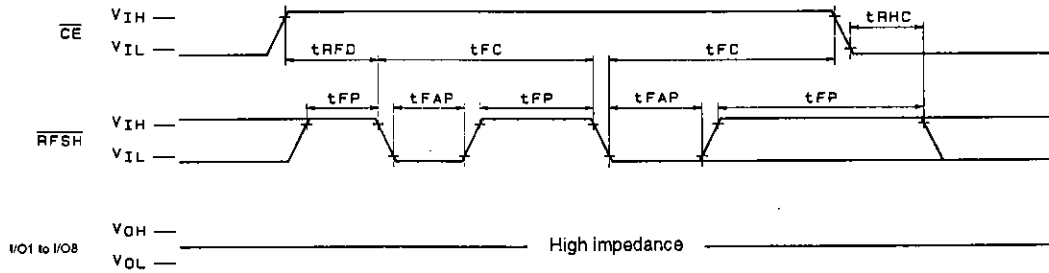
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Write Cycle 3 (\overline{OE} Fix Low)



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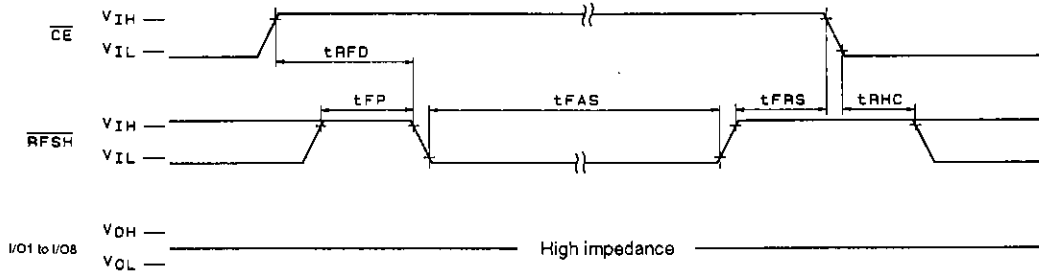
Auto-Refresh Cycle



Note: CS, \overline{OE} , \overline{WE} , A0 to A16: "H" or "L"

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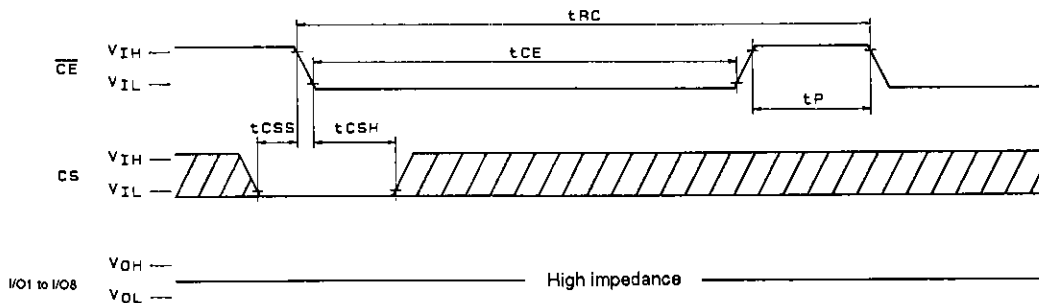
Self-Refresh Cycle



Note: CS, \overline{OE} , \overline{WE} , A0 to A16: "H" or "L"

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CS Standby Mode



Note: \overline{OE} , \overline{WE} , A0 to A16: "H" or "L"

▨ : "H" or "L"

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