



## LC322271J, M, T-70/80

### 2 MEG (131072 words × 16 bits) DRAM Fast Page Mode, Byte Write

#### Preliminary

#### Overview

The LC322271J, M and T is a CMOS dynamic RAM operating on a single 5 V power source and having a 131072 words × 16 bits configuration. Equipped with large capacity capabilities, high speed transfer rates and low power dissipation, this series is suited for a wide variety of applications ranging from computer main memory and expansion memory to commercial equipment.

Address input utilizes a multiplexed address bus which permits it to be enclosed in a compact plastic package of SOJ 40-pin, SOP 40-pin, and TSOP 44-pin. Refresh rates are within 8 ms with 512 row address (A0 to A7, A8R) selection and support Row Address Strobe ( $\overline{\text{RAS}}$ )-only refresh, Column Address Strobe ( $\overline{\text{CAS}}$ )-before- $\overline{\text{RAS}}$  refresh and hidden refresh settings. There are functions such as fast page mode, read-modify-write and byte write. The pin assignment follows the JEDEC 1 M DRAM (65536 words × 16 bits,  $1\overline{\text{CAS}}/2\overline{\text{WE}}$ ) standard.

#### Features

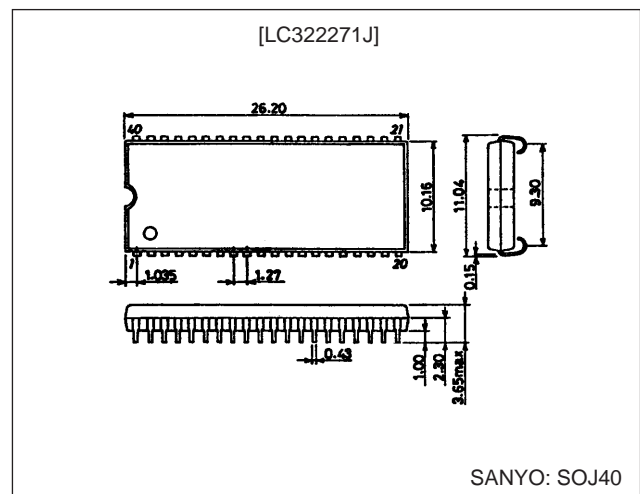
- 131072 words × 16 bits configuration.
- Single 5 V ± 10% power supply.
- All input and output (I/O) TTL compatible.
- Supports fast page mode, read-modify-write and byte write.
- Supports output buffer control using early write and Output Enable ( $\overline{\text{OE}}$ ) control.
- 8 ms refresh using 512 refresh cycles.
- Supports  $\overline{\text{RAS}}$ -only refresh,  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh and hidden refresh.
- Follows the JEDEC 1 M DRAM (65536 words × 16 bits,  $1\overline{\text{CAS}}/2\overline{\text{WE}}$ ) standard.
- $\overline{\text{RAS}}$  access time/column address time/ $\overline{\text{CAS}}$  access time/cycle time/power dissipation

- Package:  
SOJ 40-pin (400 mil) plastic package : LC322271J  
SOP 40-pin (450 mil) plastic package : LC322271M  
TSOP 44-pin (400 mil) plastic package : LC322271T

#### Package Dimensions

unit: mm

##### 3200-SOJ40



Parameter	LC322271J, M, T	
	-70	-80
RAS access time	70 ns	80 ns
Column address access time	35 ns	45 ns
$\overline{\text{CAS}}$ access time	20 ns	30 ns
Cycle time	130 ns	150 ns
Power dissipation (max.)	During operation	688 mW
	During standby	633 mW
		5.5 mW (CMOS level)/11 mW (TTL level)

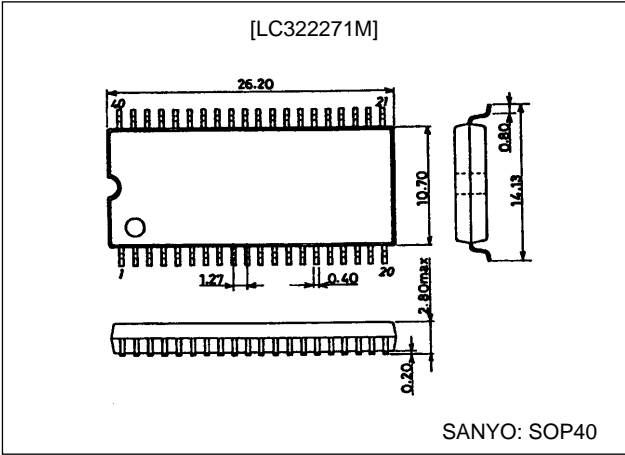
**SANYO Electric Co., Ltd. Semiconductor Business Headquarters**

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### Package Dimensions

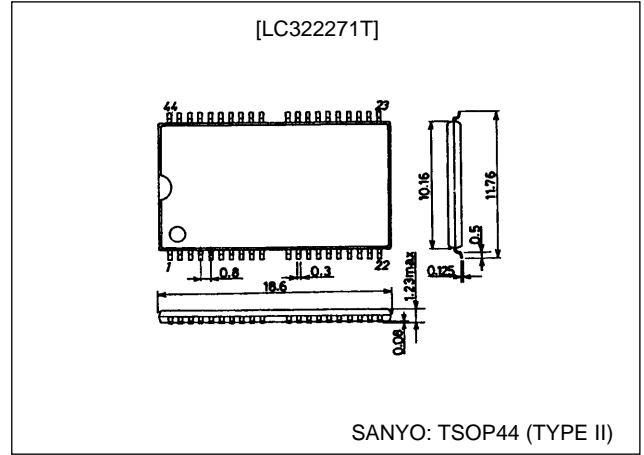
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#### 3195-SOP40

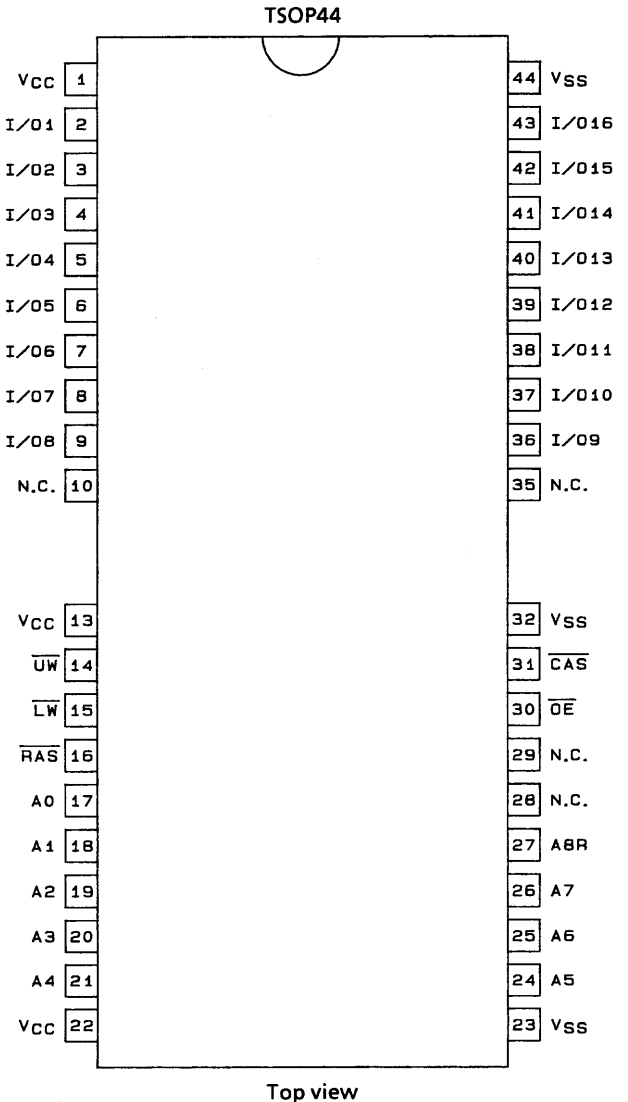
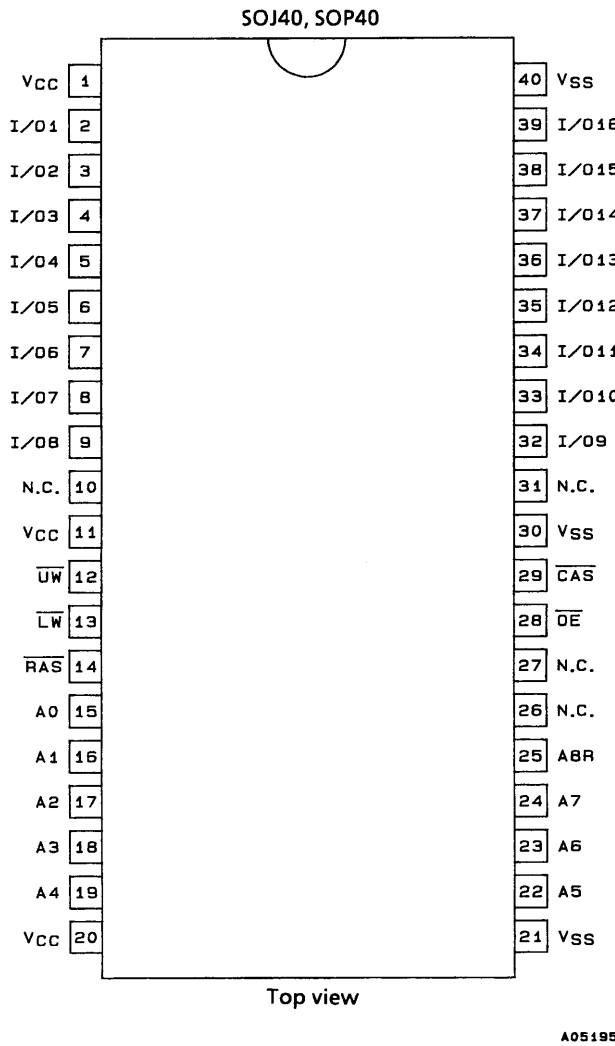


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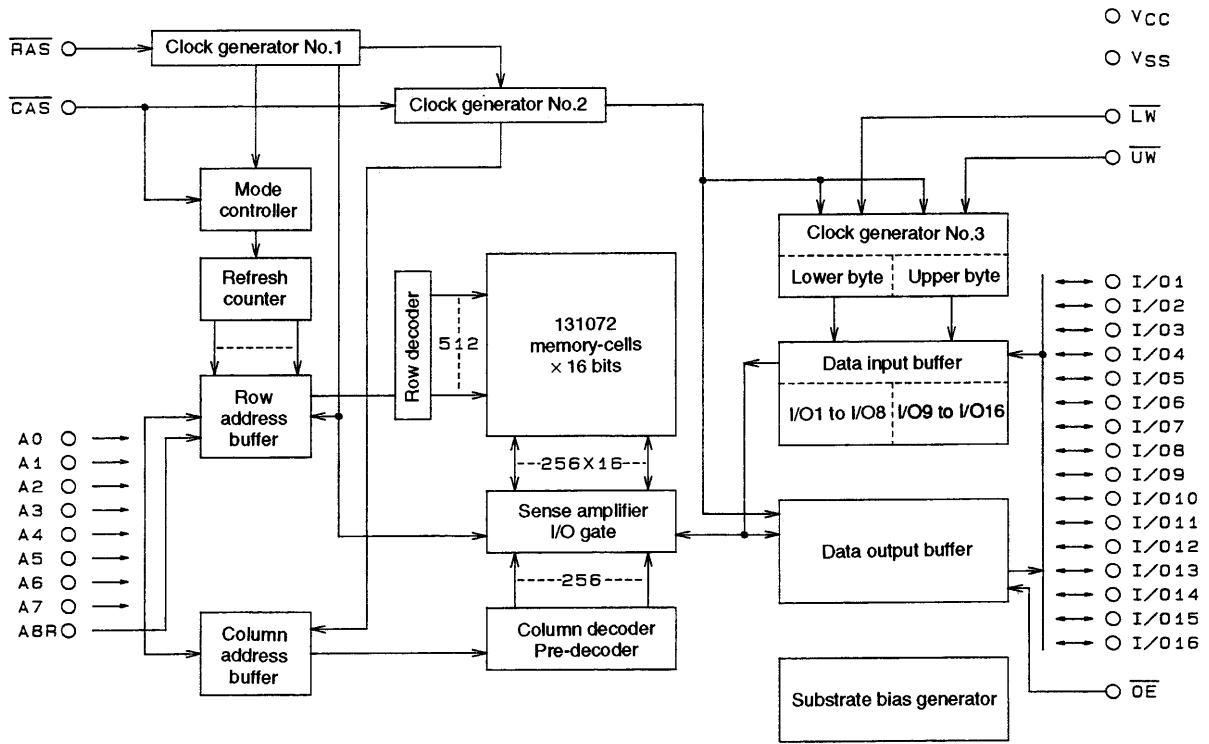
#### 3207-TSOP44



### Pin Assignments



Block Diagram



A03904

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Maximum supply voltage	$V_{CC \text{ max}}$	-1.0 to +7.0	V	1
Input voltage	$V_{IN}$	-1.0 to +7.0	V	1
Output voltage	$V_{OUT}$	-1.0 to +7.0	V	1
Allowable power dissipation	LC322271J, M	800	mW	1
	LC322271T	700		
Output short-circuit current	$I_{OUT}$	50	mA	1
Operating temperature range	$T_{opr}$	0 to +70	°C	1
Storage temperature range	$T_{stg}$	-55 to +150	°C	1

Note: 1. Stresses greater than the above listed maximum values may result in damage to the device.

## LC322271J, M, T-70/80

### DC Recommended Operating Ranges at Ta = 0 to +70°C

Parameter	Symbol	min	typ	max	Unit	Note
Power supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V	2
Input high level voltage	V <sub>IH</sub>	2.4		6.5	V	2
Input low level voltage (A0 to A7, A8R, RAS, CAS, $\overline{UW}$ , $\overline{LW}$ , OE)	V <sub>IL</sub>	-1.0*		+0.8	V	2
Input low level voltage (I/O1 to I/O16)	V <sub>IL</sub>	-0.5*		+0.8	V	2

Note: 2. All voltages are referenced to V<sub>SS</sub>.

\*: -2.0 V when pulse width is less than 20 ns.

### DC Electrical Characteristics at Ta = 0 to +70°C, V<sub>CC</sub> = 5 V ± 10%

Parameter	Symbol	Conditions	LC322271J, M, T				Unit	Note
			-70		-80			
			min	max	min	max		
Operating current (Average current during operation)	I <sub>CC1</sub>	$\overline{RAS}$ , $\overline{CAS}$ , address cycling: t <sub>RC</sub> = t <sub>RC</sub> min		125		115	mA	3, 4, 5
Standby current	I <sub>CC2</sub>	$\overline{RAS} = \overline{CAS} = V_{IH}$		2		2	mA	
$\overline{RAS}$ -only refresh current	I <sub>CC3</sub>	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$ : t <sub>RC</sub> = t <sub>RC</sub> min		125		115	mA	3, 5
Fast page mode current	I <sub>CC4</sub>	$\overline{RAS} = V_{IL}$ , $\overline{CAS}$ , address cycling: t <sub>PC</sub> = t <sub>PC</sub> min		115		90	mA	3, 4, 5
Standby current	I <sub>CC5</sub>	$\overline{RAS} = \overline{CAS} = V_{CC} - 0.2 V$		1		1	mA	
$\overline{CAS}$ -before- $\overline{RAS}$ refresh current	I <sub>CC6</sub>	$\overline{RAS}$ , $\overline{CAS}$ cycling: t <sub>RC</sub> = t <sub>RC</sub> min		125		115	mA	3
Input leakage current	I <sub>IL</sub>	0 V ≤ V <sub>IN</sub> ≤ 6.5 V, pins other than test pin = 0 V	-10	+10	-10	+10	μA	
Output leakage current	I <sub>OL</sub>	D <sub>OUT</sub> disable, 0 V ≤ V <sub>OUT</sub> ≤ 5.5 V	-10	+10	-10	+10	μA	
Output high level voltage	V <sub>OH</sub>	I <sub>OUT</sub> = -2.5 mA	2.4		2.4		V	
Output low level voltage	V <sub>OL</sub>	I <sub>OUT</sub> = 2.1 mA		0.4		0.4	V	

Note: 3. All current values are measured at minimum cycle rate. Since current flows immoderately, if cycle time is longer than shown here, current value becomes smaller.

4. I<sub>CC1</sub> and I<sub>CC4</sub> are dependent on output loads. Maximum values for I<sub>CC1</sub> and I<sub>CC4</sub> represent values with output open.

5. Address change is less than or equal to one time during RAS = V<sub>IL</sub>. Concerning I<sub>CC4</sub>, it is less than or equal to one time during 1 cycle (t<sub>PC</sub>).

### AC Electrical Characteristics at Ta = 0 to +70°C, V<sub>CC</sub> = 5 V ± 10% (Notes 6, 7 and 8)

Parameter	Symbol	-70		-80		Unit	Note
		min	max	min	max		
Random read, write cycle time	t <sub>RC</sub>	130		150		ns	
Read-write/read-modify-write cycle time	t <sub>RWC</sub>	190		200		ns	
Fast page mode cycle time	t <sub>PC</sub>	45		55		ns	
Fast page mode read-write/read-modify-write cycle time	t <sub>PRWC</sub>	95		100		ns	
$\overline{RAS}$ access time	t <sub>RAC</sub>		70		80	ns	9, 14, 15
$\overline{CAS}$ access time	t <sub>CAC</sub>		20		30	ns	9, 14
Column address access time	t <sub>AA</sub>		35		45	ns	9, 15
$\overline{CAS}$ precharge access time	t <sub>CPA</sub>		40		50	ns	9
Output low-impedance time from $\overline{CAS}$ low	t <sub>CLZ</sub>	0		0		ns	9
Output buffer turn-off delay time	t <sub>OFF</sub>	0	20	0	20	ns	10
Rise, fall time	t <sub>T</sub>	3	50	3	50	ns	
$\overline{RAS}$ precharge time	t <sub>RP</sub>	50		60		ns	
$\overline{RAS}$ pulse width	t <sub>RAS</sub>	70	10000	80	10000	ns	
$\overline{RAS}$ pulse width for fast page mode cycle only	t <sub>RASP</sub>	70	100000	80	100000	ns	

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LC322271J, M, T-70/80

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Parameter	Symbol	-70		-80		Unit	Note
		min	max	min	max		
$\overline{\text{RAS}}$ hold time	$t_{\text{RSH}}$	20		30		ns	
$\overline{\text{CAS}}$ hold time	$t_{\text{CSH}}$	70		80		ns	
$\overline{\text{CAS}}$ pulse width	$t_{\text{CAS}}$	20	10000	30	10000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	$t_{\text{RCD}}$	25	50	25	50	ns	14
$\overline{\text{RAS}}$ to column address delay time	$t_{\text{RAD}}$	17	35	17	35	ns	15
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	$t_{\text{CRP}}$	10		10		ns	
$\overline{\text{CAS}}$ precharge time	$t_{\text{CP}}$	10		10		ns	
Row address setup time	$t_{\text{ASR}}$	0		0		ns	
Row address hold time	$t_{\text{RAH}}$	12		12		ns	
Column address setup time	$t_{\text{ASC}}$	0		0		ns	
Column address hold time	$t_{\text{CAH}}$	15		20		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	$t_{\text{AR}}$	50		60		ns	
Column address to $\overline{\text{RAS}}$ lead time	$t_{\text{RAL}}$	40		45		ns	
Read command setup time	$t_{\text{RCS}}$	0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	$t_{\text{RCH}}$	0		0		ns	11
Read command hold time referenced to $\overline{\text{RAS}}$	$t_{\text{RRH}}$	0		0		ns	11
Write command hold time	$t_{\text{WCH}}$	15		15		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	$t_{\text{WCR}}$	50		60		ns	
Write command pulse width	$t_{\text{WP}}$	15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	$t_{\text{RWL}}$	25		25		ns	
Write command to $\overline{\text{CAS}}$ lead time	$t_{\text{CWL}}$	20		20		ns	
Data input setup time	$t_{\text{DS}}$	0		0		ns	12
Data input hold time	$t_{\text{DH}}$	15		20		ns	12
Data input hold time referenced to $\overline{\text{RAS}}$	$t_{\text{DHR}}$	50		60		ns	
Refresh time	$t_{\text{REF}}$		8		8	ms	
Write command setup time	$t_{\text{WCS}}$	0		0		ns	13
$\overline{\text{CAS}}$ to $\overline{\text{UW}}$ , $\overline{\text{LW}}$ delay time	$t_{\text{CWD}}$	50		50		ns	13
$\overline{\text{RAS}}$ to $\overline{\text{UW}}$ , $\overline{\text{LW}}$ delay time	$t_{\text{RWD}}$	100		100		ns	13
Column address to $\overline{\text{UW}}$ , $\overline{\text{LW}}$ delay time	$t_{\text{AWD}}$	65		65		ns	13
$\overline{\text{CAS}}$ precharge $\overline{\text{UW}}$ , $\overline{\text{LW}}$ delay time for fast page mode cycle only	$t_{\text{CPWD}}$	70		70		ns	13
$\overline{\text{CAS}}$ setup time for $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$	$t_{\text{CSR}}$	10		10		ns	
$\overline{\text{CAS}}$ hold time for $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$	$t_{\text{CHR}}$	15		15		ns	
$\overline{\text{RAS}}$ precharge $\overline{\text{CAS}}$ active time	$t_{\text{RPC}}$	10		10		ns	
$\overline{\text{CAS}}$ precharge time for $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ counter test	$t_{\text{CPT}}$	40		40		ns	
$\overline{\text{RAS}}$ hold time referenced to $\overline{\text{OE}}$	$t_{\text{ROH}}$	15		15		ns	
$\overline{\text{OE}}$ access time	$t_{\text{OEA}}$		20		25	ns	9
$\overline{\text{OE}}$ delay time	$t_{\text{OED}}$	15		15		ns	
$\overline{\text{OE}}$ output buffer turn-off delay time	$t_{\text{O EZ}}$	0		0	15	ns	10
$\overline{\text{OE}}$ command hold time	$t_{\text{OEH}}$	20		20		ns	
Data input to $\overline{\text{CAS}}$ delay time	$t_{\text{DZC}}$	0		0		ns	16
Data input to $\overline{\text{OE}}$ delay time	$t_{\text{DZO}}$	0		0		ns	16
Masked write setup time	$t_{\text{MCS}}$	0		0		ns	
Masked write hold time referenced to $\overline{\text{RAS}}$	$t_{\text{MRH}}$	0		0		ns	
Masked write hold time referenced to $\overline{\text{CAS}}$	$t_{\text{MCH}}$	0		0		ns	

## LC322271J, M, T-70/80

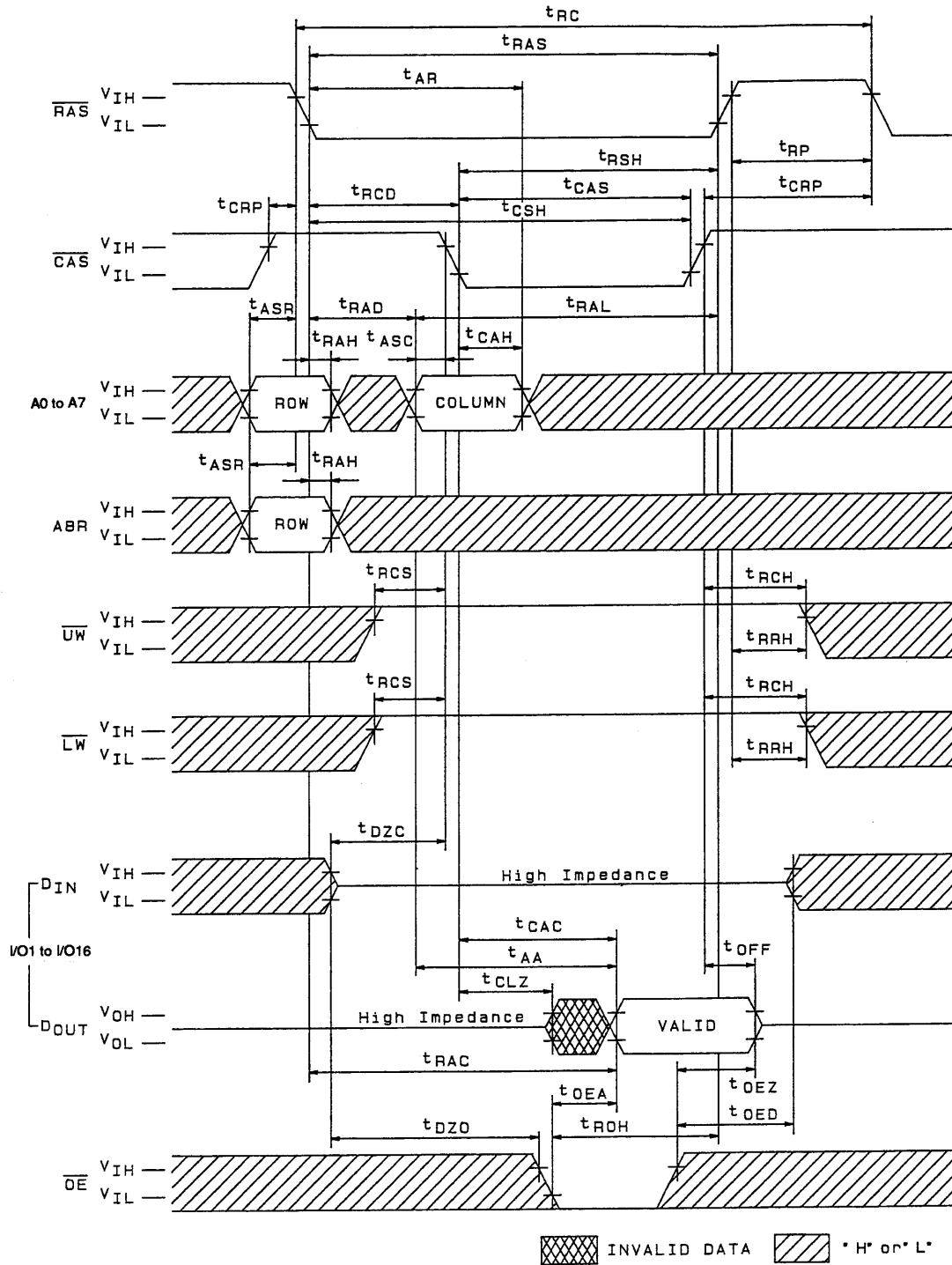
### Input/Output Capacitance at $T_a = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = 5\text{ V} \pm 10\%$

Parameter	Symbol	min	max	Unit	Note
Input capacitance (A0 to A7, A8R, $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{UW}}$ , $\overline{\text{LW}}$ , $\overline{\text{OE}}$ )	$C_{\text{IN}}$		7	pF	
Input/Output capacitance (I/O1 to I/O16)	$C_{\text{I/O}}$		7	pF	

- Note:
6. An initial pause of 200  $\mu\text{s}$  is required after power-up followed by eight  $\overline{\text{RAS}}$ -only refresh cycles before proper device operation is achieved. In case of using refresh counter, a minimum of eight  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycles instead of eight  $\overline{\text{RAS}}$ -only refresh cycles are required.
  7. Measured at  $t_T = 5\text{ ns}$ .
  8. When measuring input signal timing,  $V_{\text{IH}}$  (min) and  $V_{\text{IL}}$  (max) are used for reference points. In addition, rise and fall time are defined between  $V_{\text{IH}}$  and  $V_{\text{IL}}$ .
  9. Measured using an equivalent of 50 pF and one standard TTL loads.
  10.  $t_{\text{OFF}}$  (max) and  $t_{\text{OEZ}}$  (max) are defined as the time until output voltage can no longer be measured when output switches to a high impedance condition.
  11. Operation is guaranteed if either  $t_{\text{RRH}}$  or  $t_{\text{RCH}}$  is satisfied.
  12. These parameters are measured from the falling edge of  $\overline{\text{CAS}}$  for an early-write cycle, and from the falling edge of  $\overline{\text{UW}}$  and  $\overline{\text{LW}}$  for a read-write/read-modify-write cycle.
  13.  $t_{\text{WCS}}$ ,  $t_{\text{CWD}}$ ,  $t_{\text{RWD}}$ ,  $t_{\text{AWD}}$  and  $t_{\text{CPWD}}$  are not restrictive operating parameters for memory in that they specify the operating mode. If  $t_{\text{WCS}} \geq t_{\text{WCS}}$  (min), the cycle switches to an early-write cycle and output pins switch to high impedance throughout the cycle.  
If  $t_{\text{CWD}} \geq t_{\text{CWD}}$  (min),  $t_{\text{RWD}} \geq t_{\text{RWD}}$  (min),  $t_{\text{AWD}} \geq t_{\text{AWD}}$  (min) and  $t_{\text{CPWD}} \geq t_{\text{CPWD}}$  (min) for fast page mode cycle only, the cycle switches to a read-write/read-modify-write cycle and data output equal information in the selected cells. If neither of the above timings are satisfied, output pins are in an undefined state.
  14.  $t_{\text{RCD}}$  (max) is not a restrictive operating parameter but instead represents the point at which the access time  $t_{\text{RAC}}$  (max) is guaranteed. If  $t_{\text{RCD}} \geq t_{\text{RCD}}$  (max), access time is determined according to  $t_{\text{CAC}}$ .
  15.  $t_{\text{RAD}}$  (max) is not a restrictive operating parameter but instead represents the point at which the access time  $t_{\text{RAC}}$  (max) is guaranteed. If  $t_{\text{RAD}} \geq t_{\text{RAD}}$  (max), access time is determined according to  $t_{\text{AA}}$ .
  16. Operation is guaranteed if either  $t_{\text{DZC}}$  or  $t_{\text{DZO}}$  is satisfied.

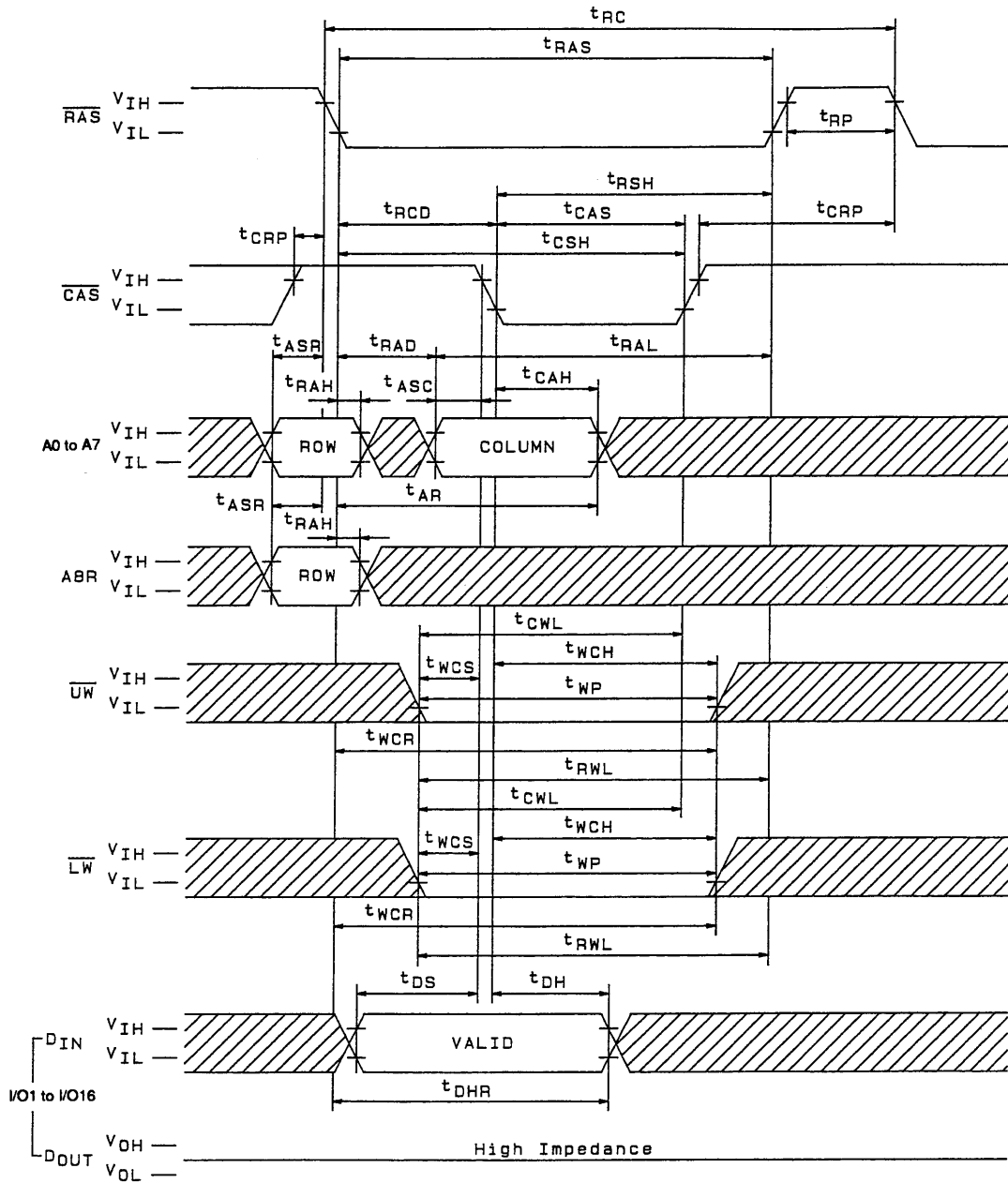
Timing Chart

Read Cycle



A02907

Early Write Cycle



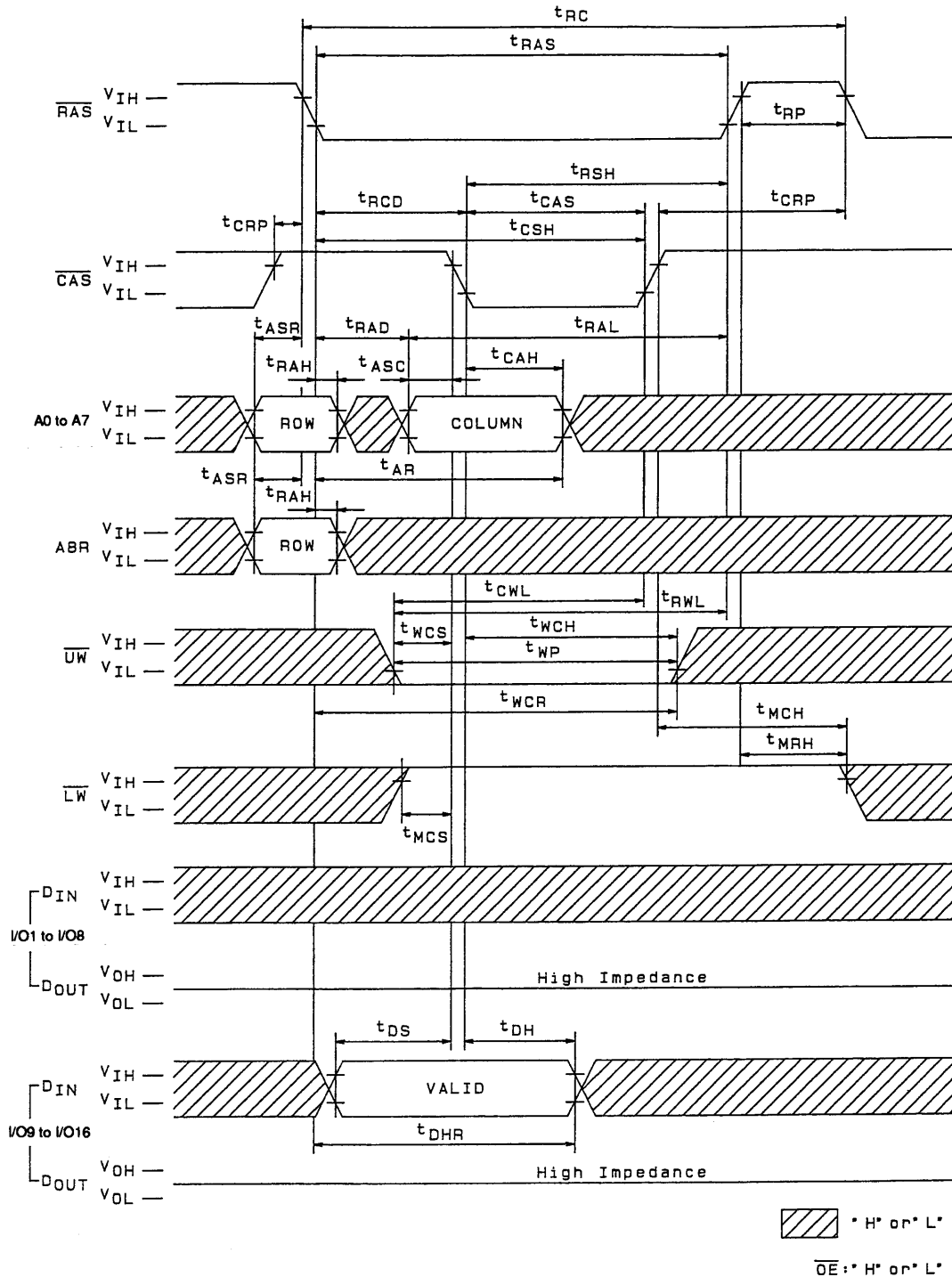
\* H\* or L\*

$\overline{OE}$ : \* H\* or L\*

A02808

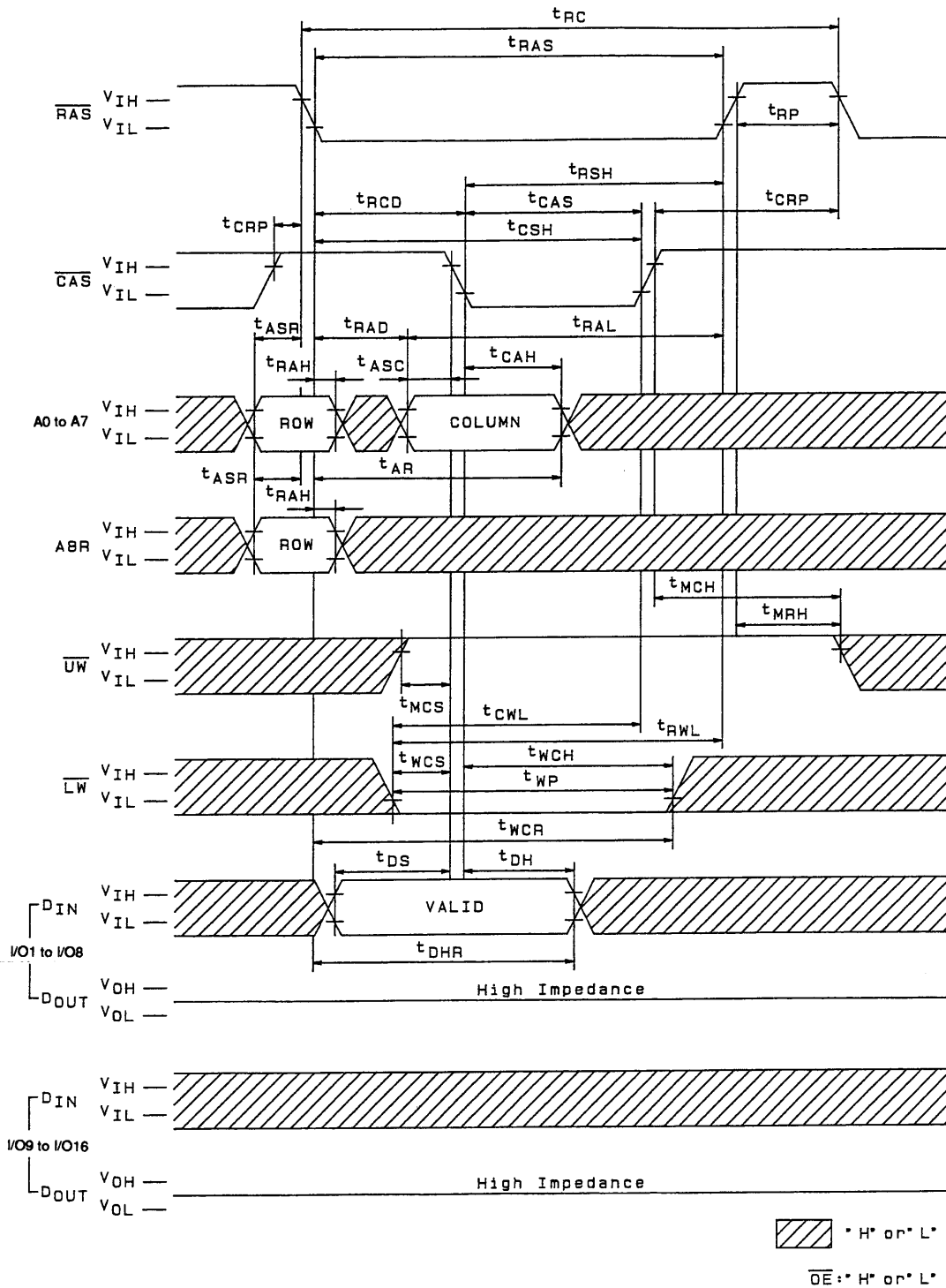


Upper Byte Early Write Cycle



A02909

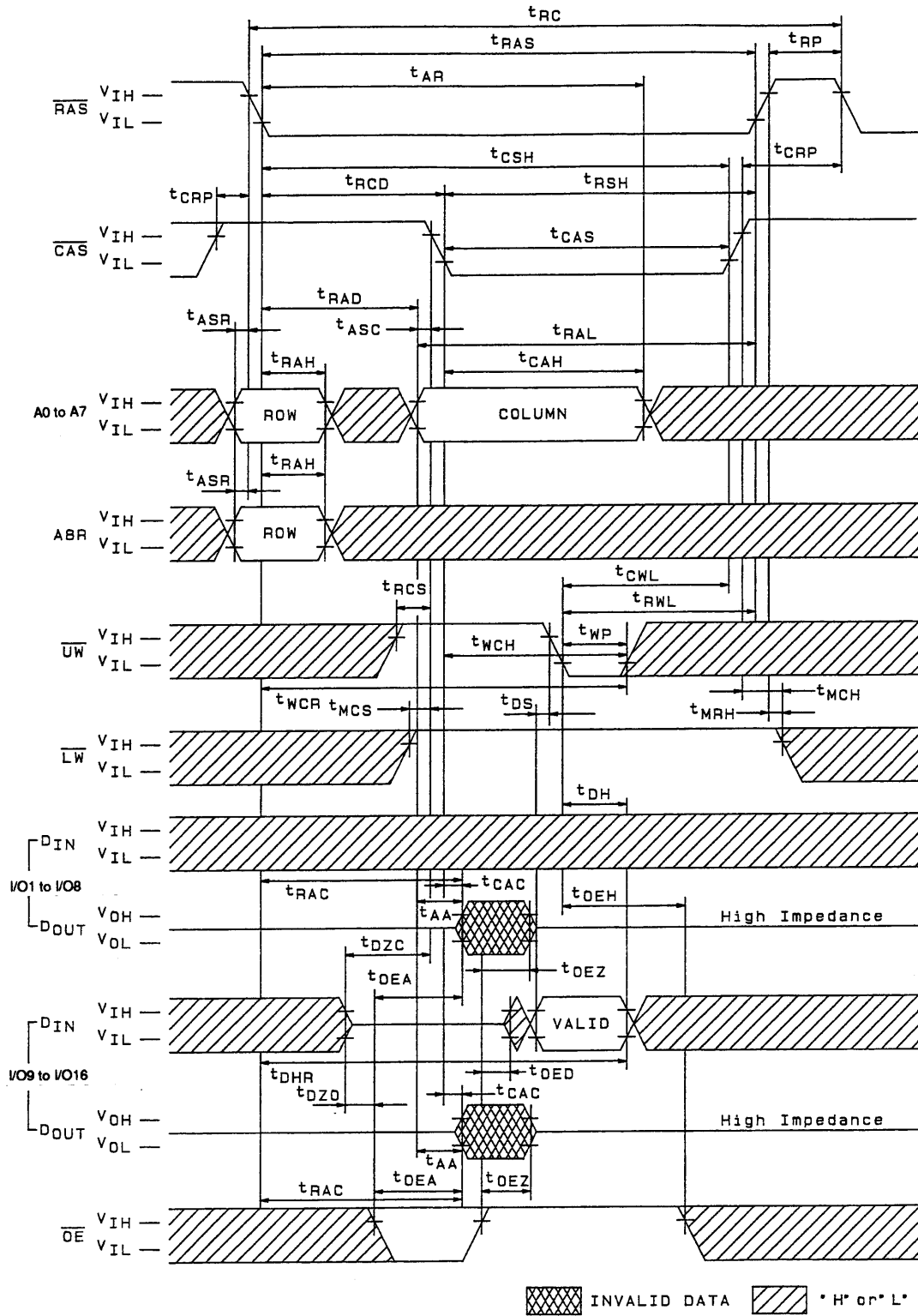
Lower Byte Early Write Cycle



A02910



Upper Byte Write Cycle ( $\overline{OE}$  Control)

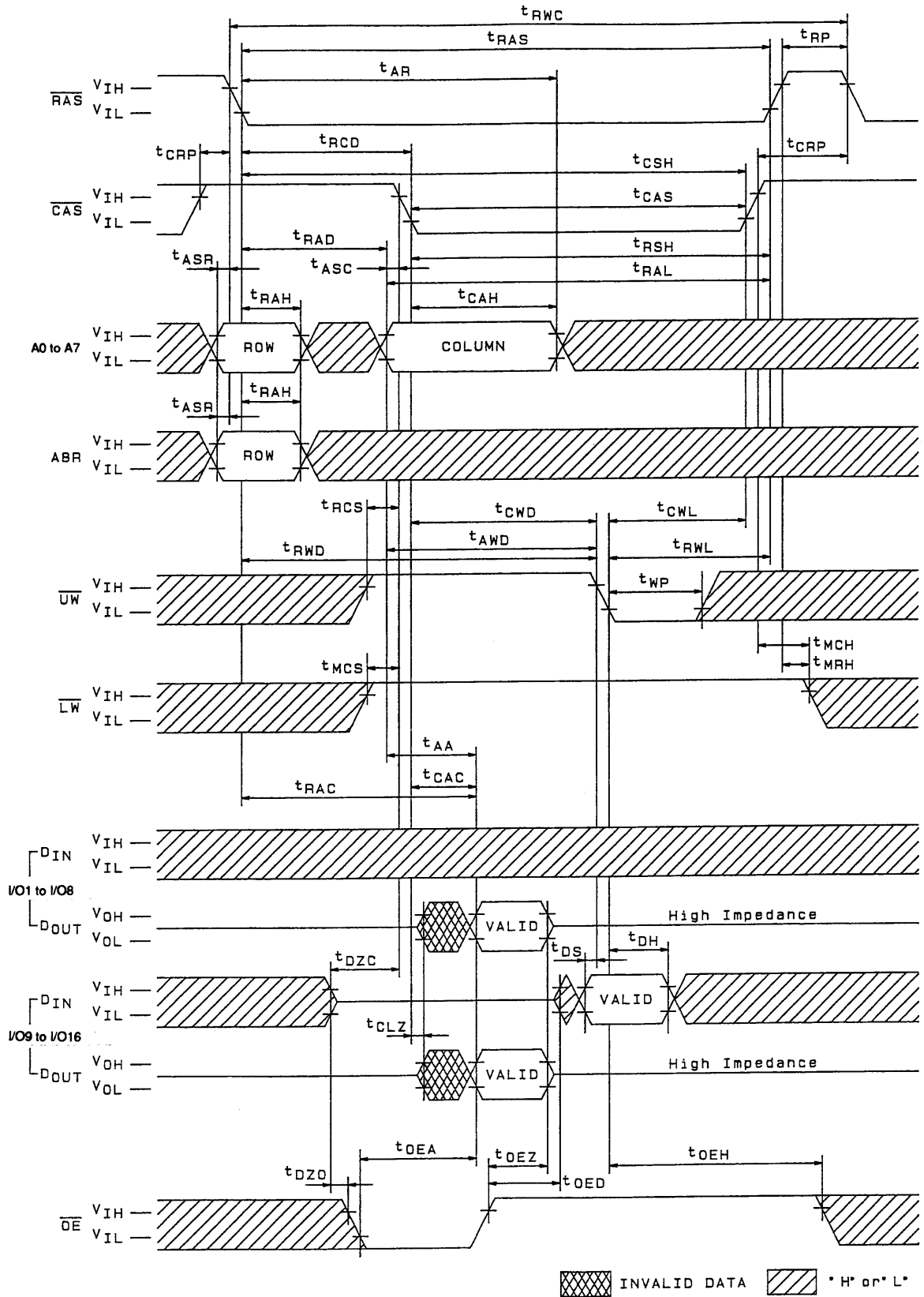


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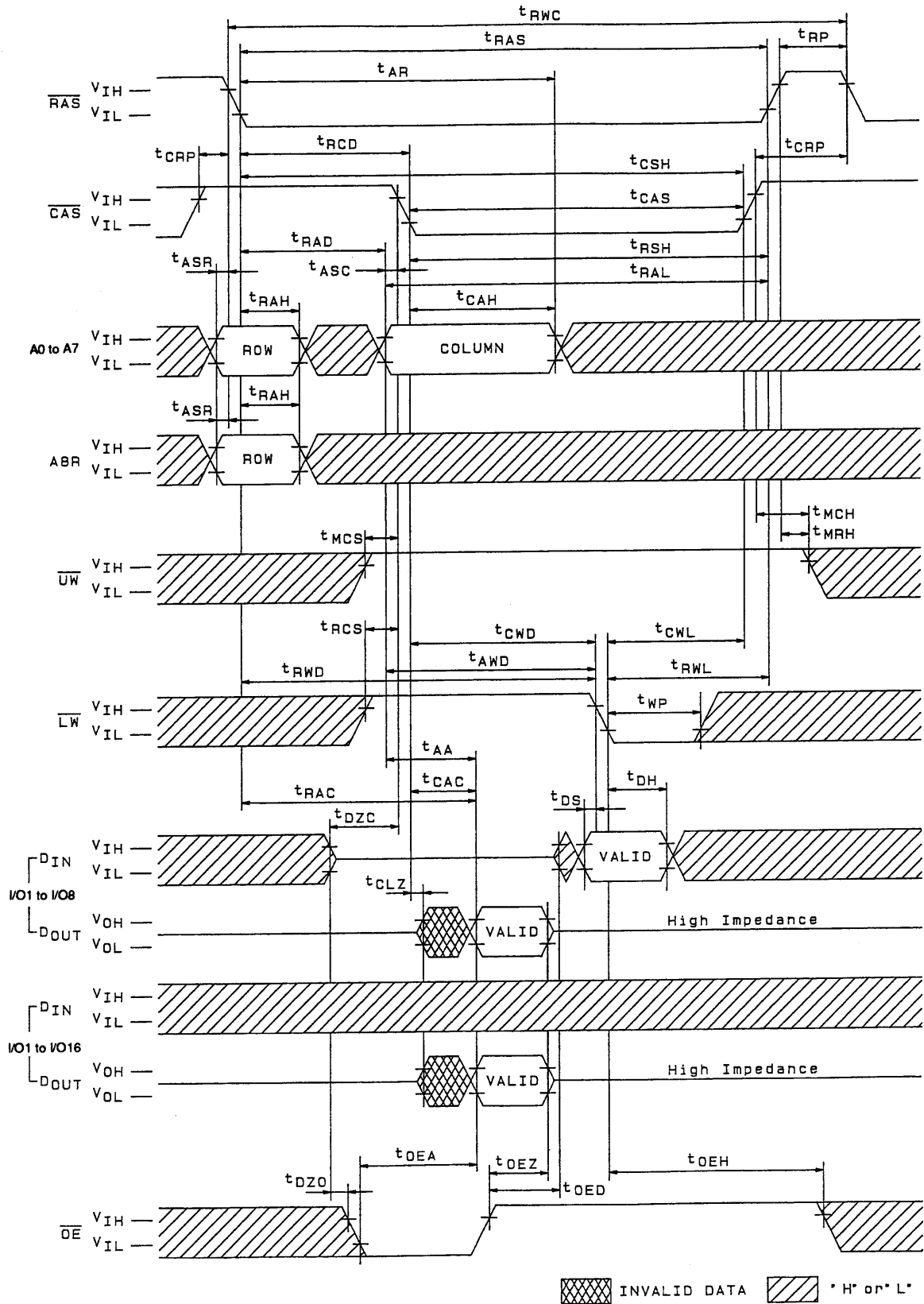




Read-Modify Upper Byte Write Cycle



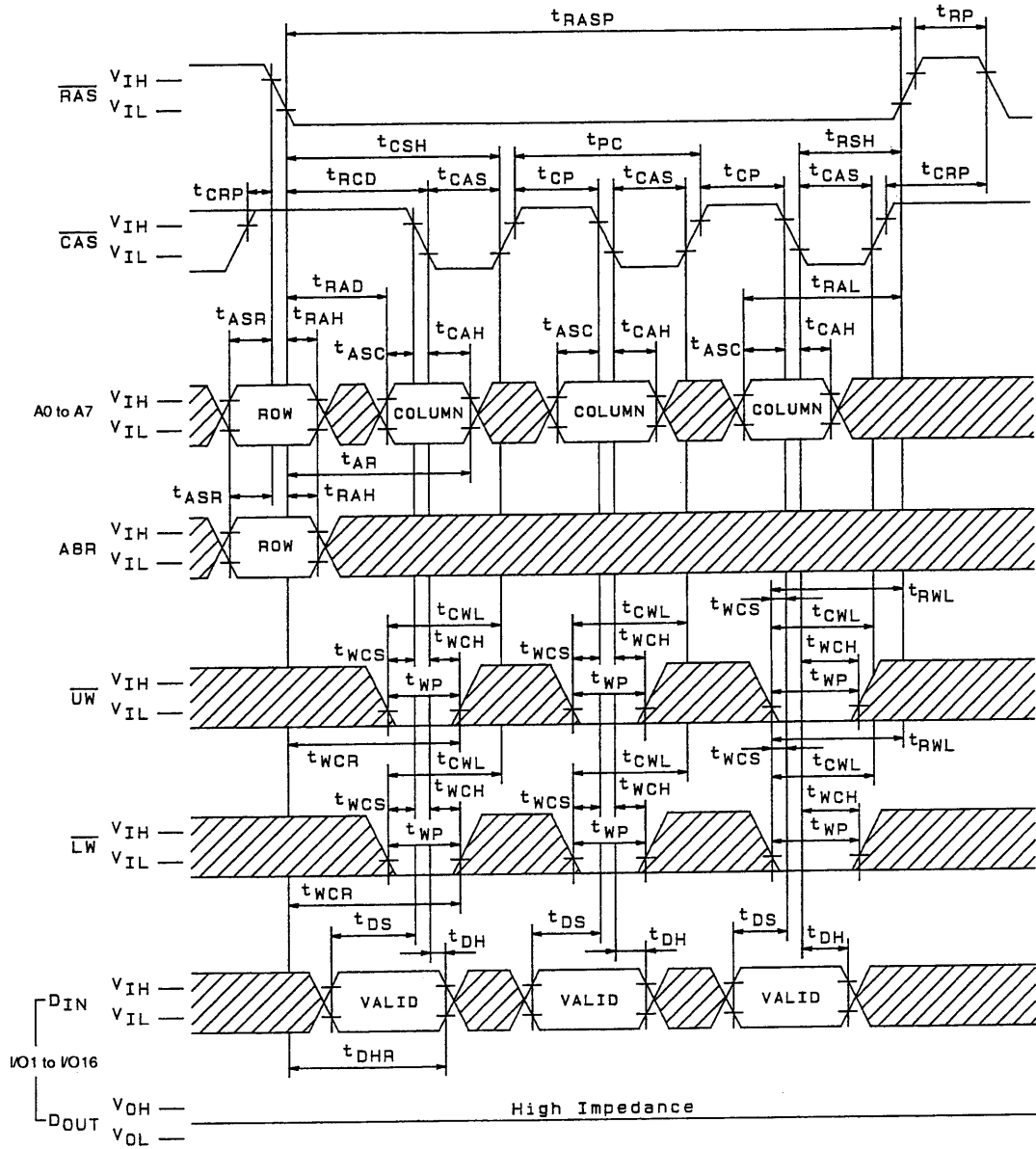
Read-Modify Lower Byte Write Cycle





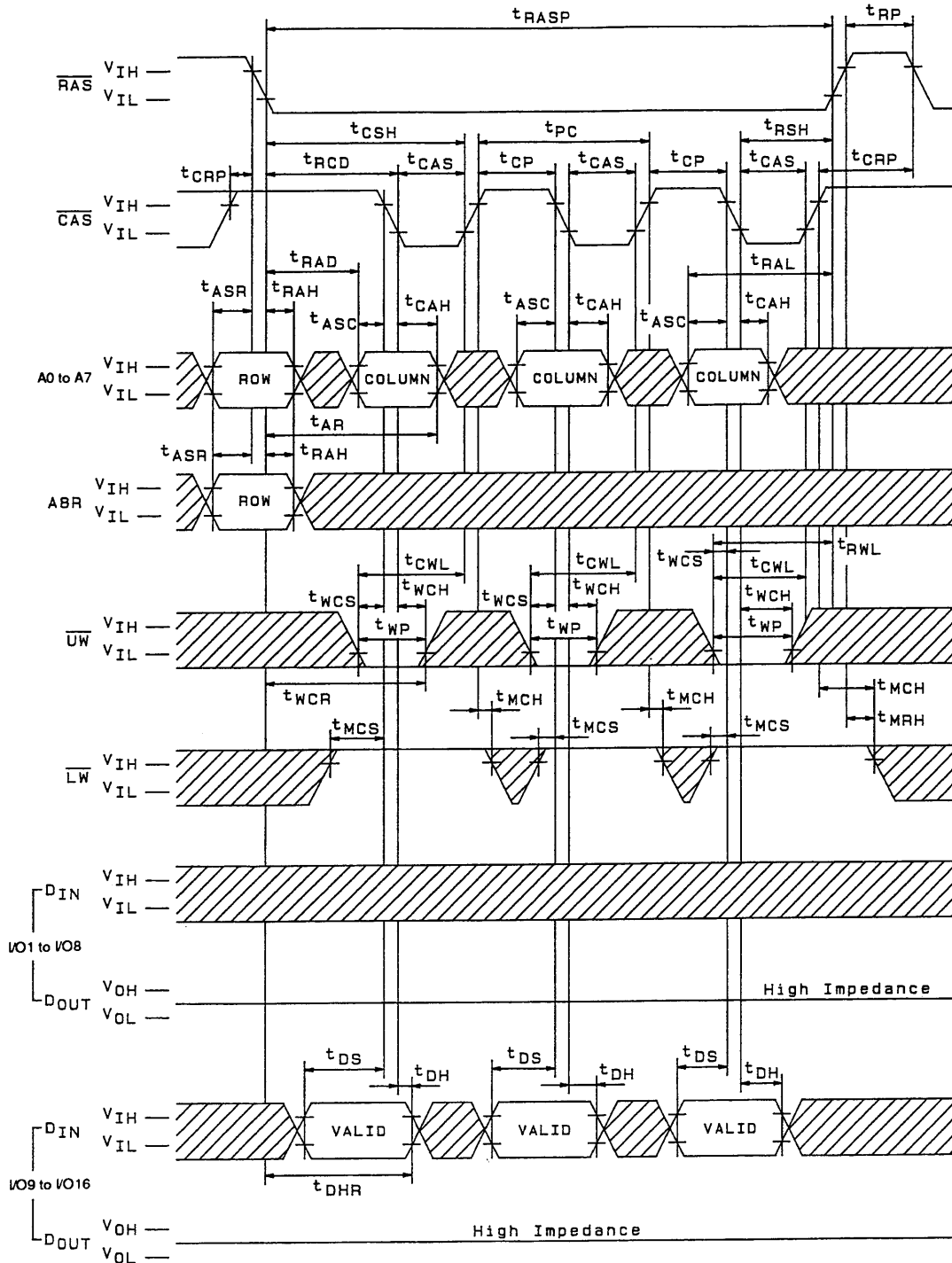


Fast Page Mode Early Write Cycle



A02918

Fast Page Mode Upper Byte Early Write Cycle

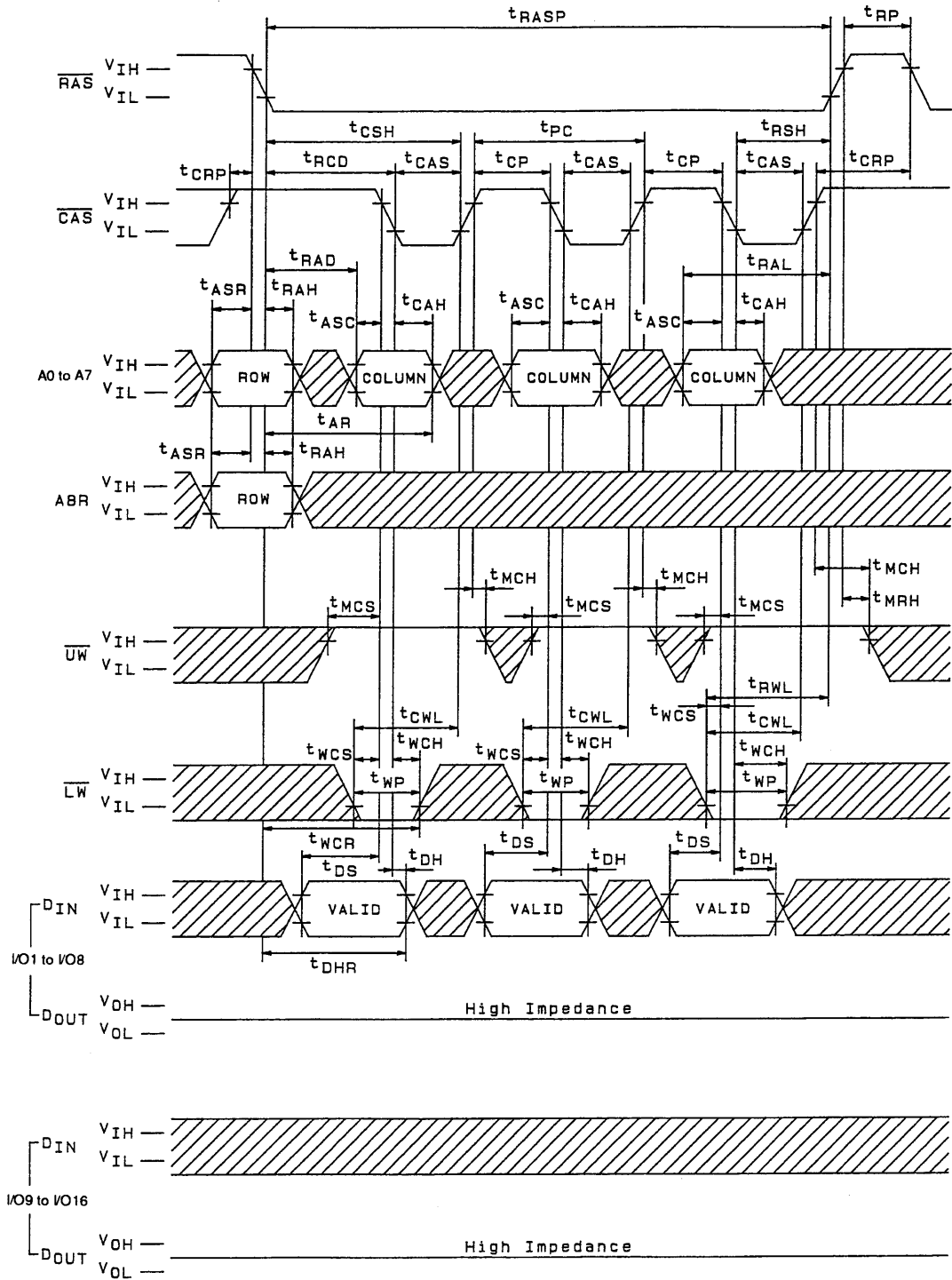


▨ \* H\* or \* L\*

$\overline{OE}$ : \* H\* or \* L\*

A02919

Fast Page Mode Lower Byte Early Write Cycle



\* H\* or L\*

$\overline{OE}$ : \* H\* or L\*

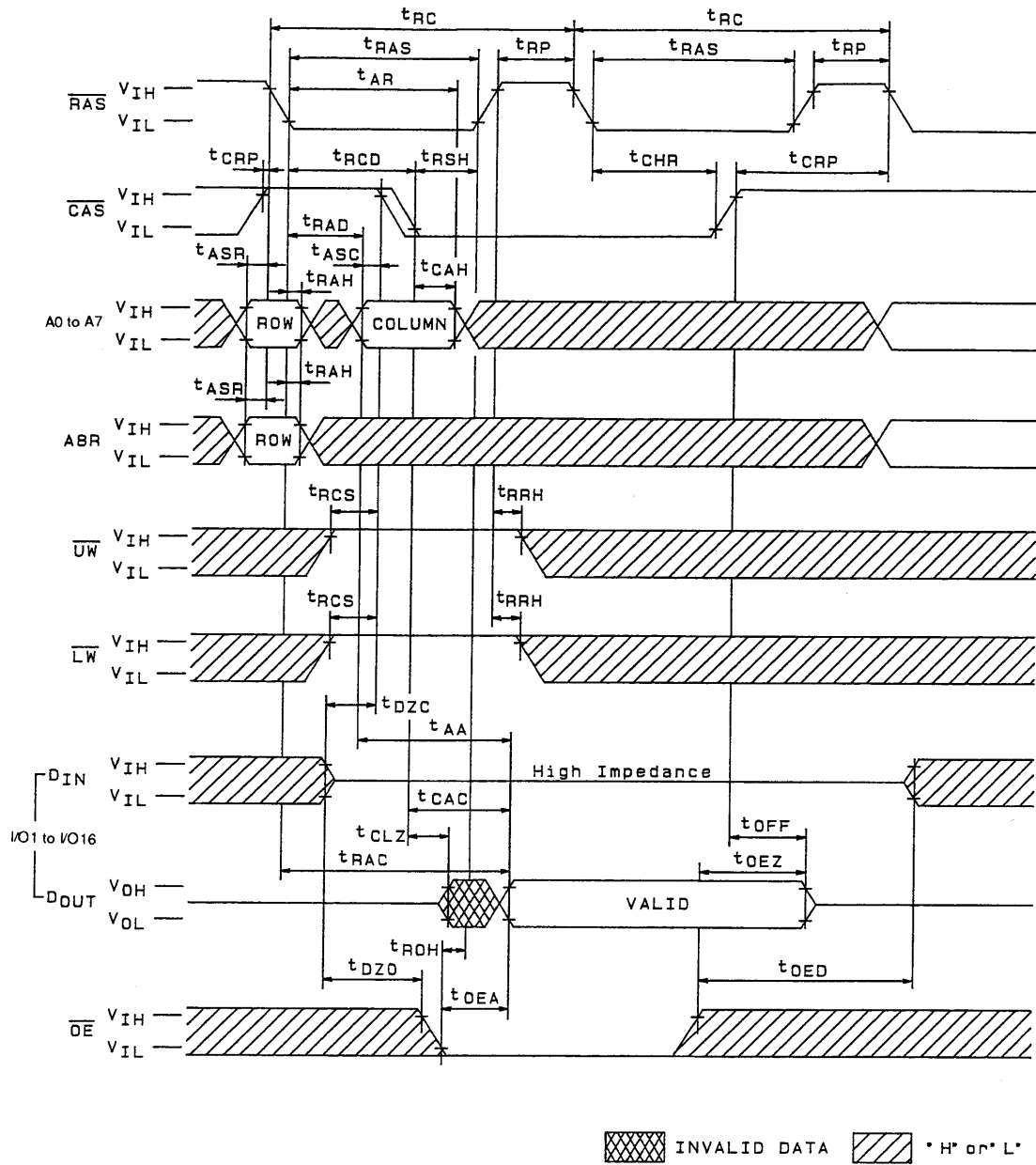
A02920







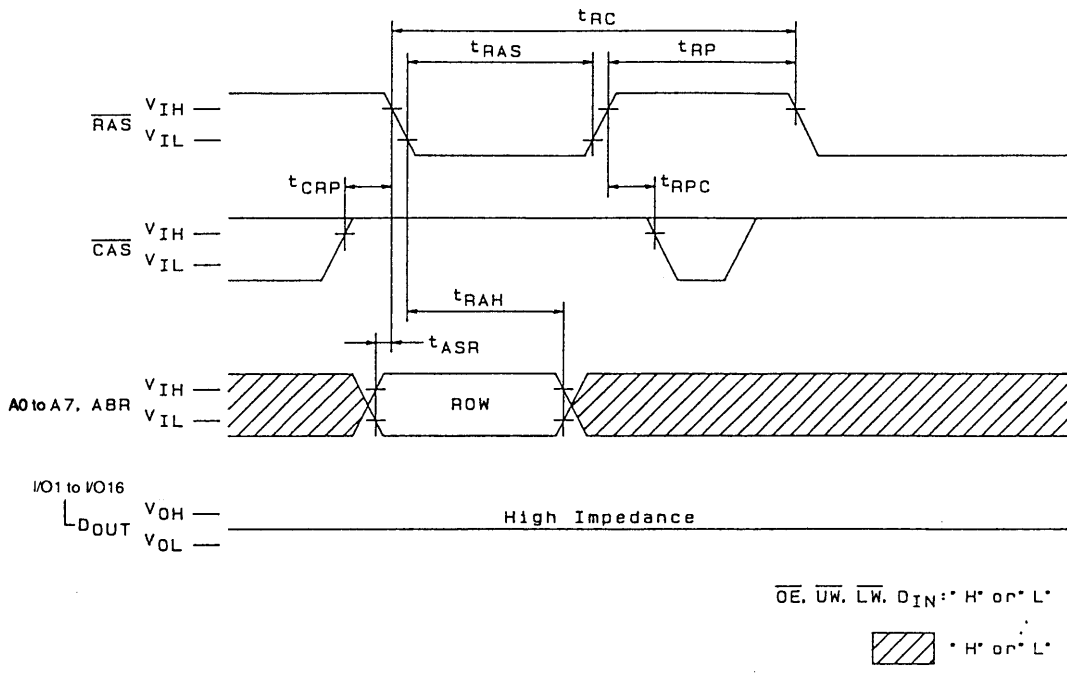
Hidden Refresh Cycle



A02924

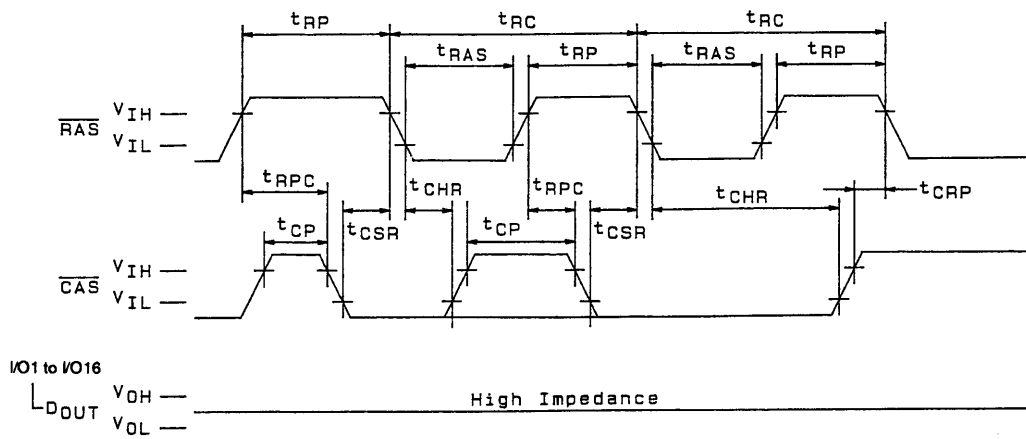


RAS-Only Refresh Cycle



A02925

CAS-Before-RAS Refresh Cycle

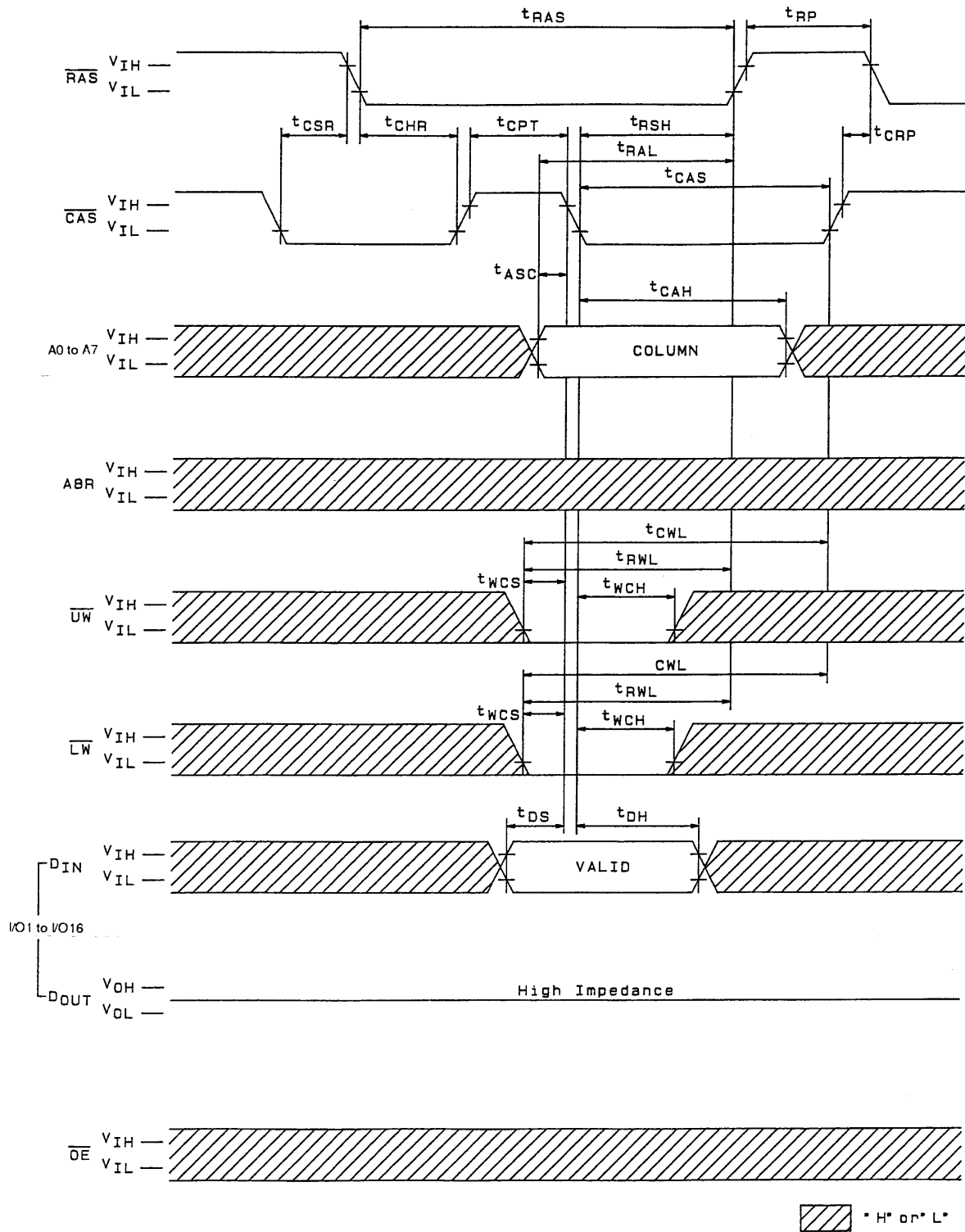


A0 to A7, ABR,  $\overline{UW}, \overline{LW}, \overline{OE}, \overline{DIN}$ : "H" or "L"

A02926



CAS-Before-RAS Refresh Counter Test Cycle (Write)





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