

SANYO	No. ※5341	LC322260J, T-70/80
	2 MEG (131072 words × 16 bits) DRAM Fast Page Mode, Byte Read/Write	

Preliminary

Overview

The LC322260J, T are CMOS dynamic RAMs operating on a single 5 V power source and having a 131072 words × 16 bits organization. Featuring a large capacity, high speed, and low power dissipation, these products are appropriate for a wide range of applications, from main and expansion memory in computer systems to consumer products. The adoption of a multiplexed input technique allows these products to be provided in compact 40-pin SOJ and 44-pin TSOP packages. These products support three refresh techniques: $\overline{\text{RAS}}$ only refresh, in which 512 row addresses (A0 to A7, A8R) are selected within 8 ms, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, and hidden refresh. Finally, these products support three memory access functions: fast page mode, read-modify-write and byte read/write.

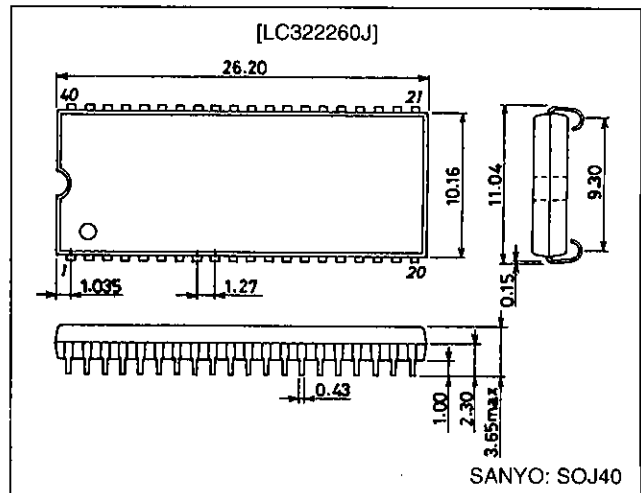
Features

- 131072 words × 16 bits configuration
- Single 5 V ± 10% power supply
- All input and output (I/O) TTL compatible
- Supports fast page mode, read-modify-write, and byte read/write using 2 $\overline{\text{CAS}}$ lines
- Early write, and output buffer $\overline{\text{OE}}$ control
- 8 ms refresh using 512 refresh cycles
- $\overline{\text{RAS}}$ only refresh, $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh, and hidden refresh
- 2 $\overline{\text{CAS}}$ and 1 $\overline{\text{WE}}$ inputs (Two $\overline{\text{CAS}}$ lines: $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$)
- Pin assignment conforms to the JEDEC standards for 4M DRAM (262144 words × 16 bits, 2 $\overline{\text{CAS}}$ /1 $\overline{\text{WE}}$ type)
- Packages
 SOJ 40-pin (400 mil) plastic package: LC322260J
 TSOP 44-pin (400 mil) plastic package: LC322260T
- $\overline{\text{RAS}}$ access time/Column address access time/ $\overline{\text{CAS}}$ access time/Cycle time/Power dissipation

Package Dimensions

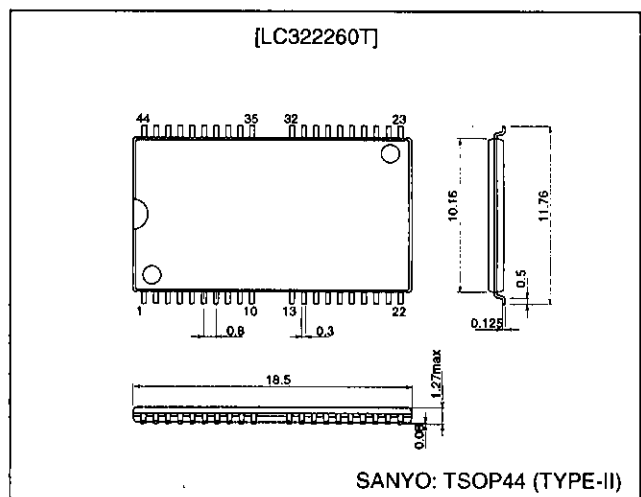
unit: mm

3200-SOJ40



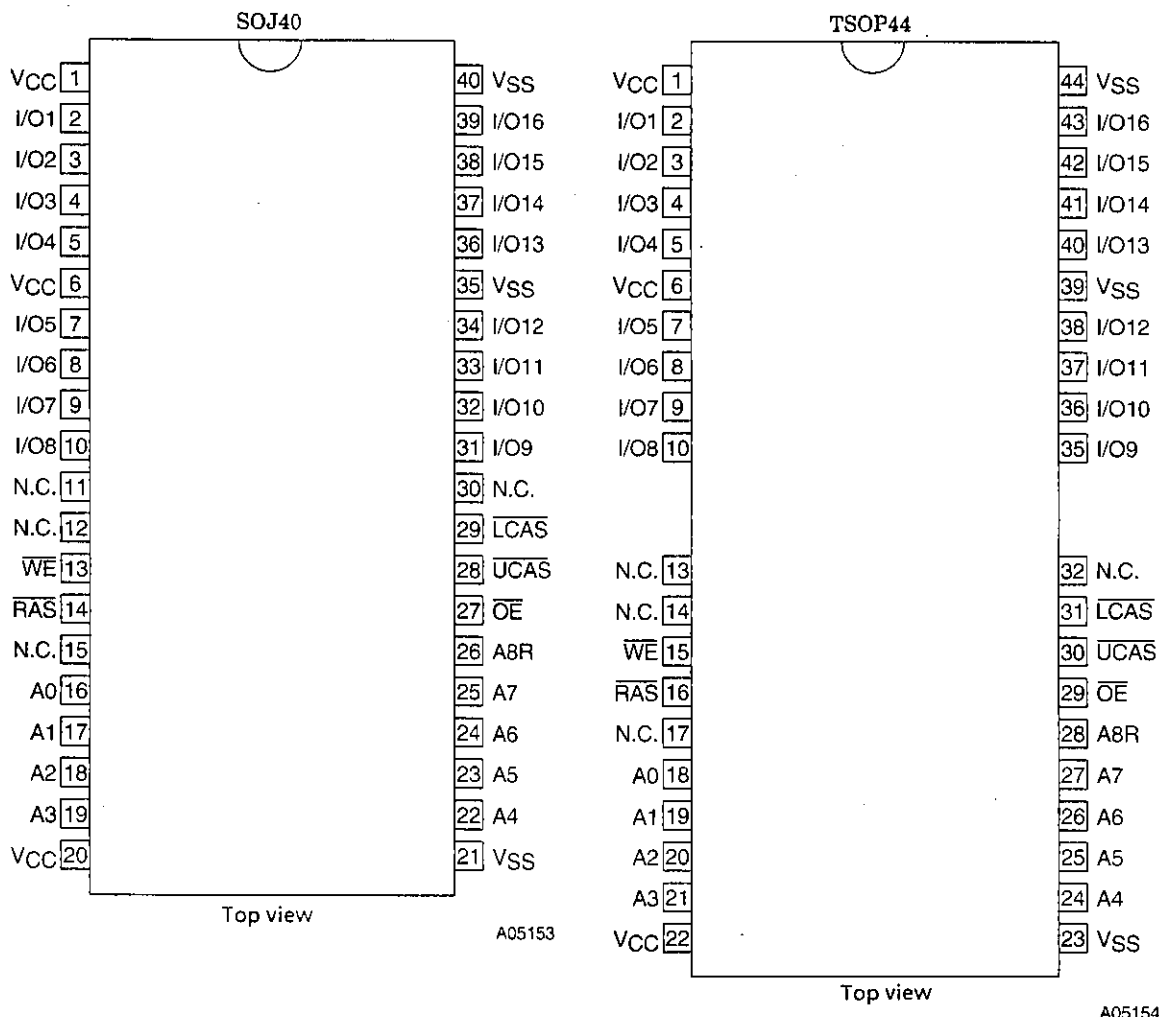
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3207A-TSOP44

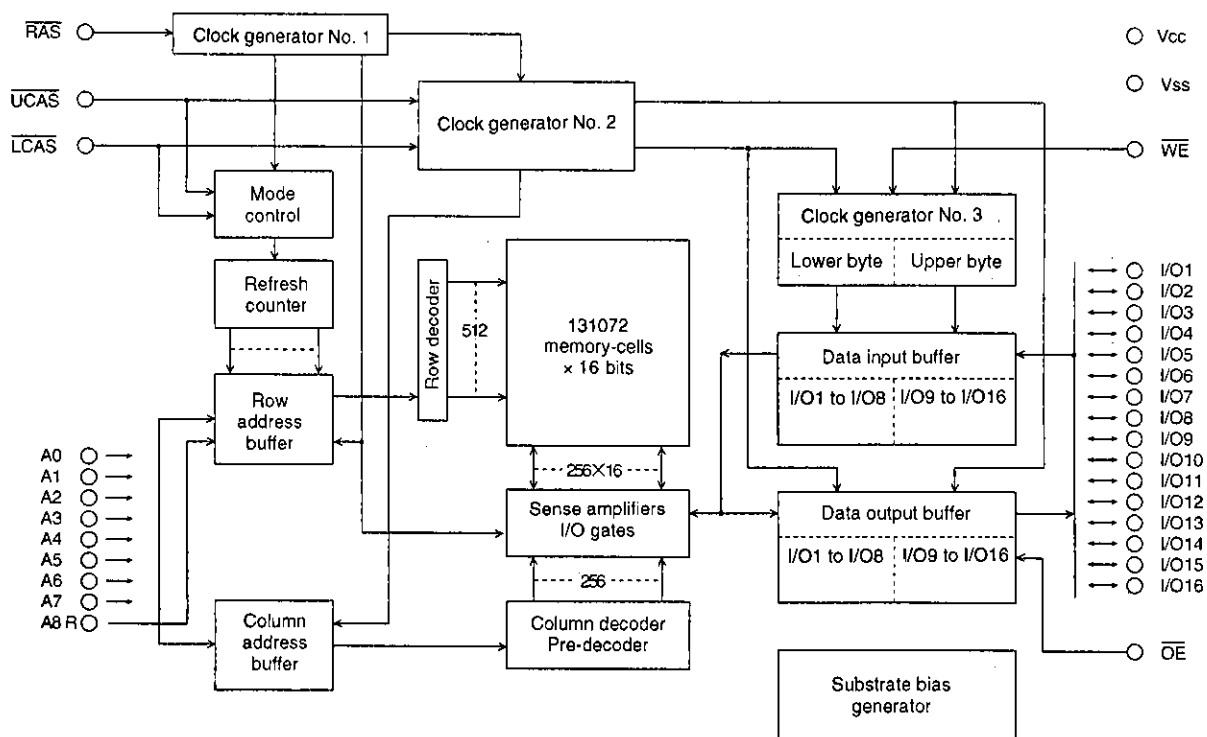


Parameter	LC322260T, J	
	-70	-80
$\overline{\text{RAS}}$ access time	70 ns	80 ns
Column address access time	35 ns	45 ns
$\overline{\text{CAS}}$ access time	20 ns	30 ns
Cycle time	130 ns	150 ns
Power dissipation	During operation	688 mW
	During standby	633 mW
		5.5 mW (CMOS level), 11 mW (TTL level)

Pin Assignments



Block Diagram



Specifications

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Maximum supply voltage	$V_{CC\ max}$	-1.0 to +7.0	V	1
Input voltage	V_{IN}	-1.0 to +7.0	V	1
Output voltage	V_{OUT}	-1.0 to +7.0	V	1
Allowable power dissipation	LC322260J	800	mW	1
	LC322260T	700		
Output shorted current	I_{OUT}	50	mA	1
Operating temperature	T_{opr}	0 to +70	°C	1
Storage temperature	T_{stg}	-55 to +150	°C	1

Note: 1. Stresses greater than the above listed maximum values may result in damage to the device.

DC Recommended Operating Ranges at $T_a = 0$ to +70°C

Parameter	Symbol	min	typ	max	Unit	Note
Supply voltage	V_{CC}	4.5	5.0	5.5	V	2
Input high-level voltage	V_{IH}	2.4		6.5	V	2
Input low-level voltage (A0 to A7, A8R, \overline{RAS} , UCAS, LCAS, WE, and OE)	V_{IL}	-1.0*		+0.8	V	2
Input low-level voltage (I/O1 to I/O16)	V_{IL}	-0.5*		+0.8	V	2

Note: 2. All voltages are referenced to V_{SS} .
* -2.0 V for pulses shorter than 20 ns.

DC Electrical Characteristics at $T_a = 0$ to +70°C, $V_{CC} = 5\ V \pm 10\%$

Parameter	Symbol	Conditions	LC322260J, T				Unit	Note
			-70		-80			
			min	max	min	max		
Operating current (average current during operation)	I_{CC1}	\overline{RAS} , UCAS, LCAS, address cycling; $t_{RC} = t_{RC\ min}$		125		115	mA	3, 4, 5
Standby current	I_{CC2}	$\overline{RAS} = \overline{UCAS} = \overline{LCAS} = V_{IH}$		2		2	mA	
\overline{RAS} -only refresh current	I_{CC3}	\overline{RAS} cycling; UCAS = LCAS = V_{IH} ; $t_{RC} = t_{RC\ min}$		125		115	mA	3, 5
Fast page mode current	I_{CC4}	$\overline{RAS} = V_{IL}$, UCAS, LCAS, address cycling; $t_{PC} = t_{PC\ min}$		115		90	mA	3, 4, 5
Standby current	I_{CC5}	$\overline{RAS} = \overline{UCAS} = \overline{LCAS} = V_{CC} - 0.2\ V$		1		1	mA	
\overline{CAS} -before- \overline{RAS} refresh current	I_{CC6}	\overline{RAS} , UCAS, and LCAS cycling; $t_{RC} = t_{RC\ min}$		125		115	mA	3
Input leakage current	I_{IL}	$0\ V \leq V_{IN} \leq 6.5\ V$, pins other than test pin = 0 V.	-10	+10	-10	+10	μA	
Output leakage current	I_{OL}	With D_{OUT} disabled, $0\ V \leq V_{OUT} \leq 5.5\ V$	-10	+10	-10	+10	μA	
Output high-level voltage	V_{OH}	$I_{OUT} = -2.5\ mA$	2.4		2.4		V	
Output low-level voltage	V_{OL}	$I_{OUT} = 2.1\ mA$		0.4		0.4	V	

Note: 3. All current values are measured at minimum cycle rate. Since current flows immoderately, if cycle time is longer than shown here, current value becomes smaller.

4. I_{CC1} and I_{CC4} are dependent on output loads. Maximum values for I_{CC1} and I_{CC4} represent values with output open.

5. Address change is less than or equal to one time during $\overline{RAS} = V_{IL}$. Concerning I_{CC4} , it is less than or equal to one time during 1 cycle (t_{PC}).

LC322260J, T-70/80

AC Electrical Characteristics at Ta = 0 to +70°C, VCC = 5 V ± 10% (See notes 6, 7, and 8.)

Parameter	Symbol	LC322260J, T				Unit	Note
		-70		-80			
		min	max	min	max		
Random read and write cycle time	t _{RC}	130		150		ns	
Read-modify-write cycle time	t _{RWC}	190		200		ns	
Fast page mode cycle time	t _{PC}	45		55		ns	
Fast page mode and read-modify-write cycle time	t _{PRWC}	95		100		ns	
RAS access time	t _{RAC}		70		80	ns	9, 14, 15
CAS access time	t _{CAC}		20		30	ns	9, 14
Column address access time	t _{AA}		35		45	ns	9, 15
CAS precharge access time	t _{CPA}		40		50	ns	9
CAS low to output low impedance time	t _{CLZ}	0		0		ns	9
Output buffer turn-off delay time	t _{OFF}	0	20	0	20	ns	10
Rise and fall times	t _T	3	50	3	50	ns	
RAS precharge time	t _{RP}	50		60		ns	
RAS pulse width	t _{RAS}	70	10000	80	10000	ns	
RAS pulse width (fast page mode cycle only)	t _{RASP}	70	100000	80	100000	ns	
RAS hold time	t _{RSH}	20		30		ns	
CAS hold time	t _{CSH}	70		80		ns	
CAS pulse width	t _{CAS}	20	10000	30	10000	ns	
RAS to CAS delay time	t _{RCD}	25	50	25	50	ns	14
RAS to column address delay time	t _{RAD}	17	35	17	35	ns	15
CAS to RAS precharge time	t _{CRP}	10		10		ns	
CAS precharge time	t _{CP}	10		10		ns	
Row address setup time	t _{ASR}	0		0		ns	
Row address hold time	t _{RAH}	12		12		ns	
Column address setup time	t _{ASC}	0		0		ns	
Column address hold time	t _{CAH}	15		20		ns	
Column address hold time (referenced to RAS)	t _{AR}	50		60		ns	
Column address to RAS read time	t _{RAL}	40		45		ns	
Read command setup time	t _{RCS}	0		0		ns	
Read command hold time (referenced to CAS)	t _{RCH}	0		0		ns	11
Read command hold time (referenced to RAS)	t _{RRH}	0		0		ns	11
Write command hold time	t _{WCH}	15		15		ns	
Write command hold time (referenced to RAS)	t _{WCR}	50		60		ns	
Write command pulse width	t _{WP}	15		15		ns	
Write command to RAS read time	t _{RWL}	20		25		ns	
Write command to CAS read time	t _{CWL}	20		20		ns	
Data input setup time	t _{DS}	0		0		ns	12
Data input hold time	t _{DH}	15		20		ns	12
Data input hold time (referenced to RAS)	t _{DHR}	50		60		ns	
Refresh time	t _{REF}		8		8	ms	
Write command setup time	t _{WCS}	0		0		ns	13
CAS to WE delay time	t _{CWD}	50		50		ns	13
RAS to WE delay time	t _{RWD}	100		100		ns	13
Column address to WE delay time	t _{AWD}	65		65		ns	13
CAS precharge time to WE delay time (fast page mode cycle only)	t _{CPWD}	70		70		ns	13
CAS setup time (CAS-before-RAS)	t _{CSR}	10		10		ns	
CAS hold time (CAS-before-RAS)	t _{CHR}	15		15		ns	
RAS precharge time, CAS active time	t _{RPC}	10		10		ns	
CAS precharge time (CAS-before-RAS counter test)	t _{CPT}	40		40		ns	

Continued on next page.

LC322260J, T-70/80

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Parameter	Symbol	LC322260J, T				Unit	Note
		-70		-80			
		min	max	min	max		
RAS hold time (referenced to \overline{OE})	t_{ROH}	15		15		ns	
\overline{OE} access time	t_{OEA}		20		25	ns	9
\overline{OE} delay time	t_{OED}	15		15		ns	
\overline{OE} output buffer turn-off delay time	$t_{O EZ}$	0	15	0	15	ns	10
\overline{OE} command hold time	$t_{OE H}$	20		20		ns	
Data input to \overline{CAS} delay time	t_{DZC}	0		0		ns	16
Data input to \overline{OE} delay time	t_{DZO}	0		0		ns	16

Note: 6. After the power is applied, 200 μ s are required after the V_{CC} achieves the regulated voltage, before memory is initialized and begins operation. In addition, before memory operation initializes, approximately 8 cycles worth of RAS dummy cycles are required. When the on-chip refresh counter is applied, approximately 8 cycles worth of CAS-before-RAS dummy cycles are required instead of the RAS dummy cycles.

7. Measured with $t_T = 5$ ns.

8. When measuring input signal timings, V_{IH} (min) and V_{IL} (max) are used for reference points. In addition, rise and fall time are defined between V_{IH} and V_{IL} .

9. Measured using an equivalent of 50-pF and one standard TTL load.

10. t_{OFF} (max) and $t_{O EZ}$ (max) are defined as the time until output voltage can no longer be measured when output switches to a high impedance condition.

11. Operation is guaranteed if either t_{RRH} or t_{RCH} is satisfied.

12. These parameters are measured from the falling edge of \overline{UCAS} or \overline{LCAS} for the early write cycle, and from the falling edge of \overline{WE} for the read-modify-write cycle.

13. t_{WCS} , t_{CWD} , t_{RWD} , t_{AWD} , and t_{CPWD} are not restrictive operating parameters for memory in that they specify the operating mode. If $t_{WCS} \geq t_{WCS}$ (min), the cycles switches to an early-write cycle and output pins switch to high impedance throughout the cycle.

If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) for fast page mode cycle only, the cycle switched to a read-write/read-modify-write cycle and data output equal information in the selected cells. If neither of the above timings are satisfied, output pins are in an undefined state.

14. t_{RCD} (max) is not a restrictive operating parameter but instead represents the point at which the access time t_{RAC} (max) is guaranteed. If $t_{RCD} \geq t_{RCD}$ (max), access time is determined according to t_{CAC} .

15. t_{RAD} (max) is not a restrictive operating parameter but instead represents the point at which the access time t_{RAC} (max) is guaranteed. If $t_{RAD} \geq t_{RAD}$ (max), access time is determined according to t_{AA} .

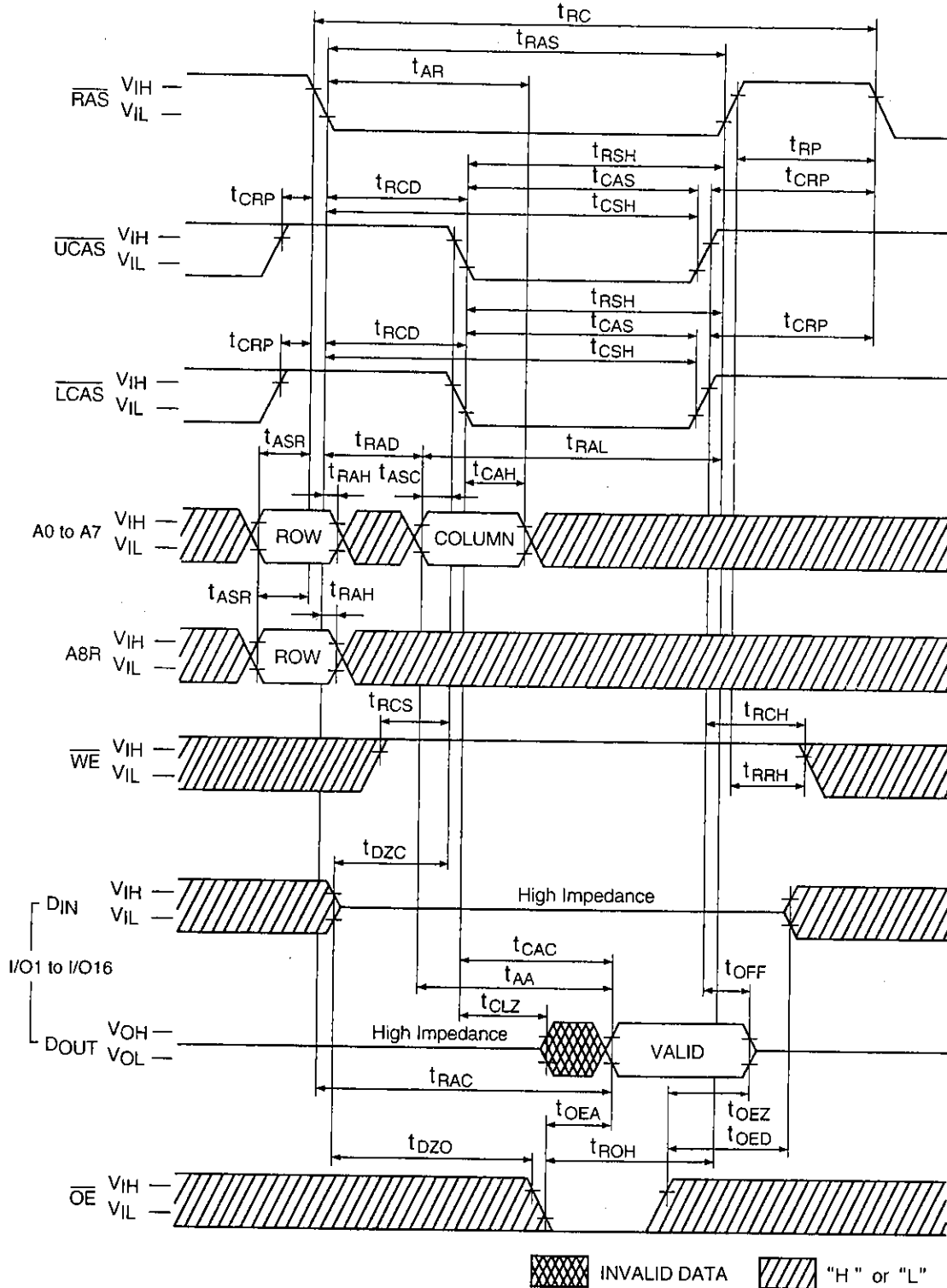
16. Operation is guaranteed if either t_{DZC} or t_{DZO} is satisfied.

Input/Output Capacitances at $T_a = 25^\circ\text{C}$, $f = 1$ MHz, $V_{CC} = 5\text{ V} \pm 10\%$

Parameter	Symbol	min	max	Unit
Input capacitance (A0 to A7, A8R, RAS, \overline{UCAS} , \overline{LCAS} , \overline{WE} , and \overline{OE})	C_{IN}		7	pF
I/O capacitance (I/O1 to I/O16)	$C_{I/O}$		7	pF

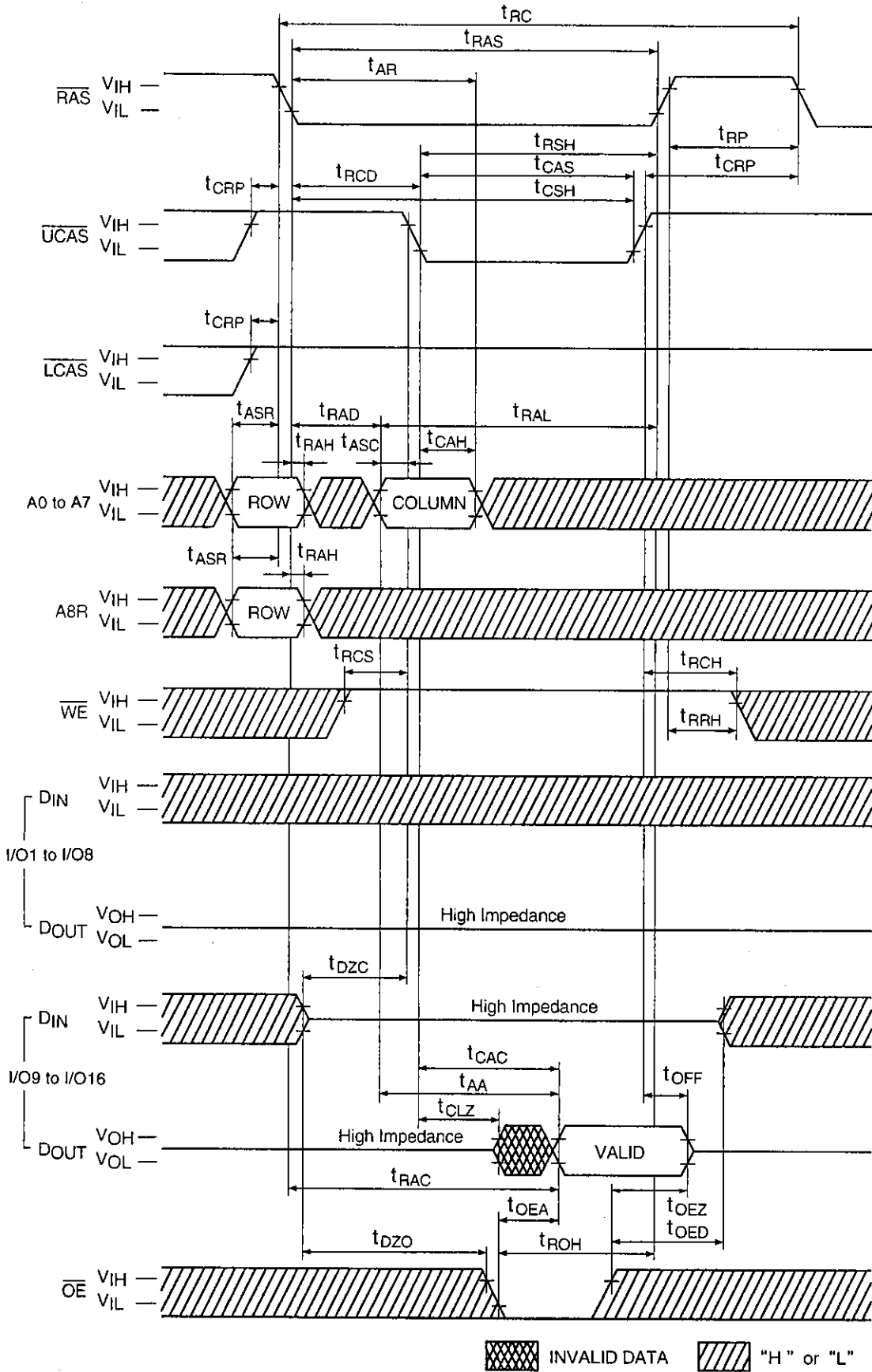
Timing Charts

Read Cycle



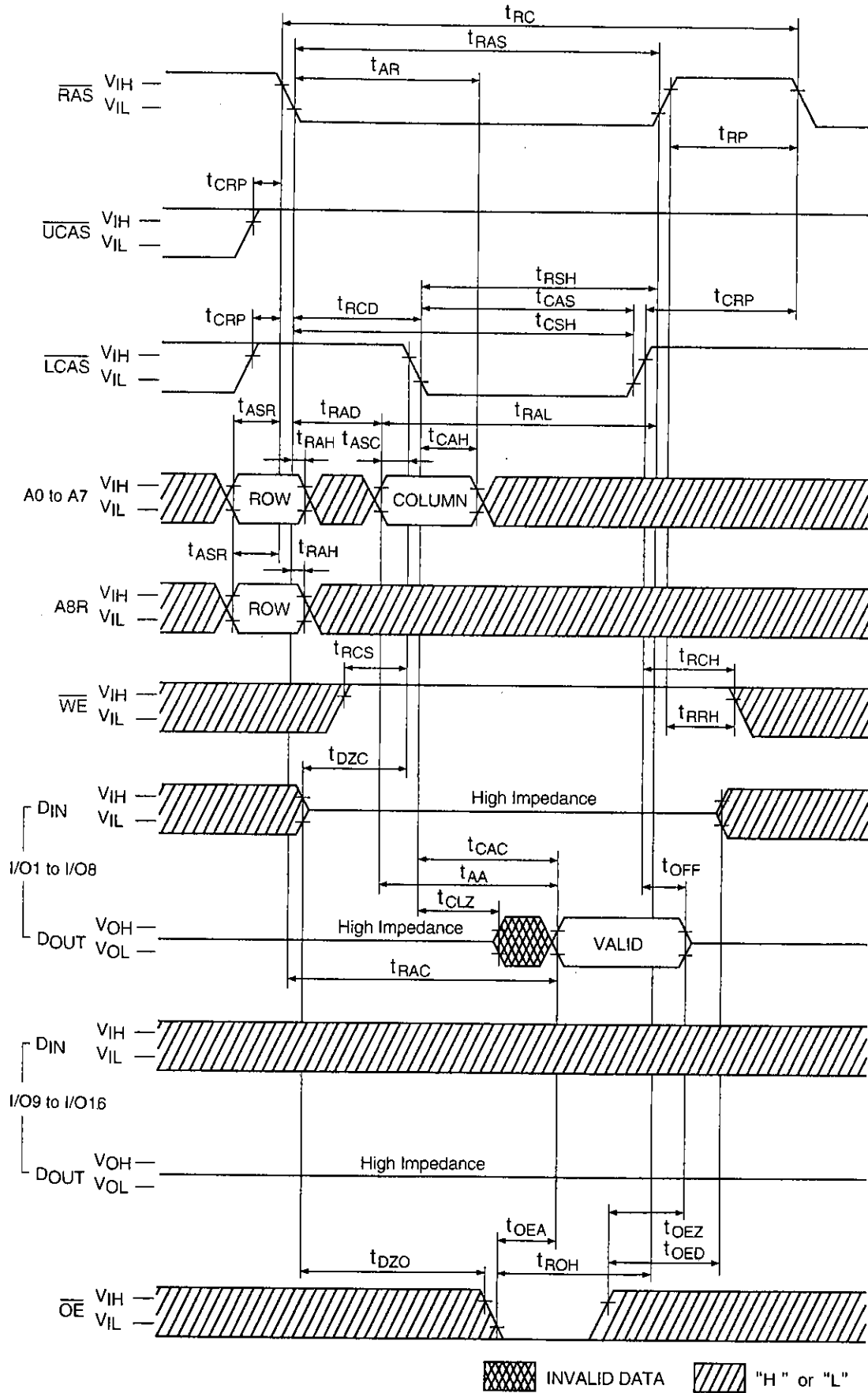
A05156

Upper Byte Read Cycle



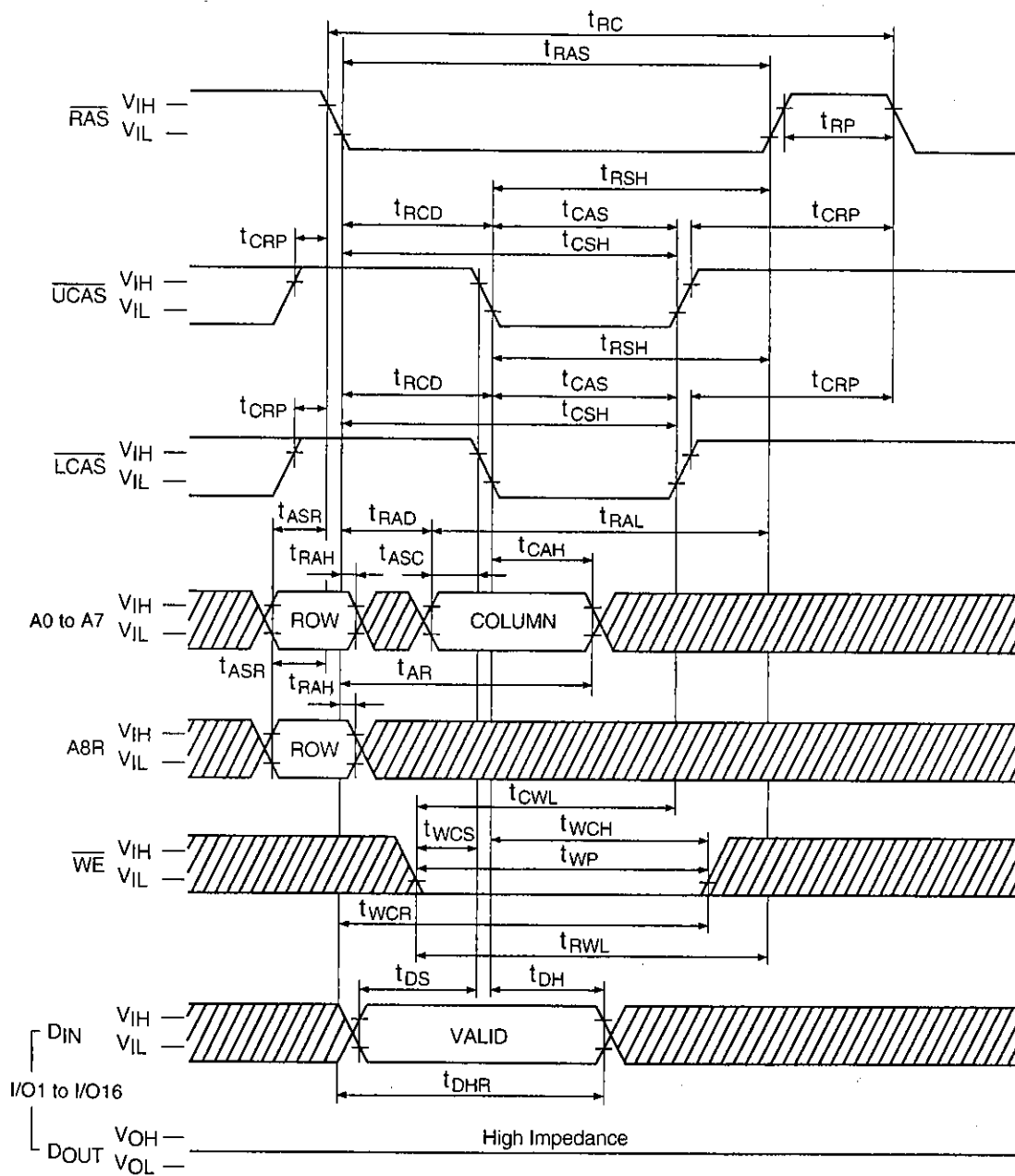
A05157

Lower Byte Read Cycle



A05158

Early Write Cycle

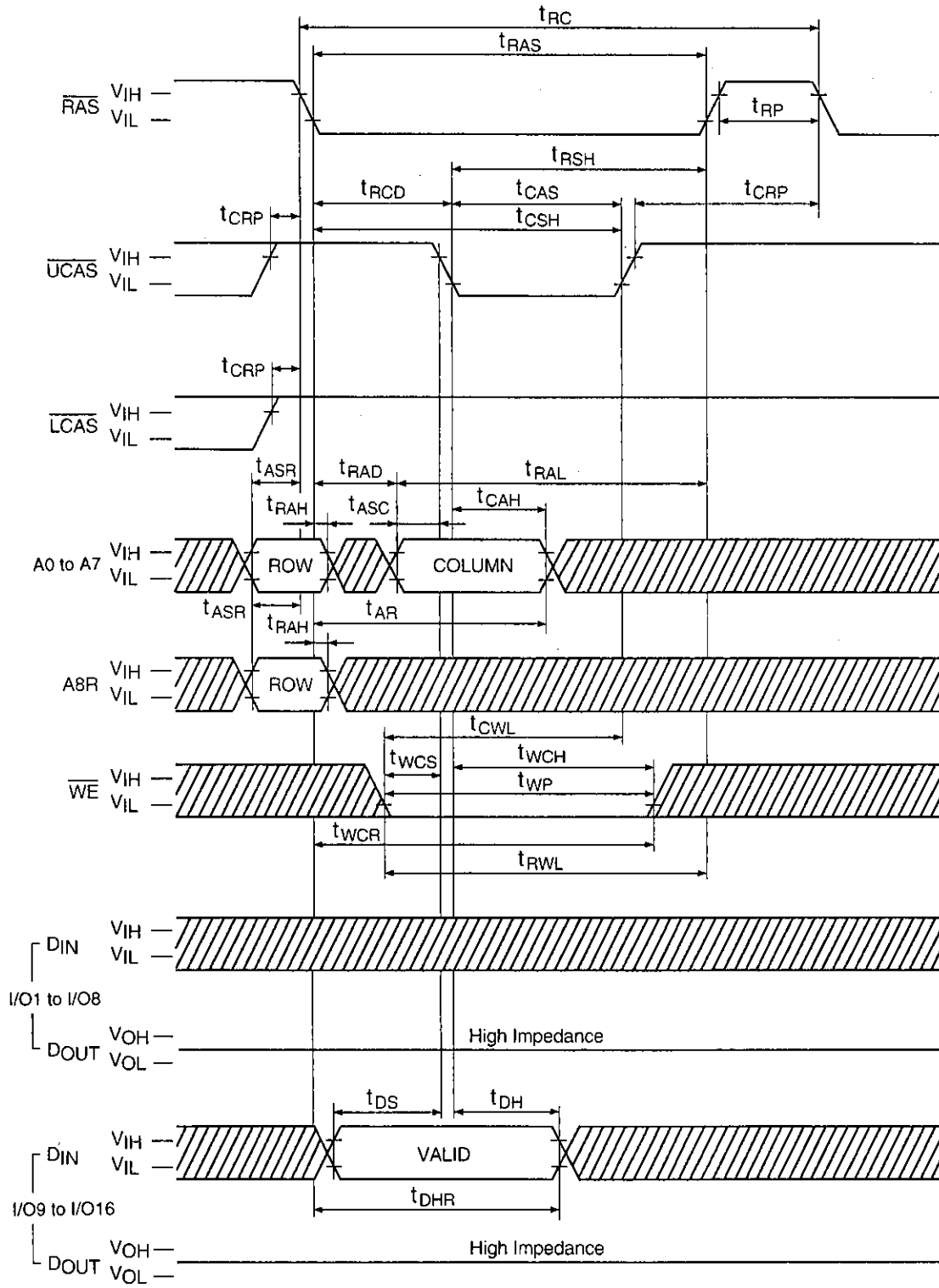



"H" or "L"

$\overline{\text{OE}}$: "H" or "L"

A05159

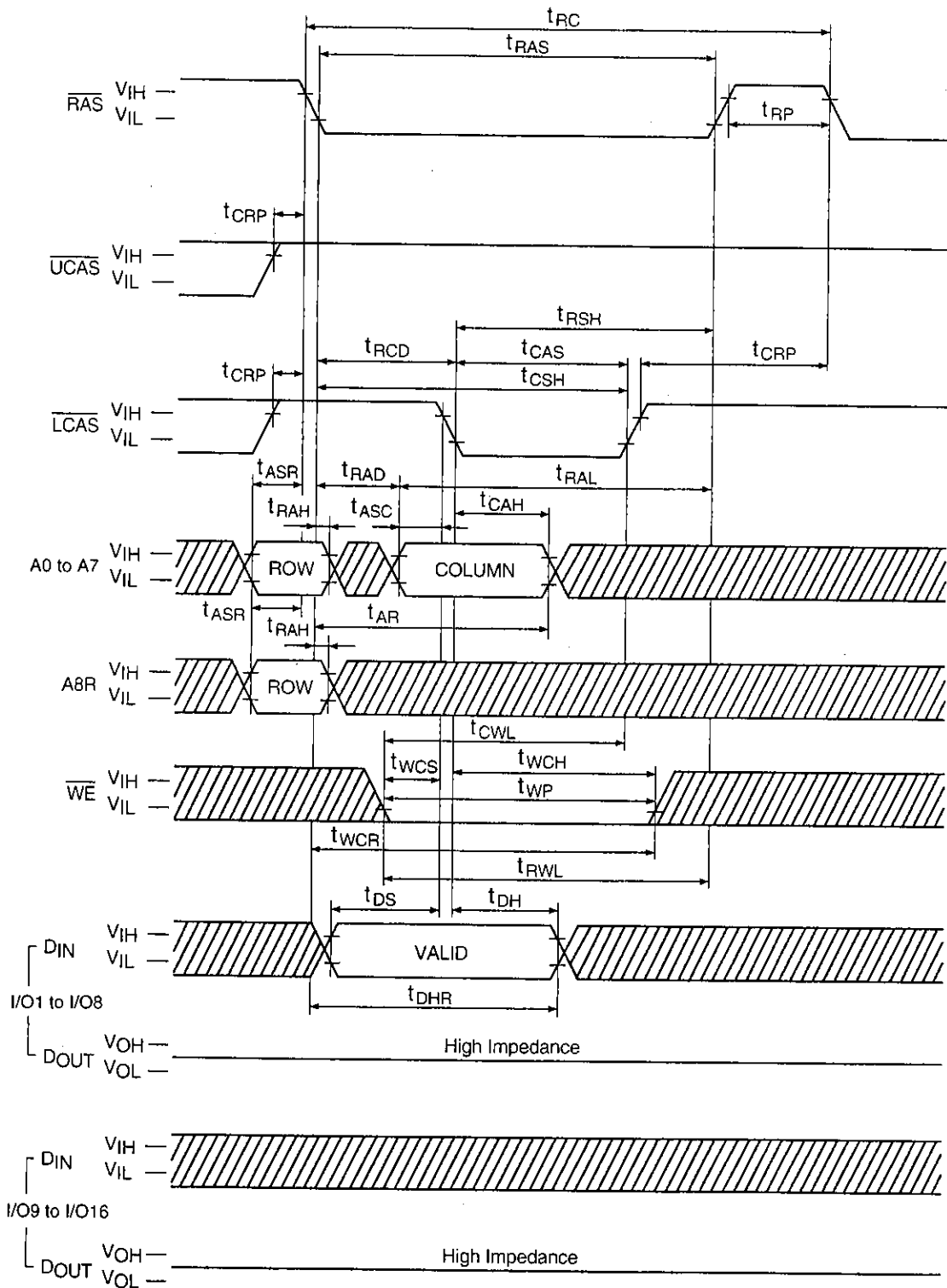
Upper Byte Early Write Cycle



 "H" or "L"
 \overline{OE} : "H" or "L"

A05160

Lower Byte Early Write Cycle

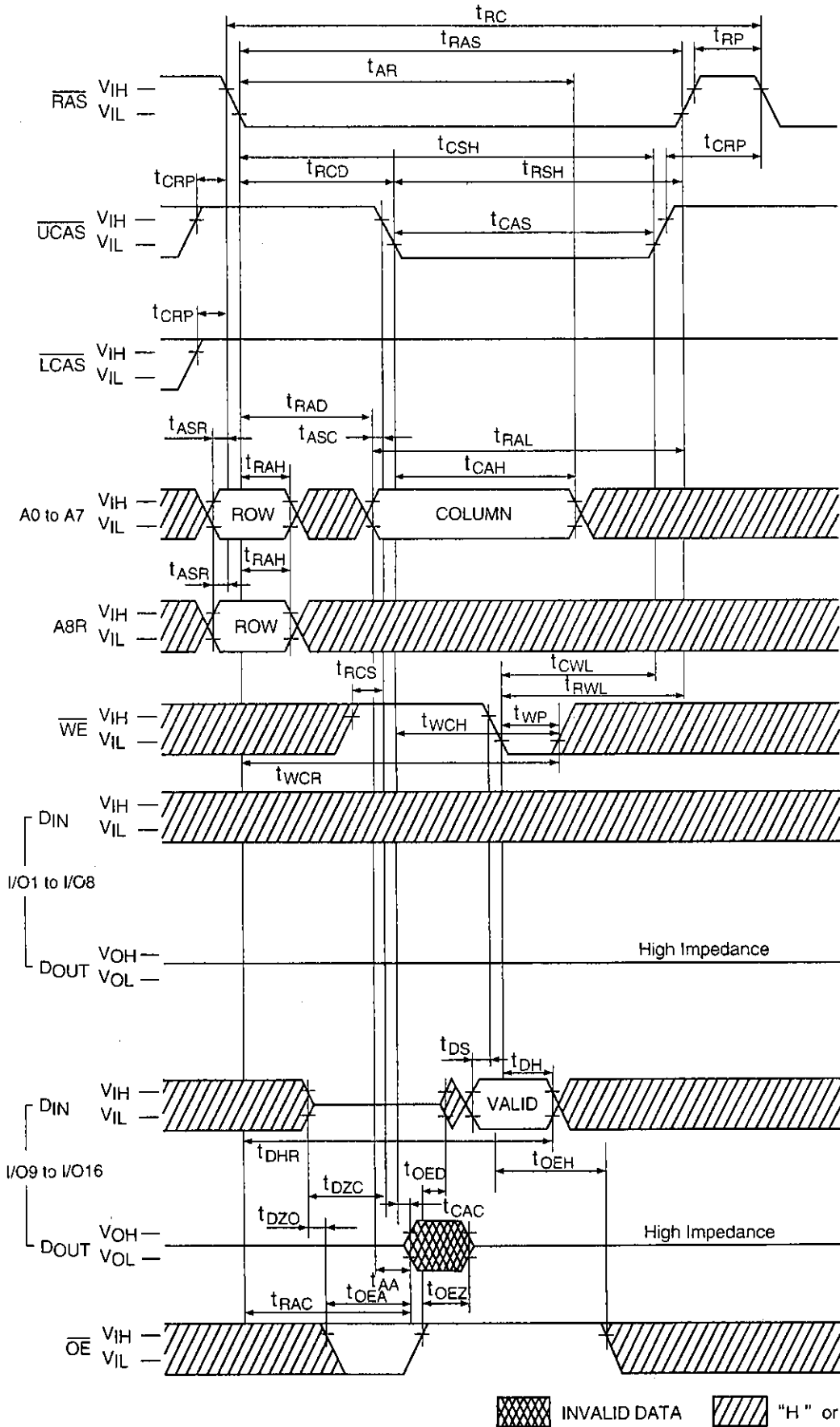


▨ "H" or "L"

\overline{OE} : "H" or "L"

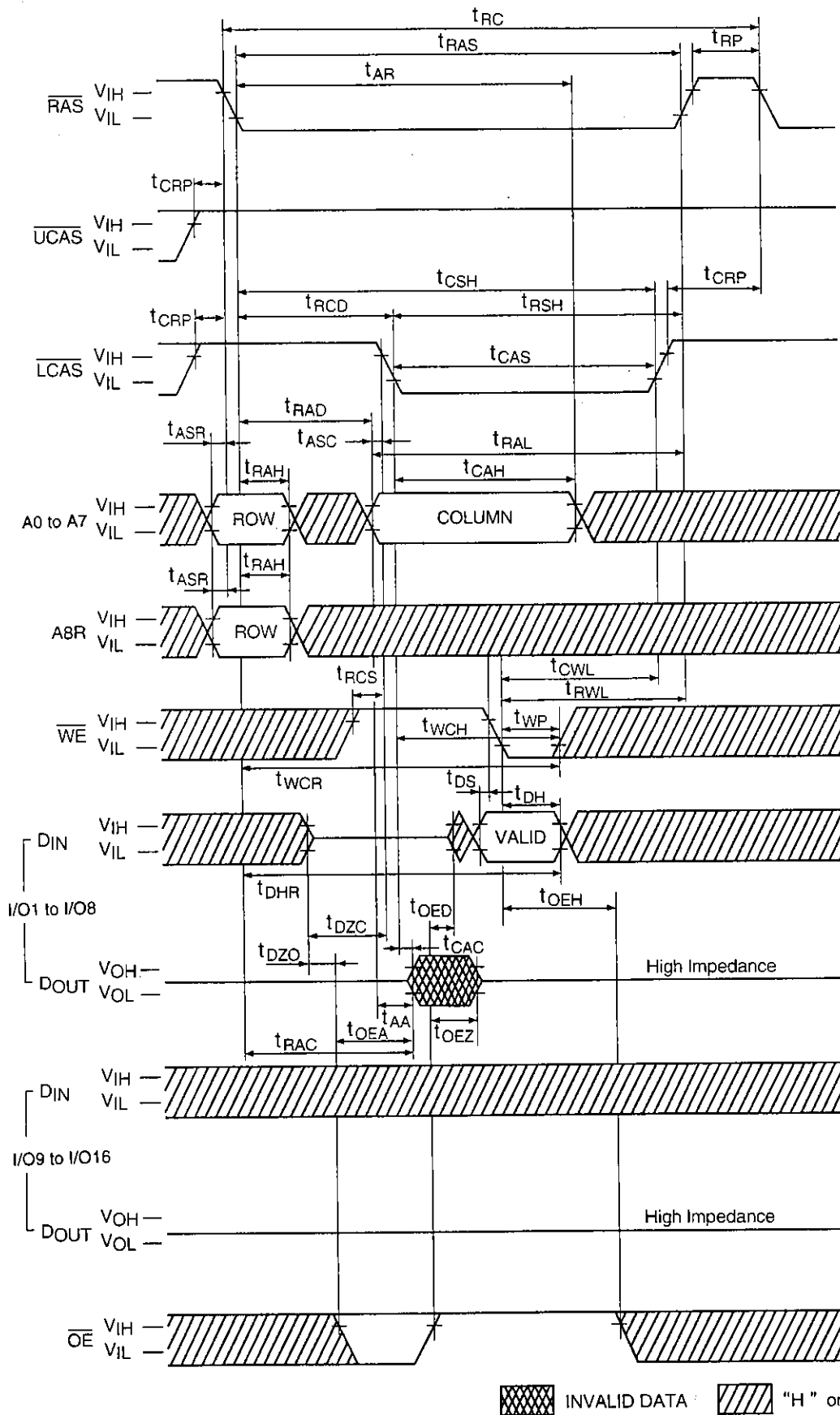
A05161

Upper Byte Write Cycle (\overline{OE} Control)

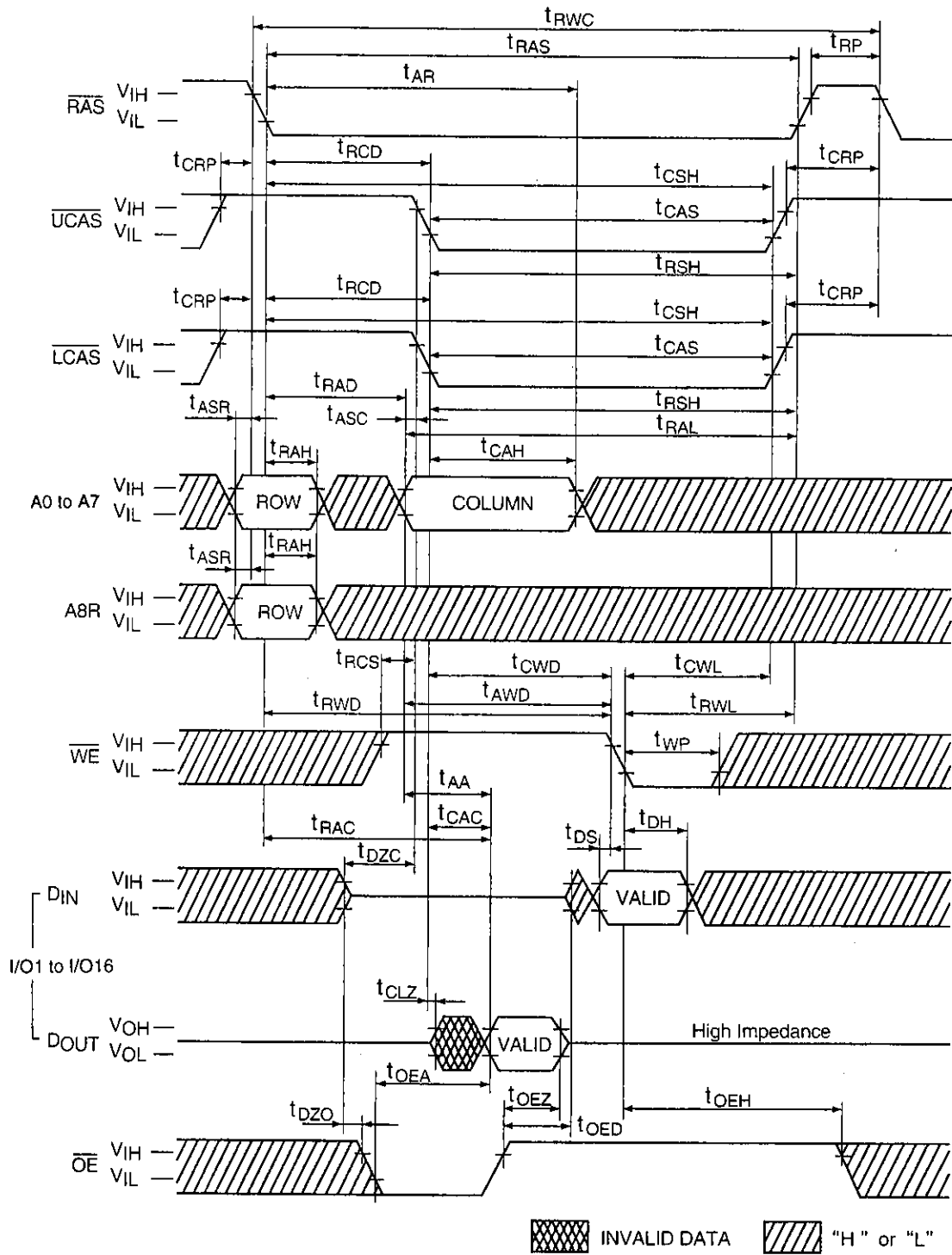


INVALID DATA "H" or "L"

Lower Byte Write Cycle (\overline{OE} Control)

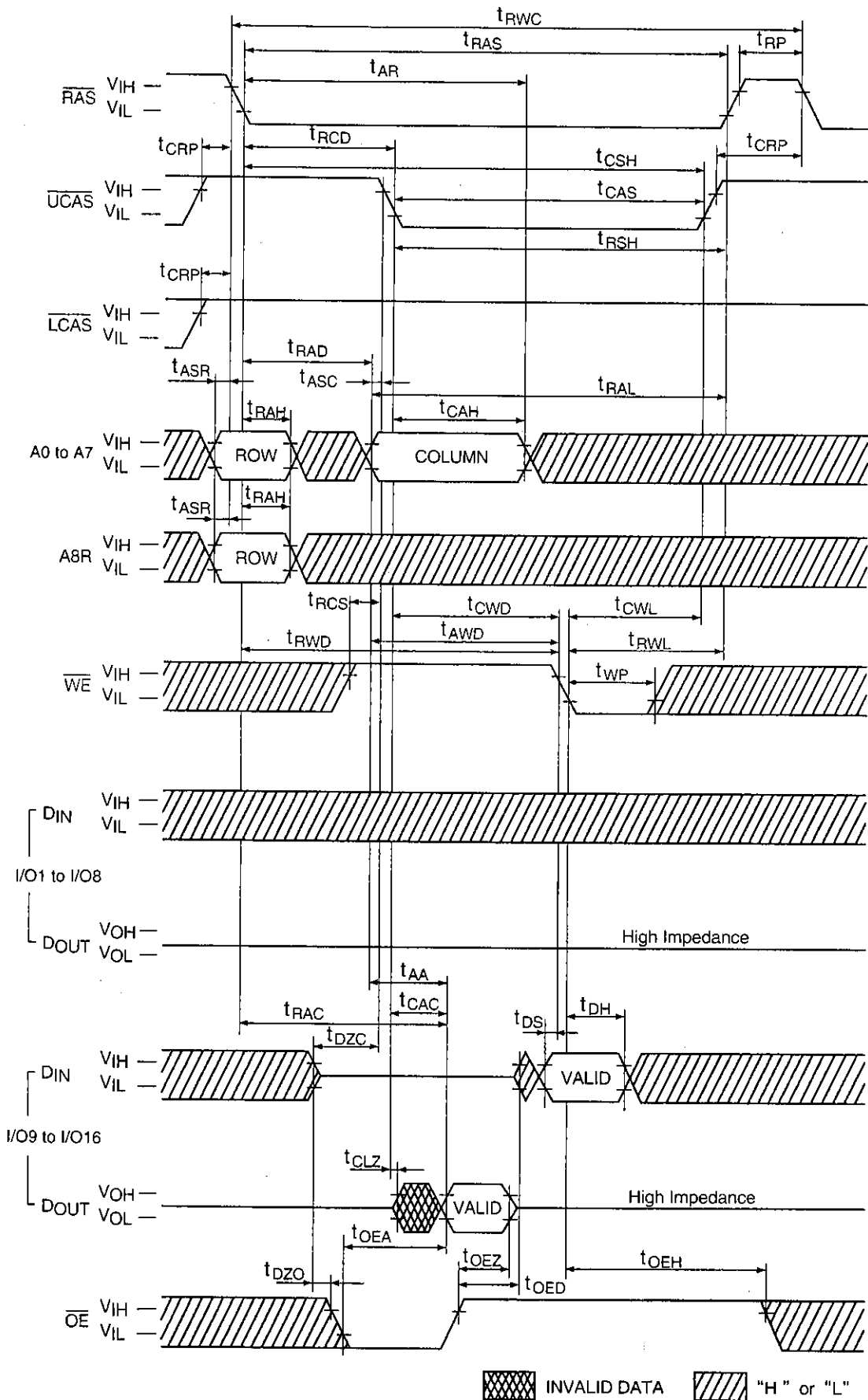


Read-Modify-Write Cycle

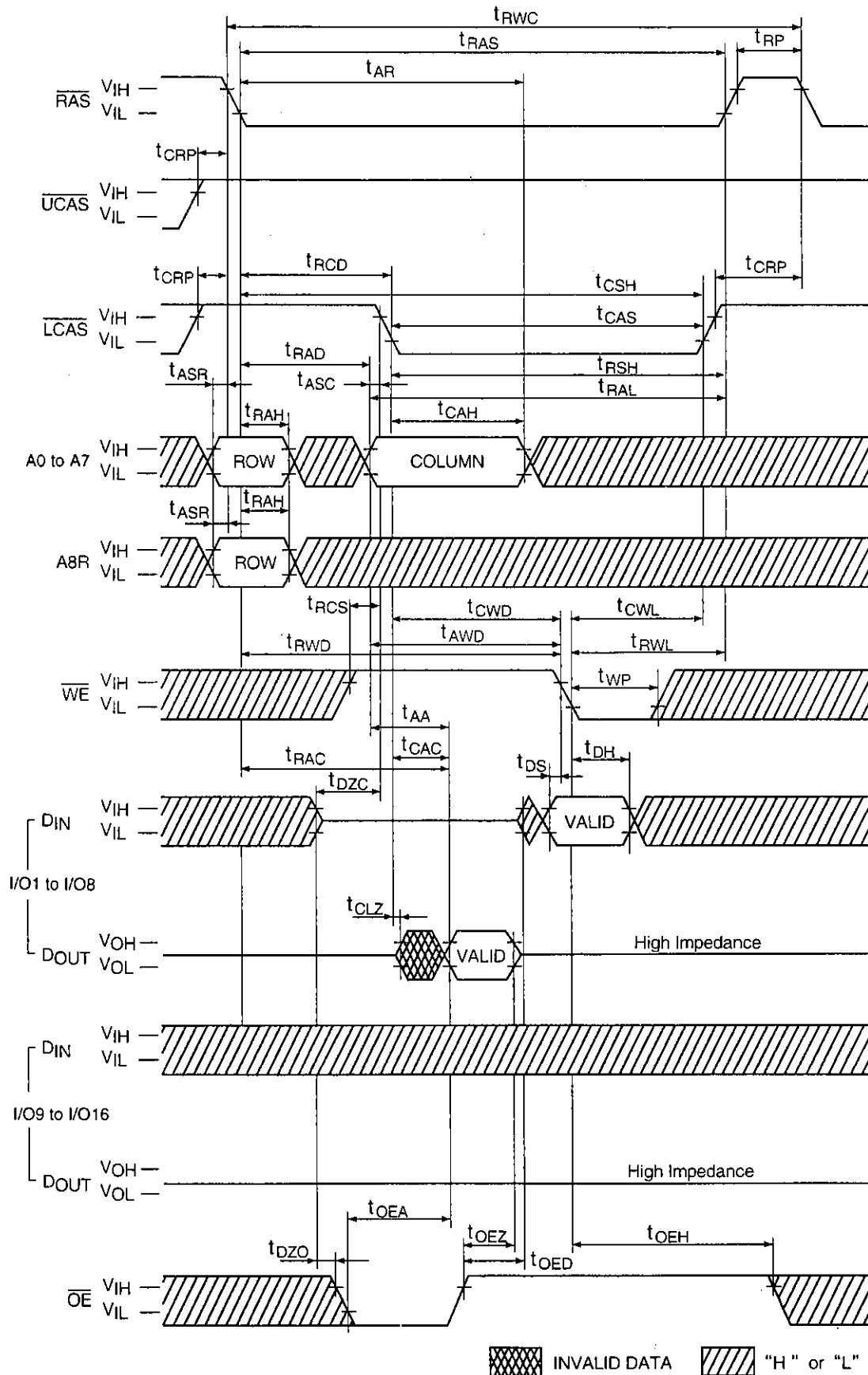


A05165

Upper Byte Read-Modify-Write Cycle

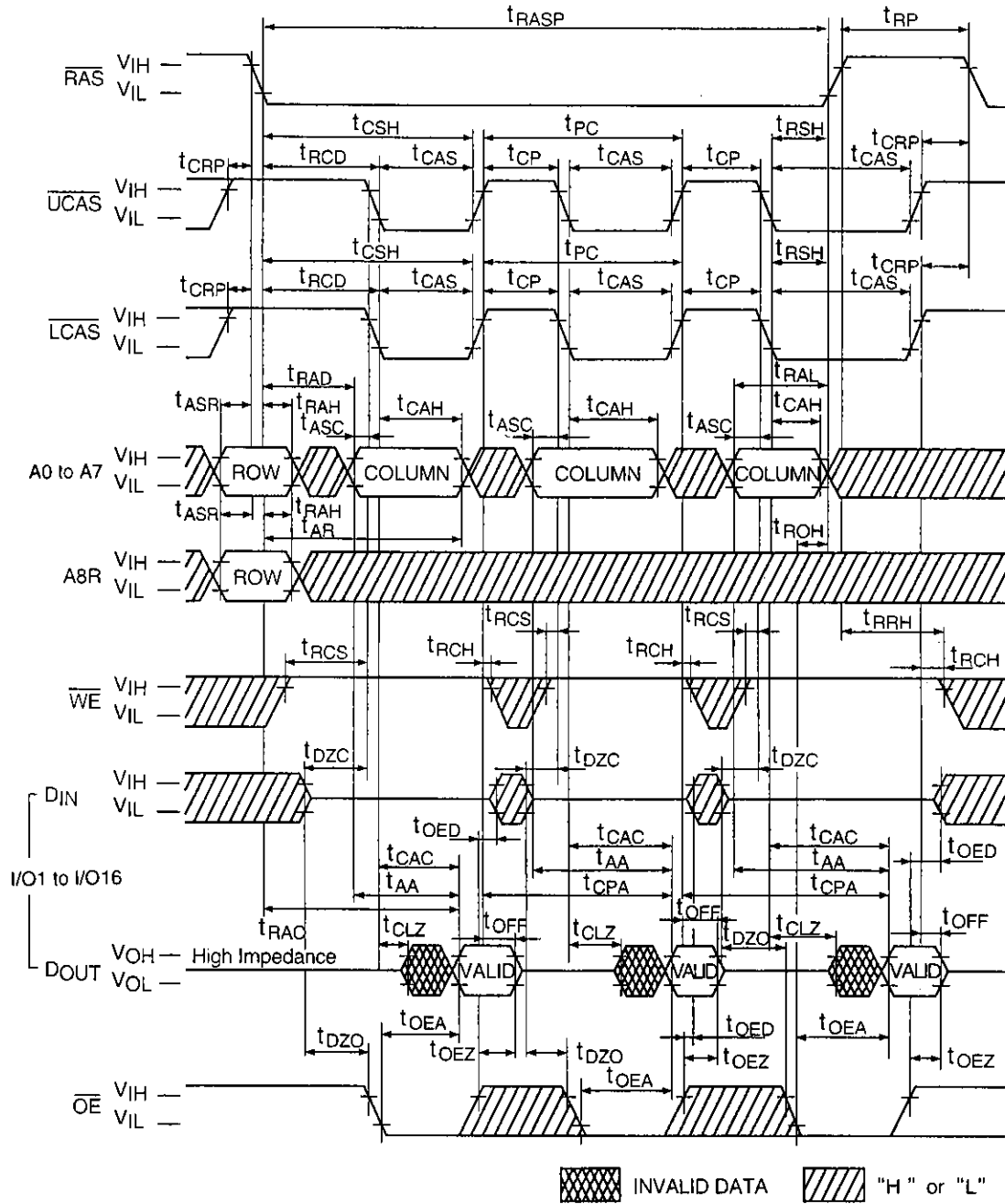


Lower Byte Read-Modify-Write Cycle



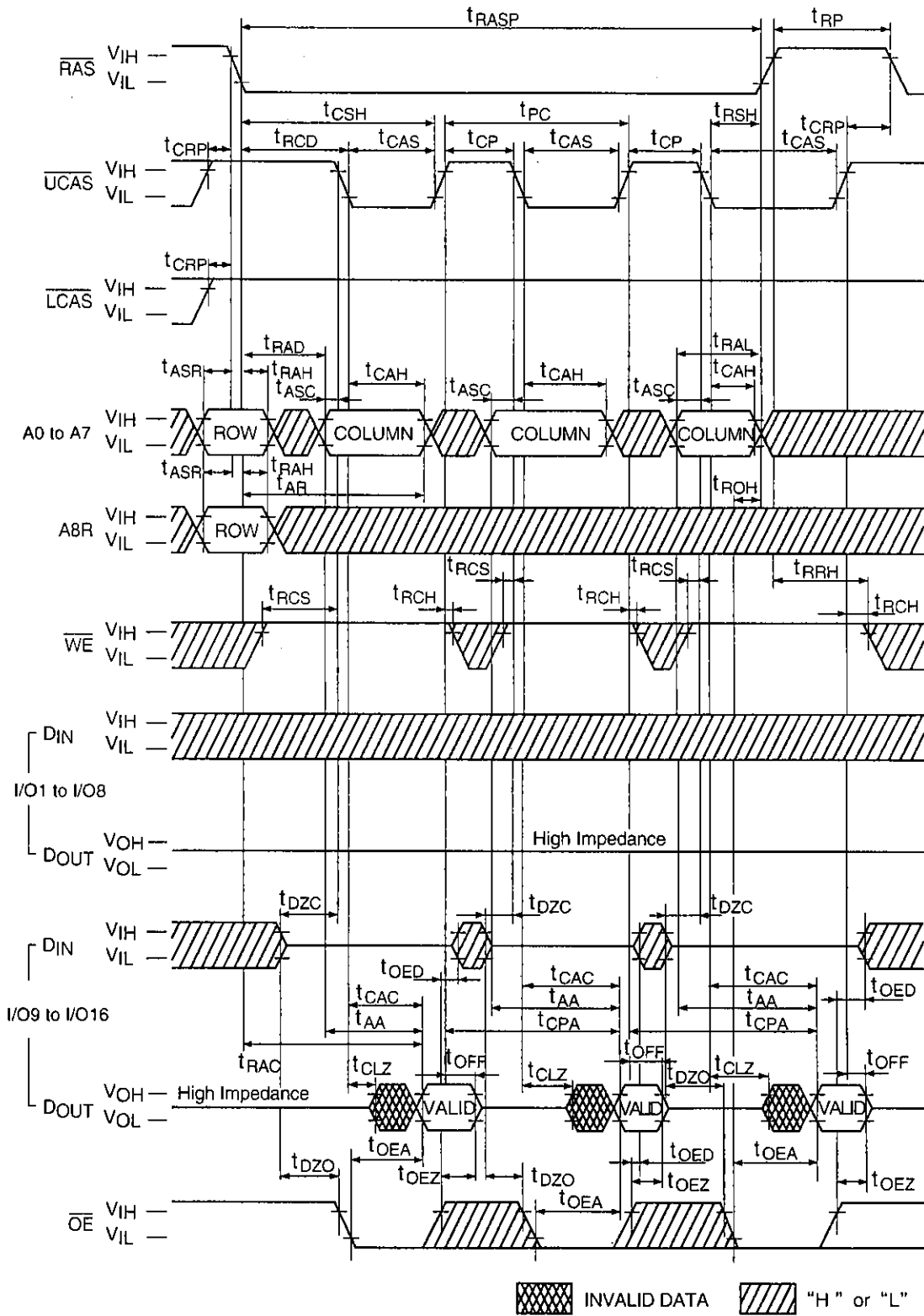
A05167

Fast Page Mode Read Cycle



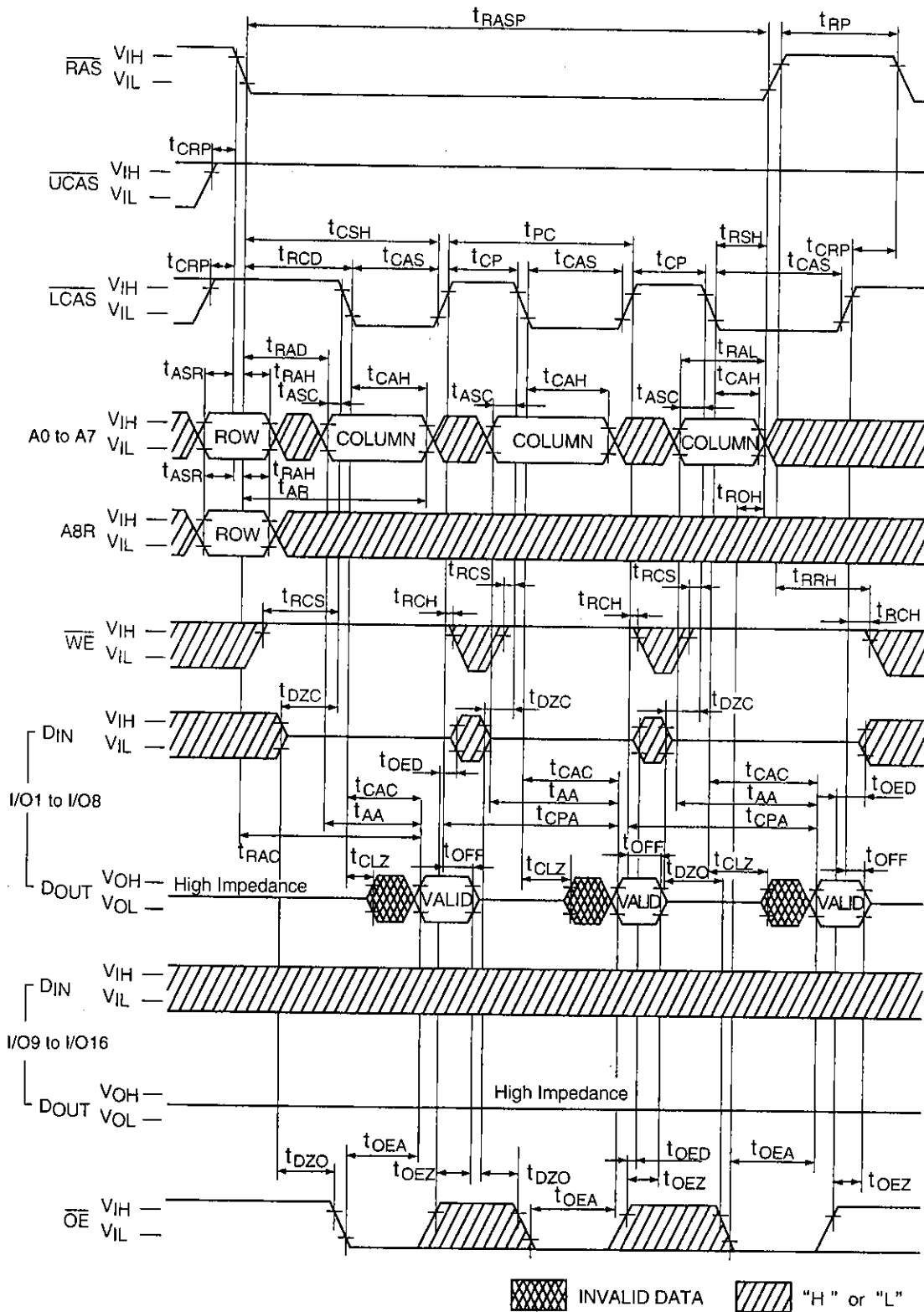
A05168

Fast Page Mode Upper Byte Read Cycle



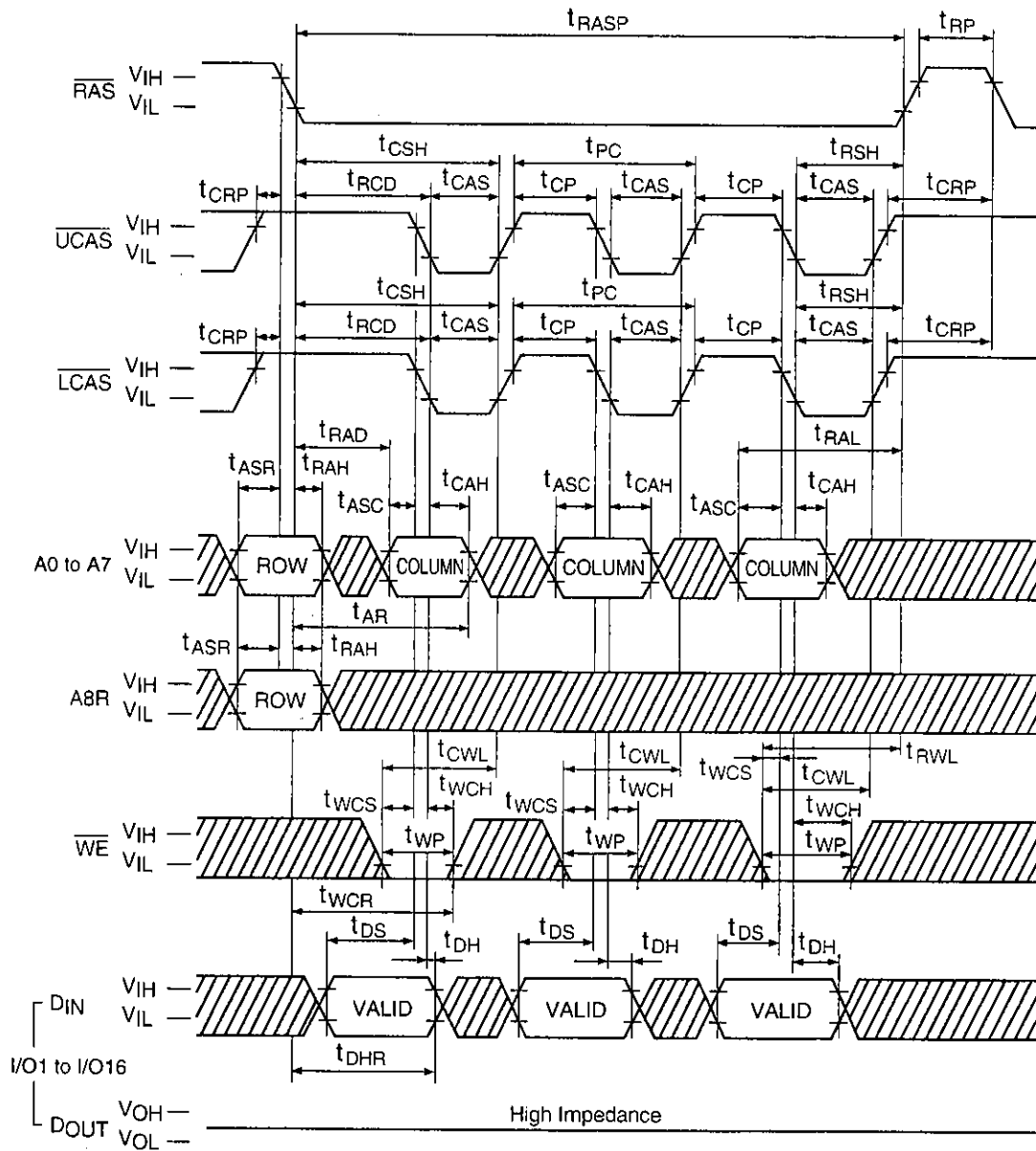
A05169

Fast Page Mode Lower Byte Read Cycle



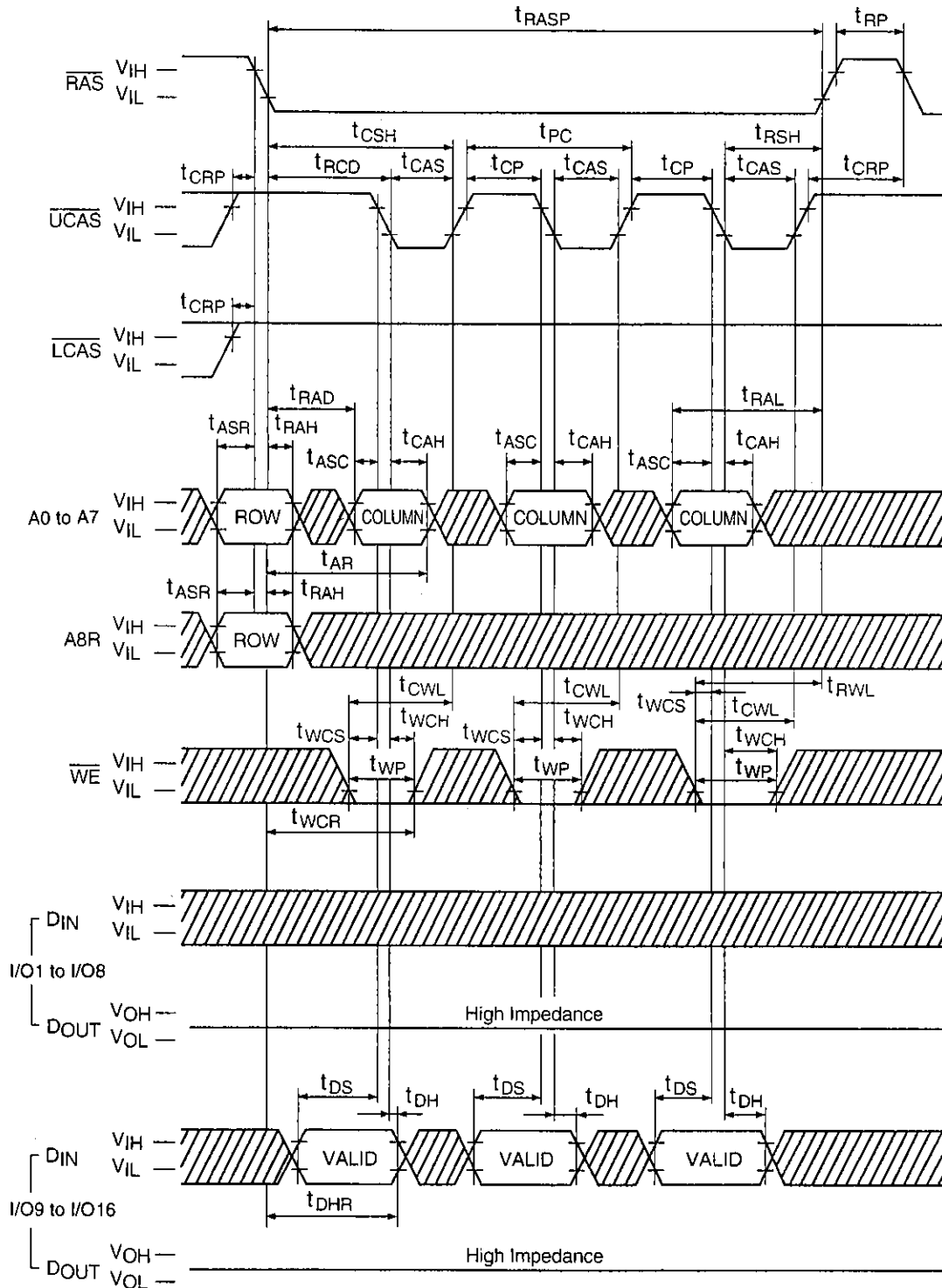
A05170

Fast Page Mode Early Write Cycle



A05171

Fast Page Mode Upper Byte Early Write Cycle

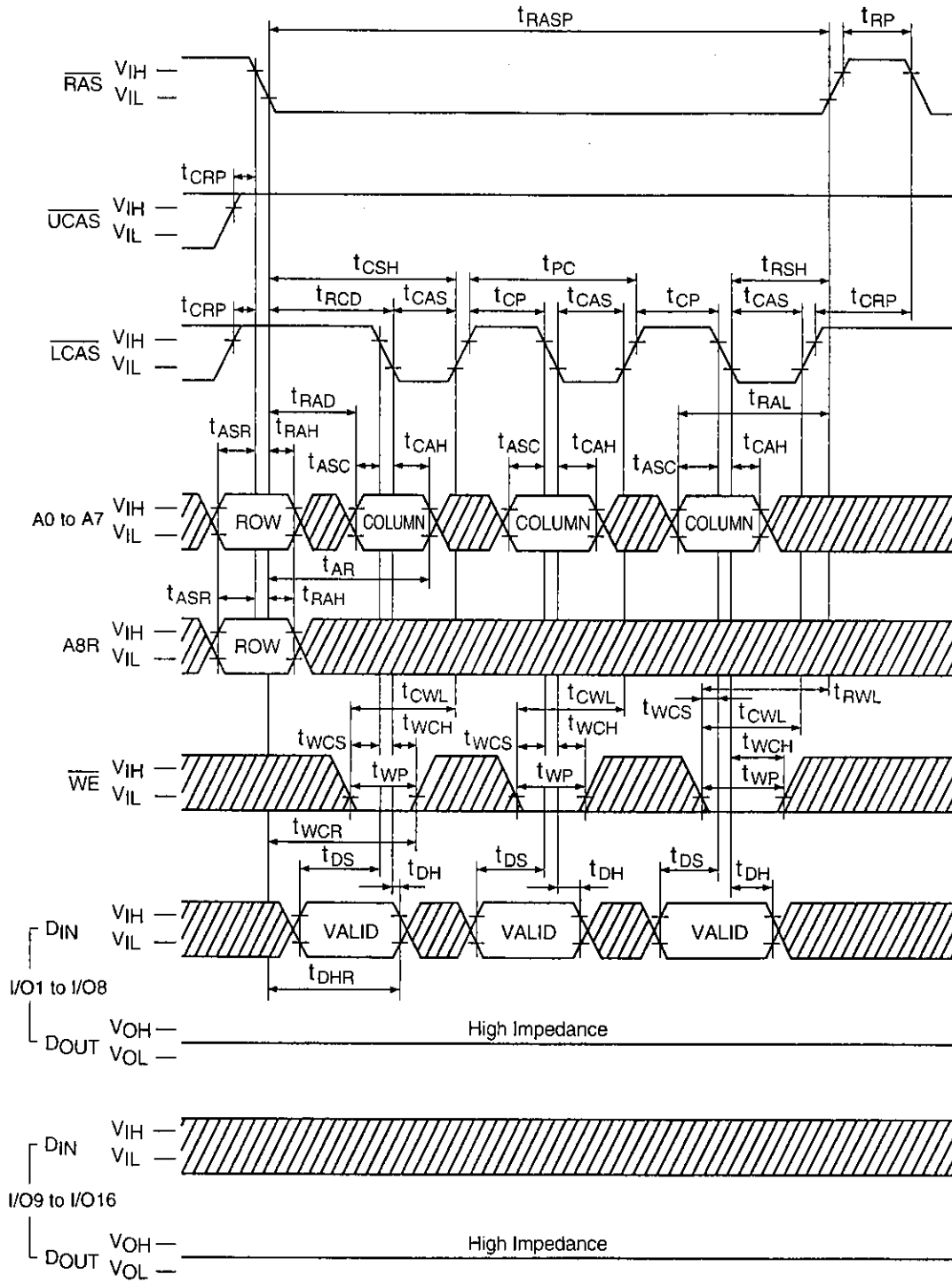


"H" or "L"

\overline{OE} : "H" or "L"

A05172

Fast Page Mode Lower Byte Early Write Cycle

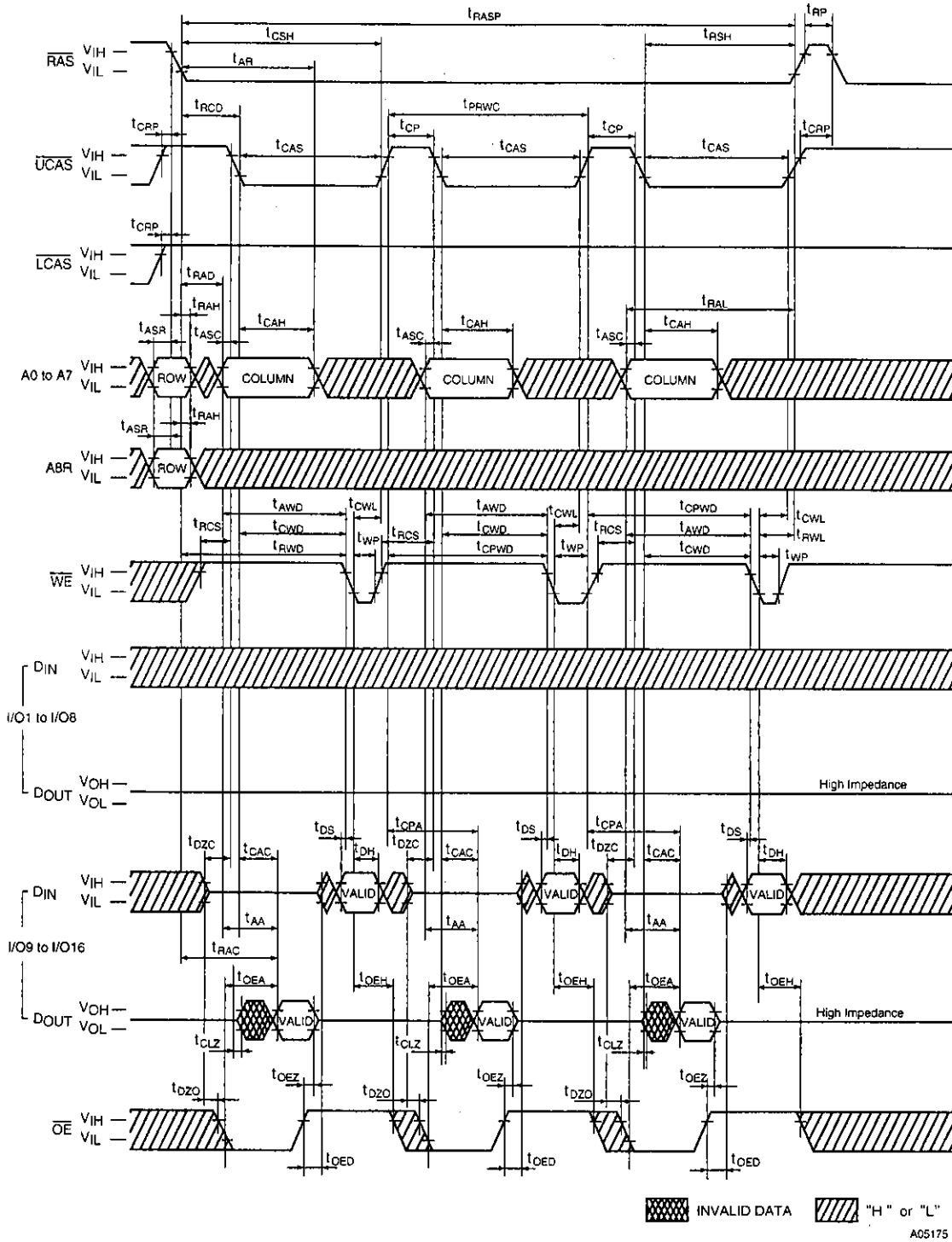


"H" or "L"

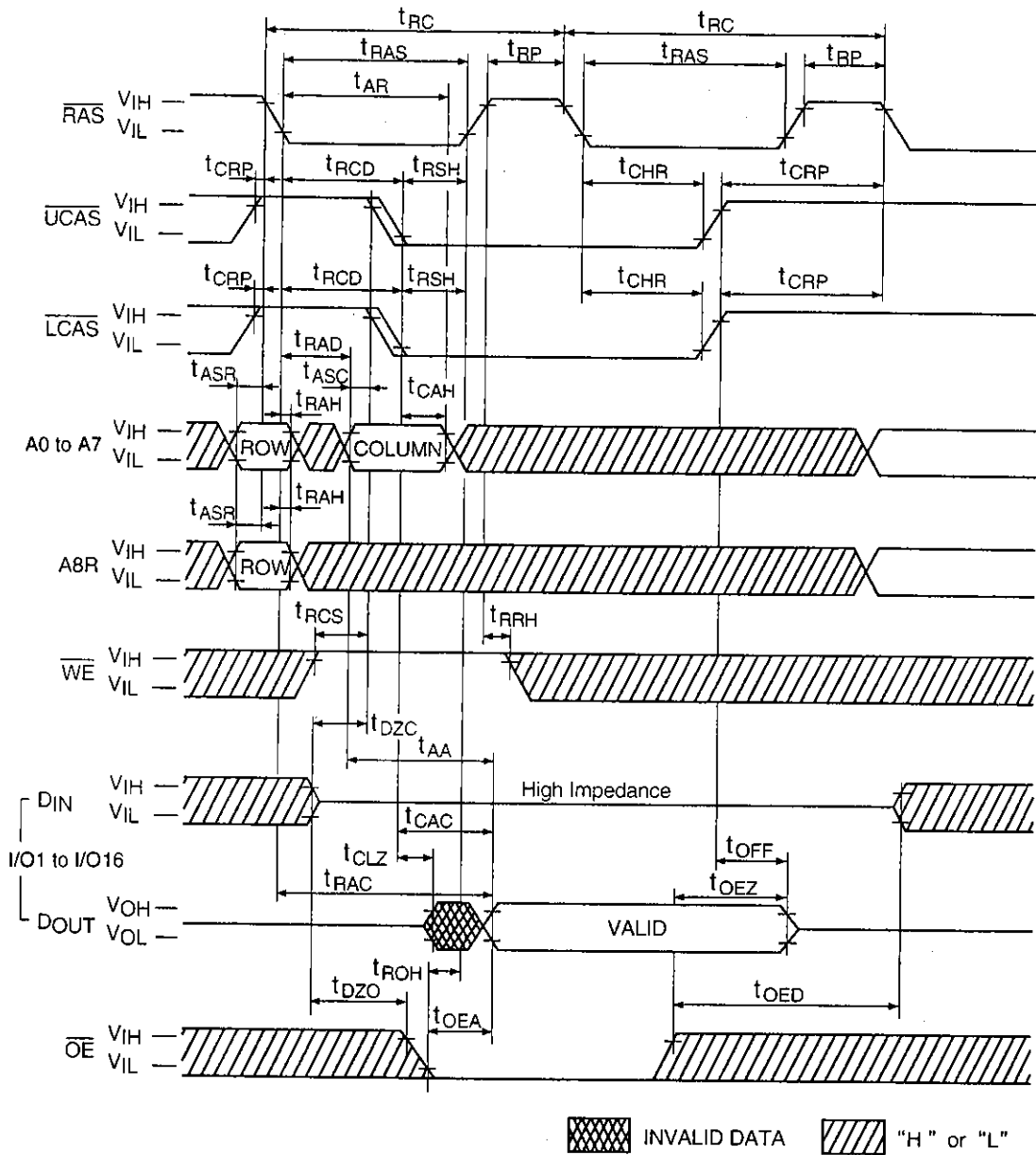
\overline{OE} : "H" or "L"

A05173

Fast Page Mode Upper Byte Read-Modify-Write Cycle

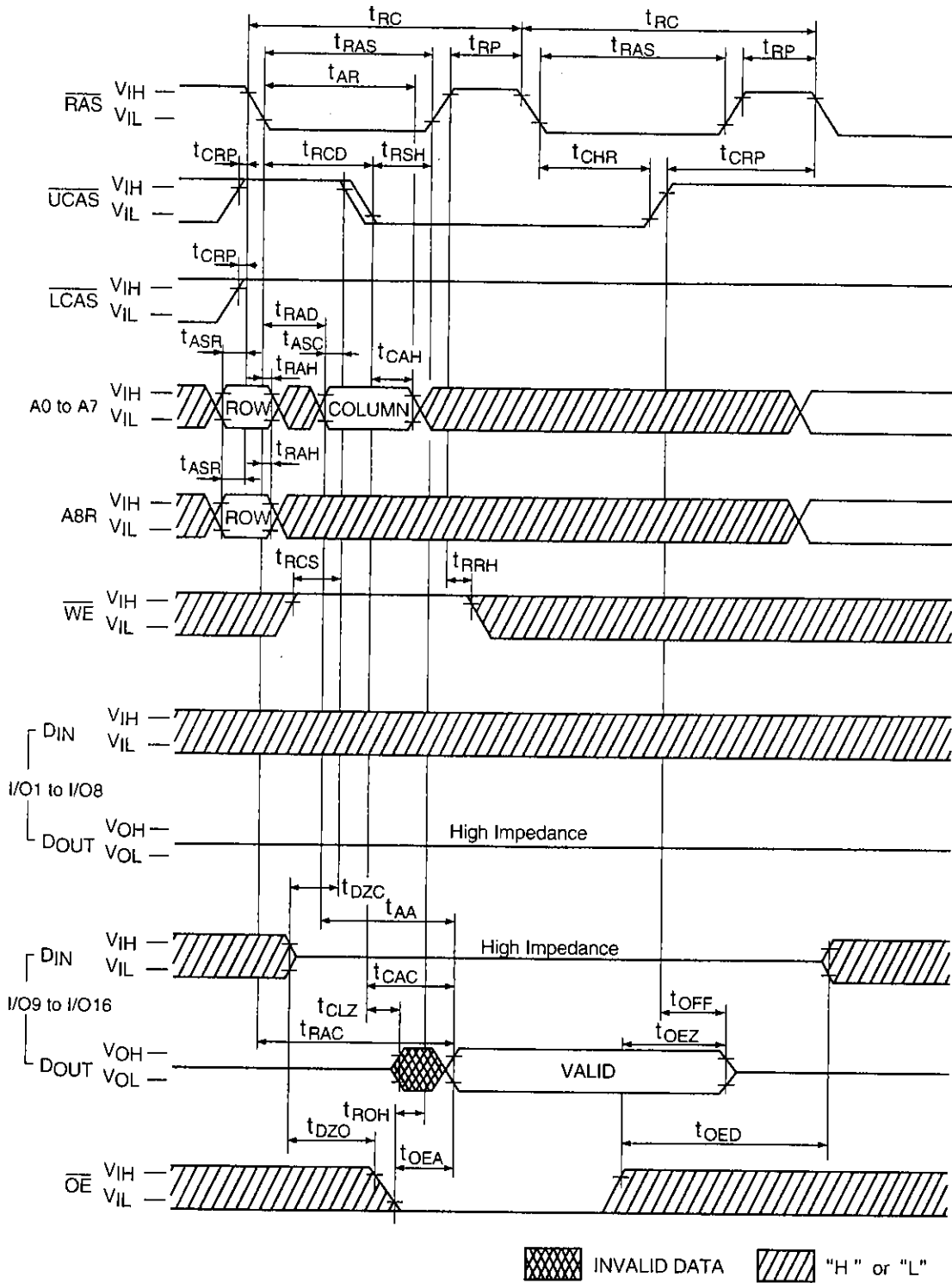


Hidden Refresh Cycle



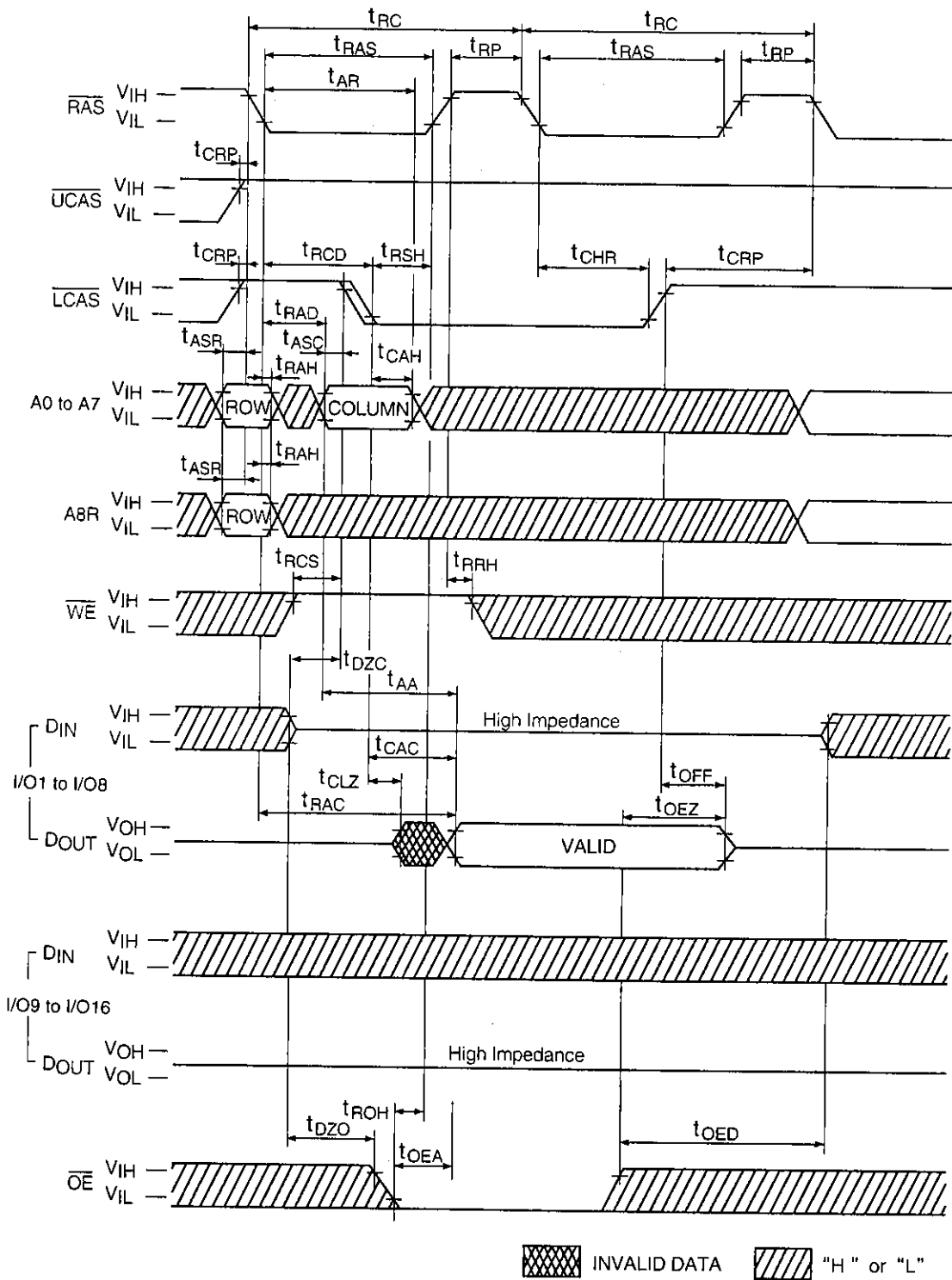
A05177

Upper Byte Hidden Refresh Cycle



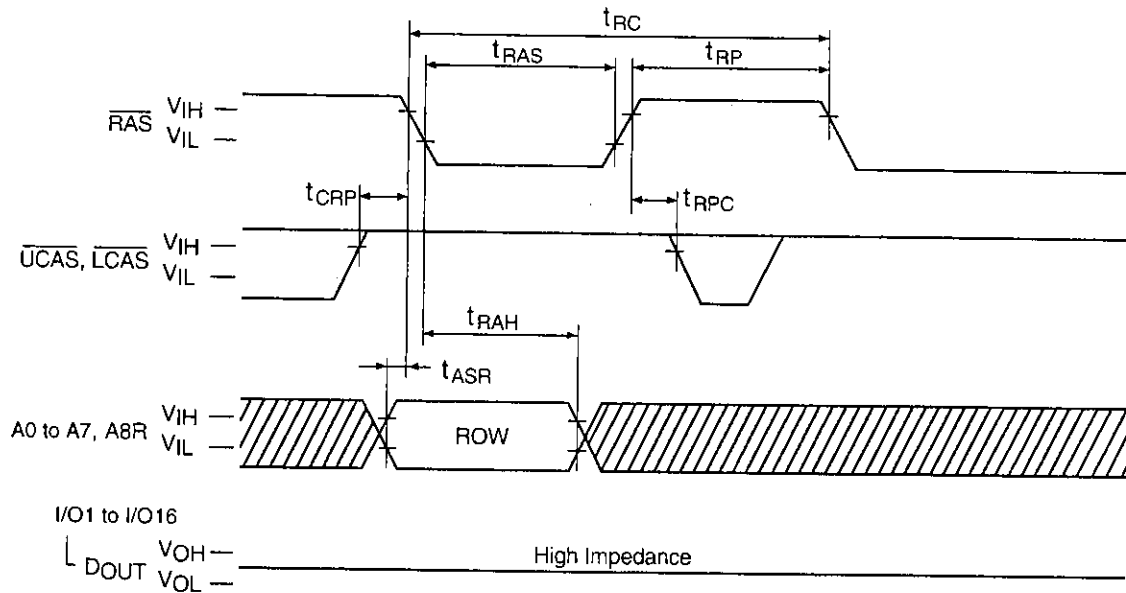
A05178

Lower Byte Hidden Refresh Cycle




A05179

RAS-Only Refresh Cycle

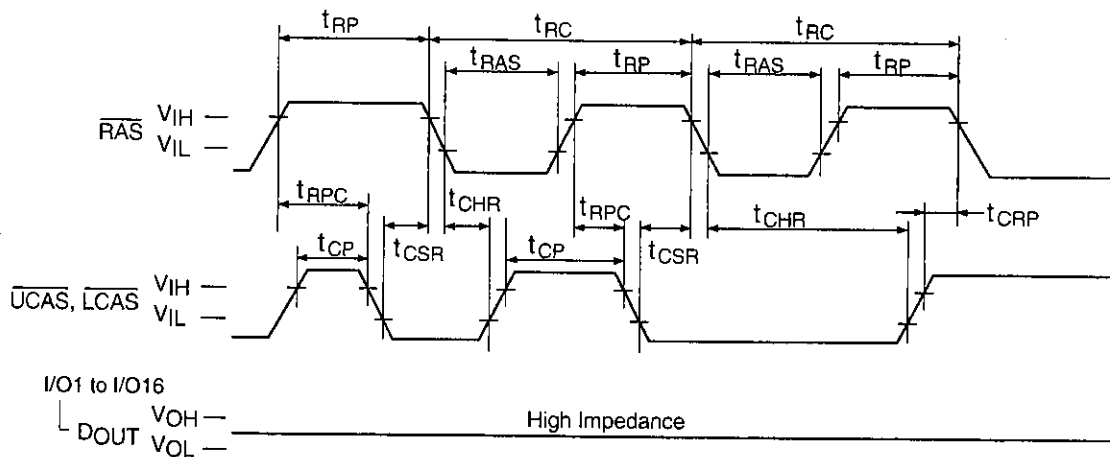


$\overline{OE}, \overline{WE}, D_{IN}$: "H" or "L"

 "H" or "L"

A05180

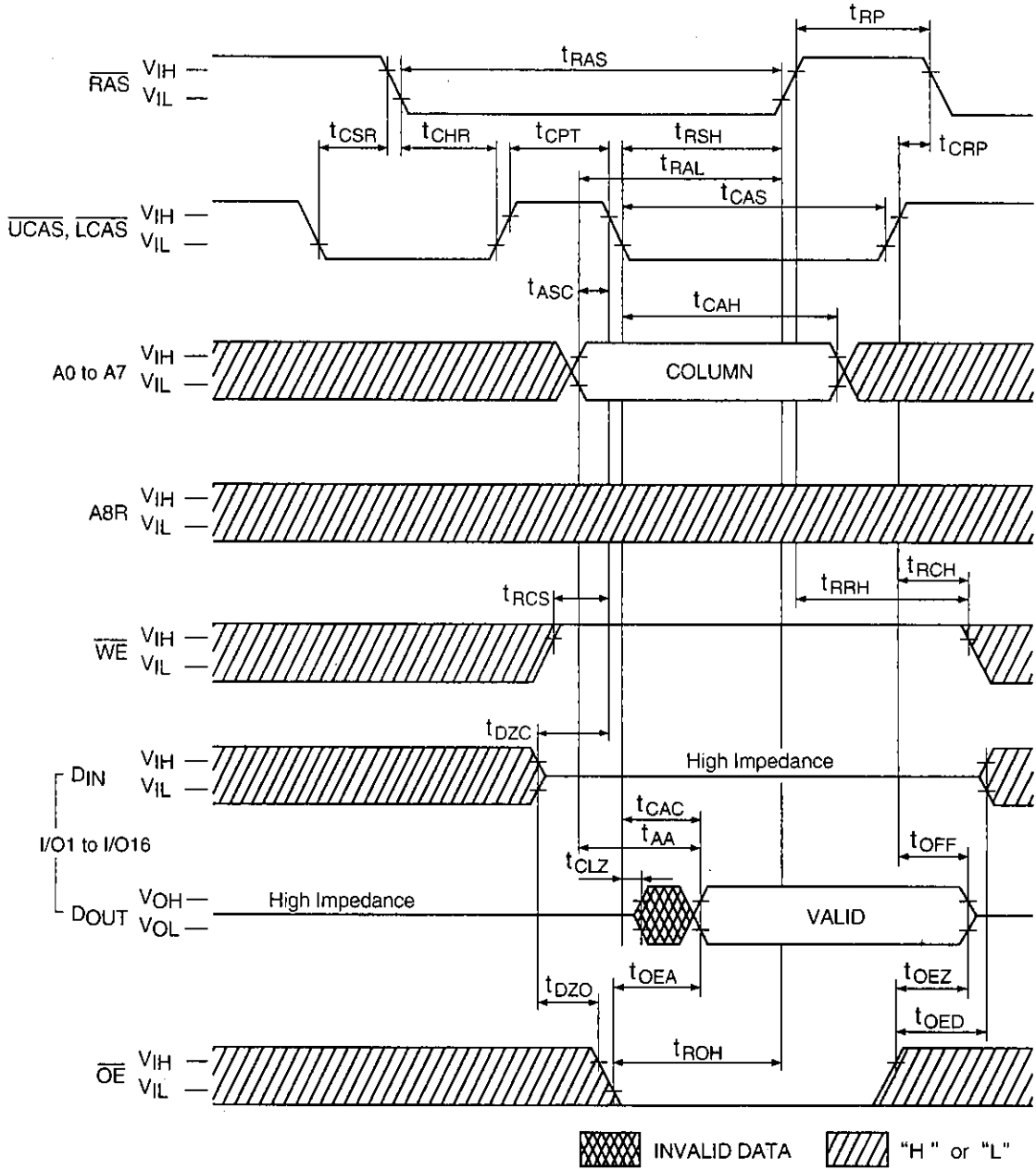
CAS-before-RAS Refresh Cycle



$A0$ to $A7$, $A8R$, \overline{WE} , \overline{OE} , D_{IN} : "H" or "L"

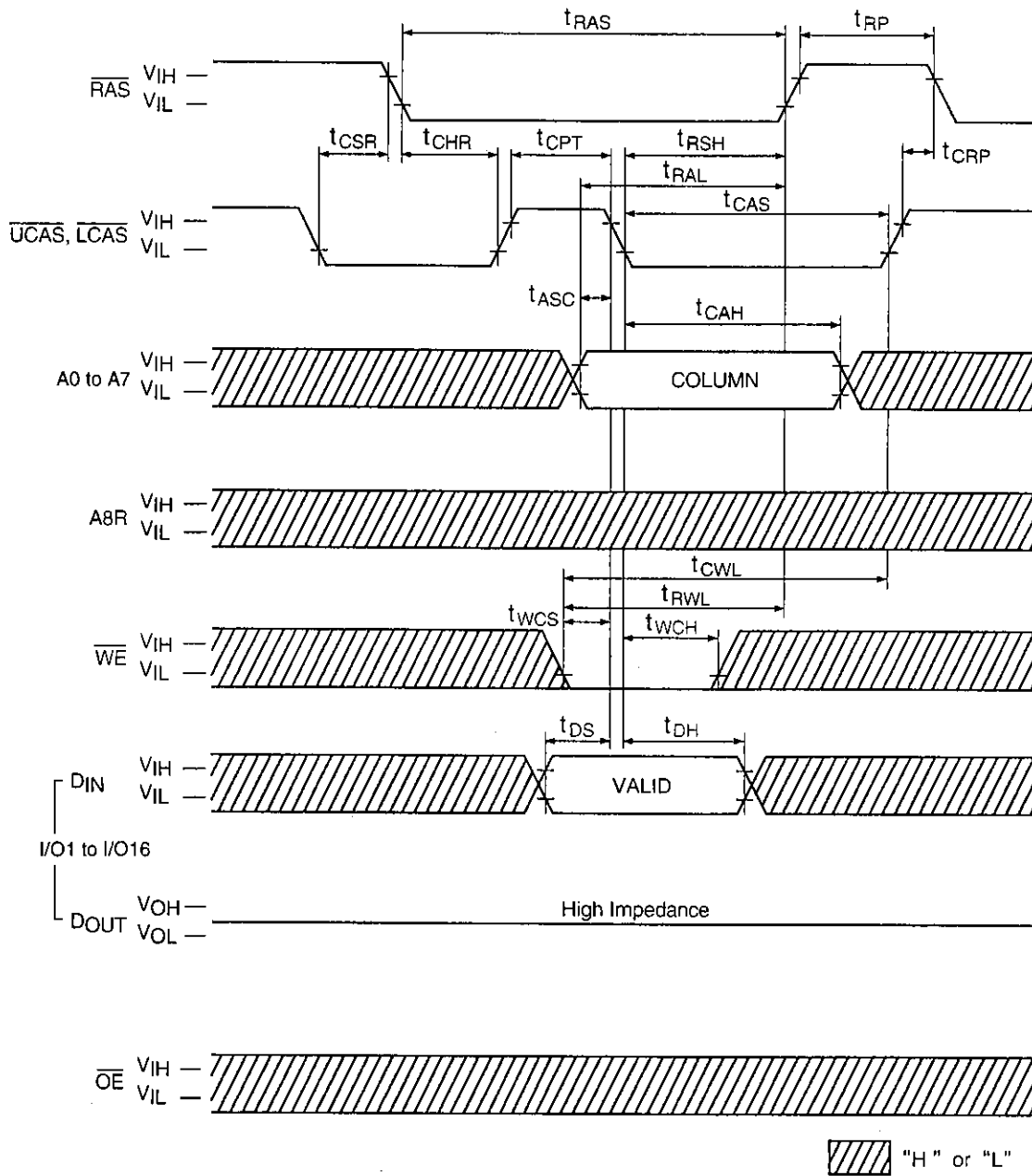
A05181

CAS-before-RAS Refresh Counter Test Cycle (Read)



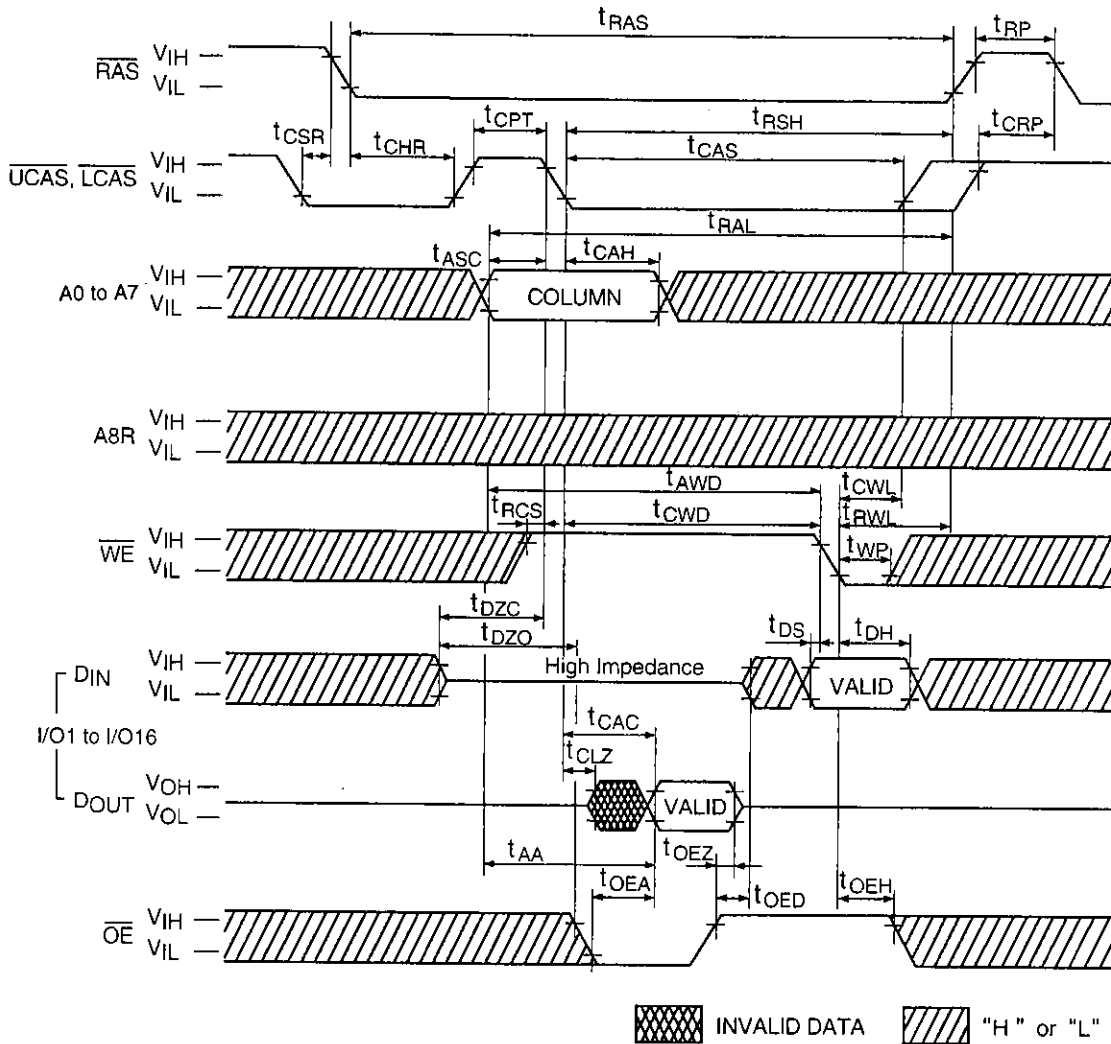
A05182

CAS-before-RAS Refresh Counter Test Cycle (Write)



A05183

CAS-before-RAS Refresh Counter Test Cycle (Read-Modify-Write)



A05184

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