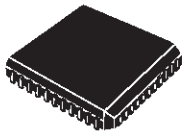
STLC3040

SUBSCRIBER LINE INTERFACE CODEC FILTER, COFISLIC

PRELIMINARY DATA

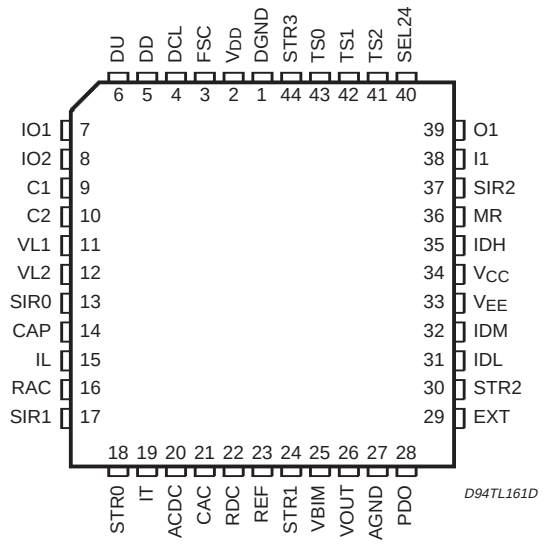
- Single chip CODEC and FILTER including all LOW-VOLTAGE SLIC functions.
- Advanced 12V BJT, 5V CMOS 0.8um technology.
- Low external component count.
- Over-sampling A/D and D/A conversion.
- No functional trimming or adjustments required.
- Serves a wide range of specifications; i.e. ITU-T, LSSGR.
- A-law, and μ-law PCM and Linear voice coding, sw selectable
- GCI compatible interface.
- Programmable Digital-Filters for impedance-matching, hybrid-balance, frequency-response and gain.
- Programmable Feeding-Resistance (2 x 50Ω to 2 x 400Ω) and current-limiting (0-69.3mA).
- Programmable voltage-drop according to transmission needs.
- 12kHz/16kHz Teletax Generation with Programmable Level 0-10 Vrms in 40mV steps including shaping and filtering.
- Integrated Ring-Generator with Zero-Crossing. Programmable frequency from 16.6Hz to 60Hz, programmable level up to 85Vrms, Integrated auto ring-trip.
- Signalling functions ON/OFF - Hook, Gnd-key with filter and Programmable persistence check.
- Advanced test capabilities:
  On-board line tests and circuit tests.
  Signalling tests for meterpulse TTX and Ringing.
- Tone generator for circuit test.
- 3 Loop-back paths.
- Three operating conditions:
  Power Down, Active, Ringing. Off-hook programmable threshold-level in each of these conditions.
- Interface to High-Voltage SLIC to select modes, provide hard or soft Polarity-Reversal and sense HV (L3000N, L3000S, STLC3170) High Thermal condition.
- On-hook transmission capability.
- Selectable 2/4MHz backplane clock.
- Standard PLCC 44 package.



PLCC44

ORDERING NUMBERS: STLC3040
STLC3040-TR

Figure 1: Pin Connection (Top view)



- On chip Line-card identification.

DESCRIPTION

The subscriber line codec-filter, STLC3040, is fabricated in BiCMOS (12V bipolar / 5V CMOS) technology. It uses Digital-Signal-Processing(DSP) to implement central-office telephone interface features: DC-feed, Supervision, PCM-Codec-Filter, Ring, Teletax metering (TTX) and Test functions. The STLC3040 is fully programmable and needs few external resistors and capacitors.

The STLC3040 interfaces the subscriber's line via the High-Voltage (HV) (L3000N, L3000S, STLC3170) device and the central-office back-

DESCRIPTION (continued)

plane via a GCI compatible interface (see fig.2). The GCI handles all STLC3040 control and voice channel.

The STLC3040 processes the transversal line-current sensed by the ST HV (L3000N, L3000S, STLC3170) Line Driver Circuit and generates voltage-drive to the line via the HV (L3000N, L3000S, STLC3170), thus synthetizing the impedances required by various world administrations .

Line impedances as well as the two-to-four wire conversion synthesis are software programmable. Also Transmit (Tx) and Receive(Rx) AC frequency–response, determined by DSP-filters, guarantee voice-band flat-response. Tx and Rx Gains are programmable as well. Digitized voice can be encoded on A-law or u-law.

The DC characteristic is obtained by selecting limit-current value, DC-feed resistance (2 X 50Ω steps) and Drop-voltage. It also permits On-hook transmission and TTX pulse injection with filtering and shaping. TTX metering pulse generation (12 or 16kHz) has programmable amplitude up to 10 Vrms.

Off-hook detection with programmable thresholds is possible in all operating modes as described in section 4.

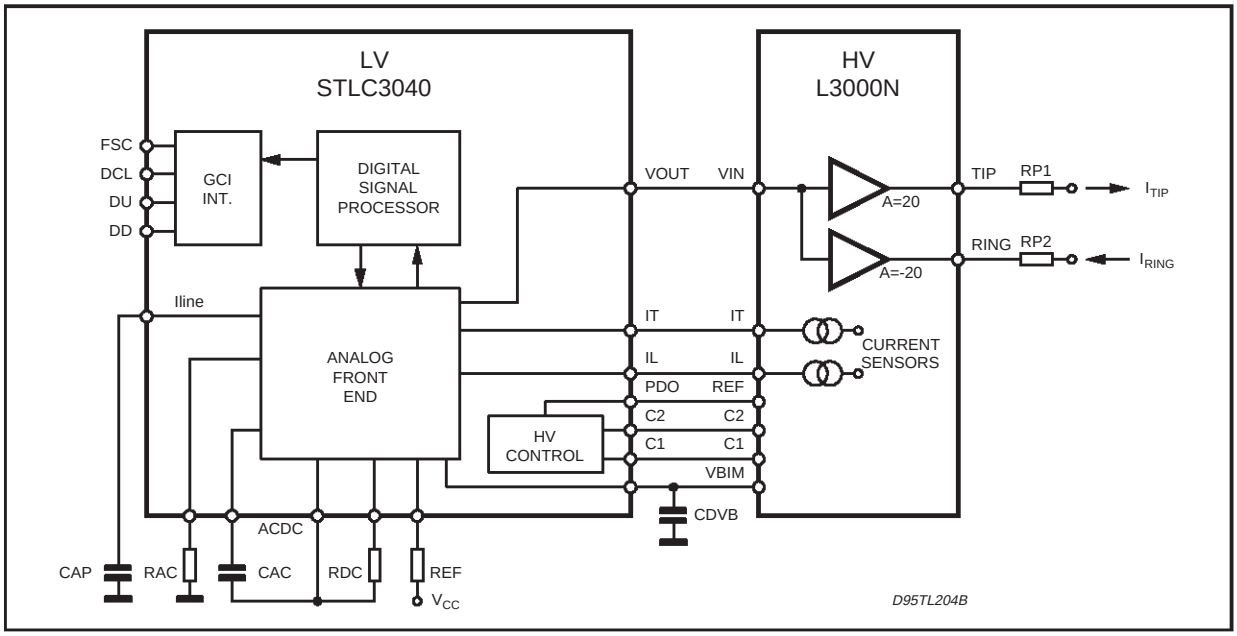
Ring-signal with zero-crossing start/stop injection is generated on chip with programmable frequency and amplitude. In addition, when Ring-trip is detected, the Ring-signal is automatically disconnected at the next zero-crossing.

Power consumption is kept low by providing a "Power-Down" mode where the HV-SLIC is switched off (Power Denial). A set of internal resistors connected to the line allows Off-hook detection in this mode. Overall power dissipation is around 50mW (max.) in Power Down mode.

Several testing features are included in the STLC3040, both for self-test and to test line leakage, capacitance ..etc, thus saving on test equipment and relays. Measured DC quantities are digitized and sent via the B1 voice channel to the backplane. With proper software selection each signal can be modulated by a 1KHz carrier before being sent to B1 voice channel. Programmable linear code, software selectable, boosts the calculation resolution.

Sigma-Delta converters (ASD: Analog, DSD: Digital) make the conversion independent of technology parameters (fig. 3).

Figure 2: Functional Diagram.



STLC3040 PIN DESCRIPTION (This list is grouped according to Function)

N.	Symbol	Type (*)	Description
POWER SUPPLY			
1	DGND	PS	Digital Ground
2	VDD	PS	+5V Digital Supply Voltage
27	AGND	PS	Analog Ground
33	VEE	PS	-5V Analog Supply Voltage
34	VCC	PS	+5V Analog Supply Voltage

STLC3040 PIN DESCRIPTION (continued)

N.	Symbol	Type (*)	Description
GCI			
40	SEL24	DI	Select Clock Frequency for GCI Interface 2MHz/4MHz not affecting the data rate (2Mbit/s) If SEL24 = 0, Clock Frequency = 2048KHz If SEL24 = 1, Clock Frequency = 4096KHz
43,42, 41	TS0,TS1, TS2	DI	GCI Select Time Slot Identifier Pins
3	FSC	DI	Frame Sync 8kHz GCI Interface
4	DCL	DI	Master Data Clock GCI Interface
5	DD	DI	Data Down link GCI Interface
6	DU	OD	Data Up link GCI Interface (Open Drain Driver)
INTERFACE TO HV SLIC			
9	C1	AI/O	State Control Signal 1. Combination of C1 and C2 defines HV (L3000N, L3000S, STLC3170) operating mode. Current sense for thermal indication.
10	C2	AO	State Control Signal 2. Combination of C1 and C2 defines HV (L3000N, L3000S, STLC3170) operating mode.
28	PDO	AO	Power down output. Proper bias current is provided to HV (L3000N, L3000S, STLC3170) by this pin. When the current is 0 the HV (L3000N, L3000S, STLC3170) goes in Power Denial (high impedance). Proper combinations of PDO with C1, C2 set additional operating modes for STLC3170 High Voltage Interface.
11,12	VL1, VL2	AI	Comparator Input. These are inputs of the comparator that senses the line voltage in Power Denial allowing Off/Hook detection in this mode.
15	IL	AI	Longitudinal Line-Current input IL = (I_{TIP} - I_{RING})/100.
19	IT	AI	Transversal Line-Current input IT=(I_{TIP} + I_{RING})/100.
25	VBIM	AI	Battery image monitor.
26	VOUT	AO	Output feeding the line voltage (DC, AC, RING, TTX) through H.V. HV (L3000N, L3000S, STLC3170).
I/O			
7, 8	IO1, IO2	DI/O	Programmable GCI controlled I/O.
39	O1	DO	Digital output written via GCI.
38	I1	DI	Digital input read via GCI.
MISCELLANEOUS FUNCTION			
29	EXT	DI	External Ring Sync. Input.
36	MR	DI	Master Reset Input. Active High. The STLC3040 is forced in Loop-open and internal registers are preset to default values.
31,32	IDL, IDM	AI	Identification Code Signals, M+L ternary digits
35	IDH	DI	H most significant bit, L least significant bit.
14	CAP	AI/O	Capacitor must be connected to this pin. Its value defines the Soft Battery Reversal slope.
16	RAC	AI/O	AC-Synthesis Reference Resistor.
20	ACDC	AI/O	AC/DC Line Split. Scaled line-current output, DC feedback input.
21	CAC	AI	Splitter Capacitor. Scaled AC line-current input.
22	RDC	AI	DC-Synthesis Reference Resistor.
23	REF	AI/O	Reference Voltage Output. A resistor on this pin sets the internal reference current.
UNUSED			
18,24	STR0,STR1	DI/O	Reserved for testing, must be shorted to DGND.
30,44	STR2,STR3		
13,17	SIR0, SIR1	DI/O	Must be left open.
37	SIR2	DI/O	Can be left open

(*)

Type	Description	Type	Description	Type	Description
AI	Analog Input	DI	Digital Input	DO	Digital Output
AO	Analog Output	PS	Chip Power/Ground	OD	Open Drain Output
AI/O	Analog Input/Output	DI/O	Digital Input/Output		

4 FUNCTIONAL DESCRIPTION

The STLC3040 is implemented by a combination of analog and digital circuits, merging the best available analog and digital processing performances of the BiCMOS technology. In particular two main blocks of the STLC3040 can be identified: an analog front end interfacing the HV (L3000N, L3000S, STLC3170) and a programmable DSP. (See fig. 3)

4.1 - Signal processing.

The line-current signal received in pin IT from the HV (L3000N, L3000S, STLC3170) is mirrored out of pin ACDC. On its way, its value is sensed to determine Off-Hook signalling. While in active conversation this istantaneous sensing is used for fast Hook signalling such as numbering. Then line-current AC and DC parts are splitted by RDC and CAC. The signal is processed to realize AC and DC impedance synthesis. Indeed IT pin carries the AC current due to voice signals present at line terminals and the DC current related to the specific V-I operating point.

During Stand-By mode signal is created by the DC current after AC part has been removed. This filtered Hook produces robust signalling in Stand-by mode or pause-period during reduced-power Ring mode.

As far as the DC characteristic is concerned, two different conditions are present and depend on loop resistance.

a) Resistive Feed Region: the SLIC kit operates as a voltage source with a series resistance equal to ($2Rp+n \cdot 2 \cdot 50\Omega$), where n can be programmed from 1 to 8 via CR8 register. Various values of voltage drops are possible as shown in Fig. 4.

b) Constant current region: when IL reaches the programmed limiting current value (from 0 to 69.3mA; 1.1mA step via CR6 register), the Kit operates as a proper constant current source. (see Fig. 4).

Concerning AC Processing the AC current-signal is converted to voltage on the reference resistor RAC (1620Ω).

Line impedance (real or complex) synthesis is carried out thanks to programmable filters. All the filters are integrated in the digital side of COFIS-LIC except the so called KA filter that is in the Analog Front End.

KD and Z (in digital side) filters allow to match the line impedance if properly programmed. Furthermore KA ensures stability to impedance synthesis loop.

In the Receive direction (Rx), the Analog Front End (AFE) receives a 1-bit modulated composite signal, which represents part of the voltage to be forced into the line. It performs DAC and filtering

Figure 3: Block Diagram.

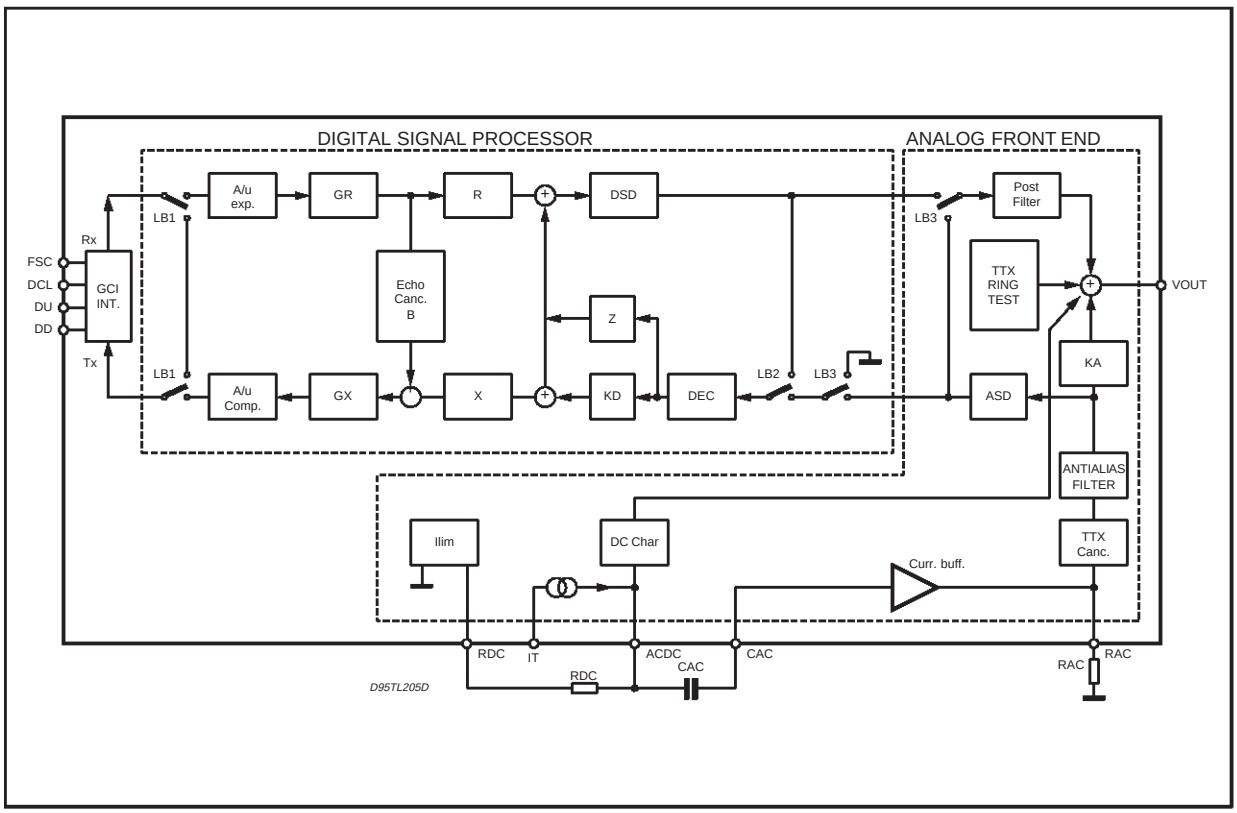
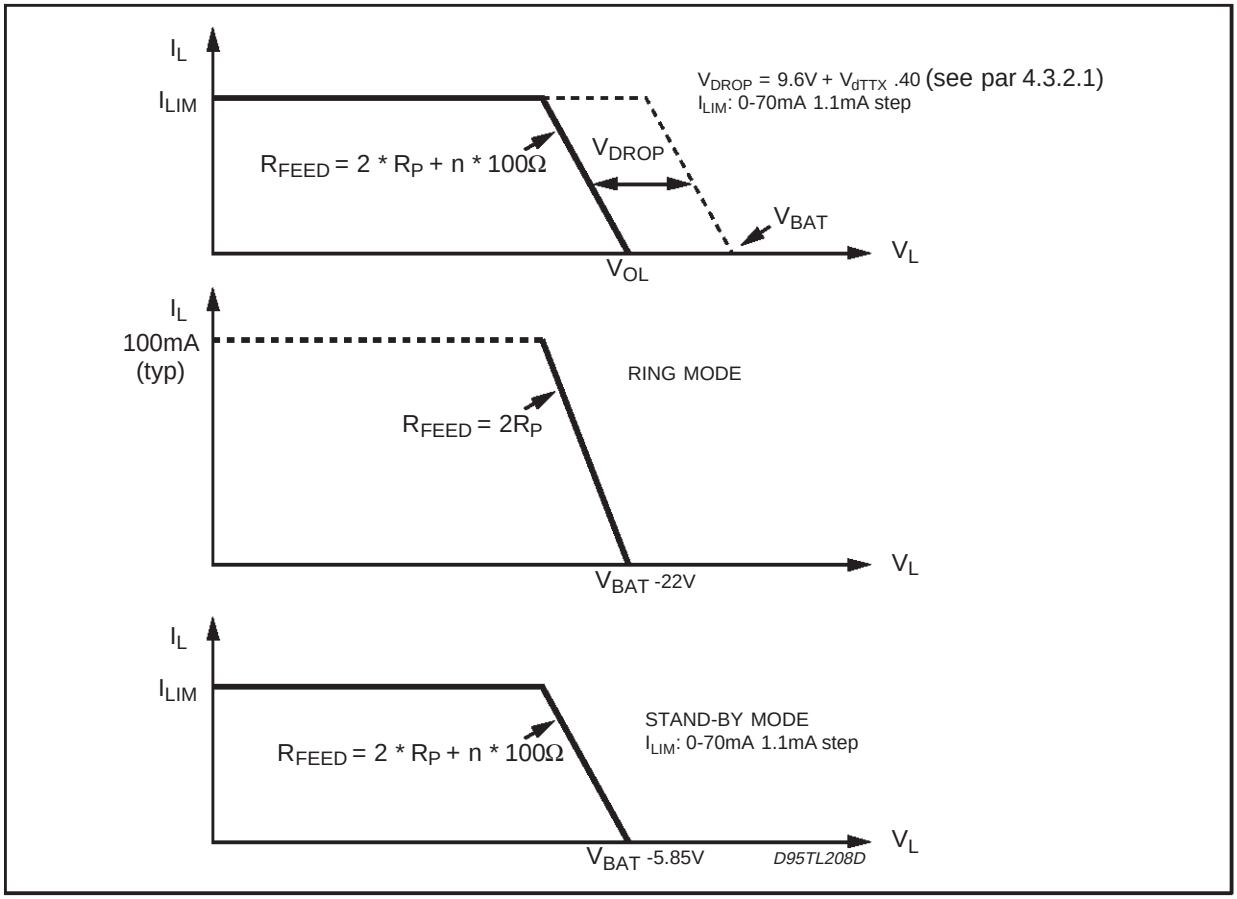


Figure 4.



functions. This voltage is then combined with the AC and DC analog impedance signals, plus a TTX pulse, in a summing buffer that feeds the Vin pin of the HV (L3000N, L3000S, STLC3170).

The architecture of the digital section is based on Digital Signal Processor which synthetises 7 digital filters (B, Z, X, R, KD, GX, GR). KA uses the some register value as KD. In Table 1 you can find the number of coefficients and their bit width for each filter.

Table 1:

FILTER	NUMBER OF COEFFICIENTS	COEFFICIENT WIDTH
B	8	14 BITS
R	4	14 BITS
X	4	14 BITS
GR	1	8 BITS
GX	1	8 BITS
KA, KD	1	8, 14 BITS (*)
Z	3	14 BITS

(*) KA is a subset of KD = most significant bits, (5-12) but sign bit, of KD register.

Filter coefficients can be programmed by 14 bits deep registers. These internal filters can be enabled setting the most significant 5 bits of CR4 register and CR11 (1). PCM encoding and ITU-T high/lowpass-filtering are done by dedicated state machines. Setting the bit 0 of CR4 register A-law or μ–law can be selected.

In order to match the complex line impedance, both amplitude and phase can be programmed using Filter Z.

The two to four wires echo cancellation is implemented thanks to programmable echo canceler (B Filter) with Gain and Group-delay equalizer.

Two programmable FIR filters X and R, can be set in order to guarantee the best overall line frequency response in the frequency domain, according to the local specifications. In this way the signal distorsion can be reduced with 14-bits resolution.

Gain Setting, both in transmission and in receive, is done by two FIR filters (GX for transmission, GR for Receive).

A coefficient optimization software let the users calculate GX and GR filters coefficients.

In transmission the maximum achievable gain without distortion is 3dB.

In receive the maximum programmable gain is 0dB.

Gain step resolution in both sides (Rx and Tx) depends on the value of the gains. See table below to gain/step accuracy.

Table 2.

Tx & Rx Gain	Step accuracy
Xmax - 6dB (1/128)	0.070dB
Xmax - 12dB (1/64)	0.14dB
Xmax - 18dB (1/32)	0.27dB
Xmax - 24dB (1/16)	0.56dB
Xmax - 30dB (1/8)	1.16dB
Xmax - 36dB (1/4)	2.5dB
Xmax - 42dB (1/2)	6.0dB

Tx: Xmax = 3dB; Rx: Xmax = 0dB

The Voice Signal Processing is shown in Block diagram in Fig.3.

In the RX direction, after being decoded, the voice sample passes through a set of interpolator and correction filters. The signal is finally oversampled to a high-rate of 256kHz before being summed to the feed-back impedance synthesis signal.

Analog circuits performs Off-Hook sense and allows On-Hook Signaling.

The longitudinal line current provided by the HV (L3000N, L3000S, STLC3170) is sensed at pin IL; Ground Key signalling is activated when the absolute longitudinal current on IL pin exceeds threshold. A low pass filter and programmable persistance filter (register CR3) elaborates the detection.

The Vbim pin receives from the HV (L3000N, L3000S, STLC3170) an information on the actual battery voltage (Vbim = Vbat/40), this voltage is then compared with the line voltage and one bit is set in the upstream data flow if Vline < (V_{OL}/2). This allows the system to be tailored for different line requirements.

Line and circuit-test functions are discussed in detail in the appendix.

The HV (L3000N, L3000S, STLC3170) is driven by the STLC3040 through two ternary pins C1 and C2 (pin 9 & 10 of STLC3040) that define the operating state of the HV (L3000N, L3000S, STLC3170) (Table 3).

C1 and C2 are set according to the content of the bytes received by STLC3040 at DD pin (pin 5) of the GCI Interface. C1 pin is internally tied to a current-sensing circuit. It senses an extra current that the HV (L3000N, L3000S, STLC3170) issues when in thermal overload conditions.

Table 3:

PDO = 50µA

		pin 9 (C1)		
		(*)V_{hv}	(*)V_{mv}	(*)Vlv
pin 10 (C2)	(*)V_{hv}	ST-BY	TIP OPEN	RING OPEN
	(*)V_{mv}	CONV.NP	BB.NP	RING NP
	(*)V_{lv}	CONV.RP	BB.RP	RING RP

PDO = 0µA

		pin 9 (C1)		
		(*)V_{hv}	(*)V_{mv}	(*)Vlv
pin 10 (C2)	(*)V_{hv}	Ext. Indication	Ext. Indication	Ext. Indication
	(*)V_{mv}	Ext. Indication	Ext. Indication	Ext. Indication
	(*)V_{lv}	Ext. Indication	Ext. Indication	Loop Open (HV Internal Resistors disconnect)

(*) V_{hv}, V_{mv}, V_{lv} see digital interface electrical characteristics.

Through PDO pin (pin 28) the STLC3040 forces the HV (L3000N, L3000S, STLC3170) in Power Denial if the current at this pin is 0. When the STLC3040 sinks 50µA the HV (L3000N, L3000S, STLC3170) will be turned on. In Power Denial, TIP and RING wires are disconnected from the HV (L3000N, L3000S, STLC3170) driver (Power Denial). Table 3 related to PDO = 0µA is valid only for STLC3170.

VL1, VL2 pins sense, the Off-Hook when HV (L3000N, L3000S, STLC3170) is in power denial, allowing very low power consumption in On-Hook condition.

Other important features, which usually require external circuitry, like Test Tones, Ringing, Metering Impulse Injection are programmable via software. Ring signals can be programmed both in Amplitude and Frequency via CR9 register.
The Metering Pulse Injection Level can be set by the CR10 register. Ring-Trip detection is performed by a dedicated internal circuitry.

4.3 Slic Kit Operating Modes

STLC3040/HV (L3000N, L3000S, STLC3170) kit can work in three main modes:

- POWER DOWN
- ACTIVE
- RING

Each mode is selected by Command-Indicate (C/I) and Monitor GCI channels. Line State changes are signalled through either upstream C/I or SR register. During the switching between any two modes the indication is frozen for 10msec in addition to the programmed persis-

tance.
All operating modes with related C/I command bits and CR register bits are shown in table 13 pag 45.

4.3.1 POWER DOWN

In this condition SLIC Kit reduces strongly its power consumption allowing Off-Hook detection. Only the internal circuitry dedicated to the Off-Hook detection is switched on.

C/I and CR1 register configuration (programmed by Monitor) defining Power Down Submodes are here below shown:

Table 4: Power Down Submodes

SLIC KIT MODE	C/I (7)	C/I (6)	C/I (5)	CR1 (7)	CR1 (3)	CR1 (2)
EXTERNAL INDICATION	0	0	0	0	X	X
LOOP OPEN	0	0	1	X	X	X
STAND BY	0	0	0	1	0	0
GROUND START	0	0	0	1	1	1

4.3.1.1 - External Indication

When this mode is selected both STLC3040 and HV (L3000N, L3000S, STLC3170) are set in Power Denial. STLC3040 cuts the bias current, sunk by the HV (L3000N, L3000S, STLC3170) via the PDO pin. In this mode the HV (L3000N, L3000S) shows a high impedance on TIP and RING pins; theHV shows on TIP pin the RT impedance and on RING pin the RR impedance if it integrates the 2 external resistors RT and RR (STLC3170). This mode is used to get a low power consumption obtaining supervision only via the STLC3040 and a resistive sensing network. The total power consumption of the SLIC Kit in this mode is under to 50mW (being almost 0 the consumption from battery).

4.3.1.2 - Loop Open

This mode can be selected only if the High Voltage integrates the two external resistors (RR, RT see fig. 5) of the feeding and sensing circuitry. This is implemented on the STLC3170 high voltage device.

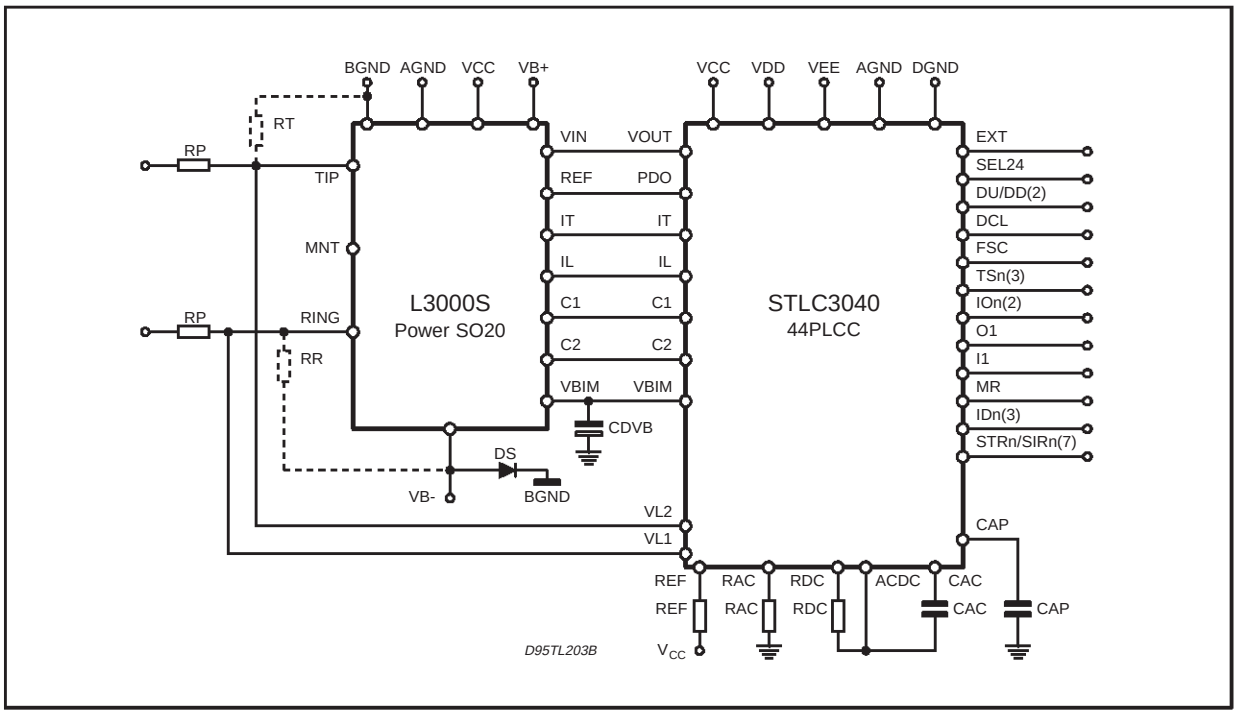
4.3.1.3 - Stand-By

SLIC behaves like a constant current source with typical 7mA feeding current. Open loop voltage is equal to (V_{bat} - 5.85V). COFISLIC power consumption is reduced to 150mW typical. Current limit and Off-Hook threshold are programmable by register CR7. Both off-hook and ground-key detectors are operating.

4.3.1.4 - Ground Start

The SLIC is set in Stand-By with the TIP wire (the most positive wire) in high impedance.
The current feeding is equal to Stand-By mode current feeding.

Figure 5: Application Diagram.



4.3.2 - ACTIVE

This operating mode is selected by the card processor after an Off-Hook detection in order to allow signal transmission on the line. Both Off-Hook and ground-key detectors are operating.
GCI Command - Indicate channel and CR1 register configuration (programmed by GCI Monitor) defining Active modes are herebelow shown:

Table 5:

SLIC MODE	C/I (7)	C/I (6)	C/I (5)	CR1 (7)	(*)CR1 (3)	(*)CR1 (2)
ACTIVE	0	1	0	X	1/0	1/0
ACTIVE + TTX	0	1	1	X	1/0	1/0

(*) This condition refers to STLC3040 only. If CR1.3 and CR1.2 are equal (either 0 or 1) both STLC3040 and HV (L3000N, L3000S, STLC3170) are in Active State. If CR1.3 and CR1.2 are different, one of two line wires will be set in high impedance, while the STLC3040 will still be in Active mode.

Current Limit and Off-Hook threshold are programmable by CR6 register. If the fifth bit of the Command-Indicate channel is set to 1 the Teletax Signal is superimposed to the voice signal.

4.3.2.1 - DC feeding

As far as DC characteristic is concerned, SLIC is basically working as a constant current device. It turns automatically into a resistive feeding when the programmed current limitation value cannot be held due to high line resistance. In active mode the constant current value is programmable in 1.1mA steps ranging from 0mA to 69.3mA. In resistive feeding region SLIC kit operates like a constant voltage source with a series impedance Rfeed = 2Rp+n · 2 · 50Ω (being Rp the external protection resistor and n a value set from 1 to 8 via CR8 register).
Voltage drop (Fig. 4) can be programmed in order to optimize voltage feeding characteristic, according to AC signal swing requested (ex: voice, voice + 2Vrms TTX, voice + 5Vrms TTX):

$$V_{DROP} = Vd3000 + 40\ (VdAC + VdTTX)$$

Vd3000 = drop due to internal HV (L3000N, L3000S, STLC3170) architecture (2.8V typ.)

VdAC = AC headroom on Vout (170mV typ.)

VdTTX = TTX headroom on Vout (from 0 to 465mV (15x31) typ. depending on programmed TTX level).

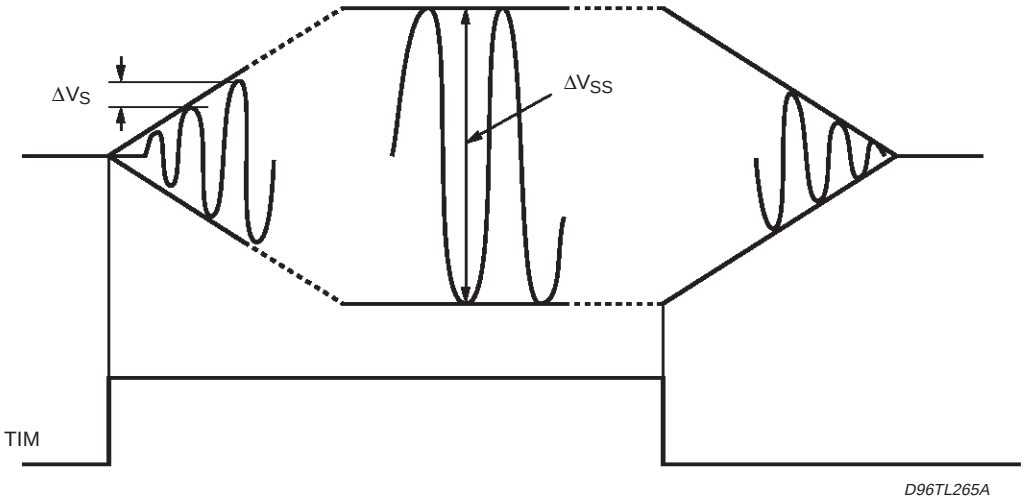
At HV (L3000N, L3000S, STLC3170) two wires the following equation must be used:

$V_{DROP(TIP/RING)}$ = 9.6V + CR10 [7..3] · 15mV · 40.

4.3.2.2 - Metering Generation

TTX signal is internally generated, filtered and shaped. Shaping is carried out by a gradual increase of metering pulse level of a level step (see CR10 register) per signal half period (please see Fig. 6). TTX can be programmed both in frequency (12 or 16 KHz) and open loop amplitude (from 0 to 10Vrms in 255 steps). The output impedance at TTX frequency is just 2 x R_p; therefore the proper value should consider the drops

Figure 6: TTX Shaping



$\Delta V_S \equiv$ 2 CR10 LSB
$\Delta V_{SS} \equiv$ PROGRAMMED VOLTAGE AS PROG IN CR10

across the 2Rp. Filtering is performed inside the device without external circuitry.

Feeding voltage polarity can be reversed in both soft and hard ways under software command.

4.3.2.3 - Boost Battery

To supply very long lines (high loop resistance), the SLIC can be set in "Boost battery" mode. In this mode the line is fed with a total battery voltage equal to |Vb+| + |Vb-|, keeping the same current limiting values as in active mode. The Vb+ battery is the same positive supply voltage needed for ringing generation.

4.3.3 - RING

In this mode COFISLIC provides ringing signal equivalent to a maximum 85Vrms ring line voltage. HV L3000N and L3000S handle a maximum 65Vrms balanced ring signal; HV STLC3170 handles a maximum 85Vrms. It is possible to reduce power consumption if Power Reduced Ring mode is chosen. The output impedance is represented only by the two Rp protection resistors and the current is limited to 100mA.
C/I and CR1 register configuration (programmed by GCI monitor channel) define Ring conditions as herebelow shown:

Table 6:

SLIC MODE	C/I (7)	C/I (6)	C/I (5)	CR1 (7)	CR1(*) (3)	CR1(*) (2)
RING	1	1	X	X	1/0	1/0
Reduced Power Ring	1	0	X	X	1/0	1/0

(*) CR1.3 has to be equal to CR1.2 : 0 or 1

If unbalanced ringing is requested, SLIC can support also external ringing injection configuration, providing both logic command for relay driver and ringing detection circuitry.

4.3.3.1 - Ring Generation

When the ringing function is selected, a low level ringing signal (1.5Vrms typ.) is generated inside the STLC3040 and provided on the VOUT pin. This signal is then amplified and injected in balanced mode into the line through the HV (L3000N, L3000S, STLC3170), with superimposed DC voltage of 24V typical. Both ringing frequency and amplitude are software programmable.

The first and the last ring cycles are synchronized by the STLC3040 so that the ringing signal always starts and stops with zero phase.

In Ring mode the Off Hook indication is asserted whenever during two consecutive ring periods (or an equivalent time in pause) the mean value of the IT current exceedes the programmed threshold. After the persistance time the Off Hook is sent to C/I upstream.

4.3.3.2 - Power Reduced Ring

The modes in Table 6 differ only during the ring-pause phase.
During the pause of reduced-power-ring mode the SLIC Kit is set in Stand-By.
The pause state is forced by stop ring command (C/I.5 downstream = 0) or by the detection of Off-Hook.

4.3.3.3 - Unbalanced Ringing

The device allows an unbalanced Ring application. This application requires an external ringing generator. A digital I/O pin can be used to drive the external relay driver.

An external ring sync. signal synchronised on the Vring zero crossing, must be provided on pin 29 of STLC3040. The external ring frequency must be the same as the value programmed in the internal register.

4.4 - TESTING FEATURES

STLC3040/HV (L3000N, L3000S, STLC3170) kit allows to perform up to 11 tests. They are aimed at covering the following issues.

1. Line and Battery Characteristics AC, DC Leakage.
2. SLIC Kit block testing.
3. Signal Path Behavior

Every test is set by internal registers, which are written through GCI data down Monitor.
Test results are typically digitalized, codified and dropped in the first PCM channel (byte B1) of GCI interface. For four go/nogo tests (Analog Loopback, Ring Generator, TTX Generator and TTX filter) the result of the test is also written in one bit of CR5 register that is readable through Monitor.
Test functions are carried out with SLIC Kit in a mode set automatically by COFISLIC. For detailed explanation about tests see chapter 6.

4.4.2 - Loop Backs

LOOP1 and LOOP2 bits of CR4 register set up some internal loop backs. This feature is typically used for COFISLIC tests (see fig. 3).
Any Loopback is enabled by CR1.5 bit. Loopback type is selected by register CR4.
There are three types of loopback.

Loopback 1 (CR4.2 = 0, CR4.1 = 1) simply copies the downstream B1 to the upstream B1 through the GCI interface. In this case no Rx signal is sent to the line. The kit operates as previously set.

Loopback 2 (CR4.2 = 1, CR4.1 = 0) sets Kit SLIC in Active mode. It copies the output of DSD (Digital Sigma Delta converter) to the input of the DEC

block, as shown in fig. 3. Rx signal goes on to the line. Please note that this loopback function cuts off the Tx channel connection to the line.
All other functionalities are those of Active mode.

Loopback 3 (CR4.2 = 1, CR4.1 = 1) sets Kit SLIC in Active mode. Rx signal is prevented to go the line. Tx path is cut off from the line as well. Output of ASD is copied to input of AFE port filter. DSP part can be still exercised via B1. All the functionalities are those of active mode.

4.4.3 - Test Tones Generation

In Active mode STL3040 can generate either 1kHz or 800Hz frequencies towards the 2-wire line. The two tones can also be enabled at the same time.

TON bit of CR1 register enables the 1 kHz test tone generator. 800Hz is enabled by CR5[3.0] = 4h.
800Hz amplitude is programmable through the same register (CR10) used to set TTX amplitude. 1kHz level is fixed at PCM full scale and can be modified changing Rx channel gain.

4.5 COFISLIC Reset

Any reset to COFISLIC sets SLIC kit in External Indication. COFISLIC is set in Power denial. There are four different reset sources:

Power-On Reset,

Reset pin MR (pin 36),

Reset bit (SOP command bit 4).

During Reset, output pins are set as follows:

DU	(pin 6)	High impedance
C1	(pin 9)	V_{hv}
C2	(pin 10)	V_{hv}
PDO	(pin 28)	High impedance
O1	(pin 39)	Low Level

Additionally a Reset of the DSP part of the COFISLIC is triggered by CLK fail detection (see also page 17).

4.5.1.1 Power On Reset

When voltage at VDD pin crosses over an internal fixed threshold (typ. 2.5V) COFISLIC is reset.

4.5.1.2 Reset Pin MR

If an high level is applied to pin 36 (MR) the COFISLIC is reset.

MR pin has built-in filter to reduce spike sensitivity. Spikes smaller than 90ns are neglected.

Therefore at MR pin a high level is surely recognised as a Reset if it is present for at least 2µs.

4.5.1.3 Reset bit RST (SOP command bit 4)

If RST bit is programmed to 1 COFISLIC is reset. SOP register is set by GCI down stream channel.

Until the end of the current command processing, the GCI is kept active.

4.5.1.4 - CLK fail Reset

Clock fail triggers a reset routine of the DSP which lasts, until the first good frame that follows the failed ones.

In active mode during the Reset routine, the voice channel of "Data up" (Du, pin 6) is forced IDLE dependent on the selected codification law.

As far as "Data down" (DD, pin 5) is concerned, the voice channel does not reach the Vout during this phase.

Z sinthesys is partially performed, the DSP branch is not active while the analog loop is kept active.

Coefficients and CR registers' contents do not change because of this partial reset, GCI state as well. Metering pulse injection signaling is not affected too. Ring generation and ring trip detection are not influenced too.

4.5.2. Start-up State

During reset the device is in Power- Denial Mode. After Reset, COFISLIC is automatically switched to its basic start-up state in which it uses internal default values for all filters and settings (AC and DC).

Programmed coefficients of filters are not reset. Bit 0 of CR6 register, FIXC, is set to 1, this means that fixed values are used after a Reset until FIXC is set to 0.
Even if FIXC = 1, both checksum and reading of filter coefficients are carried out on formerly programmed coefficient set.

Table 7: Fixed Filter Coefficients

Filter	Coefficients (h)
KA, KD	0E00
Z	019C, 24A0, 1600
X	149A, 0521, 3F40,3EF2
R	1879, 39E0, 00B4,0006
GTX	FF
GRX	60
B	0, 0, 0, 0050, 0680, 06D0, 0, 3C80

SLIC is switched to operating mode carried by GCI Command Indicate at least two frames after reset. SLIC status and Filter configuration can be changed by SOP and COP commands.

After reset the device is internally set as follows:

- configuration registers are set to their default

values (see Chapter 4-8 Configuration Register)
- RST bit (SOP command bit 4) is set to 1 to indicate that a reset has occured
- GCI interface is reset. After software Reset its former state is kept. On-going GCI communication is stopped
- DU is in high impedance state
- FIXC = 1 (CR6 Register) Fixed Coefficients are selected

– DC characteristics of SLIC-Kit
- External Indication
- Normal Battery
- Test Disabled
- Persistence for Off-Hook and I1: 10ms
- Persistence for Ground Key: 20ms
- Ring Trip threshold = 4.2mA
- Ilim = 22mA in active mode
- Ilim = 7.7mA in Stand-By mode
- Off-Hook detection threshold in active mode = 10mA
- Off-Hook detection threshold in Stand-By mode = 7.7mA
- Feeding Resistance in either Active or Stand-By mode = 2 · (50 + Rp) (fuse impedance value is not included)
- Ring: Internal
- Ring Frequency = 25Hz
- Ring Voltage = 65Vrms
- Line Voltage Drop = 28.2V
- External Indication Voltage Threshold for Off-Hook detection = 9.0V
- A-law is programmed

AC characteristics of SLIC-Kit
- Metering with Teletax
- Line Impedance: (Synthetized Impedance + 2 · Rp) = 700Ω + 2Rp
- Balance Impedance: 910Ω / / 62nF
- Tx Gain: 0dBr
- Rx Gain: -7dBr
- Teletax Voltage onto line V_{TTX} = 10Vrms
- Teletax Frequency = 16kHz
- Battery Reversal: Hard

Further after the reset
- I/O pins are set as inputs
- PD bit of CR1 is reset (means STLC3040 in Power-Denial mode).
- All bits of Signalling Register are masked
- Data Upstream C/I byte is reset to 0

Check Configuration-registers reset-value for more detailed information.

4.6 GCI Backplane Interface

GCI is a standard serial interface for interconnection of SLIC kit to the line card backplane.
The digital interface is used to transfer status information to and from the SLIC as well as to transfer filter coefficients for the DSP.

With this approach an analog Line Card could be replaced by an ISDN one and viceversa without need to change the interface to the linecard controller.
As far as physical level is concerned this standard consists of four wires:
- Serial Transmitted data to the backplane: DU
- Serial Received data from the backplane: DD
- 8KHz Frame Synchronization: FSC
- Master Data Clock (2048KHz or 4096KHz): DCL

The frame is divided into eight time-slots which contains four bytes each. Bit rate in both directions is 2048Kbit/sec and it's not affected by clock frequency. This can be chosen setting SEL24 pin. Eight GCI time slots are selectable via three pins TS2-TS0 (see Table 8).
For every time slot the first bit, received or transmitted, is the Most Significant one, according to timing diagram shown in fig. 7.
Information is clocked out on the rising edge of data clock and it is latched in on the falling edge of DCL signal.
Frame Synchronization FSC is a 8KHz signal and its rising edge gives the time reference of the first bit in the first GCI (input or output) channel and resets the slot counter at the next falling edge of the clock every frame.

Four bytes of any GCI time slot are:
- B1 channel for PCM data,
- B2 channel not used,
- M (Monitor) channel used to write and monitor COFISLIC internal registers,
- C/I (Command/Indication) channel used to set the Operating Mode.

8bits	8bits	8bits	6bits	1bit	1bit
B1	B2	MONITOR	C/I	A	E
Byte 1	Byte 2	Byte 3	Byte 4		

A single GCI channel has 256kbit/s data rate.

Exchange Protocol

STLC3040 validates a received byte if it is detected identical two consecutive times. (see figg. and 7and 8)

The exchange protocol is identical for both directions. The sender uses the E bit to indicate that it is sending a Monitor byte while the receiver uses A bit to acknowledge the received byte. When no

Table 8: GCI Time Slot assignment.

SEL24	TS2	TS1	TS0	GCI operating mode
0	0	0	0	time slot 0:DCL = 2048kHz
0	0	0	1	time slot 1:DCL = 2048kHz
0	0	1	0	time slot 2:DCL = 2048kHz
0	0	1	1	time slot 3:DCL = 2048kHz
0	1	0	0	time slot 4:DCL = 2048kHz
0	1	0	1	time slot 5:DCL = 2048kHz
0	1	1	0	time slot 6:DCL = 2048kHz
0	1	1	1	time slot 7:DCL = 2048kHz
1	0	0	0	time slot 0:DCL = 4096kHz
1	0	0	1	time slot 1:DCL = 4096kHz
1	0	1	0	time slot 2:DCL = 4096kHz
1	0	1	1	time slot 3:DCL = 4096kHz
1	1	0	0	time slot 4:DCL = 4096kHz
1	1	0	1	time slot 5:DCL = 4096kHz
1	1	1	0	time slot 6:DCL = 4096kHz
1	1	1	1	time slot 7:DCL = 4096kHz

Figure 7.

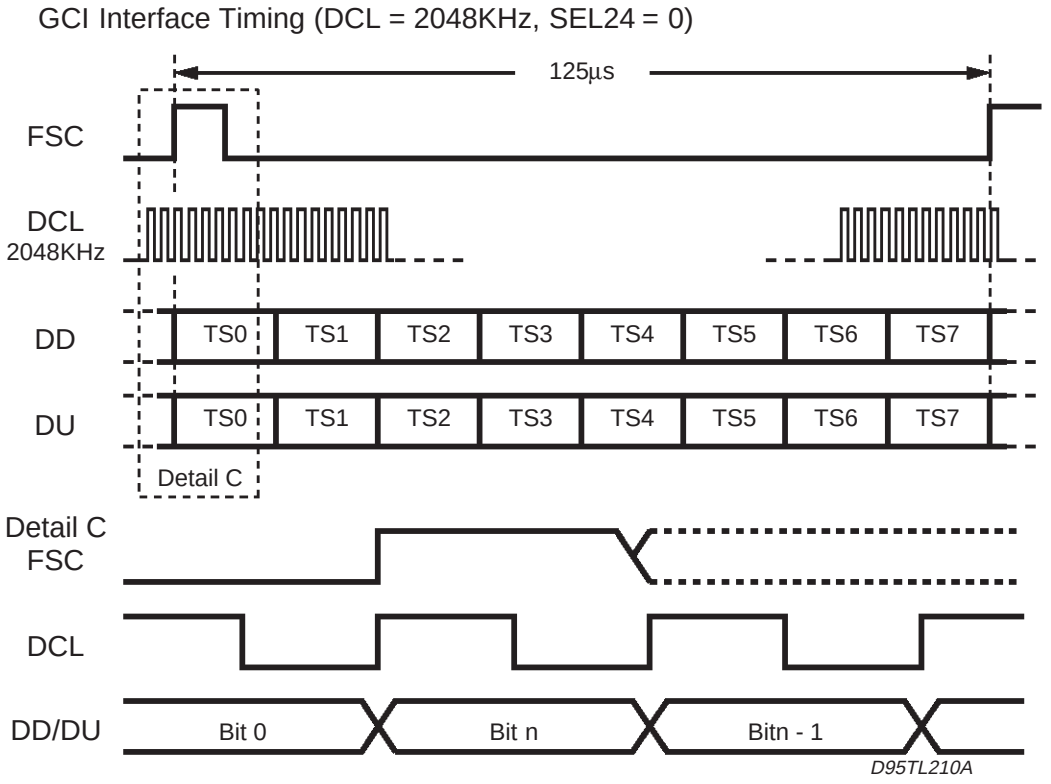
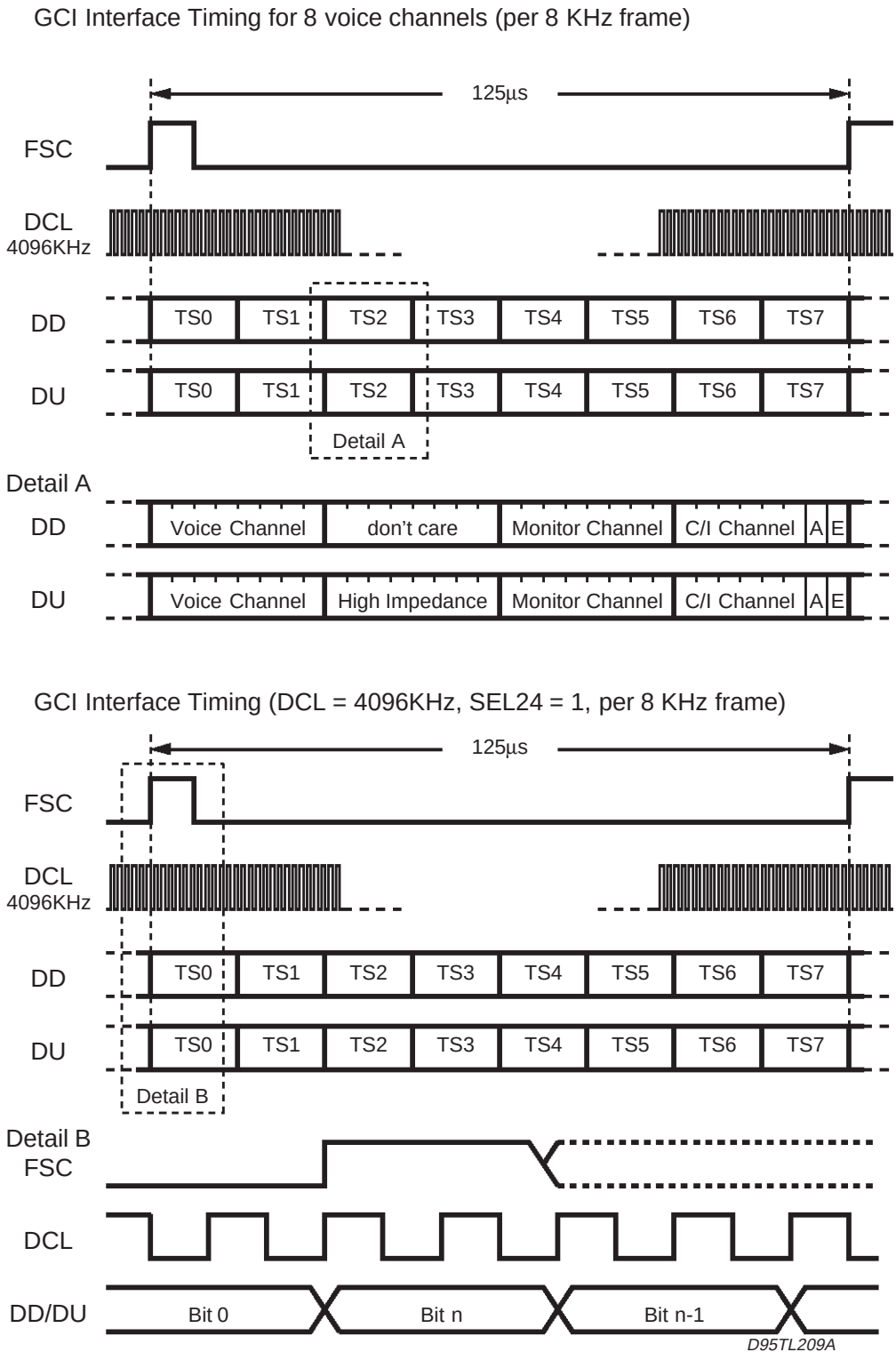


Figure 7. (continued)



message is transferred, E bit and A bit are forced to inactive state (high = 5V).

A transmission is started by the sender (Transmit section of the Monitor channel protocol handler) by putting the E bit from inactive to active state (low = 0V) and by sending the first byte on Monitor channel in the same frame. Transmission of a message is allowed only if A bit, sent from the receiver, has been set inactive for at least one consecutive frame. When the receiver is ready, it validates the incoming byte when received identical in two consecutive frames. Then, the receiver sets A bit from the inactive to the active state (preacknowledgement) and maintain active at least in the following frame (acknowledgement).

If validation is not possible (two last bytes received are not identical) the receiver aborts the message by setting the A bit active for only a single frame.The second byte can be transmitted by the sender putting the E bit from the active to the inactive state and sending the second byte on the Monitor channel in the same frame . The E bit is set inactive for only one frame. If it remains inactive more than one frame, it means an end of message. The second byte may be transmitted only after receiving of the pre-acknowledgement of the previous byte . Each byte has to be transmitted at least in two consecutive frames.

The receiver validates the current received byte as for the first one and then set the A bit in the next two frames first from the active state to the inactive state (pre-acknowledgement) and back to the active (acknowledgement). If the receiver cannot validate the received current byte (two bytes received not identical)it pre-acknowledges normally but lets the A bit in the inactive state in the next frame which indicates an abort request . If a message sent by the COFISLIC is aborted, the COFISLIC will send again the complete message until receiving of an acknowledgement . A message received by the COFISLIC can be acknowledged or aborted with flow Control.

The most significant bit (MSB) of Monitor byte is sent first on the Monitor channel. E & A bits are active low and inactive state on DU is 5 V. When no byte is transmitted, Monitor channel time slot on DU is in the high impedance state.

The GCI interface transmitter will abort after 8 times during which it hasn't succesfully received any acknowledge from the device upstream. The GCI interface receiver will go in abort request mode after 8 times of unsuccessful attempts to get 2 identical copies of the data. This means that after 8 frames of unsuccessful handshake, the GCI interface transmitter will abort while the receiver will make a request for abort.

4.6.1 B1/B2 Channels

4.6.1.1 PCM codifications

GCI interface extracts receiving PCM data from the B1 channel on DD pin and outputs PCM bytes on DU pin.

4.6.1.2 Linear codification

STLC3040 allows Linear codification simply setting two bits of CR12 register.
COMTX (bit 0) enables the linear code in transmission, while COMRX (bit 1) enables the linear code in receive.

STLC3040's linear code consists of 16 bits which means a range from (-2^{15}) to (2^{15}-1) Linear Code is housed in B1 and B2 channels, B1 is the least significant byte end B2 is the most significant byte.

15 bits are dedicated to the module while the most significant bit is the sign bit.
If bit 15 (sign bit) = 0 bit 14.....bit 0 represent the module.
If bit 15 = 1 module is got by 2-complementing bit 14 ..... bit 0.

4.6.2 C/I Channel

Command/Indicate byte is a 6 bits wide command full duplex transmission.
Internal C/I registers will be loaded if downstream command is stable for two frames.

Also upstream Command/Indicate byte lasts for at least two consecutive 8KHz frames. Command/Indicate is mainly used to set SLIC operating mode and to monitor subscriber On/Off-Hook and Ground-Key detection.
Any change of line conditions like On-Off/Hook and Ground Key is signalled via upstream C/I. HOOK and GNDK bits always reflect line conditions even if corresponding bits of Signalling Register are masked by CR12 register. Bit 5 of upstream Command/Indicate says that at least one of Signalling Register six most significant bits has changed its logical value.
Bit 5 of upstream Command/Indicate does not change if related bits of Signalling Register have been masked by CR12 register.

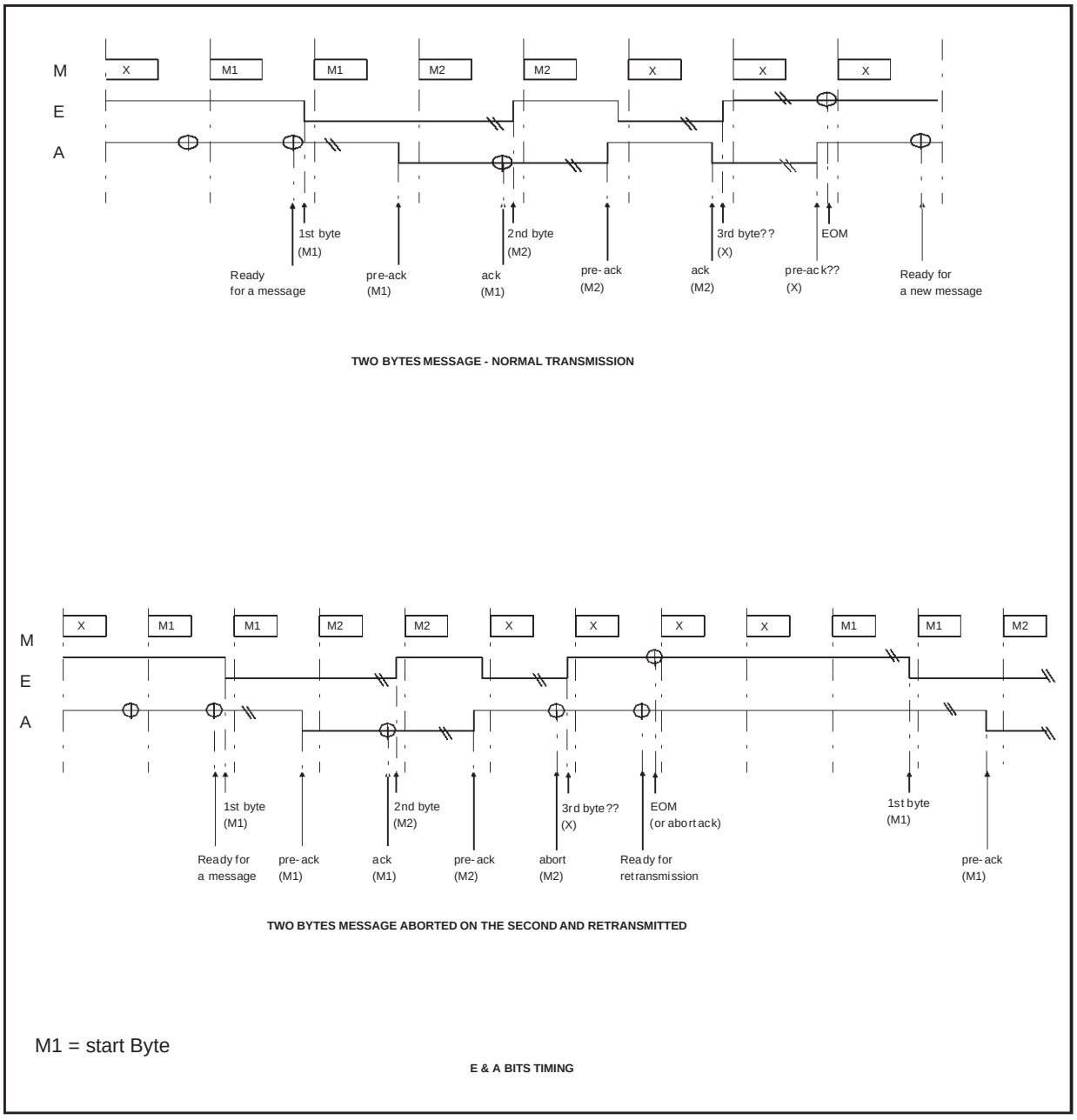
Input/Output pins (IO1/2,I1,O1) can be set and monitored by C/I channel too. Note that there is no address in both directions because there is one GCI time slot per each COFISLIC.

C/I channel in Downstream direction consists of six bits as shown below :

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2
RING	CONV	TIM	IO1	IO2	O1

Basically the first 3 Most significant Bits of C/I downstrean operate as follows. For a complete description please refer to Table 13.

Figure 8: GCI Monitor Channel messaging examples.



RING = Sets COFISLIC into ringing state.
= 0 COFISLIC is not in ringing state.
= 1 COFISLIC is in ringing state.

CONV = Sets COFISLIC into power up state.
= 0 COFISLIC is in a power down state.
= 1 COFISLIC in power up state.

TIM = Timing bit to control the timing of ringing and meterpulses.
= 0 COFISLIC is in ringing pause
or no meterpulse is on.
= 1 COFISLIC is in ringing
or output of a meterpulse is running.

IO1, IO2 define the value for the programmable Input/Output pins (7, 8) if programmed as output pins by CR2 register.

IO1 = 0 The related pin 7 at the digital interface of the COFISLIC is set to a logic 0

= 1 The related pin 7 at the digital interface of the COFISLIC is set to a logic 1

IO2 = 0 The related pin 8 at the digital interface of the COFISLIC is set to a logic 0

= 1 The related pin 8 at the digital interface of the COFISLIC is set to a logic 1

O1 sets value for fixed output pin 39

= 0 The related pin 39 at the digital interface of the COFISLIC is set to a logic 0

= 1 The related pin 39 at the digital interface of the COFISLIC is set to a logic 1

C/I channel in Upstream direction is herebelow described:

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2
HOOK	GNDK	SLCX	IO1	IO2	I1

HOOK indicates loop condition:

= 0 Subscriber is On-Hook

= 1 Subscriber is Off-Hook

GNDK indicates Ground Key detection:

= 0 No Detected Longitudinal Current

= 1 Detected Longitudinal Current

SLCX is the summary output of the signalling register (See TOP command)

= 0 No unmasked bit in signalling register has toggled

= 1 An unmasked bit in signalling register, has toggled, it is reset only if SR register is read.

IO1,IO2 give logical state of programmable Input/Output pins (7, 8)

IO1 = 0 Corresponding pin 7 at digital interface of COFISLIC is receiving a logic 0

= 1 Corresponding pin 7 at digital interface of COFISLIC is receiving a logic 1

IO2 = 0 Corresponding pin 8 at digital interface of the COFISLIC is receiving a logic 0

= 1 Corresponding pin 8 at digital interface of COFISLIC is receiving a logic 1

If as per CR1 register IO1 and IO2 are programmed as outputs, data up command indicate, IO1 and IO2 are set to 1

I1 gives logical state of fixed input pin 38.

= 0 pin 38 is receiving a logic 0.

= 1 pin 38 is receiving a logic 1.

4.7.1 Monitor-Channel (M-channel)

As already mentioned COFISLIC can be programmed and monitored via GCI Monitor.
Data transfer from and to STLC3040 starts with a specific byte, called Start Byte:

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
1	0	0	0	0	0	0	X

In downstream a second byte selects one of the three different kinds of commands which Monitor channel transfers: SOP, COP, TOP.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
X	R/W	X	X	B3	B2	X	X

R/W	= 0	Write Operation
	= 1	Read Operation
B3	B2	
0	1	SOP command
1	1	TOP command
X	0	COP command

For SOP, COP, TOP commands the Start Byte is 81 in DU directions.
SOP commands set and monitor COFISLIC status.
TOP commands read Signalling register and coefficient checksum.
COP commands set and read filters coefficient.
SOP and COP can be either write or read commands, while TOP is used only for reading.
A write command (SOP and COP) can be followed by up to 14 bytes. An answer to SOP, COP, TOP commands consists of maximum 16 bytes. First byte is always the start byte (81h).

Registers from CR1 to CR12 are accessed by SOP command both in reading and writing. TOP command is used to read the Signalling Register and the Coefficient Checksum. The RAM, where filters coefficient are stored, is accessed by COP commands.
A fourth command of the Monitor Channel is the so called Channel Identification Command (CIC). This command will be run if the COFISLIC receives the following code on the Monitor Channel for at least two frames:

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
1	0	0	0	0	0	0	0

Upon CIC command is received COFISLIC will place two bytes on DU line, each byte is repeated at least twice.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
1	0	0	0	CONF(3)	CONF(2)	CONF(1)	CONF(0)

This byte replaces usual Start byte. Low nibble CONF(3)-CONF(0) defines the identification code according to the logic values of three input pins IDH (pin 35), IDL and IDM (pin 31 and 32).

Herebelow it is the Table of Identification:

Table 9:

IDH	IDM	IDL	Id. Code
+5V	-5V	-5V	0
+5V	-5V	0V	1
+5V	-5V	+5V	2
+5V	0V	-5V	3
+5V	0V	0V	4
+5V	0V	+5V	5
+5V	+5V	-5V	6
+5V	+5V	0V	7
0V	+5V	0V	8
0V	+5V	-5V	9
0V	0V	+5V	A
0V	0V	0V	B
0V	0V	-5V	C
0V	-5V	+5V	D
0V	-5V	0V	E
0V	-5V	-5V	F

Data transfer is completed by the next byte:

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
1	0	0	0	1	0	0	0

4.7.1.1 TOP Command

As above mentioned TOP command allows reading Signalling Register and Coefficient RAM checksum.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
X	R/W	X	X	1	1	LSEL1	LSEL0

R/W = 0 No Operation
= 1 Read Operation

LSEL1	LSEL0	
0	0	1 byte for signalling register reading
0	1	1 byte for signalling register and 2 bytes for filter coefficients checksum reading, low byte is read first and then high byte.
1	0	15 bytes for Line Card Identification Code reading

In answer to TOP command COFISLIC will place the Start byte first.

Coefficient checksum is defined by this algorithm:

$$X^{16} \oplus X^{10} \oplus X^{7} \oplus X \oplus 1$$

This algorithm guarantees a fault coverage of:
$(1 - 2^{-15})$

SIGNALLING REGISTER (SR)

SR provides information about loop condition: Off/OnHook condition, line constant current, line voltage. It also signals temperature alarm related to HV SLIC (L3000N, L3000S, STLC3170) and clock fails (see page 10). The Clock fail indication is set whenever the number of DCL periods in one frame (between two-FSC pulses) is different from the standard one.
Hook and Ground Key state variations toggle the related bits of SR register and therefore switch HOOK and GNDK bits of upstream C/I.
Every change of any of the six most significative bits of SR register is summarized in SLCX bit (bit 5) of upstream Command/Indicate, provided that these bits are not masked by CR12 register. Masking acts only on SLCX bit.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
HOOK	GNDK	VB_2	ILIM	TEMP	CK_FAIL	XX	XX

Reset Value: 00h

HOOK indicates loop condition (same as in upstream C/I):

= 0 Subscriber is On-Hook

= 1 Subscriber is Off-Hook

GNDK shows a Ground Key detection (same as in upstream C/I):

= 0 No Detected Longitudinal Current

= 1 Detected Longitudinal Current

VB_2 half battery voltage across the line is detected

(V_{LINE} compared to $\frac{V_{OL}}{2}$).

This bit is designed to indicate the line DC operating point only in Stand-By and Active modes, with no TTX injection

= 0 if ($|V_{LINE}| < |\frac{V_{OL}}{2}|$)

= 1 if ($|V_{LINE}| > |\frac{V_{OL}}{2}|$)

where: $|V_{LINE}| = |V_{TIP} - V_{RING}|$

$|V_{OL}| = |V_{BAT} - V_{DROP}|$

ILIM Current Limit Region
This interrupt is automatically masked in Ringing Mode

= 0 Resistive Feeding Region

= 1 Constant Current Feeding Region

TEMP Temperature alarm of HV SLIC (L3000N, L3000S, STLC3170) which is signalled through HV (L3000N, L3000S, STLC3170) interface

= 0 Normal Temperature

= 1 Temperature Alarm from HV (L3000N, L3000S, STLC3170)

CK_FAIL Receiving Clock and/or Synchronization signals failures

= 0 no Detected Clock or Sync fails

= 1 Detected Clock or Sync fails

Bits ILIM, TEMP, VB_2 have 7ms persistance fixed.

4.7.1.2 COP Command

Every COP command is started by the Start Address. A second byte contains the RAM address related to the programmable filters.
Address is defined by the least significative five bits except the third one which identifies a COP command.
COP commands consist of maximum 14 bytes used to set and monitor digital filter coefficients.

COP register:

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
X	R/W	COD5	COD4	COD3	COD2	COD1	COD0

R/W = 0 Subsequent bytes are written to COFISLIC

= 1 Subsequent bytes are read from COFISLIC

COD2 = 0 Identifies a COP command COD5, COD4, COD3, COD1, COD0 bits identify filters address as shown here below (Table 10).

For every coefficient, but B filter, with 14bit width the Least significant Byte is sent first. In the Most Significant Byte the first two bits must be stuffed with 0.

For B Filter the 14 bytes are the result of the concatenation of the 8 coefficients of 14 bits

4.7.1.3 SOP Command

Reading and writing of CR and SOP register is performed via SOP commands. Configuration, operation and test data can be set and updated by this command. As for every Monitor channel command the SOP is started by Start Byte, in downstream, followed by a byte that sets the SOP register.

SOP register:

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
X	R/W	POL	RST	0	1	LSEL1	LSEL0

R/W = 0 Write to Cofislic

= 1 Read Operation

POL = 0 Normal Polarity Feeding

= 1 Reverse Polarity Feeding

RST = 0 Normal Operation

= 1 Reset, set the COFISLIC to the basic setting mode

After a reset, RST is set to 1. RST is toggled to 0 after a SOP read operation with LSEL bits programmed to 00b.

If R/W = 0		Write to COFISLIC
LSEL1	LSEL0	
0	0	No byte is following
0	1	Two bytes, which write CR1 and CR2 Registers, follow
1	0	12 bytes, which set CR1,.,CR12 registers, follow
1	1	Not available
If R/W = 1		Read from COFISLIC
LSEL1	LSEL0	
0	0	Replies the SOP * command received by COFISLIC
0	1	Replies the SOP * command received by COFISLIC, followed by two bytes: CR1, CR2 Registers
1	0	Replies the SOP * command received by COFISLIC, followed by twelve bytes: CR1, CR2 CR12 Registers
1	1	Not available

SOP *: during the on going SOP command SOP* is the previously processed SOP command.

Table 10:

COD5	COD4	COD3	COD1	COD0	ADDRESS	Following Bytes
0	0	0	0	1	Filter B	14
0	0	0	1	1	Filter R	8
0	0	1	0	1	Filter X	8
0	1	1	1	1	Filter GR	1
1	0	0	0	1	Filter GX	1
0	1	1	0	1	Filter KA, KD	2
1	0	0	1	1	Filter Z	6

Filters coefficients must be evaluated using a proper ST simulation software.

4.8 Configuration Registers

As already mentioned, Configuration Registers are set and read by SOP command.

CR1 sets SLIC kit operating features and some test features.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
PD	N/BB	LB	TON	HIA	HIB	DHP	COR

Reset value = 00 h.

PD sets the kit either in Stand By or External Indication/Loop open (for further details please see table 13 pag. 45)

= 0 SLIC kit (STLC3040/HV (L3000N, L3000S, STLC3170)) in External Indication Mode

= 1 SLIC kit (STLC3040/HV (L3000N, L3000S, STLC3170)) in Stand By Mode

N/BB sets COFISLIC Battery Mode

= 0 Normal Battery

= 1 Boosted Battery

LB enables Loop Back functions for on chip test

= 0 normal function (no loop back)

= 1 Loop Back as defined in CR4 register

TON enables 1KHz test tone generator

= 0 Test Tone Generator Off

= 1 Test Tone Generator On

HIA and HIB set tip and ring status in active and standby mode

		Standby		Active	
HIA	**HIB**	**TIP**	**RING**	**TIP**	**RING**
0	0	normal	normal	normal	normal
0	1	normal negative	Hiz	normal negative	Hiz
1	0	Hiz	normal	Hiz	normal
1	1	Hiz	normal	normal	normal

DHP enables High-Pass filter for test purpose

= 0 High Pass filter On

= 1 High Pass filter Off

COR cuts off Receive Path for test purpose

= 0 Receive Path transmission is enabled

= 1 Receive Path is disable

CR2 enables or disables Test Mode, Teletax Signal Shaping Mode and sets the I/O pin direction. The high nibble is only readable and defines test mode results.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
XVA	OKTON	OKTTX	OKRNG	TMN	NOSL	IO1	IO2

Reset value: 00h

XVA Internal measurement results shown in the following three bits are or not valid (read only)

= 0 the following 3 ok-bits are not valid

= 1 the following 3 ok-bits are valid

OKTON Test Tone meaurement information (read only), see test mode 7

= 0 Test tone level out of defined range

= 1 Test tone level in defined range

OKTTX Test teletax metering information (read only), see Test Mode D and E

= 0 Test teletax metering different from the defined value

= 1 Test teletax metering equal to the defined value

OKRNG Test Ring tone information (read only), see Test Mode C

= 0 Ring tone level out of defined range

= 1 Ring tone level within the defined range.

TMN Enables or disables COFISLIC testmodes (see chapter 6)

= 0 stops the assigned tests (normal mode)

= 1 starts the assigned tests selected by Register CR5

NOSL Defines if the shaping of teletax signal is switched On or Off

= 0 Teletax shaping is on

= 1 Hard switch of Teletax signal

IO1 Selection for programmable I/O pin IO1

= 0 sets pin IO1 as input

= 1 sets pin IO1 as output

IO2 Selection for programmable I/O pin IO2

= 0 sets pin IO2 as input

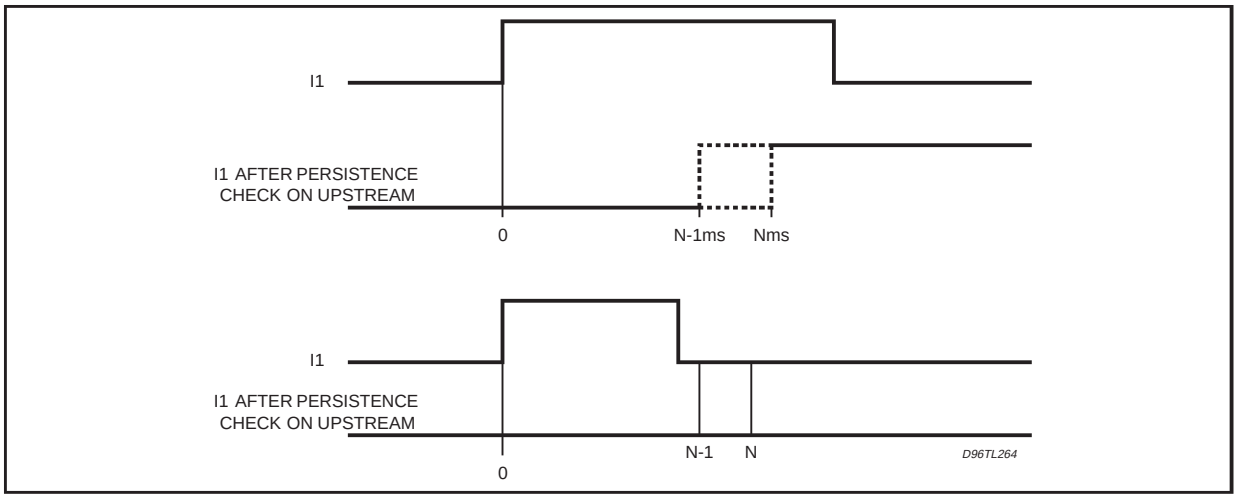
= 1 sets pin IO2 as output

CR3 sets Persistence Check for upstream signalling: Off-Hook and Ground-Key.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DUP3	DUP2	DUP1	DUP0	DUB3	DUB2	DUB1	DUB0

Reset value: A5 h
Persistence Reset value is 10 ms both for Off-Hook and I1 input pin. 20ms for Ground-Key.

Figure 9.



DUP3-DUP0 Persistence check for signalling upstream Off-Hook and I1. New status information will be transmitted upstream, after it has been stable for from (N-1) to N millisecond (see fig. 9). N is programmable in range of 1 to 15 ms in steps of 1 ms. DUP3-DUP0 = 0000 means no persistence check.

DUB3-DUB0 Persistence check for signalling upstream Ground-Key. New status information will be transmitted upstream, after it has been stable for N millisecond. N is programmable in range from 0 to 60 ms in steps of 4 ms. DUB3-DUB0 = 0000 means no persistence check.

CR4 enables internal filters B, Z, X, R, GX/GR. It also programs the Loop Back and sets the codification law: A-law or µ-law.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
B	Z	X	R	GX/GR	LOOP1	LOOP0	A/U

Reset value: F9h

B represents B-filter

= 0 B-filter is Off, Related Transfer Function is zero (HB = 0)

= 1 B-filter is On, Related Transfer Function (HB) is defined by programmed filter coefficients (COP command)

Z represents Z-filter

= 0 Z-filter is Off, Related Transfer Function is zero (HZ = 0)

= 1 Z-filter is On, Related Transfer Function (HZ) is defined by programmed filter coefficients (COP command)

X represents X-filter

= 0 X-filter is Off, Related Transfer Function (HX = 1) is one

= 1 X-filter is On, Related Transfer Function (HX) is defined by programmed filter coefficients (COP command)

R represents R-filter

= 0 R-filter is Off, Related Transfer Function (HR = 1) is one

= 1 R-filter is On, Related Transfer Function (HR) is defined by programmed filter coefficients (COP command)

GX/GR represents GX/GR-filter

= 0 GX/GR-filter is Off, Related Transfer Function (HGX/GR = 1) is one

= 1 GX/GR-filter is On, Related Transfer Function (HGX/GR) is defined by programmed filter coefficients (COP command)

LOOP1-LOOP0 select the loop back (see Block Diagram fig. 3 and paragraph 4.42)

= 00 No loop-Back

= 01 Loop-Back only GCI interface (LB1 on).

= 10 Loop-Back the digital part (Digital Sigma-Delta converter is included, LB2 on).

= 11 Loop-Back the Analog part (Analog Sigma-Delta converter is included, LB3 on).

A/U chooses coding law

= 0 µ-law coding

= 1 A-law coding

CR5 sets ring-trip thresholds and test modes

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
RTV3	RTV2	RTV1	RTV0	TESM3	TESM2	TESM1	TESM0

Reset value: 60h.

RTV3-RTV0 set Ring-Trip Threshold Value. This value is programmable in the range from 9.6/16 mA to 9.6 mA in steps of 9.6/16 mA.

= 0h corresponds to 9.6/16 mA

= Fh corresponds to 9.6 mA

For further details please see parameters I_{RNGGTH} (pag 34)

TESM3-TESM0 select the testmode.

= 0h	No-Test
= 1h	TST-LEAK [CR8.1 = 0, CR5(3:0) = 01h]
= 2h	TST-LKA [CR8.1 = 0, CR5(3:0) = 02h]
= 4h	TST-800Hz
= 5h	TST-TONE-CAL
= 7h	TST-ALB
= 8h	DON'T USED
= 9h	TST-LINE-IMPDC
= Ah	TST-LINE-IMPAC
= Ch	TST-IRING
= Dh	TST-PTTX
= Eh	TST-TTXFILT
= Fh	TST-ILIM

Every test will be described in Chapter 6

CR6 sets current limitation values and off-hook threshold in Active mode.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
ILIM5	ILIM4	ILIM3	ILIM2	ILIM1	ILIM0	ITHR	FIXC

Reset Value: 51h

ILIM5-ILIM0 Set Current Limit in Active mode. Current Limit is programmable in range of 0mA to 69.3mA in steps of 1.1mA.

= 000000 corresponds to 0mA

= 111111 correspondso to 69.3mA

ITHR Defines Off-Hook threshold value in Active mode

= 0 Threshold at 10mA

= 1 Threshold at 13mA

Loop indication is set if a loop current greater than 10mA or 13mA is detected.

FIXC, COFISLIC uses either fixed coefficients or programmed ones.

= 0 Programmed coefficients used

= 1 Fixed coefficients used (see paragraph 4.5.2)

CR7 sets current-limit value and Off-Hook threshold in Stand-By mode.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
PDSV5	PDSV4	PDSV3	PDSV2	PDSV1	PDSV0	PDDIS	RTEN

Reset Value: 1Ch

PDSV5-PDSV0 Set Current Limit and Off-hook threshold in Stand-by mode.
Programmable range is from 0mA to 69.3mA in steps of 1.1mA.

= 0000 corresponds to 0mA

= 1111 corresponds to 69.3mA

At reset the value will be 7.7mA.

PDDIS used for state setting as per table 14 (pag 45)

RTEN enables Ring-trip in test mode TST-IRING

= 0 Ring-trip disabled

= 1 Ring-trip enabled

CR8 sets synthesized feeding resistance, TTX frequencies. The least significant bit sets the ringing source: internal or external.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
RFED2	RFED1	RFED0	TTX12	TTXNO	SOREV	XRNG	TMM

Reset Value: 00h

RFED2-RFED0 Values of the synthesized feeding resistance'.
DC Synthesis Value = $2 \cdot Rp + 2 \cdot 50\Omega \cdot [RFED[2:0] + 1]$

TTX12 selects Teletax frequencies

= 0 16KHz teletax

= 1 12KHz teletax

TTXNO sets Battery Reversal for metering instead of 16/12KHz pulse

=0 Metering with Teletax pulse

=1 Metering with Battery reversal

SOREV selects hard or soft Battery Reversal

= 0 Hard Battery Reversal

= 1 Soft Battery Reversal

XRNG selects ringing source: internal or external

= 0 Internal Ring

= 1 Ring signal from EXT pin

TMM enables sign modulation at 1kHz square wave of measurement carried out during test mode

= 0 No Modulation

= 1 Modulation enabled

CR9 programs Ring frequency and amplitude.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
RVR	RNGF2	RNGF1	RNGF0	RNGV3	RNGV2	RNGV1	RNGV0

Reset Value: 2F h

RVR fixes Ring Voltage Range

= 0 Ring Amplitude = 34.4Vrms + RNGV [3:0] x 2.039Vrms

= 1 Ring Amplitude = 45Vrms + RNGV [3:0] x 2.66Vrms

Reset Value is 65 V_{rms}

RNGF2-RNGF0 select Ring frequency value

= 0h 16.6Hz Ringing Frequency
= 1h 20Hz Ringing Frequency
= 2h 25Hz Ringing Frequency
= 3h 50Hz Ringing Frequency
= 4h 60Hz Ringing Frequency
= 5h Ringing Frequency not used
= 6h Ringing Frequency not used
= 7h Ringing Frequency not used

Ring Reset Value is 25 Hz
RNGV3-RNGV0 fix Ring Voltage programmation step.

CR10 sets Teletax Voltage Level.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
TTXV7	TTXV6	TTXV5	TTXV4	TTXV3	TTXV2	TTXV1	TTXV0

Reset Value: FF h

TTXV7-TTXV0

Teletax Amplitude [V] = TTXV (7:0) · $10V_{rms}/255$. A dc drop (TTXV [7:3] · 15mV · 40)is applied as indicated in electric specification section.

CR11 Bit (7:4) set External-indication threshold

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
ETHR3	ETHR2	ETHR1	ETHR0	STRES3	TXONE	DHPRX	X

RESET value = 10 h

ETHR [3:0] set the External-indication threshold:

for ETHR[3:0] = 0h, threshold = 0V;

for ETHR[3:0] > 0h:

Threshold = 8V + ETHR [3 : 0] · 1V

TXONE and STRES3 must be always programmed to 0

DHPRX = 1 disable the Rx high pass filter

CR12 can mask the effect on SLCX of the six most significant bits of Signalling Register. If a bit is masked it will not affect the SLCX bit of upstream C/I channel. The unmasked SR bits are used to trigger an event-detect circuit and will latch the SR signals into a shadow register whenever an event occurs. An event is defined as a toggling of one or more of the enabled SR bits. Once the interrupt is set and the shadow registers are latched, any further event does not influence the interrupt or the shadow registers.
With the SR TOP READ command, the byte representing the SR will be sent out to the DU depending on the values of the MASK bits. For unmasked SR bit its shadow register bit is sent out; otherwise the value of SR bit is sent out. At the end of the readout of the above byte, the interrupt bit is cleared and two things could happen. If the contents of the shadow register differ from the enabled SR (meaning there was at least one toggle of the enabled SR bits between the time when the interrupt bit is set and the TOP READ command), then the SR byte will be latched into the shadow register while the interrupt bit (SLCX) will remain cleared (low) for 2 frames and then will be set high. On the other hand, if the contents of the shadow-register are equal to the enabled SR, then the interrupt bit remains cleared and will be set only by the next event. At reset, the shadow register content mirrors that of SR register. A mask-bit change causes SR to be latched in the shadow-Register, nevertheless the SCLX bit is cleared

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
HOOK	GNDK	VB_2M	ILIM	TEMP	CLKF	COMRX	COMTX

Reset Value: FFh

HOOK Mask bit for Hook information in the signalling register

= 1 No influence on SLCX bit (Upstream C/I.5)
= 0 Each change of the HOOK bit sets SLCX bit (Upstream C/I.5)

GNDK Mask bit for Ground Key information in the signalling register

= 1 No influence on SLCX bit (Upstream C/I.5)
= 0 Each change of the GNDK bit sets SLCX bit (Upstream C/I.5)

VB_2M Mask bit for half-battery information in the signalling register

= 1 No influence on SLCX bit (Upstream C/I.5)
= 0 Each change of the VB_2 bit sets SLCX bit (Upstream C/I.5)

ILIM Mask bit for current limit information in the signalling register

= 1 No influence on SLCX bit (Upstream C/I.5)
= 0 Each change of current limit bit sets SLCX bit (Upstream C/I.5)

TEMP Mask bit for temperature information in the signalling register

= 1 No influence on SLCX bit (Upstream C/I.5)
= 0 Each change of the temperature bit sets SLCX bit (Upstream C/I.5)

CLKF Mask bit for clock-fail information in the signalling register

= 1 No influence on SLCX bit (Upstream C/I.5)
= 0 Each change of the clock-fail bit sets SLCX bit (Upstream C/I.5)

COMRX = 0 Linear code in Rx is enabled
= 1 PCM in Rx is Enabled

COMTX = 0 Linear code Tx is enabled
= 1 PCM in Tx is enabled

4.9. COFSLIC PROGRAMMING PROCEDURE

SOP - Write Commands

DD	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DU
Address	1	0	0	0	0	0	0	1		Idle								
SOP-Write 0 Byte		0			0	1	0	0		Idle								

DD	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DU
Address	1	0	0	0	0	0	0	1		Idle								
SOP-Write 2 Bytes		0			0	1	0	1		Idle								
CR1	Data									Idle								
CR2	Data									Idle								

DD	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DU
Address	1	0	0	0	0	0	0	1		Idle								
SOP-Write 12 Bytes		0			0	1	1	0		Idle								
CR1	Data									Idle								
:	:									:								
CR12	Data									Idle								

COP - Write Commands

DD	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DU
Address	1	0	0	0	0	0	0	1		Idle								
COP-Write 8 Bytes	X	0	0	0	0	0	1	1		Idle								
Coeff. 1	Data									Idle								
:	:									:								
Coeff. 8	Data									Idle								

SOP - Read Commands

DD	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DU
Address	1	0	0	0	0	0	0	1		Idle								
SOP-Read	X	1	X	X	0	1	0	0		Idle								
	Idle									1	0	0	0	0	0	0	1	Address
	Idle									0	0			0	1	(*) LSEL1	(*) LSEL0	SOPK-1
	Idle																	

DD	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DU
Address	1	0	0	0	0	0	0	1		Idle								
SOP-Read	X	1	X	X	0	1	0	1		Idle								
	Idle									1	0	0	0	0	0	0	1	Address
	Idle													0	1	(*) LSEL1	(*) LSEL0	SOPK-1
	Idle									Data								CR1
	Idle									Data								CR2

DD	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DU
Address	1	0	0	0	0	0	0	1		Idle								
SOP-Read 12 Bytes		1				1	1	0		Idle								
	Idle									1	0	0	0	0	0	0	1	Address
	Idle													0	1	(*) LSEL1	(*) LSEL0	SOPK-1
	Idle									Data								CR1
	:									:								:
	Idle									Data								CR12

(*) LSEL1, LSEL0 of previous SOP processed command, SOPK-1 is former SOP command

TOP - Read Commands

DD	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DU
Address	1	0	0	0	0	0	0	1		Idle								
TOP-Read 1 Byte	X	1	X	X	1	1	0	0		Idle								
	Idle									1	0	0	0	0	0	0	1	Address
	Idle									Data								SR

DD	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DU
Address	1	0	0	0	0	0	0	1		Idle								
TOP-Read 3 Bytes	X	1	X	X	1	1	0	1		Idle								
	Idle									1	0	0	0	0	0	0	1	Address
	Idle									Data								SR
	Idle									Data								CKS1
	Idle									Data								CKS2

DD	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DU
Address	1	0	0	0	0	0	0	1		Idle								
TOP-Read 15 Bytes	X	1	X	X	1	1	1	0		Idle								
	Idle									1	0	0	0	0	0	0	1	Address
	Idle									Data								IDCOD0
	:									:								:
	Idle									Data								IDCOD14

COP - Read Commands

DD	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DU
Address	1	0	0	0	0	0	0	1		Idle								
COP-Read 8 Bytes	X	1	0	0	0	0	1	1		Idle								
	Idle									1	0	0	0	0	0	0	1	Address
	Idle									Data								Coeff. 1
	:									:								:
	Idle									Data								Coeff. 8

5. APPLICATION & EXTERNAL COMPONENTS LIST

Typical COFISLIC application is shown in Fig. 5. It shows the HV (L3000N, L3000S, STLC3170) driving the phone line and interfacing the COFISLIC with the external components summarized in the following table.

Table 11:

Ref	Typ. Value	Function
R_{REF}	37.2kΩ 1%	Bias resistor (I_{ref}) @ V_{DD}
R_{AC}	1620Ω 1%	AC reference impedance
R_{DC}	820Ω 1%	DC reference impedance
C_{AC} (*)	11µF 5V 20%	AC/DC current splitting
DS	BAT 49	Protective Shottky Diode
CAP	100nF	Battery Reversal Capacitor
CDVB	47µF - 20V ±20%	Battery Voltage Rejection

(*) unbiased capacitor

L3000N and L3000S require dotted components (see fig. 5) for Off/Hook detection in "External Indication" (see table 12).

Table 12:

Ref	Typ. Value	Function
RT, RR	33kΩ	Line Feed

6. INTEGRATED TEST FEATURES

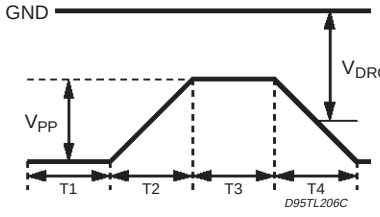
The device has built-in several functionalities dedicated to perform generic testing.
Each test is enabled if CR2.3 (TMN) bit is set to 1.
In each test description more details about active functionalities are written.

6.1.1. LINE TEST MODE 1 (TST-LEAK)

Enabled by CR2.3 = 1 and CR5 (3:0) = 01h and CR8.1 = 0.

A trapezoidal signal (see Fig. 10) is sent to 2-wire line.

Figure 10.



T1=T2=T3=T4=100ms

V_{DROP} = -170mV - 15 CR10[7:3]

$V_{PP} = \frac{25}{40}$ V if CR9.7=0

$V_{PP} = \frac{32.7}{40}$ V if CR9.7=1

$V_{OUT} = (V_{PP} + V_{DROP} + R_X) = \frac{17}{13}$ if CR 9.7 = 1

$V_{OUT} = (V_{PP} + V_{DROP} + R_X) = 1$ if CR 9.7 = 0

If CR1.2 = 0, CR1.3 = 0, line current is measured allowing line resistance and capacitance to be obtained.

If CR1.2 = 1, CR1.3 = 0, TIP wire leakage to ground is measured with RING wire in high impedance.

If CR1.2 = 0, CR1.3 = 1, RING wire leakage to ground is measured with TIP wire in high impedance.

Measured value, available on Tx B1 byte:

$$\frac{I_t}{50} \cdot \left(\frac{R_{DC}}{6} // C_{AC} \right) \cdot \text{Tx GAIN}$$

I_t = transversal line current
R_{DC} = DC reference resistance (typically 820Ω)
CR8.0 = 1 Active Modulation for returned value.

Operating Mode:	Test dedicated, H.V. Active
B filter:	Off
Z filter:	Off
Rx Path:	Functional
Tx Path:	Functional with input connected to RDC resistance.
R, X, GX, GR Filters:	Programmable
KD filter:	Programmable (suggested max value to avoid saturation = 0800h)
DC Synthesis:	Off
TTX:	Not Applicable
Internal Tone Generation in Rx:	Only 1KHz Available
Hook Detection:	As in Active Mode
I_{LIM}	Off
High-Pass Filters:	Controlled by CR1.1
Reverse Polarity	set by SOP register Command
Boosted Battery	set by CR1 register

6.1.2. LINE TEST MODE 2 (TST-LKA)

Enabled by CR2.3 = 1, CR5 [3:0] = 02h and CR8.1 = 0.

The setup is the same of Test 1 except the measured value that is:

$$\frac{I_t}{50} \cdot \frac{R_{DC}}{6} \cdot \text{Tx GAIN}$$

If CR1.2 = 1, CR1.3 = 0, TIP wire leakage to ground is measured with RING wire in high impedance.

If CR1.2 = 0, CR1.3 = 1, RING wire leakage to ground is measured with TIP wire in high impedance.

6.1.4. TEST MODE 4 (TST-800Hz)

The device is in Active mode. An 800Hz tone is injected into the line. The tone amplitude is programmable through TTX voltage register (CR10). 1KHz tone can be added (CR1.4), in this case Rx input is disabled.

6.1.5. TEST MODE 5 (TST-TONE-CAL)

It carries out a tone calibration.
1KHz frequency is sent to backplane (TX direction)
Returned Information on Tx B1 byte:

1KHz Tone at the maximum digital level

Operating Mode:	Active
B filter:	Programmable
Z Synthesis:	Programmable
Rx Path:	Functional
Tx Path:	Off
R, GR Filters:	Gain as per programmed coefficients
DC Synthesis:	On
TTX:	Functional
Internal Tone Generation in Rx:	1KHz available
I_{LIM}:	On
Hook Detection:	As in Active
High Pass Filters:	Controlled by CR1.1 and CR11.1

6.1.6. TEST MODE 7 (TST-ALB)

A 1KHz Tone can be generated in digital section. This Test mode is equivalent to the Active mode. Disabling B filter, the gain of the whole path (Rx + HV (L3000N, L3000S, STLC3170) + external load + Tx) can be measured.

The measurement is carried out by a window detector placed at the input of the PCM encoder.

The window detector compares the negative or positive amplitude peak (it depends on the programmed battery polarity) of the input signal with a range of values.
The range is centred around 6dB below the PCM full scale. Range width is ±0.5dB or ±1.5dB depending on the programmed polarity.

Returned information on upstream GCI channel:

1. $\frac{I_t}{50} \cdot R_{AC} \cdot$ Tx GAIN
2. CR2.6 (OKTON)
3. CR2.7 (XVA) = 1means measurement has settled

CR2.6 = 1 means signal level within the window range.

When this Test mode is on, all the functionalities of Active mode are still available. In addition the window detector is switched on.

6.1.7. TEST MODE 9 (TST-LINE-IMPDC)

In this mode thr Rx channel is functional and its gain is increased by a factor 16 (the same gain is also applied to the 1KHz enabled by CR1.4).

Z, ILIM and DC feed characteristics are disabled.

A drop of roughly 3.9V/step is superimposed to the line under control of CR10 [7:3].

Tx path is fully functional and controllable. Transversal line current (I_t) is measured across the parallel R_{DC}, C_{AC}:

$$\frac{I_t}{50} \cdot \text{Tx GAIN} \cdot \left(\frac{R_{DC}}{6} // C_{AC} \right)$$

Modulated if TMM = 1 in CR8 register.

Operating Mode:	Test Dedicated, H.V. set by downstream C/I
B Filter:	Programmable
Z Filter:	Off
Rx Path:	Functional
Tx Path:	Functional
R, X, GR, Gx:	Programmable
KD:	Programmable (Suggested max. value to avoid saturation = 800h)
DC Synthesis:	Only Programmable Voltage drop
TTX:	Not Applicable
Internal Tone Generation in Rx:	1KHz available
Hook detection:	As in active mode
I_{LIM}	As per programmed value in Active mode
High Pass Filters	Controlled by CR1.1 and CR11.1
Reverse Polarity	Set by SOP register command

6.1.8. TEST MODE A (TST-LINE-IMPAC)

This test follows the same procedure as Test 9 having the sensing done only on R_{DC}.
Measured value:

$$\frac{i_t}{50} \cdot \text{Tx GAIN} \cdot \frac{R_{DC}}{6}$$

6.1.9. TEST MODE C (TST-IRING)

Normal Ring signal (no power reduced mode available) is generated and sent to 2-wire in order to test internal ring generator. Frequency and Amplitude are programmable by CR5 register.

Auto Ring Trip function can be disabled by R_{TEN}

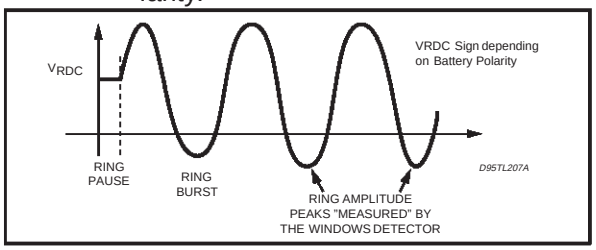
bit (CR7 Register). The Hook state is anyway sent upstream.

Returned Information on upstream GCI channel:

1. $\frac{I_t}{50} \cdot \frac{R_{DC}}{6} \cdot$ Tx GAIN
2. CR2.4 (OKRNG)
   OKRNG = 1 means that ring amplitude is within the accepted range see fig. 11.
3. CR2.7(XVA) = 1 means measurement has settled.

Modulated if TMM = 1 in CR2 Register.

Figure 11: V_{RDC} sign depending on Battery Polarity.



Connecting a known impedance across the line and considering the programmed Ring level (CR9 register), a window detector, as for Test 7, allows to monitor if the signal at PCM encoder input is in the correct range.

Through this procedure the ring functionality including several effects, HV device, protect resistor, battery voltage etc, can be evaluated.

Operating Mode:	Ring
B Filter:	Off
Z Filter:	Off
Rx Path:	Off
Tx Path:	Functional
X, Gx:	Programmable
KD:	Programmable (Suggested max value to avoid saturation = 800h)
DC Synthesis:	Off
TTX:	Not applicable
Internal Tone Generation in Rx:	Not applicable
Hook detection	As in Ring Mode
I_{LIM}:	Off
High Pass Filters:	Controlled by CR1.1 and CR11.1

6.1.10. TEST MODE D (TST-PTTX)

800Hz tone is sent to 2-wire. This pseudo TTX signal (800Hz) requires C/I.5 bit (TIM) set to 0. Shaping functions are disabled. The internal window detector is enabled as for Test Mode 7.
Measured line current gives information about amplitude of generated pseudo TTX and consequently about the functionalities of TTX generation circuitry. 800Hz frequency is used instead of standard 12KHz/16KHz, because 12KHz or 16KHz would be cut out by filters in Tx path.
Returned Information on TXB1 channel:

$$\frac{I_t}{50} \cdot R_{AC} \cdot G_{TX}$$

Operating Mode:	Active
B filter:	Programmable
Z filter:	Programmable
Rx Path:	Functional
Tx Path:	Functional
R, X, GR, Gx:	Programmable
KD:	Programmable (suggested max value to avoid saturation = 800h
DC Synthesis:	Functional
TTX:	800Hz with programmable amplitude
Internal Tone Generation in Rx:	1KHz Available
Hook detection:	As in active
I_{Lim}:	Functional
High Pass Filters:	Controlled by CR1.1 and CR11.1

6.1.11. TEST MODE E (TST-TTXFILT)

Purpose of this test is to check the functionality of the TTX filter.
A TTX signal at 12kHz or 16kHz superimposed to a 1KHz tone, enabled by CR1.4, is sent to the line.
Returned Information on upstream GCI channel:

1. $\frac{I_t}{50} \cdot R_{AC} \cdot$ Tx GAIN
2. CR2.5 (OKTTX)
3. CR2.6 (OKTON)
4. CR2.7(XVA) = 1 means measurement has settled.

OKTTX says that programmed TTX level has been caught up.
OKTON set to 1 indicates that 1kHz tone has not been compressed by the superimposed TTX signal. In this case the TTX filter properly works.

Operating Mode:	Active
B Filter:	Programmable
Z Filter:	Programmable
Tx Path:	Functional
Rx Path:	Functional
R, X, GR, GX	Programmable
KD:	Programmable (suggested max value to avoid saturation = 800h

DC Synthesis:	Functional
TTX:	ON with programmable amplitude and frequency.
Internal Tone Generation in Rx	1KHz available
Hook detection	As in Active Mode
I_{LIM}	Functional
High Pass Filter	Controlled by CR1.1 and CR11.1

6.1.12. TEST MODE F (TST-DC LOOP)

Purpose of this test is to check if DC characteristics (R_{FEED} and I_{LIM}) synthesis works correctly.

A trapezoidal signal (see Fig. 10) is sent to the 2-wire line.

Returned information on Tx B1 byte:

$$\frac{I_t}{50} \cdot \left(\frac{R_{DC} // C_{AC}}{6} \right) \cdot \text{Tx GAIN}$$

Operating Mode:	Test Dedicated, H.V. Active
B Filter:	Off
Z Filter:	Off
Tx Path:	Functional
Rx Path:	Functional with input connected to R_{DC} resistance.
R, X, GR, Gx	Programmable
KD:	Programmable (Suggested max value to avoid saturation = 800h)
DC Synthesis:	Functional
TTX:	Not applicable
Internal Tone Generation in Rx:	1kHz available
Hook detection:	As in Active Mode
I_{LIM}:	Functional
High Pass Filters:	Controlled by CR1.1 and CR11.1
Reverse Polarity:	Set by SOP register command Boosted Battery

ABSOLUTE MAXIMUM RATINGS (*)

Symbol	Parameter	Test condition	Min.	Max.	Unit
V_{dd}	Positive Digital Supply Voltage Referred to DGND		-0.3	+5.5	V
V_{CC}	Positive Analog Supply Voltage Referred to AGND		-0.3	+5.5	V
V_{EE}	Negative Analog Supply Voltage Referred to AGND		-5.5	+0.3	V
AGND to DGND	Difference AGND to DGND		-0.3	+0.3	V
V_{CC} to V_{DD}	Difference V_{CC} to V_{DD}		-0.3	+0.3	V
I_{LTH}	DC input and output current at any input or output pin (free from latch-up)			100	mA
T_j	Maximum Junction Temperature		150		°C
T_{stg}	Storage Temperature Range		-55	+150	°C
V_{IGCI}	Voltage Referred to DGND	Input GCI pins 3, 4, 5, 40, 41, 42 and 43	-0.3	V_{DD} +0.3	V
V_{OGCI}		Output GCI pin 6	-0.3	VDD +0.3	V
V_{THVI}	Voltage Referred to AGND	Interface to H.V. pins: 9, 10	V_{EE} -0.3	V_{CC} +0.3	V
I_{PDN}	Input Current	Interface to H.V. pin: 28	-0.5	0.5	mA
V_{LINT}	Voltage Referred to AGND	Interface to line pins: 11,12	-80	80	V
V_{CHVI}		Interface to H.V. Current Input pins: 15, 19	V_{EE} -0.3	V_{CC} +0.3	V
V_{BHVI}		Voltage Reference Input pin: 25	V_{EE} -0.3	V_{CC} +0.3	V
V_{2WI}	Voltage Referred to AGND	Ouput Buffer pin: 26	V_{EE} -0.3	V_{CC} +0.3	V
V_{DIO}	Voltage Referred to DGND	I/O pins: 7, 8, 38, 39	-0.3	V_{DD} +0.3	V
V_{MIS}		Ring Sync pins: 29, 36	-0.3	V_{DD} +0.3	V
V_{DUN}		Reserved pins: 37, 44	-0.3	V_{DD} +0.3	V
V_{TID}	Voltage Referred to AGND	Identification Code pins:31, 32	V_{EE} -0.3	V_{CC} +0.3	V
V_{BID}		Identification Code pin: 35	-0.3	V_{CC} +0.3	V
V_{CREV}		Battery Reversal capacitor input pin: 14	V_{EE} -0.3	+0.3	V
V_{ACDC}		AC and DC - synthesis Reference Resistor pins 16, 22	-3	+3	V
		AC/DC line split pin: 20	V_{EE} -0.3	V_{CC} +0.3	V
		AC splitter capacitor pin: 21	-0.3	+0.3	V
V_{OREF}		Reference Voltage output pin: 23	-0.3	V_{CC} +0.3	V
V_{AUN}		Reserved pins: 13, 17, 18, 24, 30	-0.3	V_{CC} +0.3	V

(*) Stresses in excess of those listed under "Absolute Maximum Rate" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied.

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to Ambient Max.	60	°C/W

OPERATING RANGE

Symbol	Parameter	Value	Unit
V_{DD}	Positive Digital Supply Voltage Referred to DGND	4.75 to 5.25	V
V_{CC}	Positive Analog Supply Voltage Referred to AGND	4.75 to 5.25	V
V_{EE}	Negative Analog Supply Voltage Referred to AGND	-4.75 to -5.25	V
DGND to AGND	Difference AGND to DGND	0	V
T_{op}	Ambient Operating Temperature	-40 to +85	°C

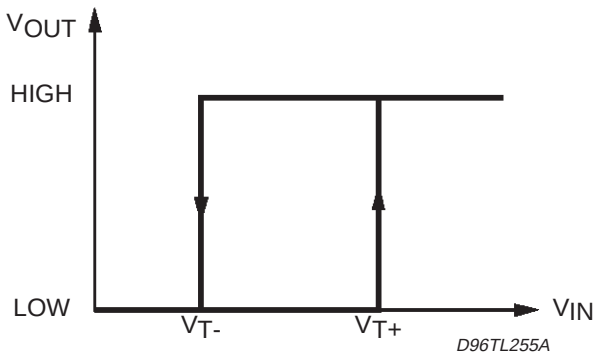
DIGITAL INTERFACE ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70°C, V_{DD} = V_{CC} = 5V ±5%, V_{EE} = -5V ±5%, AGND = DGND = 0V; for operating in ext. temp. range -40° +85°C the same limits are confirmed by characterisation data unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Notes
V_{il}	Input Voltage at Logical "0"	Pins 29,35,36,38,40,41,42,43.	0		1.5	V	
		Pins 7, 8 [when inputs]	0		1.5	V	
V_{ih}	Input Voltage at Logical "I"	Pins 29,35,36,38,40,41,42,43	V_{DD}-1.5			V	
		Pins 7, 8 [when inputs]	V_{DD}-1.5			V	
I_i	Input Current	0V < V_{in} < V_{DD}	-1		1	µA	1
V_{ol}	Output Voltage at Logical "0"	Pin 7, 8 (when outputs), 39 I_{OI} = 4mA			0.45	V	
V_{oh}	Output Voltage at logical "I"	Pin 7, 8 (when outputs), 39 I_{Oh} = -3mA	V_{DD}-0.45			V	
V_{T+}	Positive going Threshold	pins: 3, 4, 5			3.15	V	2
V_{T-}	Negative going Threshold		1.35			V	2
V_H	Threshold Hysteresis		0.5			V	
V_{OLOD}	Output Voltage at Logical "0"on open drain output	pin: 6, I_O = 7.5mA			0.45	V	
V_{hv1}, V_{hv2}	Output Voltage at High Level on pins 9, 10	pin 10: I_O = 10µA pin 9: 10µA ≤ I_O ≤ 300µA	2		5	V	
V_{mv1}, V_{mv2}	Output Voltage at Zero Level on pins 9, 10	pin 10: I_O = 10µA pin 9: 10µA ≤ I_O ≤ 300µA	-1		1	V	
V_{lv1}, V_{lv2}	Output Voltage at Low Level on pins 9, 10	pin 10: I_O = 10µA pin 9: 10µA ≤ I_O ≤ 300µA	-5		-2	V	
V_{ihID}	Ternary input pins 31, 32 High level		2		V_{CC}	V	
V_{ilID}	Ternary input pins 31, 32 Low level		V_{EE}		-2	V	
V_{imID}	Ternary input pins 31, 32 medium level		-1		1	V	

(1) for all the digital inputs: TTL, CMOS, 3-Levels, with Hysteresis. Except pins 18, 24, 30, 44, 43, which have internally 22KΩ pull-down.

(2) see figure 12.

Figure 12.



SUPPLY CURRENTS: see Table 13 with coefficient and configuration register contents set as per default values after reset; T_{amb} = 0 to 70°C, V_{DD} = V_{CC} = 5V ±5%, V_{EE} = -5V ±5%, AGND = DGND = 0V. Typical values are measured at T_{amb} = 25°C, V_{DD} = V_{CC} = 5V, V_{EE} = -5V ; for operating in ext. temp. range -40° +85°C the same limits are confirmed by characterisation data unless otherwise specified.

	VOLTAGE SUPPLY		
OPERATING MODES	V_{DD}	V_{CC}	V_{EE}
ACTIVE	I_{DDACT} Min Typ 8mA Max 13mA	I_{CCACT} Min Typ Max 23mA	I_{EEACT} Min Typ Max 23mA
POWER DENIAL	I_{DDPDEN} Min Typ Max 3mA	I_{CCPDEN} Min Typ Max 5mA	I_{EEPDEN} Min Typ Max 2mA
RING	I_{DDRNG} Min Typ Max 13mA	I_{CCRNG} Min Typ Max 23mA	I_{EERNG} Min Typ Max 23mA
STAND-BY	I_{DDSTB} Min Typ Max 7mA	I_{CCSTB} Min Typ Max 13mA	I_{EESTB} Min Typ Max 10mA

DC ELECTRICAL CHARACTERISTICS OF ANALOG PINS

(T_{amb} = 0 to 70°C, V_{DD} = V_{CC} = 5V±5%, V_{EE} = -5V ±5%, AGND = DGND = 0V; for operating in ext. temp. range -40° +85°C the same limits are confirmed by characterisation data unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$IPDO_{HiZ}$	Leakage Current at pin 28 in High impedance	V_{PDO} = +1.0V	-1		1	µA
$IPDO_{LOZ}$	Sinked Current at pin 28 in low impedance	VPDO = +1.0V	45		55	µA
VPDO	Operating Voltage at pin 28		0		5	V
VL1, VL2	Operating Voltage at pin 11, 12		-70		+70	V
I_{tmax}	Absolute Value of Input Current at pin 19				2.6	mA
I_{lmax}	Absolute Value of Input Current at pin 15				2.6	mA
V_{BIM}	Battery Image Voltage		-3.5		0	V
V_{OUT}	2-wire Ouput Voltage		-3.3		3.3	V
Z_{VOUT}	2-wire Output Impedance			200		Ω
I_{VOUT}	2-wire Output Current		-1		1	mA
RAC, CAP, ACDC,CAC, RDC, REF	see External Component List					

DC ELECTRICAL CHARACTERISTICS OF ANALOG PINS

(T_{amb} = 0 to 70°C, V_{DD} = V_{CC} = 5V±5%, V_{EE} = -5V ±5%, AGND = DGND = 0V; for operating in ext. temp. range -40° +85°C the same limits are confirmed by characterisation data unless otherwise specified)

Active Mode (see Table 13)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Notes
$VOUT_{DROP}$	Operation Dropout Voltage on pin 26	It = 0 DD (pin 5): Idle CR1.6 (N/BB) = 0	V_{OUT1} -30	V_{OUT1}	V_{OUT1} +30	mV	1
	Operation Dropout Voltage on pin 26	It = 0 DD (pin 5): Idle CR1.6 (N/BB) = 1	-725	-685	-645	mV	
RFEED	DC feeding resistance on pin 26	It < Ilim/50 DD (pin 5): Idle CR1.6 (N/BB) = X	RFEED1 -10%	RFEED1	RFEED1 +10%	Ω	2

DC ELECTRICAL CHARACTERISTICS OF ANALOG PINS (continued)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit	Notes
RFEEDL	DC feeding resistance in limited current pin 26	It ≥ Ilim/50 DD (pin 5): Idle CR1.6 (N/BB) = X		15			kΩ	
ILIM/50	Programmable Limitation current on pin 19	CR1.6 (N/BB) = 0		-10%	IL1	+10%	mA	3
		CR1.6 (N/BB) = 1 It < 1mA		-10%	IL1	+10%	mA	3
$I_{POFF-HK}$	Programmable off-hook threshold for positive transition on pin 19	CR6.1 (ITHR) = 0 SOP.5 (POL) = X	0 < T_{amb} < 70°C -40 < T_{amb} < +85°C	180 175	200 195	220 220	µA µA	
		CR6.1 (ITHR) = 1 SOP.5 (POL) = X	0 < T_{amb} < 70°C -40 < T_{amb} < +85°C	234 225	260 255	286 286	µA µA	
$I_{NOFF-HK}$	Programmable off-hook threshold for negative transition on pin 19	CR6.1 (ITHR) = 0 SOP.5 (POL) = X	0 < T_{amb} < 70°C -40 < T_{amb} < +85°C	160 155			µA µA	
		CR6.1 (ITHR) = 1 SOP.5 (POL) = X	0 < T_{amb} < 70°C -40 < T_{amb} < +85°C	214 205			µA µA	
$OFFHK_{PERS}$	Off-hook persistency check	CR6.1 (ITHR) = X			N_H		ms	4
I_{PGNDK}	Ground-key bit current threshold for positive transition on pin15	SOP.5 (POL) = X		|140|		|240|	µA	
I_{NGND}	Ground-key threshold for negative transition			|120|			µA	
$GNDK_{PERS}$	Ground-key persistence check				N_G		ms	5
I_{thv}	Current drained for thermal overload from pin9	SR.3 (TEMP) = 0				180	µA	
		SR.3 (TEMP) = 1		320		800	µA	
H_{ITHV}	Thermal overload hysteresis				20		µA	
VB/2	Voltage on pin25 to toggle the SR.5 bit (VB_2)	See test conditions 8 C/I.6 (conv) = 1 SOP.5 (POL) = 0		V_{BIMT} -20%	V_{BIMT}	VBIMT +20%	V	
$SR_{BITPERS}$	Limiting current, thermal overload, half battery bit persistence			5.5		8.5	ms	

Stand-By Mode (see Table 13)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Notes
$V_{ODROPSBY}$	Stand-by Dropout Voltage on pin 26	It = 0µA	-85	-70	-55	mV	
$RFEED_{SBY}$	DC feeding resistance on pin 26	It < Ilim/50	-10%	RFEED1	+10%	Ω	2
RFEEDL	Stand-by DC feeding resistance in limited current pin 26	It ≥ Ilim/50	15			kΩ	
$ILIM/50_{SBY}$	Programmable limitation current in stand-by on pin 19		-10%	ILSBY	+10%	µA	6
$I_{OFF-HKSBY}$	Stand-by programmable off-hook threshold on pin 19		-10%	ILSBY	+10%	µA	6
$OHK_{SBYPERS}$	Stand-by off-hook persistence check			N_H		ms	4
$I_{SBYGNDK}$	Stand-by ground-key bit current threshold for positive transition on pin 15		|140|		|240|	µA	
$GND_{SBYPERS}$	Stand-by ground-key persistence check			N_G		ms	5
I_{SBYthv}	Current drained for thermal overload from pin 9 in stand-by	SR.3 (TEMP) = 0			180	µA	
		SR.3 (TEMP) = 1	320		800	µA	
$SR_{SBYBITPERS}$	Limiting current, thermal overload, half battery bit persistence in stand-by		5.5		8.5	ms	

DC ELECTRICAL CHARACTERISTICS (continued)

Ring Mode (Downstream C/I.7 [RING] = 1 see Table 13)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Notes
$V_{ODROPRNG}$	Ring mode Dropout Voltage on pin 26 Ring On	Downstream C/I.5 (TIM) = 1 & C/I.6 (CONV) = X	-20		20	mV	
	Ring mode Dropout Voltage on pin 26 Reduced Power Ring Pause	Downstream C/I.5 (TIM) = 0 & C/I.6 (CONV) = 0	-85	-70	-55	mV	
	Ring mode Dropout Voltage on pin 26 Ring Pause	Downstream C/I.5 (TIM) = 0 & C/I.6 (CONV) = 1	-20		20	mV	
$RFEED_{RNG}$	Ring mode DC feeding resistance on pin 26	Downstream C/I.5 (TIM) = 0 & C/I.6 (CONV) = 1 It < Ilim/50	-10%	0	+10%	Ω	2
$RFEEL_{RNG}$	Ring DC feeding resistance in limited current on pin 26	It ≥ Ilim/50	15			kΩ	
$ILIM/50_{RNG}$	Programmable limitation current on pin 19 in reduced power ring pause	Downstream C/I.5 (TIM) = 0 & C/I.6 (CONV) = 0	-10%	ILSBY	+10%	µA	6
OHK_{RNGPER}	Ring mode off-hook persistence check			N_H		ms	4
GND_{RNGPER}	Ring mode ground-key persistence check			N_G		ms	5
I_{SBYthv}	Current drained for thermal overload from pin 9 in ring mode	SR.3 (TEMP) = 0 Downsteam C/I.5 (TIM) = 0 & C/I.6 (CONV) = 0			180	µA	
		SR.3 (TEMP) = 1 Downsteam C/I.5 (TIM) = 0 & C/I.6 (CONV) = 0	320		800	µA	
$SR_{RNGBITPER}$	Limiting current, thermal overload, half battery bit persistence in ring mode		5.5		8.5	ms	
I_{RNGGTH}	Ring trip off-hook current threshold on pin 19	Downstream C/I.5 (TIM) = 1 & C/I.6 (CONV) = X OR Downsteam C/I.5 (TIM) = 0 & C/I.6 (CONV) = 1	-10%	THR	+10%	µA	7
		Downsteam C/I.5 (TIM) = 0 & C/I.6 (CONV) = 0	-10%	ILSBY	+10%	µA	6
$I_{RNGGNDKTH}$	Ring ground-key bit current threshold for positive transition on pin15	Downsteam C/I.5 (TIM) = X & C/I.6 (CONV) = X	|140|		|240|	µA	

Power Denial Mode (Downstream C/I.[7,5] [RING, CONV, TIM] = 0, CR1.7 [PD] 0, see Table 13.

$DV_{OFFHKPD}$	Power denial differential voltage off-hook threshold		-15%		+15%		
$CV_{OFFHKPD}$	Power denial threshold voltage off-hook common mode range		-60		+60	V	
OHK_{PERSPD}	Off-hook persistence check in power denial mode	CR6.1 (ITHR) = X		N_H		ms	4

Notes:
(1) VOUT1 = -(170mV + CR10[7..3] · 15mV)
(2) RFEED1 = (RDC/6.56) · (1+CR8 · [7..5])
(3) IL1 = (CR6[7..2] · 1.1mA)/50
(4) NH = CR3 [7..4] · 1ms
(5) NG = CR3 [3..0] · 4ms
(6) ILSBY = (CR7 [7..2] · 1.1mA)/50
(7) THR = {(1 + CR5[7..4]) · 9.6mA/16}/50

AC ELECTRICAL CHARACTERISTICS OF ANALOG PINS

T_{amb} = 0 to 70°C, V_{DD} = V_{CC} = 5V±5%, V_{EE} = -5V ±5%, AGND = DGND = 0V (see Table 13); for operating in ext. temp. range -40° +85°C the same limits are confirmed by characterisation data unless otherwise specified.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G_X	Absolute gain in T_X	see fig. 13 Normal temp. range Extended temp. range	-0.2 -0.4		0.2 0.4	dB dB
G_R	Absolute gain in R_X	see fig. 13 Normal temp. range Extended temp. range	-0.2 -0.4		0.2 0.4	dB dB
THD_X	Total harmonic distortion in T_X	see fig. 13; f_{ref} = 1kHz; reference signal level 0dBm0 @ digital side; measurements of 2nd and 3rd order harmonics			-48	dB
THD_R	Total harmonic distortion in R_X				-48	dB
G_{FTX}	Gain Variation with frequency in T_X	fref = 1kHz; reference signal level @ digital side; -10dBm0		see fig.12		
G_{FRX}	Gain Variation with frequency in R_X			see fig.12		
G_{LTX}	Gain Variation with level in T_X	Sinusoidal Test Method; f_{ref} = 1kHz; reference signal level @ digital side; -10dBm0		see fig.13		
G_{LRX}	Gain Variation with level in Rx			see fig.13		
S/N_{TX}	Signal to noise ratio in T_X	Sinusoidal Test Method; f_{ref} = 1kHz;		see fig.14		
S/N_{RX}	Signal to noise ratio in Rx					
N_{TP}	Idle channel noise in transmit	see test cond. 1 Teletax enabled with Downstream C/I.5 (TIM) = 0; A-Law $0 < T_{amb} < 70°C$ $-40 < T_{amb} < +85°C$		 -73 -71	 -67	 dBmp dBmp
N_{RP}	Idle channel noise in receive	Teletax enabled with Downstream C/I.5 (TIM) = 0; A-Law			12	μV_p
N_{TTX-TP}	Idle channel noise in receive with metering pulse on output	see test cond. 1 Teletax enabled with Downstream C/I.5 (TIM) = 1; A-Law			12	μV_p
SOS_{RX}	Spurious out of band signals at analog output	see test cond. 2, Sinusoidal test method			-31	dB
SOS_{TX}	Spurious out of band signals at digital output				-25	dB
Thl	Cofislic Transhybrid loss	see test cond. 3	40			dB
Arl	Return loss	see test cond. 4	25			dB
$PSRR_{P2W}$	Positive power supply rejection ratio on 2-wire	V_{RIPPLE} = 100mV, 300Hz ≤ f ≤ 3400Hz, on V_{CC} Residual measured on V_{OUT} (pin 26) see test cond. 5			-56	dB
$PSRR_{PGCI}$	Positive power supply rejection ratio on data-up GCI	V_{RIPPLE} = 100mV, 300Hz ≤ f ≤ 3400Hz, on V_{CC} Residual measured on 5GCI data-up DU (pin 6) see test cond. 5			-30	dB
$PSRR_{N2W}$	Negative power supply rejection ratio on 2-wire	V_{RIPPLE} = 100mV, 300Hz ≤ f ≤ 3400Hz, on V_{EE} Residual measured on V_{OUT} (pin 26) see test cond. 5			-56	dB
$PSRR_{NGCI}$	Negative power supply rejection ratio on data-up GCI	V_{RIPPLE} = 100mV, 300Hz ≤ f ≤ 3400Hz, on V_{EE} Residual measured on GCI data-up DU (pin 6) see test cond. 5			-30	dB

AC ELECTRICAL CHARACTERISTICS OF ANALOG PINS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{2WRNG}	Ring amplitude at 2-wire output V_{OUT} (pin 26)	see test cond. 6	-5%	$2W_{RNG}$	+5%	Vrms
THD_{RNG}	Total harmonic distortion in Ring mode	see test cond. 6			2%	
V_{TTX}	2-wire amplitude at V_{OUT} (pin 26) during teletax emission	see test cond. 7	-5%	$2W_{TTX}$	+5%	Vrms
THD_{TTX}	Total harmonic distortion during teletax emission	see test cond. 7			2%	

ABSOLUTE GAIN Rx/Tx (law A)

CR[1] = 00 CR[7] = 1C
CR[2] = 00 CR[8] = 08
CR[3] = 00 CR[9] = 2F
CR[4] = F9 CR[10] = 00
CR[5] = 60 CR[11] = 10
CR[6] = 50 CR[12] = 03

GR = FFh (255)
GX = FFh (255)
K = 1000h (4096)

R | 1000h (4096) |
| 0h (0) |
| 0h (0) |
| 0h (0) |

X | 1000h (4096) |
| 0h (0) |
| 0h (0) |
| 0h (0) |

B[1..8] = 0
Z[1..3] = 0
Reference frequency = 1kHz

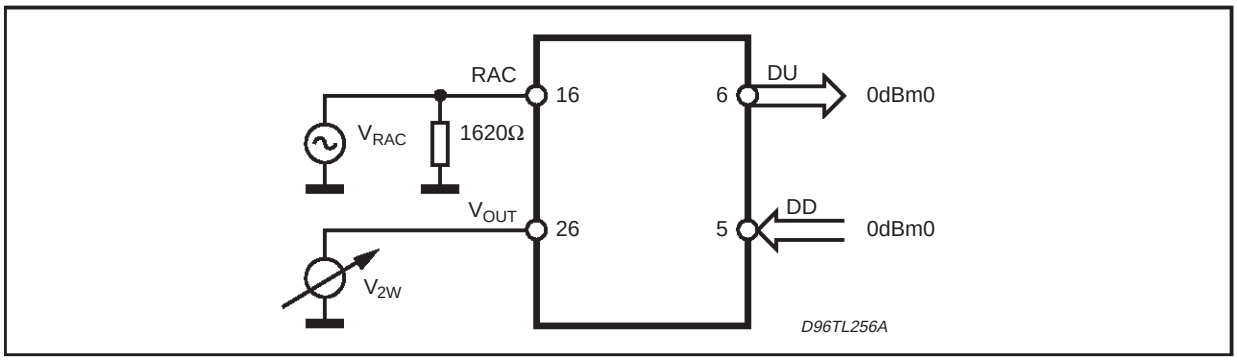
target Vout represents the rms level to be measured at Vout starting from a DD Vpcm (dBm0) code with a certain set of coefficient.
target Vout = (mVrms) = (2 · 1.514 · 2) · [10^ ((Vpcm - 3.14)/20)]/16 · (0.98 (R[1]/8192) · (GR/256)/(2 · sqr (2)))

Example if DD Vpcm = 0dBm0 target Vout = 45.5mVrms (0dBm0/COFISLIC)
absolute gain = 20 · log (Vout / target Vout)

target DU represents the dBm0 level expected on DU with a certain set of coefficient and a Vrac of 41.4Vrms
VRac_ref is the amplitude of the sine wave (1kHz) to be applied on RAC (pin 16) in order to expect on DU a Vpcm dBm0 level with the same set of coefficient.
target DU (dBm0) = 3.14 + 20 · Log((0.0414 · 3 · (2 · sqr(2)) / 1.514) · 16 · (K/8192) · (X[1]/8192) · (GX/256) · 0.966)
VRac_ref = (41.4mV · 10^ ((Vpcm - target DU)/20)

Example if target DU = 0dBm0 then VRac_ref = 32.3mVrms (A_law)
absolute gain = dBm0 level on DU (full scale 3.14dBm0 A_law)

Figure 13.



FREQUENCY RESPONSE Rx/Tx

CR[1] = 00	CR[7] = 1C
CR[2] = 00	CR[8] = 08
CR[3] = 00	CR[9] = 2F
CR[4] = F9	CR[10] = 00
CR[5] = 60	CR[11] = 10
CR[6] = 5C	CR[12] = 03
GR = 79h	(121)
GX = 80h	(128)
K = 1000h	(4096)

R	| 1DBCh	(7612) |
	| 1AE6h	(6886) |
	| 24B8h	(-6984)|
	| 8CCh	(2252) |
X	| 3CFChh	(-772) |
	| 3F41h	(-191) |
	| 1476h	(5238) |
	| 1449h	(5193) |

Z[1..3] = 0
B[1..8] = 0
Reference frequency = 1kHz

Multitone on DD (pin 5) total level = -10dBm0

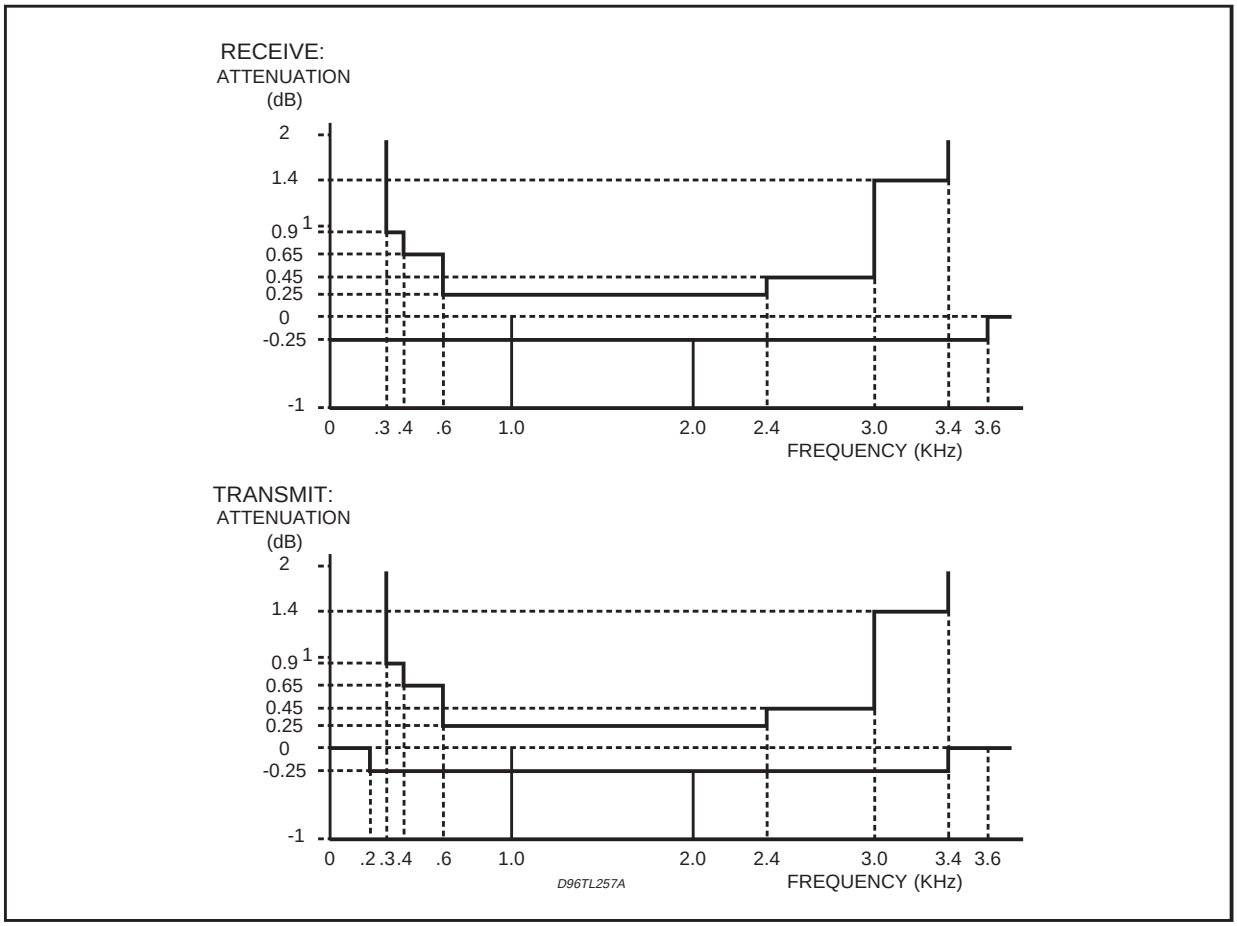
Multitone on VRac (pin 16) total amplitude about 24mVp

freq.resp. Rx = 20 · log(V2w fx / V2w 1kHz)

freq.resp. Tx = dBm0 level at fx - dBm0 level at 1kHz

where 300Hz < fx < 3.400kHz

Figure 14.



GAIN TRACKING Rx/Tx

CR[1] = 00	CR[7] = 1C
CR[2] = 00	CR[8] = 08
CR[3] = 00	CR[9] = 2F
CR[4] = F9	CR[10] = 00
CR[5] = 60	CR[11] = 10
CR[6] = 50	CR[12] = 03
GR = FFh	(255)
GX = FFh	(255)
K = 1000h	(4096)

R	| 1000h	(4096) |
	| 0h	(0) |
	| 0h	(0) |
	| 0h	(0) |
X	| 1000h	(4096) |
	| 0h	(0) |
	| 0h	(0) |
	| 0h	(0) |

B[1..8] = 0

Z[1..3] = 0

Reference frequency = 1kHz

Reference level on DD = -10dBm0 (or expected value at Vout, pin 26, in the range of 14.39mVrms)

Voutref = voltage on Vout with DDref = -10dBm0

Voutmes = voltage on Vout with -55dBm0 < DDmes < 3dBm0

Rx gain tracking = 20 · log (Vout mes / Voutref) - (DDmes - DDref)

Tx gain tracking = starting from the same consideration of the absolute gain.

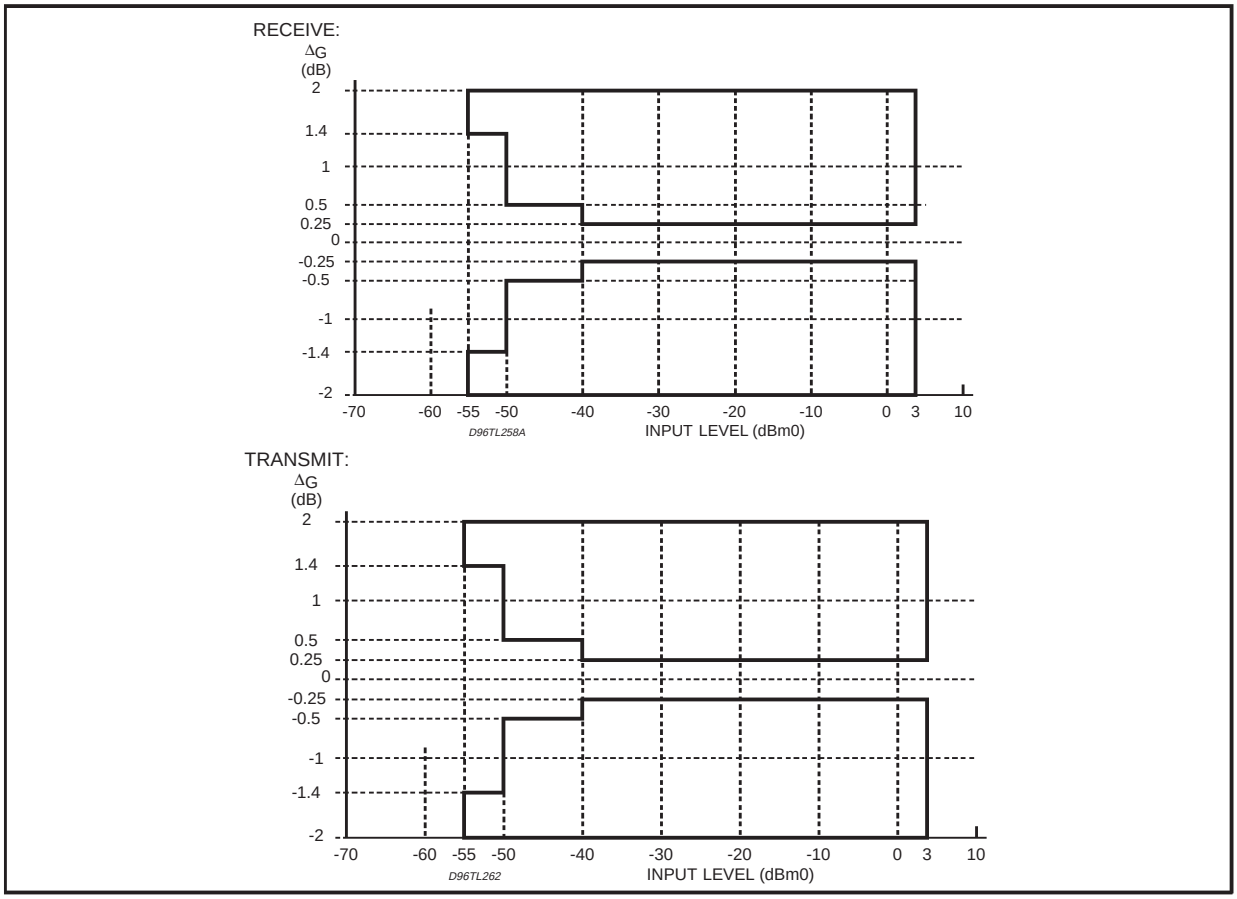
target DU represents the dBm0 level expected on DU with a certain set of coefficient and a Vrac of 41.4Vrms
VRac_ref is the amplitude of the sine wave (1kHz) to be applied on RAC (pin 16) in order to expect on DU a Vpcm dBm0 level with the same set of coefficient.
target DU (dBm0) = 3.14 + 20 · ((0.0414 · 3 · (2 · sqr(2)) / 1.514) · 16 · (K/8192) · (X[1]/8192) · (GX/256) · 0.966)
VRac_ref = 41.4mV · 10^ ((Vpcm - target DU)/20)

DUref = dBm0 level at DU with (target DU) ref = -10dBm0

DUmes = dBm0 level at DU with -55dBm0 < (target DU) mes < 3dBm0

Tx gain tracking = (DUmes - DUref) - ((target DU)mes - (target DU)ref)

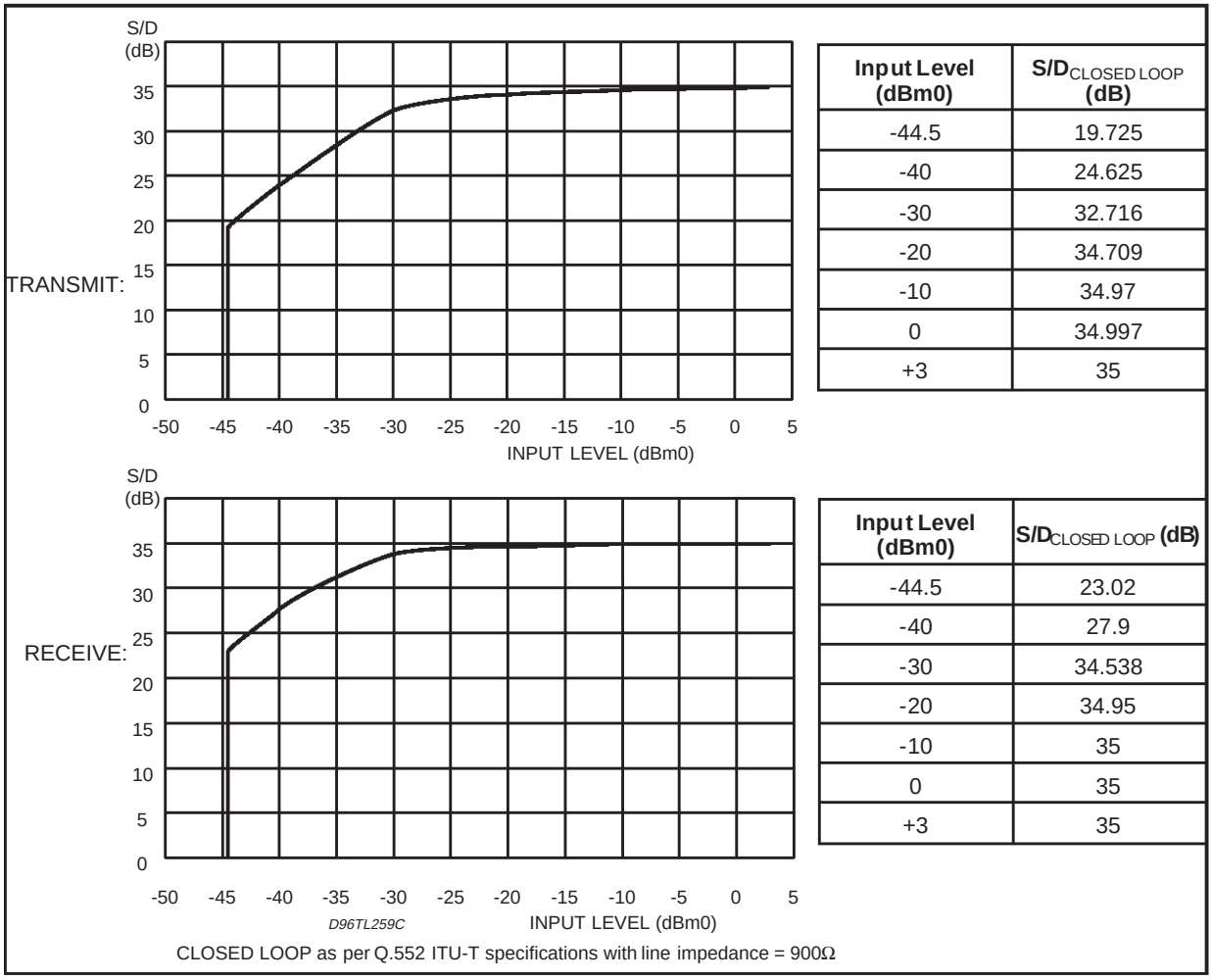
Figure 15. (Valid for 0 < T_{amb} < 70°C)



SIGNAL TO NOISE RATIO

Use the same Test Configuration of Gain Tracking Test.

Figure 16. (Valid for 0 < T_{amb} < 70°C)

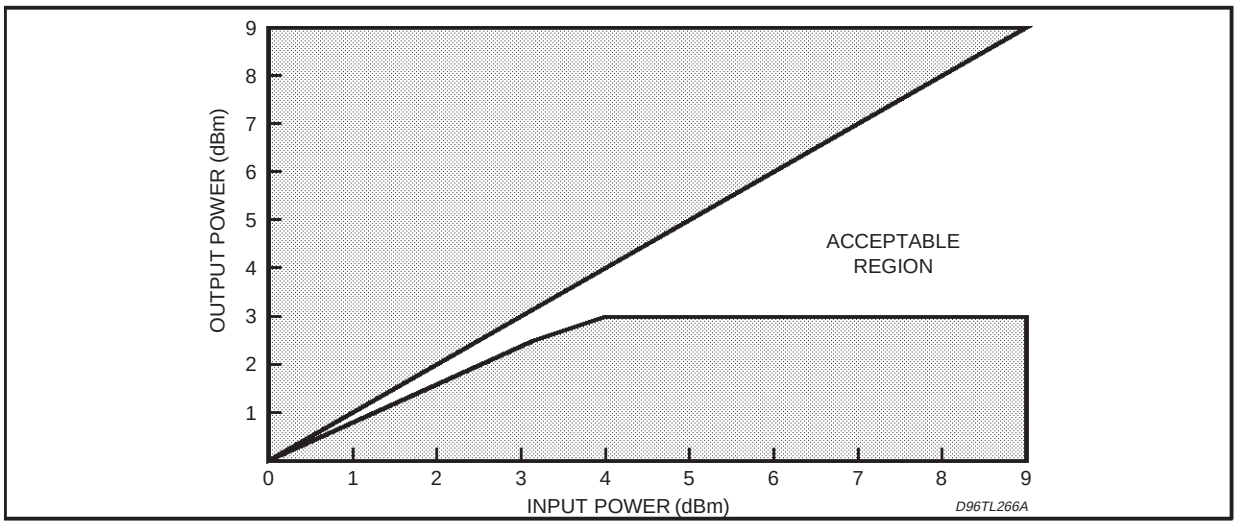


Input Level (dBm0)	$S/D_{CLOSED\ LOOP}$ (dB)
-44.5	19.725
-40	24.625
-30	32.716
-20	34.709
-10	34.97
0	34.997
+3	35

Input Level (dBm0)	$S/D_{CLOSED\ LOOP}$ (dB)
-44.5	23.02
-40	27.9
-30	34.538
-20	34.95
-10	35
0	35
+3	35

CLOSED LOOP as per Q.552 ITU-T specifications with line impedance = 900Ω

Figure 17: Overload Compression (Transmit: measured with sine wave f = 984Hz).



IDLE_CHANNEL NOISE Rx/Tx (TTX off) (Test Cond. 1)

CR[1] = 00	CR[7] = 1C
CR[2] = 00	CR[8] = 08
CR[3] = 05	CR[9] = 2F
CR[4] = F9	CR[10] = 00
CR[5] = 60	CR[11] = 10
CR[6] = 50	CR[12] = FF
GR = FFh	(255)
GX = B4h	(180)
K = 05A0h	(1440)

R	09CDh	(2509)
	042Dh	(1069)
	0919h	(2329)
	39BBh	(-1605)
X	178Dh	(6029)
	0E31h	(3633)
	2922h	(-5854)
	0CCFh	(3279)
Z	39D3h	(-1581)
	0859h	(2137)
	21EDh	(-7699)
B	000Dh	(13)
	3F0Eh	(-242)
	00AB	(171)
	039Eh	(926)
	0483h	(1155)
	044Fh	(1103)
	03AB	(939)
	3C00h	(-1024)

DD = idle code (A_law)

Id_ch_noise at Tx = dBm0 level at DU

Id_ch_noise at Rx = voltage (rms) at Vout (µVrms) (psophometric weighted)

OUT OF BAND NOISE (Test Cond. 2)

CR[1] = 00	CR[7] = 1C
CR[2] = 00	CR[8] = 08
CR[3] = A5	CR[9] = 2F
CR[4] = F9	CR[10] = 00
CR[5] = 60	CR[11] = 10
CR[6] = 50	CR[12] = FF
GR = FFh	(255)
GX = FFh	(255)
K = 05A0h	(1440)

R	1000h	(4096)
	0h	(0)
	0h	(0)
	0h	(0)
X	1000h	(4096)
	0h	(0)
	0h	(0)
	0h	(0)
Z	39D3h	(-1581)
	0859h	(2137)
	21EDh	(-7699)

B[1..8] = 0

Z[1..3] = 0

Out of band signal at Analog output (Rx)

DD 5 frequencies between 2.8 and 3.8kHz + single frequency at 1kHz, the total amplitude is 0dBm0 (in this condition the expected value on 2W at 1kHz is about 23mVrms)

OBN on Vout = $\frac{V_{out} @ (32KHz \pm 5freq.)}{V_{out} @ 1kHz}$

OBN (out of band noise) min 31dB

Out of band signal at Digital output (Tx)

VRAC = 5 frequencies between 32kHz – 3.8kHz and 32kHz - 2.8kHz + single frequency at 1kHz.
The total amplitude to be applied on VRAC (pin 16) is calculated applying the same law of the absolute gain. $V_{RACpicco}$ = 133mV.

OBN on Tx = dBm0 level at 1kHz - dBm0 level at each frequency reflected in band.

OBN (out of band noise) min 25dB.

ECHO CANCELLING (Test Cond. 3)

CR[1] = 20 *)	CR[7] = 1C
CR[2] = 00	CR[8] = 08
CR[3] = A5	CR[9] = 2F
CR[4] = FD	CR[10] = 00
CR[5] = 60	CR[11] = 10
CR[6] = 50	CR[12] = FF

GR = FFh	(255)
GX = FFh	(255)
K = 0100h	(256)

R	1FFFh	(8191)
	0h	(0)
	0h	(0)
	0h	(0)
X	1FFFh	(8191)
	0h	(0)
	0h	(0)
	0h	(0)
Z	0800h	(2048)
	3000h	(-4096)
	1000h	(4096)
B	3FE0h	(-32)
	0h	(0)
	14h	(20)
	34h	(52)
	22Ch	(556)
	4h	(4)
	8h	(8)
	3FE0h	(-32)

*) CR[1] = 20h means digital loop-back 2 on.

DD = tone at 1kHz and -5dBm0

measured_result = (tone level on DD) - (tone level onDU)

RETURN LOSS (Test Cond. 4)

CR[1] = 00	CR[7] = 1C
CR[2] = 00	CR[8] = 08
CR[3] = A5	CR[9] = 2F
CR[4] = F9	CR[10] = 00
CR[5] = 60	CR[11] = 10
CR[6] = 60	CR[12] = FF

GR = 0
GX = 0
K = 05A0 (1440)

R[1..4] = 0
X[1..4] = 0

Z	39D3h	(-1581)
	0859h	(2137)
	1E13h	(7699)

B[1..8] = 0

multitone applied on RAC of amplitude 100mVp and measure performed on Vout

COFISLIC return loss	$\left\lvert \frac{F(s) - F(m)}{F(s) + F(m)} \right\rvert$

where F(s) is the ideal transfer function (RAC/Vout) from simulation

F(m) is the measured transfer function

P.S.R.R. from VEE and VCC (Test Cond. 5)

CR[1] = 00	CR[7] = 1C
CR[2] = 00	CR[8] = 08
CR[3] = A5	CR[9] = 2F
CR[4] = F9	CR[10] = 00
CR[5] = 60	CR[11] = 10
CR[6] = 50	CR[12] = FF

GR = FFh (255)
GX = B4h (180)
K = 05A0h (1440)

R	09CDh	(2509)
	042Dh	(1069)
	0919h	(2329)
	39BBh	(-1605)
X	178Dh	(6029)
	0E31h	(3633)
	2922h	(-5854)
	0CCFh	(3279)
Z	39D3h	(-1581)
	0859h	(2137)
	21EDh	(-7699)
B	Dh	(13)
	3F0Eh	(-242)
	00ABh	(171)
	039Eh	(926)
	0483h	(1155)
	044Fh	(1103)
	03ABh	(939)
	3C00h	(-1024)

DD = idle code

Stimulus applied on VEE and VCC separately as a multitone (5 tone) of amplitude 100mVp

PSRR on Rx (Vout)
= 20 · log (Vout at each tone / amplitude of the same tone applied on VEE or VCC)

if referred to TIP/RING wire
= above measure - 20log(20)
(20 is due to the effect of closed loop)

PSRR on Tx (DU)

considering as dBm0 reference level an amplitude of 0.775Vrms
= 20 · log ((0.775 · 10^ (dBm0 level at each tone / 20)) / amplitude of the same tone applied on VEE or VCC)

RING FUNCTIONALITY (Test Cond. 6)

f ring = 50Hz = CR9 [6..4]
2 W_{RNG} = as volt on = $((CR9[3..0] \cdot \frac{2.039\,Vrms + 34.4}{Vrms})/40)/\sqrt{1 + (fring/200Hz)^2}$

I_{HOOK_RING} = {(1+CR5 [7..4]) · 9.6mA/16}/50

RVR if 1 Vring on TIP/RING = Vring · 17/13

CR[1] = 80	CR[7] = 1C
CR[2] = 03	CR[8] = 08
CR[3] = 20	CR[9] = Ring f/V
CR[4] = F9	CR[10] = FF
CR[5] = I prog	CR[11] = 10
CR[6] = FC	CR[12] = FF

GR = GX = 40h (64)
K = 06A1h (1697)
Z = [1..3] = 0
B = [1..8] = 0

R	1000h	(4096)
	0h	(0)
	0h	(0)
	0h	(0)
X	1000h	(4096)
	0h	(0)
	0h	(0)
	0h	(0)

Ring ON

$2W_{RNG}$ (reported on TIP/RING wire) = (Vout pk · 40) / sqr (2)

Ring PAUSE

$2W_{RNG}$ = V2wpk

TELETAX (Test Cond. 7)

$2W_{TTX}$ amplitude on Vout = (10Vrms · (CR10[7..0] / 255))/40

TTx offset = CR10 [7..3] · 15mV + X

where X depends on normal or boosted battery

CR[1] = 01h	CR[7] = 1Ch
CR[2] = 00h	CR[8] = 10h
CR[3] = A5h	CR[9] = 2Fh
CR[4] = F9h	CR[10] = 32h
CR[5] = 60h	CR[11] = 10h
CR[6] = 50h	CR[12] = FFh
GR = FFh	(255)
GX = B4h	(180)
K = 05A0h	(1440)

R	| 09CDh	(2509) |
	| 042Dh	(1069) |
	| 0919h	(2329) |
	| 39BBh	(-1605)|
X	| 178Dh	(6029) |
	| 0E31h	(3633) |
	| 2922h	(-5854) |
	| 0CCFh	(3279) |

HALF BATTERY DETECTION (Test Cond. 8)

CR[1] = 00h	CR[7] = FCh
CR[2] = 03h	CR[8] = 08h
CR[3] = 00h	CR[9] = 2Fh
CR[4] = F9h	CR[10] = 00h
CR[5] = 60h	CR[11] = 10h
CR[6] = FEh	CR[12] = DFh
GR = 40h	(64)
GX = 40h	(64)
K = 06A1h	(1697)

Z = [1..3] = 0h (0)

B = [1..8] = 0h (0)

R	| 1000h	(4096) |
	| 0h	(0) |
	| 0h	(0) |
	| 0h	(0) |
X	| 1000h	(4096) |
	| 0h	(0) |
	| 0h	(0) |
	| 0h	(0) |

chip status: conversation normal polarity

Z	| 39D3h	(-1581) |
	| 0859h	(2137) |
	| 21EDh	(-7699) |
B	| 000Dh	(13) |
	| 3F0Eh	(-242) |
	| 00AB	(171) |
	| 039Eh	(926) |
	| 0483h	(1155) |
	| 044Fh	(1103) |
	| 03AB	(939) |
	| 3C00h	(-1024) |

TTx amplitude on TIP/RING wire = Vout TTX · 40

TTx Offset = Vout dc level

measurement of 2nd/3rd harmonic noise (psoph. weighted on Vout)

target V_{BIM} (V_{BIMT}) represents the voltage to supply the V_{BIM} (Pin 25) to toggle the SR.5 bit (VB_2)

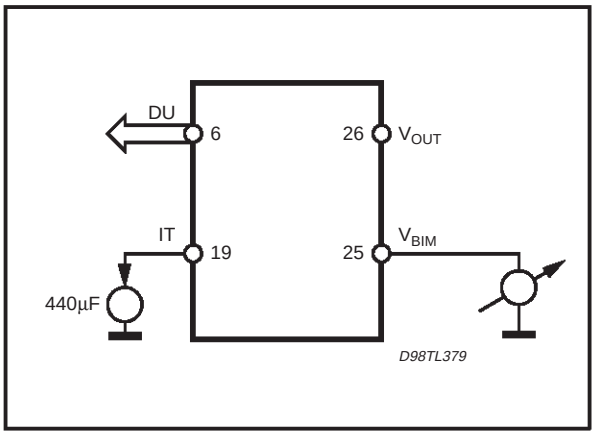
target V_{BIM} =

$$= 2\left(\frac{drop}{2} + I_T \cdot R_{DC} \cdot 0.288 + I_T \cdot R_{DC}\frac{(CR8\,[7.5]+1)\cdot 125\Omega}{R_{DC}}\right)$$

Where:
I_T = -440µA
drop = V_{OUT} for I_T = 0
R_{DC} = 820Ω

If STLC3040 is in kit with HV (L3000N, L3000S, STLC3170) the SR.5 bit (VB_2) toggles when $|V_{LINE}| > |V_{OL} / 2|$ see 4.7.1.1 paragraph.

Figure 18.



GROUP DELAY
Guaranteed by design

Group Delay absolute values: Signal level 0dBm0

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
D_{XA}	Transmit delay	f = 1.5kHz			300	µs
D_{RA}	Receive delay	f = 1.5kHz			250	µs

Figure 19: Group Delay Distortion receive and transmit: Signal level 0dBm0, f_{TEST} @ T_{Gmin}

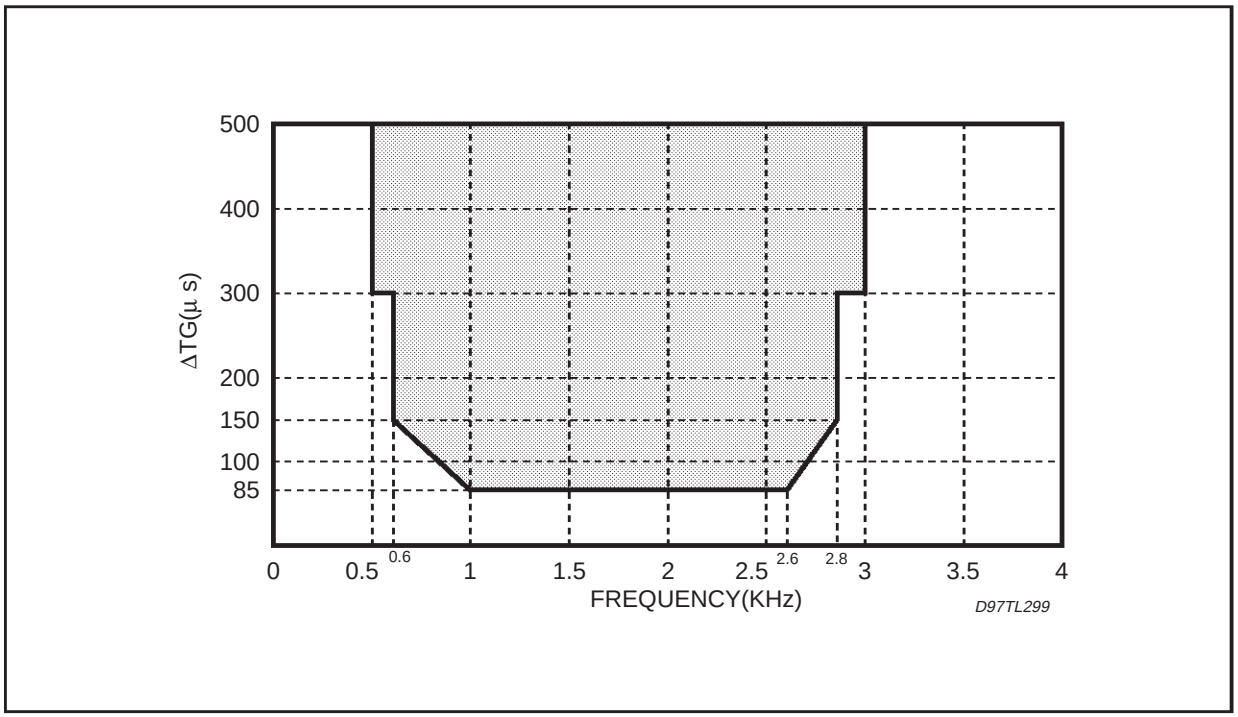


Table 13: Complete list of mode control bits.

Mode name for SLIC Kit	CI.7	CI.6	CI.5	CR1.7	CR1.3 | CR1.2	CR8.3	CR0.5	CR1.6	CR7.1	C/I · Hook	Mode LV Part	Mode HV Part	6V Interface PDN C1 C2
Ext. Ind.	0	0	0	0	X | X	X	X	X	X	X	Poweden	PoweDen + 2 · 15k	Hiz not Vlv Vlv
Stand-by	0 0 0	0 0 0	0 0 0	1 1 1	0 | 0 0 | 0 0 | 0	X X X	X X X	X X X	1 0 0	X 0 1	StdBy StdBy StdBy	StdBy StdBy Acts.	LoZ Vhv Vhv LoZ Vhv Vhv LoZ Vhv Vmv
Ground Start	0	0	0	1	1 | 1	X	X	X	X	X	StdBy	HiA	LoZ Vmv Vhv
Loop open	0	0	1	X	X | X	X	X	X	X	X	PowDen	PowDen	HiZ Vlv Vlv
Conv. N.P.	0	1	0	X	0 | 0 or 1 | 1	X	0	0	X	X	Act.	Act.	LoZ Vhv Vmv
Conv. R.P.	0	1	0	X	0 | 0 or 1 | 1	X	1	0	X	X	Act.	Act. + RP	LoZ Vhv Vlv
Boost N.P.	0	1	0	X	0 | 0 or 1 | 1	X	0	1	X	X	Act.	Boost	LoZ Vmv Vmv
Boost R.P.	0	1	0	X	0 | 0 or 1 | 1	X	1	1	X	X	Act.	Boost+RP	LoZ Vmv Vlv
Conv. NP+ TTx 12kHz/16kHz	0	1	1	X	0 | 0 or 1 | 1	0	0	0	X	X	Act. + OF	Act.	LoZ Vhv Vmv
Conv. NP+ TTx Reversal	0	1	1	X	0 | 0 or 1 | 1	1	0	0	X	X	Act.	Act. + RP	LoZ Vhv Vlv
Conv. RP+ TTx 12kHz/16kHz	0	1	1	X	0 | 0 or 1 | 1	0	1	0	X	X	Act. + OF	Act. + RP	LoZ Vhv Vlv
Conv. RP+ TTx Reversal	0	1	1	X	0 | 0 or 1 | 1	1	1	0	X	X	Act.	Act.	LoZ Vhv Vmv
Boost NP + TTx 12kHz/16kHz	0	1	1	X	0 | 0 or 1 | 1	0	0	1	X	X	Act. + OF	Boost	LoZ Vmv Vmv
Boost NP + TTx Reversal	0	1	1	X	0 | 0 or 1 | 1	1	0	1	X	X	Act.	Boost + RP	LoZ Vmv Vlv
Boost RP + TTx 12kHz/16kHz	0	1	1	X	0 | 0 or 1 | 1	0	1	1	X	X	Act. + OF	Boost + RP	LoZ Vmv Vlv
Boost RP + TTx Reversal	0	1	1	X	0 | 0 or 1 | 1	1	1	1	X	X	Act.	Boost	LoZ Vmv Vmv
Ring. Pause red. Power	1 1 1	0 0 0	0 0 0	X X X	0 | 0 or 1 | 1 0 | 0 or 1 | 1 0 | 0 or 1 | 1	X X X	X X X	X X X	1 0 0	X 0 1	StdBy StdBy StdBy	StdBy StdBy Act.	LoZ Vhv Vhv LoZ Vhv Vhv LoZ Vhv Vmv
Ring red Pow	1	0	1	X	0 | 0 or 1 | 1	X	0	X	X	0	Ring+RB	Ring	LoZ Vlv Vmv
Ring red Pow + Reversal	1	0	1	X	0 | 0 or 1 | 1	X	1	X	X	0	Ring+RB	Ring +RP	LoZ Vlv Vlv
Stand-By	1 1	0 0	1 1	X X	0 | 0 or 1 | 1 0 | 0 or 1 | 1	X X	X X	X X	1 0	1 1	StdBy StdBy	StdBy Act.	LoZ Vhv Vhv LoZ Vhv Vmv
Ring Pause	1	1	0	X	0 | 0 or 1 | 1	X	0	X	X	X	Ring	Ring	LoZ Vlv Vmv
Ring Pause + Reversal	1	1	0	X	0 | 0 or 1 | 1	X	1	X	X	X	Ring	Ring +RP	LoZ Vlv Vlv
Ringing	1 1	1 1	1 1	X X	0 | 0 or 1 | 1 0 | 0 or 1 | 1	X X	0 0	X X	X X	0 1	Ring+RB Ring	Ring Ring	LoZ Vlv Vmv LoZ Vlv Vmv
Ringing + RP	1 1	1 1	1 1	X X	0 | 0 or 1 | 1 0 | 0 or 1 | 1	X X	1 1	X X	X X	0 1	Ring+RB Ring	Ring +RP Ring +RP	LoZ Vlv Vlv LoZ Vlv Vlv
HiA	0 1 0 0 1 1	0 0 1 1 1 X	0 0 0 1 0 1	1 X X X X X	1 | 0 1 | 0 1 | 0 1 | 0 1 | 0 1 | 0	X X X X X X	X X X X X X	X X X X X X	X X X X X X	X X X X X X	StdBy StdBy Act. Act. +OF Ring Ring+RB	HiA HiA HiA HiA HiA HiA	LoZ Vmv Vhv LoZ Vmv Vhv LoZ Vmv Vhv LoZ Vmv Vhv LoZ Vmv Vhv LoZ Vmv Vhv
HiB	0 1 0 0 1 1	0 0 1 1 1 X	0 0 0 1 0 1	1 X X X X X	0 | 1 0 | 1 0 | 1 0 | 1 0 | 1 0 | 1	X X X X X X	X X X X X X	X X X X X X	X X X X X X	X X X X X X	StdBy StdBy Act. Act. +OF Ring Ring+RB	HiB HiB HiB HiB HiB HiB	LoZ Vlv Vhv LoZ Vlv Vhv LoZ Vlv Vhv LoZ Vlv Vhv LoZ Vlv Vhv LoZ Vlv Vhv

'0 | 1': at the Bits HiA and HiB means HiA = 0 and HiB = 1.

'+RB': Additional ring burst on.

'+OF': Additional out of band frequency.

'X': don't care means any combination is valid in this mode.

'+RP': Additional DC voltage in A/B wire reversed.

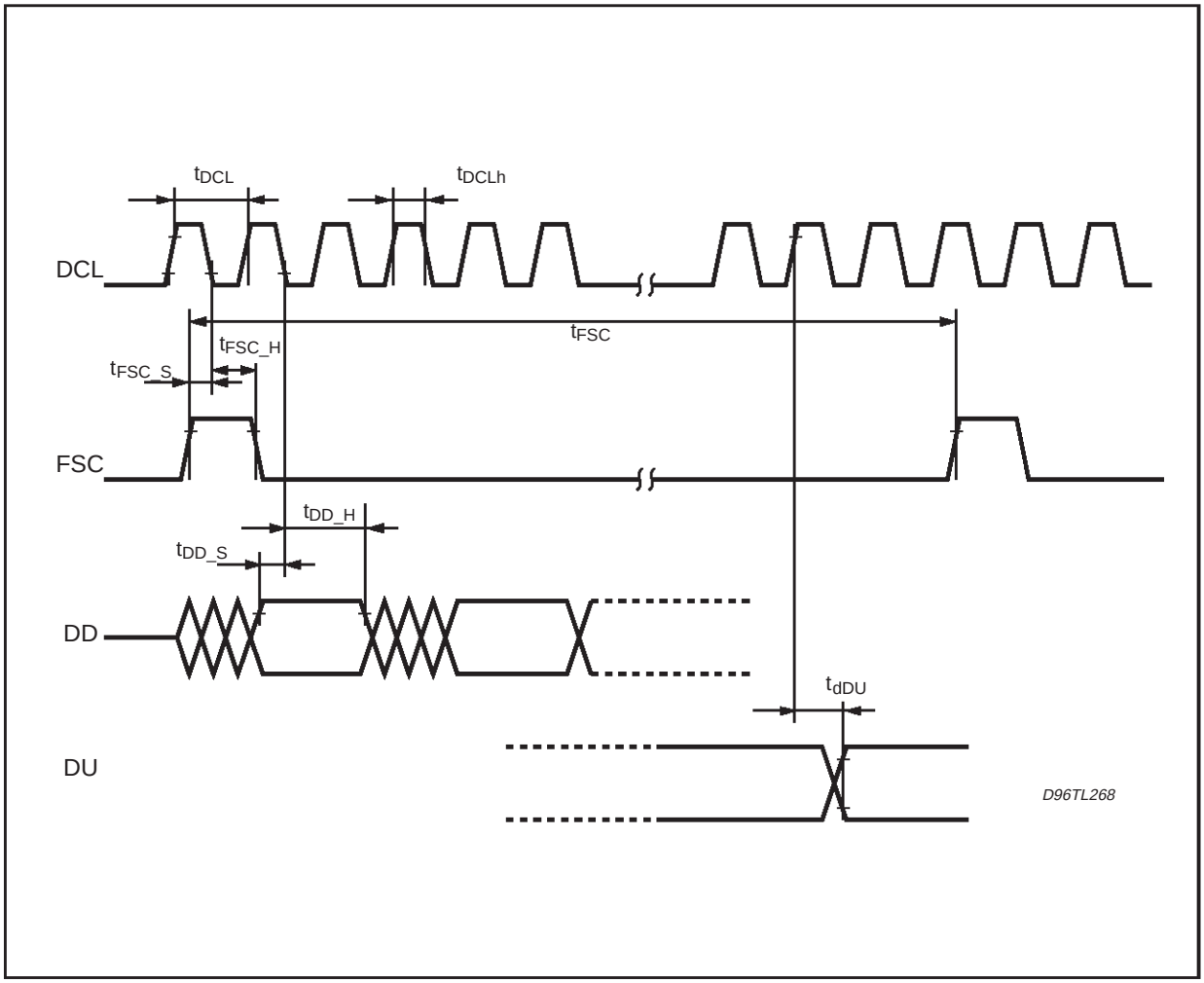
'+BB': Feeding with additional +Vbatt.

'LoZ': The PDN output (LW Part) pin has low impedance to ground.

'HiZ': The PDN output Pin (LV partl has high impedance or +5V to ground).

TIMING OF GCI INTERFACE

Figure 20: DCL, FSC, DU and DD Characteristics.



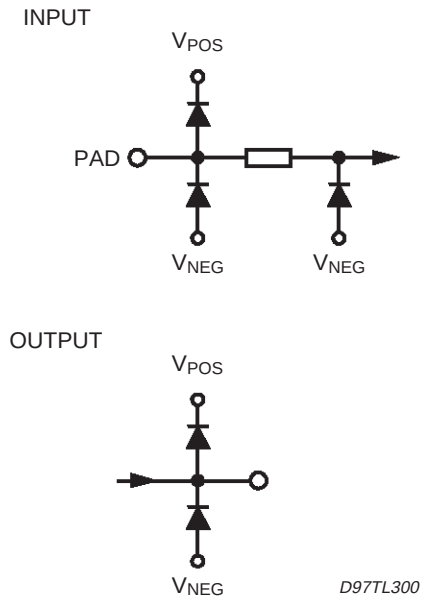
Switching characteristics

Symbol	Parameter	Limit Values			Units
		min.	typ.	max.	
t_{DCL}	Period DCL 'slow' mode (*)		1/2048kHz		
t_{DCL}	Period DCL 'fast' mode (**)		1/4096kHz		
	DCL Duty Cycle	40		60	%
t_{FSC}	Period FSC		125		µs
$t_{FSC\ S}$	FSC set-up time	70	t_{DCLh}		ns
$t_{FSC\ H}$	FSC hold time	40			ns
$t_{DD\ S}$	DD data in set-up time	20			ns
$t_{DD\ H}$	DD data in hold time	50			ns
t_{dDU}	DU data out delay		150 (***)	250	ns

(*) DCL = 2048KHz: $t_{FSC} = 256 * t_{DCL}$
(**) DCL = 4096KHz: $t_{FSC} = 512 * t_{DCL}$
(***) Depending on Pull up resistor (typical 1....10kΩ)

APPENDIX 1
Internal Protections of digital pins.

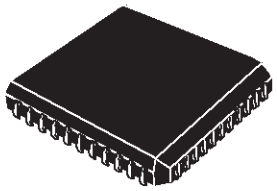
Figure A1.



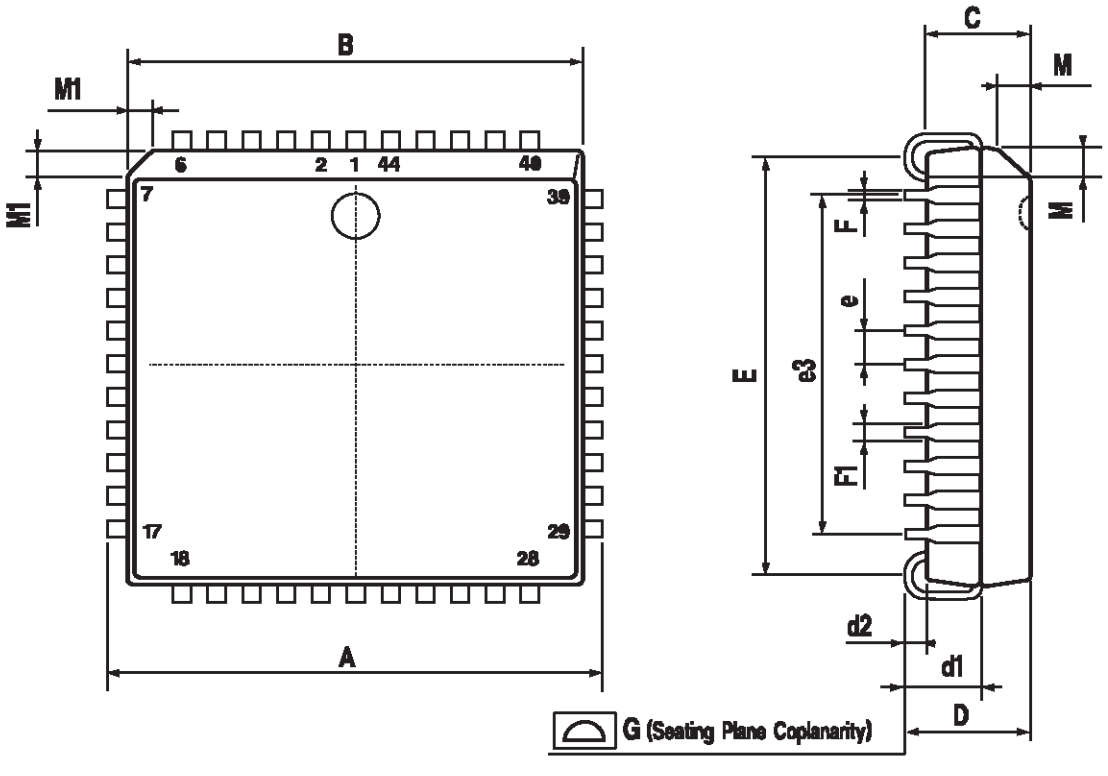
V_{POS} = V_{CC} or V_{DD}
V_{NEG} = DGND or AGND or V_{EE}

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	17.4		17.65	0.685		0.695
B	16.51		16.65	0.650		0.656
C	3.65		3.7	0.144		0.146
D	4.2		4.57	0.165		0.180
d1	2.59		2.74	0.102		0.108
d2		0.68			0.027	
E	14.99		16	0.590		0.630
e		1.27			0.050	
e3		12.7			0.500	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.16			0.046	
M1		1.14			0.045	

OUTLINE AND MECHANICAL DATA



PLCC44



ESD - The STMicroelectronics Internal Quality Standards set a target of 2 KV that each pin of the device should withstand in a series of tests based on the Human Body Model (MIL-STD 883 Method 3015): with C = 100pF; R = 1500Ω and performing 3 pulses for each pin versus V_{CC} and GND.

Device characterization showed that, in front of the STMicroelectronics Internaly Quality Standards, all pins, of STLC3040 except H.V ones (11, 12), withstand at least 1.5kV. H.V. pins n. 11, 12 withstand up to 350V due to their specific functionality.

The above points are not expected to represent a pratical limit for the correct device utilization nor for its reliability in the field. Nonetheless they must be mentioned in connection with the applicability of the different SURE 6 requirements to STLC3040.