Ordering number : EN*5041A

CMOS LSI

LC11011-141

Computer Image Signal Processing Full-Color Gray-Scale Processor

Preliminaly

Overview

The LC11011-141 is a pseudo gray scale processor for TFT LCD. It allows LCD panels with inputs of three to six bits per RGB to display the equivalent of 16.7 million colors.

Features

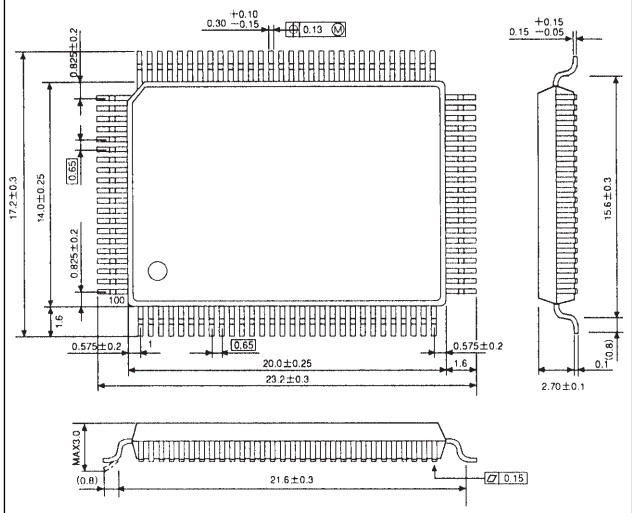
- Handles 8-bits of input data (256-scale data) for each of the RGB colors.
- Operating mode selection of three, four, or six bit driver outputs
- Realizes reduced resolution loss (as compared to dithering techniques) by using intra- and inter-frame error diffusion processing.
- Supports both 5 V and low voltage (3.3 V) operation.
- Operates with arbitrary clock frequencies up to 50 MHz (at 5 V) or up to 30 MHz (at 3.3 V).
- Can operate independently of the number of displayed pixels since internal operation is controlled by the horizontal and vertical synchronization signals.

Package Dimensions

unit: mm

3151-QFP100E

[LC11011-141]



SANYO: QFP100E

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		–0.3 to +7.0	V
Input and output voltages	V_I, V_O		–0.3 to V_{DD} + 0.3	V
Operating temperature	Topr		0 to +70	°C
Storage temperature	Tstg		–40 to +125	°C

Electrical Characteristics: At an operating voltage of 5.0 V

Operating Ranges at Ta = 0 to +70°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Input voltage	V_{IN}		0		V_{DD}	V
Clock frequency	f_{clk}				50	MHz

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DC Characteristics at Ta = 0 to +70°C, V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
High level input voltage	V_{IH}	CMOS level	0.7 V_{DD}			V
Low level input voltage	V_{IL}	CMOS level			0.3 V_{DD}	V
High level output voltage	V_{OH}	I_{OH} (–4 mA)	2.4			V
Low level output voltage	V_{OL}	I_{OL} (4 mA)			0.4	V
Supply current	I_{CC}	*		40	70	mA

Note: * The test conditions are: f_{CP} = 25.175 MHz, V_{DD} = 5.0 V, C_L = 15 pF (measured with VGA timing)

Switching Characteristics at Ta = 0 to +70°C, V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, C_L = 15 pF

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Dot clock cycle time	Tdclk		20			ns
Hsync low level pulse width	Thpw		2 Tdclk			ns
Vsync low level pulse width	Tvpw		2 Tdclk			ns
Data setup time	Tdsu		5			ns
Data hold time	Tdhd		5			ns
Control signal setup time	Tcsu		5			ns
Control signal hold time	Tchd		5			ns
CLK propagation delay time	Ttdhh		2	3	6	ns
CLK propagation delay time	Ttdll		2	4	7	ns
CLKB propagation delay time	Ttdhl		2	4	7	ns
CLKB propagation delay time	Ttdlh		2	4	7	ns
Control signal propagation delay time	Ttctl		2 Tdclk + 3	2 Tdclk + 6	2 Tdclk + 10	ns
Data output propagation delay time	Ttdata		2 Tdclk + 3	2 Tdclk + 6	2 Tdclk + 11	ns

Electrical Characteristics: At an operating voltage of 3.3 V

Operating Ranges at Ta = 0 to +70°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		3.0	3.3	3.6	V
Input voltage	V_{IN}		0		V_{DD}	V
Clock frequency	f_{clk}				30	MHz

DC Characteristics at Ta = 0 to +70°C, V_{SS} = 0 V, V_{DD} = 3.0 to 3.6 V

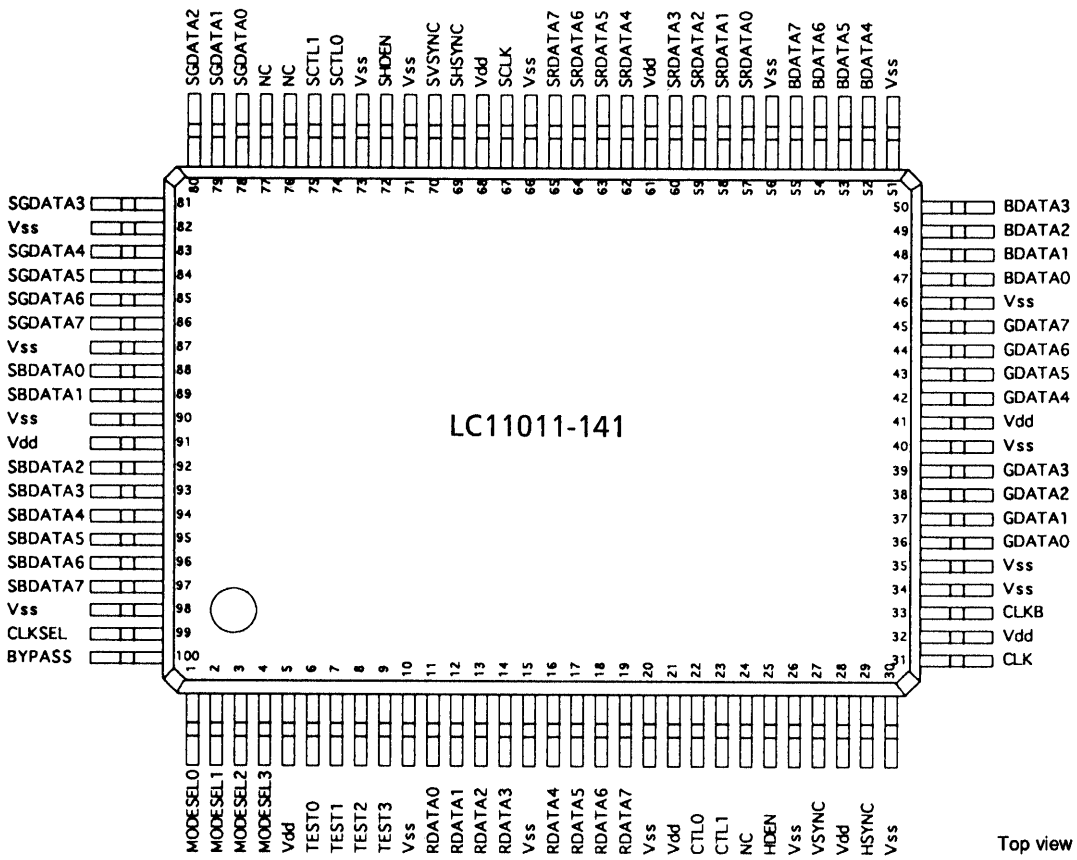
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
High level input voltage	V_{IH}	CMOS level	0.7 V_{DD}			V
Low level input voltage	V_{IL}	CMOS level			0.3 V_{DD}	V
High level output voltage	V_{OH}	I_{OH} (–2 mA)	2.2			V
Low level output voltage	V_{OL}	I_{OL} (2 mA)			0.4	V
Supply current	I_{CC}	*		30	45	mA

Note: * The test conditions are: f_{clk} = 25.175 MHz, V_{DD} = 3.3 V, C_L = 15 pF (measured with VGA timing)

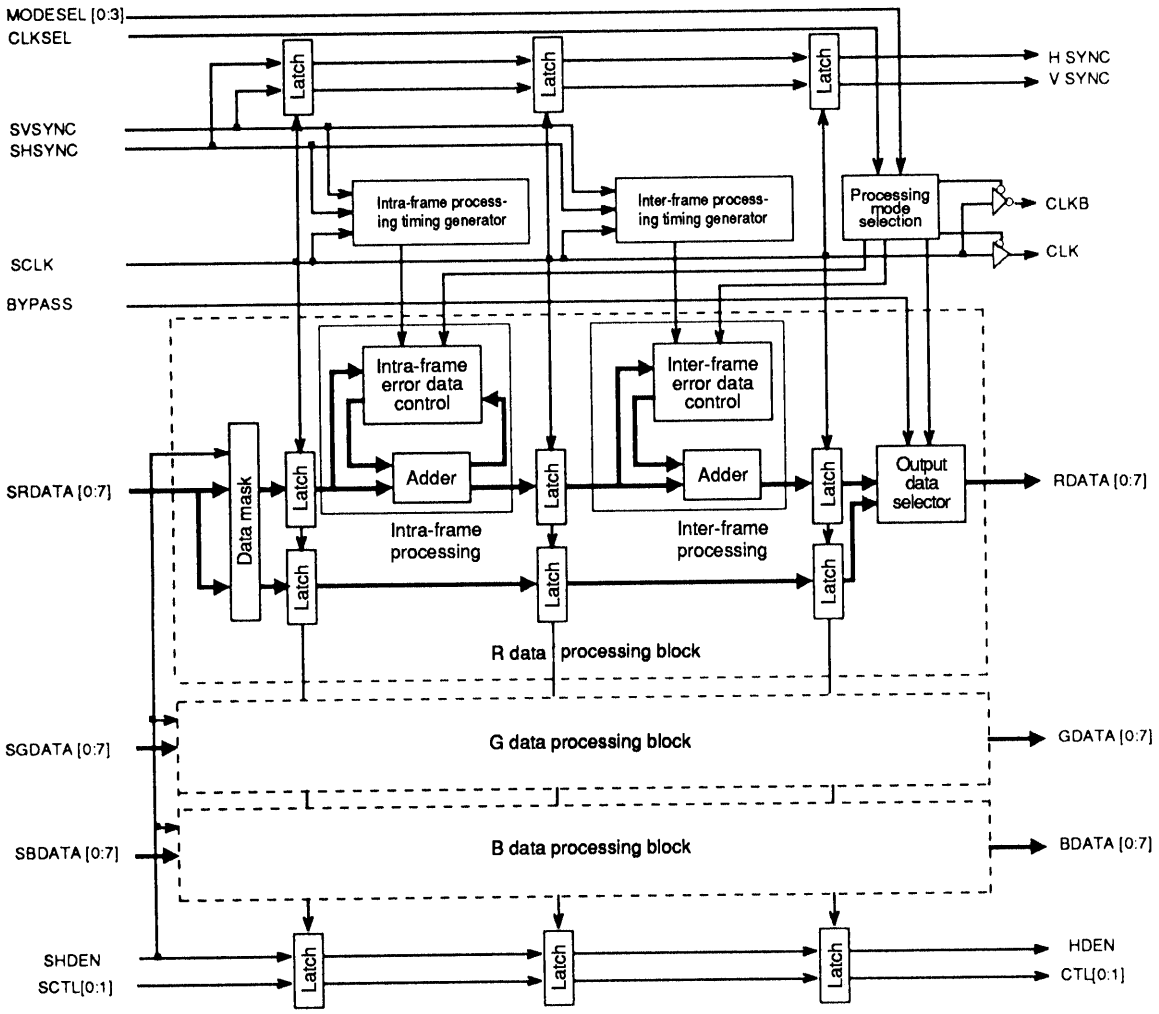
Switching Characteristics at Ta = 0 to +70°C, V_{SS} = 0 V, V_{DD} = 3.0 to 3.6 V, C_L = 15 pF

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Dot clock cycle time	Tdclk		33			ns
Hsync low level pulse width	Thpw		2 Tdclk			ns
Vsync low level pulse width	Tvpw		2 Tdclk			ns
Data setup time	Tdsu		10			ns
Data hold time	Tdhd		10			ns
Control signal setup time	Tcsu		10			ns
Control signal hold time	Tchd		10			ns
CLK propagation delay time	Ttdhh		2	5	12	ns
CLK propagation delay time	Ttdll		2	6	14	ns
CLKB propagation delay time	Ttdhl		2	6	14	ns
CLKB propagation delay time	Ttdlh		2	6	14	ns
Control signal propagation delay time	Ttctl		2 Tdclk + 5	2 Tdclk + 10	2 Tdclk + 22	ns
Data output propagation delay time	Ttdata		2 Tdclk + 5	2 Tdclk + 10	2 Tdclk + 24	ns

Pin Assignment



Block Diagram



Pin Functions

<table>
<tr><th>Symbol</th><th>Pin No.</th><th>I/O</th><th>Function</th></tr>
<tr><td>V_{DD}</td><td>5, 21, 28, 32, 41, 61, 68, 91</td><td>Input</td><td>Power supply (+5 V)</td></tr>
<tr><td>V_{SS}</td><td>10, 15, 20, 26, 30, 34, 35, 40, 46,51, 56, 66, 71, 73, 82, 87, 90, 98</td><td>Input</td><td>GND (0 V)</td></tr>
<tr><td>NC</td><td>24, 76, 77</td><td>—</td><td>Must be left open.</td></tr>
<tr><td>MODESEL0</td><td>1</td><td>Input</td><td rowspan="4">Mode selection signals [0:3] for the gray scale mode.
The setting process for the mode selection lines is described below.
MODESEL0 is the LSB, and MODESEL3 is the MSB.
Note that modes 8, 9, C, D and E are compatible with the LC1001-131 (a product that handles 6-bits of input for each of the RGB signals).

<table>
<tr><th colspan="2">Color scale mode</th><th>0</th><th>1</th><th>2</th><th>3</th><th>4</th><th>5</th><th>6</th><th>7</th><th>8</th><th>9</th><th>A</th><th>B</th><th>C</th><th>D</th><th>E</th><th>F</th></tr>
<tr><td colspan="2">MODESEL0
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<tr><td rowspan="2">Processing</td><td>Intra-frame processing</td><td>Y</td><td>Y</td><td rowspan="2">R</td><td>Y</td><td rowspan="2">R</td><td>Y</td><td>Y</td><td>Y</td><td>Y</td><td>Y</td><td rowspan="2">R</td><td rowspan="2">R</td><td>Y</td><td>Y</td><td>Y</td><td rowspan="2">R</td></tr>
<tr><td>Inter-frame processing</td><td>Y</td><td>Y</td><td>Y</td><td>N</td><td>N</td><td>N</td><td>Y</td><td>Y</td><td>N</td><td>N</td><td>N</td></tr>
<tr><td colspan="2">Number of valid input bits</td><td>8</td><td>8</td><td></td><td>8</td><td></td><td>8</td><td>8</td><td>8</td><td>6</td><td>6</td><td></td><td></td><td>6</td><td>6</td><td>6</td><td></td></tr>
<tr><td colspan="2">Number of output bits</td><td>3</td><td>4</td><td></td><td>6</td><td></td><td>4</td><td>5</td><td>6</td><td>3</td><td>4</td><td></td><td></td><td>3</td><td>4</td><td>5</td><td></td></tr>
</table>
Note: Y = yes, N = no, R = reserved

<table>
<tr><td>Gray scale modes 0, 8 and C</td><td>Operating mode for TFT-LCD modules using 3-bit source drivers.</td></tr>
<tr><td>Gray scale modes 1 and 9</td><td>Operating mode for TFT-LCD modules using 4-bit source drivers.</td></tr>
<tr><td>Gray scale mode 3</td><td>Operating mode for TFT-LCD modules using 6-bit source drivers.</td></tr>
<tr><td>Gray scale modes 5 and D</td><td>Operating mode for TFT-LCD modules that perform FRC or other inter-frame processing.</td></tr>
<tr><td>Gray scale modes 6, 7 and E</td><td>Operating mode for TFT-LCD modules that perform FRC or other inter-frame processing.</td></tr>
</table>
Note: Do not use gray scale modes 0, 1, 3, 8 and 9 with LCD modules that perform FRC or other inter-frame processing.</td></tr>
<tr><td>MODESEL1</td><td>2</td><td>Input</td></tr>
<tr><td>MODESEL2</td><td>3</td><td>Input</td></tr>
<tr><td>MODESEL3</td><td>4</td><td>Input</td></tr>
<tr><td>BYPASS</td><td>100</td><td>Input</td><td>Input bypass pin. When this pin is low, the LC11011-141 performs no gray scale processing, but rather simply passes the input signals through unchanged. When a low level input on this pin is sampled on the rising edge of the clock, the IC will begin the output of unchanged data two clock cycles later.</td></tr>
<tr><td>TEST0</td><td>6</td><td>Input</td><td rowspan="4">Test pins [0:3]; left open in normal operation.</td></tr>
<tr><td>TEST1</td><td>7</td><td>Input</td></tr>
<tr><td>TEST2</td><td>8</td><td>Input</td></tr>
<tr><td>TEST3</td><td>9</td><td>Input</td></tr>
<tr><td>SCLK</td><td>67</td><td>Input</td><td>Display dot clock input. Data is processed according to this clock signal.</td></tr>
<tr><td>SRDATA [0:7]</td><td>57 to 60, 62 to 65</td><td>Input</td><td rowspan="3">Input pins for red, green and blue scale data. SRDATA7, SGDATA7, and SBDATA7 are the MSBs. SRDATA0, SGDATA0, and SBDATA0 are the LSBs.</td></tr>
<tr><td>SGDATA [0:7]</td><td>78 to 81, 83 to 86</td><td>Input</td></tr>
<tr><td>SBDATA [0:7]</td><td>88, 89, 92 to 97</td><td>Input</td></tr>
<tr><td>Shsync</td><td>69</td><td>Input</td><td rowspan="2">Horizontal and vertical synchronization signal inputs. These are the sources for the Hsync and Vsync signals. These are also used to control data processing. These are low level active signals.</td></tr>
<tr><td>Svsync</td><td>70</td><td>Input</td></tr>
<tr><td>SHDEN</td><td>72</td><td>Input</td><td>Horizontal data valid period signal input. Set this pin high during periods when the horizontal data is valid. If this signal is not used, tie it high, and set the input data to zero during the horizontal blanking period.</td></tr>
<tr><td>SCTL0</td><td>74</td><td>Input</td><td rowspan="2">LCD control inputs. Input control signals that must be matched to the data signal timing. These are the sources for the CTL signals. If the CTL [0:1] signals are not used, there is no need to input the SCTL [0:1] signals.</td></tr>
<tr><td>SCTL1</td><td>75</td><td>Input</td></tr>
<tr><td>CLKSEL</td><td>99</td><td>Input</td><td rowspan="3">CLKSEL is the dot clock output selection. It is used to select the output mode of the dot clock signal output pin.
If CLKSEL is low: A signal with the same phase as the SCLK pin is output from the CLK pin.
If CLKSEL is high: A signal with the opposite phase from the SCLK pin is output from the CLKB pin.</td></tr>
<tr><td>CLK</td><td>31</td><td>Output</td></tr>
<tr><td>CLKB</td><td>33</td><td>Output</td></tr>
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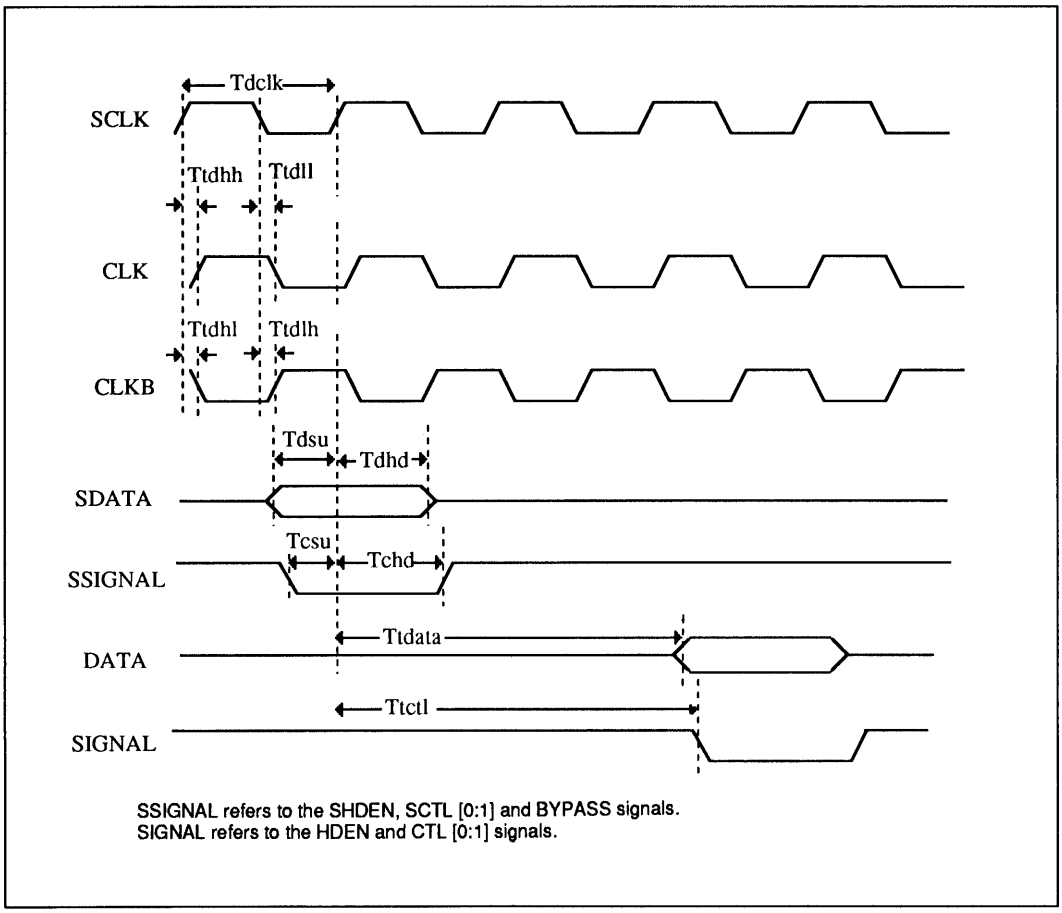
Symbol	Pin No.	I/O	Function
RDATA [0:7]	11 to 14, 16 to 19	Output	Red, green and blue gray scale data output pins. These are delayed by 2 clock cycles with respect to the input data. RDATA7, GDATA7 and BDATA7 are the MSBs. In modes 0, 8, C and F, RDATA5, GDATA5 and BDATA5 are the LSBs. In these modes, RDATA [0:4], GDATA [0:4] and BDATA [0:4] are not used. In modes 1, 5, 9 and D, RDATA4, GDATA4 and BDATA4 are the LSBs. In these modes, RDATA [0:3], GDATA [0:3] and BDATA [0:3] are not used. In modes 6 and E, RDATA3, GDATA3 and BDATA3 are the LSBs. In these modes, RDATA [0:2], GDATA [0:2] and BDATA [0:2] are not used. In modes 3 and 7, RDATA2, GDATA2 and BDATA2 are the LSBs. In these modes, RDATA [0:1], GDATA [0:1] and BDATA [0:1] are not used.
GDATA [0:7]	36 to 39, 42 to 45	Output	
BDATA [0:7]	47 to 50, 52 to 55	Output	
Vsync	27	Output	Horizontal and vertical synchronization signal outputs. To match the data signal timing these are delayed by two clock cycles with respect to their input signals.
Hsync	29	Output	
HDEN	25	Output	Horizontal data valid period signal output
CLT0	22	Output	LCD control signal outputs. To match the data signal timing these are delayed by two clock cycles with respect to the SCTL [0:1] input signals.
CLT1	23	Output	

Timing Chart



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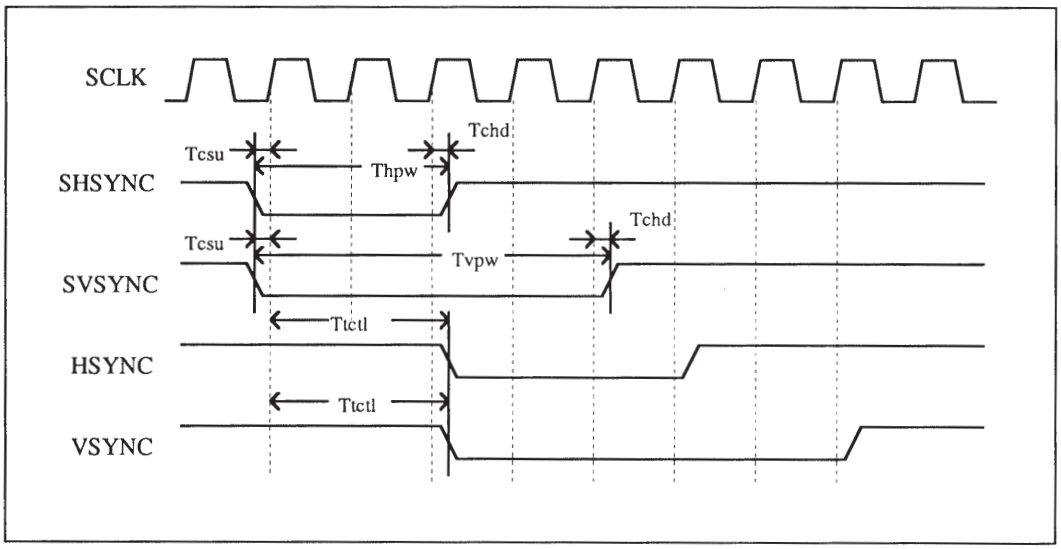

This LSI is an improved version of the ALC1009-141.

Usage Note

Since this LSI performs spatial modulation using an error diffusion algorithm, patterns that differ from the original images may be displayed for certain display pattern and gray-scale mode combinations.