Ordering number: EN ※ 5076A

CMOS LSI

SANYO

No. ※ 5076A

LC11012-141

Computer Image Signal Processing Full-Color Gray-Scale Processor

Preliminary

Overview

The LC11012-141 is a pseudo gray-scale processor for TFT-LCD panel displays. It allows TFT-LCD panels with 3- or 4-bit input digital drivers to display the equivalent of 16.7 million colors.

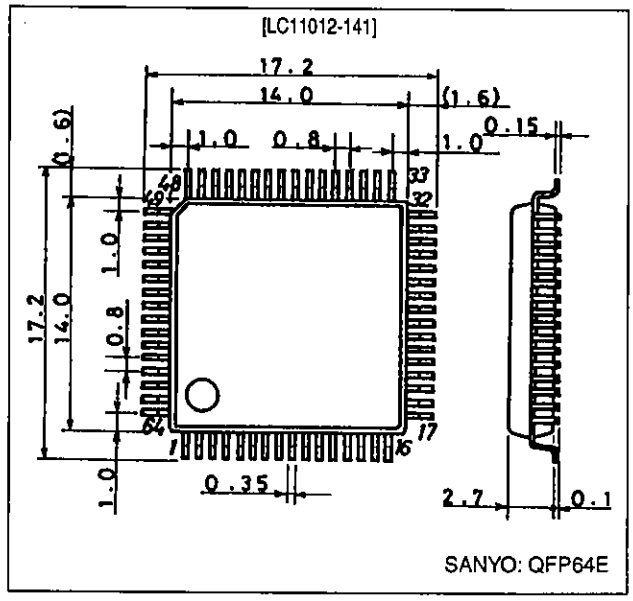
Features

- Handles 8 bits of input data (256-level gray scale data) for each of the RGB colors
- Realizes reduced resolution loss (as compared to dithering techniques) by using intra-frame and inter-frame error diffusion processing
- Incorporates a new full-coloration algorithm, formerly best done using computers
- Operating mode selection of outputs for 3- or 4-bit drivers
- Supports both 5V and low-voltage 3.3V operation
- Operates with arbitrary clock frequencies up to 40MHz (5V supply) and 30MHz (3.3V supply)
- Can operate independently of the number of displayed pixels since internal operation is controlled by the horizontal and vertical synchronization signals.
- Power-save function to stop the internal operation processing circuits, and output the clock, sync signals and control signals

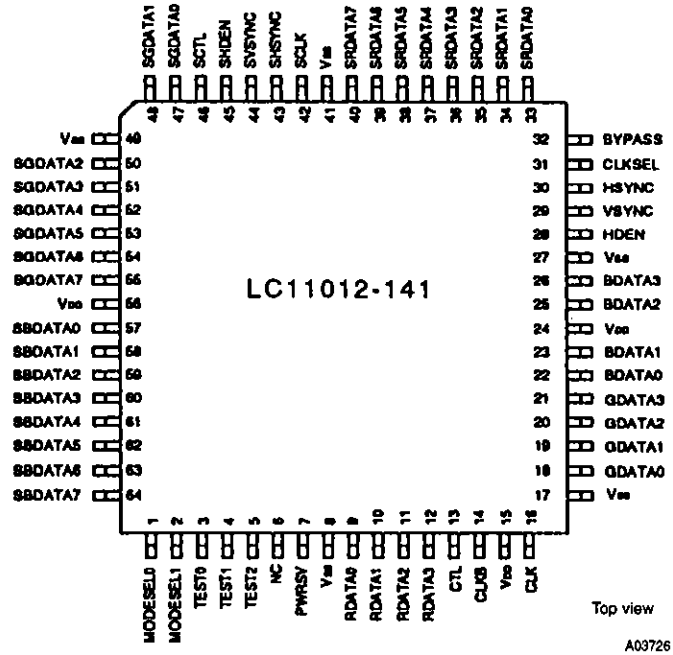
Package Dimensions

unit: mm

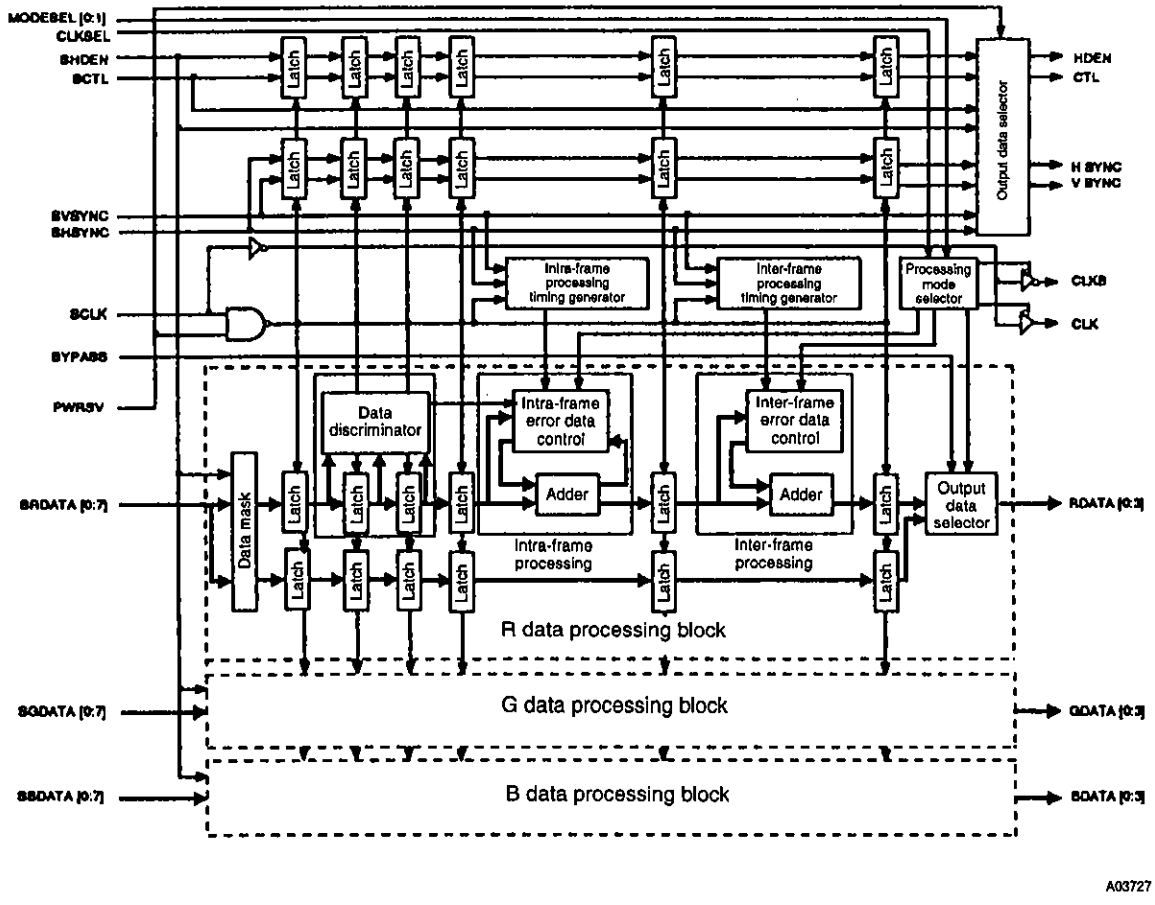
3159-QFP64E



Pin Assignment



Block Diagram



Pin Functions

<table>
<tr><th>Symbol</th><th>Pin No.</th><th>I/O[1]</th><th>Function</th></tr>
<tr><td>V_{DD}</td><td>15, 24, 56</td><td></td><td>Power supply (+5V)</td></tr>
<tr><td>V_{SS}</td><td>8, 17, 27, 41, 49</td><td></td><td>Ground (0V)</td></tr>
<tr><td>NC</td><td>6</td><td></td><td>Must be left open.</td></tr>
<tr><td>MODESEL [0:1]</td><td>1, 2</td><td>I</td><td>Mode selection signals [0:1] for the gray-scale mode.
The setting process for the mode selection lines is described below.
MODESEL0 is the LSB and MODESEL1 is the MSB.
Note that the mode number (0 to 3) and the gray-scale processing differ from existing devices.
<table>
<tr><th colspan="2">Gray-scale mode</th><th>0</th><th>1</th><th>2</th><th>3</th></tr>
<tr><td colspan="2">MODESEL0</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td colspan="2">MODESEL1</td><td>L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td rowspan="2">Processing</td><td>Intra-frame processing</td><td>Yes</td><td>Yes</td><td>Yes</td><td rowspan="2">Reserved</td></tr>
<tr><td>Inter-frame processing</td><td>Yes</td><td>Yes</td><td>No</td></tr>
<tr><td colspan="2">Number of valid input bits</td><td>8</td><td>8</td><td>8</td><td></td></tr>
<tr><td colspan="2">Number of output bits</td><td>3</td><td>4</td><td>4</td><td></td></tr>
</table>
<table>
<tr><th>Gray-scale mode[1]</th><th>LCD module</th></tr>
<tr><td>0</td><td>Operating mode for TFT LCD modules with 3-bit source driver</td></tr>
<tr><td>1</td><td>Operating mode for TFT LCD modules with 4-bit source driver</td></tr>
<tr><td>2</td><td>Operating mode for TFT LCD modules with 3-bit source driver that perform FRC or other inter-frame processing</td></tr>
</table>
1. Do not use gray-scale modes 0 and 1 with TFT LCD modules that perform FRC or other inter-frame processing.</td></tr>
<tr><td>BYPASS</td><td>32</td><td>I</td><td>Gray-scale processing bypass pin. When a low-level input on this pin is sampled on the falling edge of the clock, the IC will begin the output of unchanged data five clock cycles later. Data is output via the internal latch circuit. Data is not output, however, when the SCLK clock signal is not input.</td></tr>
<tr><td>TEST [0:2]</td><td>3, 4, 5</td><td>I</td><td>Test pins [0:2]; left open for normal operation</td></tr>
<tr><td>SCLK</td><td>42</td><td>I</td><td>Display dot clock signal input. Data is processed according to this clock signal.</td></tr>
<tr><td>SRDATA [0:7]</td><td>33 to 40</td><td>I</td><td rowspan="3">Input pins for red, green and blue gray-scale data. SRDATA7, SGDATA7 and SBDATA7 are the MSBs. SRDATA0, SGDATA0 and SBDATA are the LSBs.</td></tr>
<tr><td>SGDATA [0:7]</td><td>47, 48, 50 to 55</td><td>I</td></tr>
<tr><td>SBDATA [0:7]</td><td>57 to 64</td><td>I</td></tr>
<tr><td>SHSYNC</td><td>43</td><td>I</td><td rowspan="2">Horizontal and vertical synchronization signal inputs. These are the sources for the HSYNC and VSYNC signals. They are also used to control data processing. Active-low signals.</td></tr>
<tr><td>SVSYNC</td><td>44</td><td>I</td></tr>
<tr><td>SHDEN</td><td>45</td><td>I</td><td>Horizontal data valid-period signal input. Set this pin high during periods when the horizontal data is valid. If this signal is not used, tie it high and set the input data to 0 during the horizontal blanking period.</td></tr>
<tr><td>SCTL</td><td>46</td><td>I</td><td>LCD control signal input. Input control signal that must be matched to the data signal timing. This is the source for the CTL signal. If the CTL signal is not used, there is no need to input the SCTL signal.</td></tr>
<tr><td>CLKSEL</td><td>31</td><td>I</td><td rowspan="3">CLKSEL is the dot clock output select pin. It is used to select the output mode of the dot clock signal output pin.
If CLKSEL is low: A signal with the opposite phase from the SCLK pin is output from the CLK pin.
If CLKSEL is high: A signal with the same phase as the SCLK pin is output from the CLKB pin.</td></tr>
<tr><td>CLK</td><td>16</td><td>O</td></tr>
<tr><td>CLKB</td><td>14</td><td>O</td></tr>
<tr><td>RDATA [0:3]</td><td>9 to 12</td><td>O</td><td rowspan="3">Red, green and blue gray-scale data output pins. These are delayed by five clock cycles with respect to the input data.
RDATA3, GDATA3 and BDATA3 are the MSBs.
In mode 0: RDATA1, GDATA1 and BDATA1 are the LSBs. In this mode RDATA0, GDATA0 and BDATA0 are set low.
In modes 1 and 2: RDATA0, GDATA0 and BDATA0 are the LSBs.</td></tr>
<tr><td>GDATA [0:3]</td><td>18 to 21</td><td>O</td></tr>
<tr><td>BDATA [0:3]</td><td>22, 23, 25, 26</td><td>O</td></tr>
<tr><td>VSYNC</td><td>29</td><td>O</td><td rowspan="2">Vertical and horizontal synchronization signal outputs. To match the data signal timing, these outputs are delayed by five clock cycles with respect to their input signals. When PWRSV is low, these signals are output without being latched internally.</td></tr>
<tr><td>HSYNC</td><td>30</td><td>O</td></tr>
</table>

Symbol	Pin No.	I/O[1]	Function
HDEN	28	O	Horizontal data valid-period signal output.To match the data signal timing, this output is delayed by five clock cycles with respect to the SHDEN input signal. When PWRSV is low, this signal is output without being latched internally.
CTL	13	O	LCD control signal output. To match the data signal timing, this output is delayed by five clock cycles with respect to the SCTL input signal. When PWRSV is low, this signal is output without being latched internally.
PWRSV	7	I	Power-save control input. When this input goes low, the internal clock stops and the LSI enters power-save mode. Output data are held high. VSYNC, HSYNC, HDEN and CTL control signals, and either CLK or CLKB are output without being latched internally. Tie high or leave open for normal operation.

1. I = input, O = output

Specifications (Electrical characteristics values are provisional only and are subject to change.)

Absolute Maximum Ratings at V_{SS} = 0V

Parameter	Symbol	Ratings	Unit
Maximum supply voltage	V_{DD} max	–0.3 to +7.0	V
Input/output voltage	V_I, V_O	–0.3 to V_{DD} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–40 to +125	°C

Electrical Characteristics at an operating voltage of 5.0V

Allowable Operating Ranges at Ta = 0 to +70°C

Parameter	Symbol	min	typ	max	Unit
Supply voltage	V_{DD}	4.5	5.0	5.5	V
Input voltage	V_{IN}	0	–	V_{DD}	V
Clock frequency	f_{clk}	–	–	40	MHz

DC Characteristics at Ta = 0 to +70°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V

Parameter	Symbol	Conditions	min	typ	max	Unit
High-level input voltage	V_{IH}	TTL compatible	2.2	–	–	V
Low-level input voltage	V_{IL}	TTL compatible	–	–	0.8	V
High-level output voltage	V_{OH}	I_{OH} = –2mA	2.4	–	–	V
Low-level output voltage	V_{OL}	I_{OL} = 2mA	–	–	0.4	V
Current dissipation (1)	I_{CC}	Note 1	–	45	70	mA
Current dissipation (2)	I_{CPS}	Note 2	–	9	12	mA
Current dissipation (3)	I_{CST}	Note 3	–	–	200	µA

Notes. 1. f_{clk} = 25.175MHz, V_{DD} = 5.0V, C_L = 15pF, (measured with VGA timing)
2. PWRSV = low, f_{clk} = 25.175MHz, V_{DD} = 5.0V, C_L =15pF (control signals)
3. V_{DD} = 5.0V, all output pins = open, all input pins = V_{DD} or V_{SS}

Switching Characteristics at Ta = 0 to +70°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V, C_L = 15pF

Parameter	Symbol	min	typ	max	Unit
Dot clock cycle time	Tdclk	25	–	–	ns
Hsync low-level pulse width	Thpw	2Tdclk	–	–	ns
Vsync low-level pulse width	Tvpw	2Tdclk	–	–	ns
Data setup time	Tdsu	5	–	–	ns
Data hold time	Tdhd	5	–	–	ns
Control signal setup time	Tcsu	5	–	–	ns

Parameter	Symbol	min	typ	max	Unit
Control signal hold time	Tchd	5	–	–	ns
CLK propagation delay time	Ttdhh	4	6	12	ns
CLK propagation delay time	Ttdll	4	6	13	ns
CLKB propagation delay time	Ttdhl	4	7	13	ns
CLKB propagation delay time	Ttdlh	4	6	12	ns
Control signal propagation delay time	Ttctl	5Tdclk + 4	5Tdclk + 7	5Tdclk + 13	ns
Data output propagation delay time	Ttdata	5Tdclk + 4	5Tdclk + 7	5Tdclk + 14	ns

Electrical Characteristics at an operating voltage of 3.3V

Allowable Operating Ranges at Ta = 0 to +70°C

Parameter	Symbol	min	typ	max	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Input voltage	V_{IN}	0	–	V_{DD}	V
Clock frequency	f_{clk}	–	–	30	MHz

DC Characteristics at Ta = 0 to +70°C, V_{DD} = 3.0 to 3.6V, V_{SS} = 0V

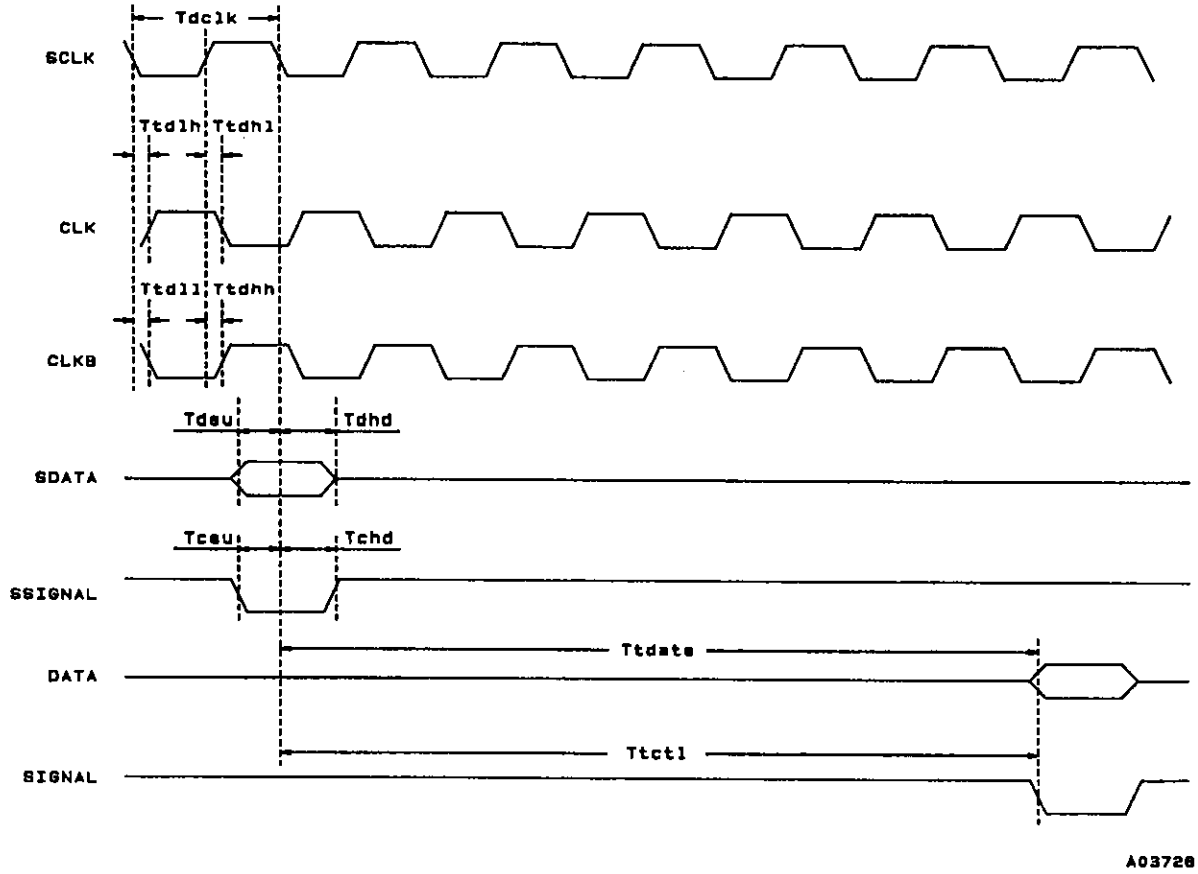
Parameter	Symbol	Conditions	min	typ	max	Unit
High-level input voltage	V_{IH}		2.0	–	–	V
Low-level input voltage	V_{IL}		–	–	0.5	V
High-level output voltage	V_{OH}	I_{OH} = –1mA	2.4	–	–	V
Low-level output voltage	V_{OL}	I_{OL} = 1mA	–	–	0.4	V
Current dissipation (1)	I_{CC}	Note 1	–	30	45	mA
Current dissipation (2)	I_{CPS}	Note 2	–	5	8	mA
Current dissipation (3)	I_{CST}	Note 3	–	–	160	µA

Notes. 1. f_{clk} = 25.175MHz, V_{DD} = 3.3V, C_L = 15pF, (measured with VGA timing)
2. PWRSV = low, f_{clk} = 25.175MHz, V_{DD} = 3.3V, C_L =15pF (control signals)
3. V_{DD} = 3.3V, all output pins = open, all input pins = V_{DD} or V_{SS}

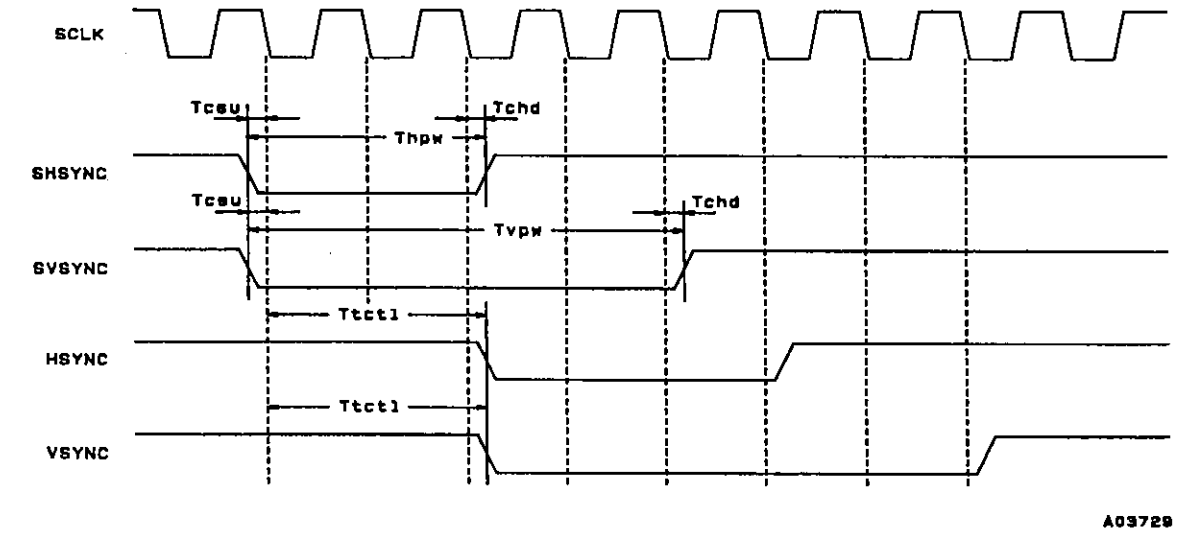
Switching Characteristics at Ta = 0 to +70°C, V_{DD} = 3.0 to 3.6V, V_{SS} = 0V, C_L = 15pF

Parameter	Symbol	min	typ	max	Unit
Dot clock cycle time	Tdclk	33	–	–	ns
Hsync low-level pulse width	Thpw	2Tdclk	–	–	ns
Vsync low-level pulse width	Tvpw	2Tdclk	–	–	ns
Data setup time	Tdsu	10	–	–	ns
Data hold time	Tdhd	10	–	–	ns
Control signal setup time	Tcsu	10	–	–	ns
Control signal hold time	Tchd	10	–	–	ns
CLK propagation delay time	Ttdhh	5	10	23	ns
CLK propagation delay time	Ttdll	5	10	23	ns
CLKB propagation delay time	Ttdhl	5	11	25	ns
CLKB propagation delay time	Ttdlh	5	10	22	ns
Control signal propagation delay time	Ttctl	5Tdclk + 5	5Tdclk + 10	5Tdclk + 25	ns
Data output propagation delay time	Ttdata	5Tdclk + 5	5Tdclk + 11	5Tdclk + 27	ns

Timing Diagrams



SSIGNAL refers to the SHDEN, SCTL, BYPASS and PWRSV signals.
SIGNAL refers to the HDEN and CTL signals.



Usage Note

Since this LSI performs spatial modulation using an error diffusion algorithm, patterns that differ from the original images may be displayed for certain display pattern and gray-scale mode combinations.