Ordering number : EN5980

Monolithic Linear IC

LA9605W

MD Player RF and Matrix Signal-Processing IC

Overview

The LA9605W integrates MiniDisk playback functions, including servo error signal generation, RF signal processing, and wobble signal binarization output on a single chip. The LA9605W, when combined with an LC89640, can implement a complete MD player system.

Features

- Allows the servo error signal level to be set to an arbitrary level using a VCA circuit.
- Few peripheral components required.
- Ultraminiature package

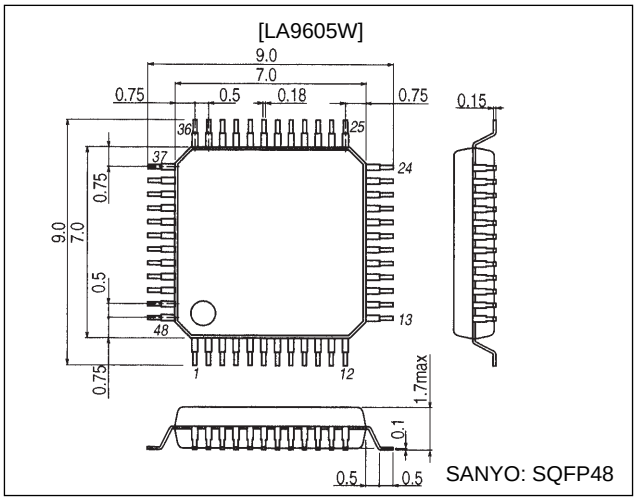
Functions

- Servo signal I-V conversion amplifier
- Pit/groove switching RF amplifier
- RF equalizer amplifier
- Servo signal VCA
- APC circuit
- Focus error amplifier
- Tracking error amplifier
- HFL circuit
- Defect detection circuit
- ADIP amplifier
- Pre-pit circuit (pit/groove discrimination circuit)
- ADIPCR

Package Dimensions

unit: mm

3163A-SQFP48



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Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		7	V
Allowable power dissipation	Pd max	When mounted on a 114.3 × 76.1 × 1.6-mm single-sided glass-epoxy printed circuit board. Ta ≤ 75 °C	350	mW
Operating temperature	Topr		–25 to +75	°C
Storage temperature	Tstg		–40 to +150	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		5	V
Operating supply voltage range	V_{CC} op		2.7 to 5.5	V

Electrical Characteristics at Ta = 25°C, V_{CC} = 5 V

Parameter		Symbol	Conditions	Ratings			Unit
				min	typ	max	
Current drain		I_{CC}		18	32	46	mA
[RF AMP GROVE]							
Gain		$VG_{RFMG}1$	EQ_O/I : J = V_C	27	30	33	dB
[RF AMP MO.PIT]							
Offset		$V_{OS\ RFMP}1$	RF_O1 : I = J = V_C	V_C – 245	V_C – 185	V_C – 125	mV
Gain		$VG_{RFMP}1$	EQ_O/I : I = J	15	18	21	dB
[RF AMP AL]							
Offset		$V_{OS\ RFAP}1$	RF_O1 : I = J = V_C	V_C – 152	V_C – 92	V_C – 32	mV
Gain		$VG_{RFAP}1$	EQ_O/I : I = J = V_C	5.5	8.5	11.5	dB
[RF AMP]							
Output level	H	$V_{ORFH}1$	EQ_O : RFI1 = V_C + 1 V	3.5	4.1		V
	L	$V_{ORFL}1$	EQ_O : RFI1 = V_C – 1 V		0.9	1.5	V
[ABCD GR]							
Gain		$VG_{ABG}1$	ABCD/A (10 kHz) : A = B = C = D, SGC = 0.78 V	17.5	20.5	23.5	dB
Output level	H	$V_{OABGH}2$	ABCD : A = B = C = D = V_C – 400 mV, SGC = 0.78 V	4.5	4.9		V
	L	$V_{OABGL}2$	ABCD : A = B = C = D = V_C + 400 mV, SGC = 0.78 V		0.1	0.5	V
[ABCD PIT]							
Gain		$VG_{ABP}1$	ABCD/A (10 kHz) : A = B = C = D, SGC = 0.3 V	10.6	13.6	16.6	dB
Frequency characteristics		$V\Delta G_{ABP}1$	ABCD/A (10 kHz) – ABCD/A (35 kHz), SGC = 0.3 V	3.9	6.9	9.9	dB
[FOCS]							
Output level	H	$V_{OFOH}1$	FE : B = D = V_C + 825 mV, A = C = V_C, SGC = 0.3 V	4.5	4.9		V
	L	$V_{OFOL}1$	FE : B = D = V_C – 825 mV, A = C = V_C, SGC = 0.3 V		0.1	0.5	V
Gain		$V_{GFO}1$	FE/A (5 kHz) : A = –B = C = –D, SGC = 0.3 V	13.9	16.9	19.9	dB
Frequency characteristics		$V\Delta_{GFO}1$	FE/A (5 kHz) – FE/A (26 kHz) : A = –B = C = –D, SGC = 0.3 V	0.4	3.4	6.4	dB
[TE GR]							
Output level	H	$V_{OTEGH}1$	TE : F = V_C + 200 mV, E = V_C, SGC = 0.78 V	4.5	4.9		V
	L	$V_{OTEGL}1$	TE : F = V_C – 200 mV, E = V_C, SGC = 0.78 V		0.1	0.5	V
Gain		$VG_{TEG}1$	TE/E (5 kHz) : E = –F, SGC = 0.78 V	31.4	34.4	37.4	dB
Frequency characteristics		$V\Delta G_{TEG}1$	TE/E (5 kHz) – TE/E (38 kHz) : E = –F, SGC = 0.78 V	1.8	4.8	8.8	dB
[TE PIT]							
Gain		$VG_{TEP}1$	TE/E (5 kHz) : E = –F, SGC = 0.3 V	25.2	28.2	31.2	dB
Frequency characteristics		$V\Delta G_{TEP}1$	TE/E (5 kHz) – TE/E (38 kHz) : E = –F, SGC = 0.3 V	1.8	4.8	8.8	dB
[ADIP]							
Output level	H	$V_{OADH}1$	CAD : A = D = V_C + 0.4 V, B = C = V_C	1.4	1.7	2.0	V
	L	$V_{OADL}1$	CAD : A = D = V_C – 0.4 V, B = C = V_C	3.1	3.3	3.6	V

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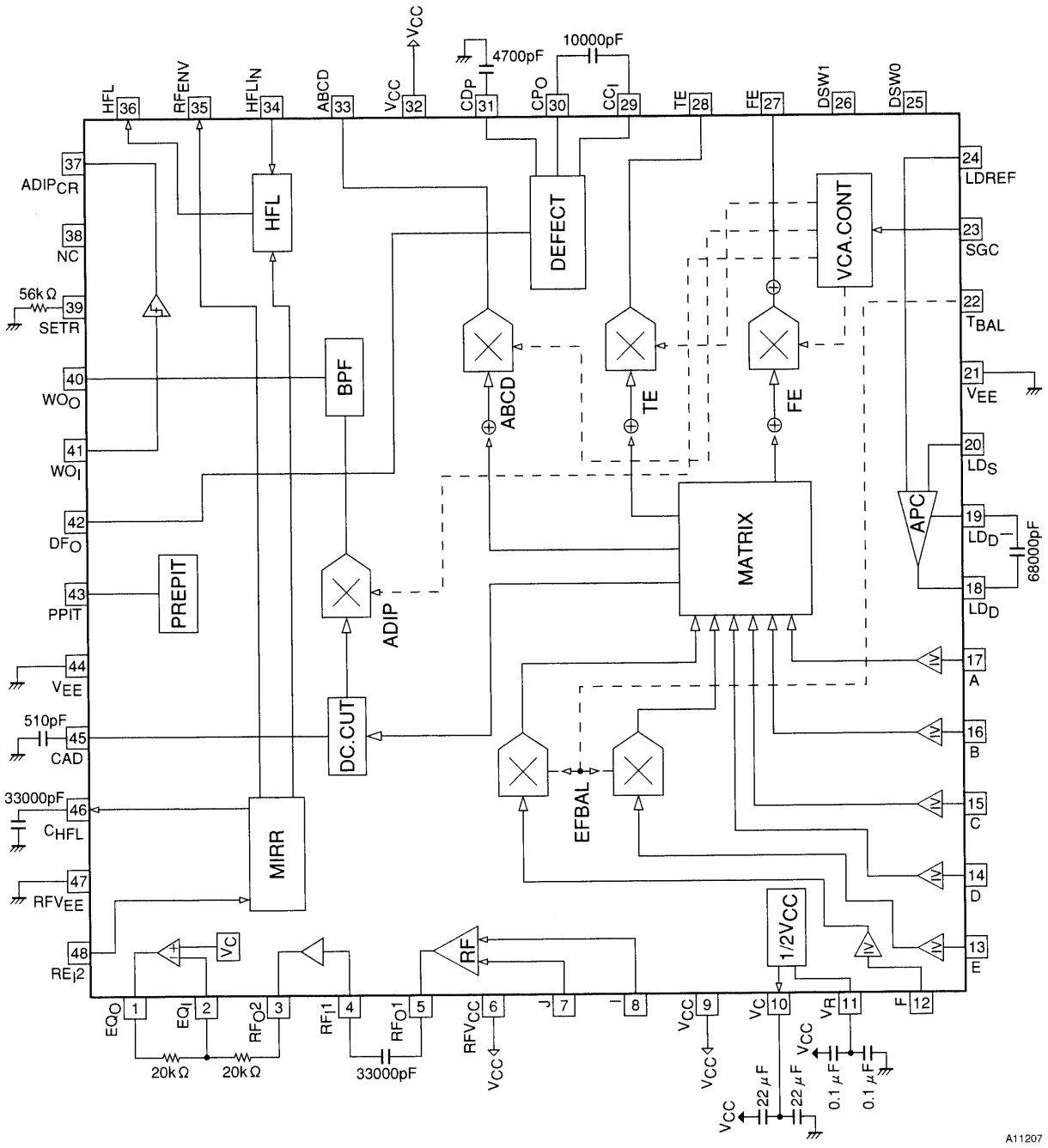
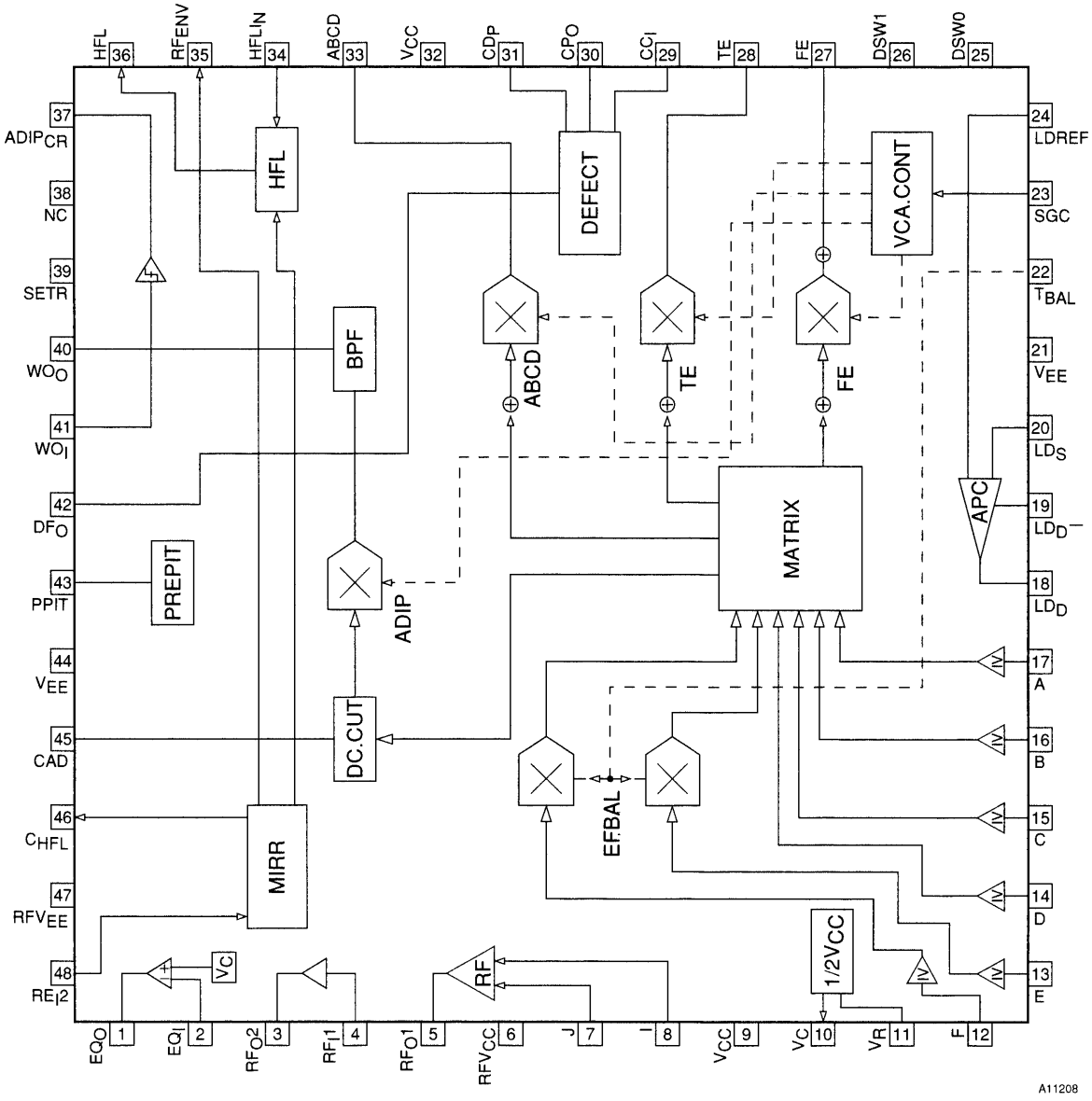
Parameter		Symbol	Conditions	Ratings			Unit
				min	typ	max	
[APC LDON]							
Output level	H	$V_{OLH}1$	LD_D : LD_{REF} = 0 V, LD_S = 1 V	3.7	4.2	4.7	V
	L	$V_{O\ LL}1$	LD_D : LD_{REF} = 1 V, LD_S = 0 V	0.3	0.8	1.3	V
[APC LDOFF]							
Off voltage		$V_{OLOF}1$	LD_D : LD_{REF} = 1 V, LD_S = 0 V	3.7	4.2	4.7	V
[HFL]							
Output level	H	$V_{OHFLH}1$	HFL : HFL_{IN} = V_C – 0.1 V	4.6	4.8		V
	L	$V_{OHFLL}1$	HFL : HFL_{IN} = V_C		0.2	0.4	V
[DEFCT]							
Output level	H	$V_{ODEFH}1$	DFO : CC_I = 1.5 V	4.6	4.9		V
	L	$V_{ODEFL}1$	DFO : CC_I = OPEN, A = B = C = D = V_C – 200 mV		0.1	0.4	V
[VC reference voltage]							
		VO_{SC}	V_C :	2.35	2.5	2.65	V
		VO_{CLSO}	V_C : V_C – 1 mA	2.35	2.5	2.65	V
		VO_{CLSI}	V_C : V_C + 1 mA	2.35	2.5	2.65	V
[PREPIT MO]							
High-level output voltage		$VO_{PPH}1$	PPIT : I = J = 200 kHz (95 mVp-p + V_C + 0.125 V)	4.6	4.8		V
Low-level output voltage		$VO_{PPL}1$	PPIT : I = J = 30 kHz (95 mVp-p + V_C + 0.125 V)		0.2	0.4	V
High/low level switching time		DTPP1	PPIT : I = J = 200 kHz to 30 kHz (95 mVp-p + V_C + 0.125 V)	70	150	230	µs
[BPF]							
Gain		$VG_{BF}1$	$WO_{O/A}$ (22.05 kHz) : A = –B = –C = D, SGC = 0.3 V	23.8	26.8	29.8	dB
Filter characteristics		$VG_{BF}2$	VG_{BF1}/VG_{BF2} : (16 kHz), SGC = 0.3 V	0.8	4.8	9.8	dB
		$VG_{BF}3$	VG_{BF1}/VG_{BF3} : (30 kHz), SGC = 0.3 V	0.4	4.4	9.4	dB
[I – V]							
IV voltage A		ΔV_{RA}	A : V (–1 µA) – V (–2 µA)	70	100	130	mV
IV voltage B		ΔV_{RB}	B : V (–1 µA) – V (–2 µA)	70	100	130	mV
IV voltage C		ΔV_{RC}	C : V (–1 µA) – V (–2 µA)	70	100	130	mV
IV voltage D		ΔV_{RD}	D : V (–1 µA) – V (–2 µA)	70	100	130	mV
IV voltage E		ΔV_{RE}	E : V (–1 µA) – V (–2 µA)	70	100	130	mV
IV voltage F		ΔV_{RF}	F : V (–1 µA) – V (–2 µA)	70	100	130	mV
Ta = 25°C, V_{CC} = 2.7 V							
[FOCS]							
Offset		$V_{OSFO}1$	FE : A = B = C = D = OPEN, SGC = 0.78 V	–300	0	+300	mV
[COMP]							
Offset		$V_{OSCO}1$	WO_I : WO_I = OPEN	–15	0	+15	mV

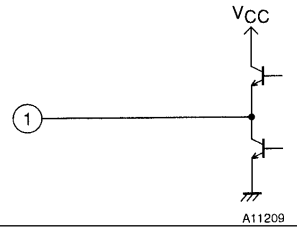
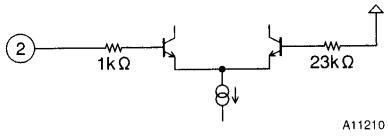
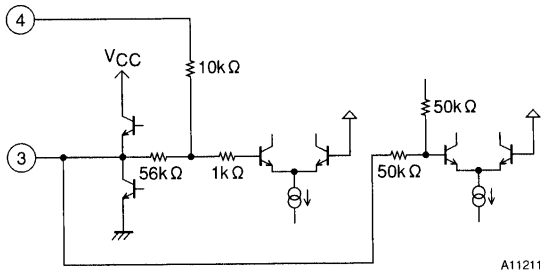
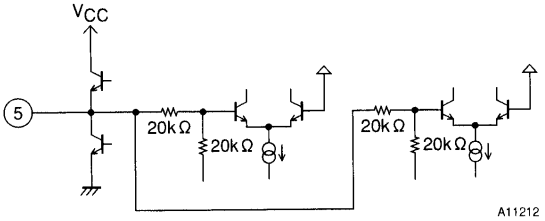
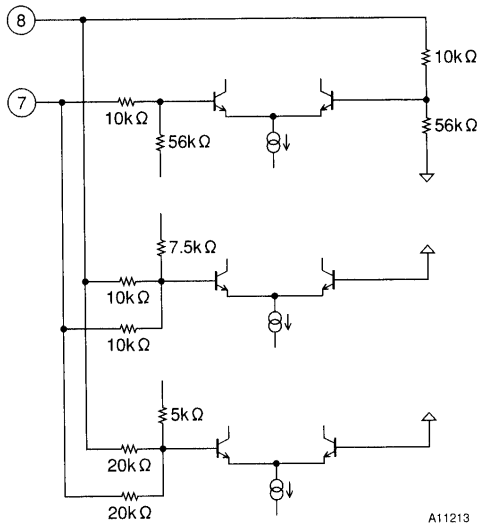
Test Circuit



Block Diagram and Pin Assignment



Pin Functions

Pin No.	Pin	I/O	Function	Equivalent circuit
1	EQ_O	O	RF equalizer output	
2	EQ_I	I	RF equalizer input	
3	RF_O2	O	RF output	
4	RF_I1	I	RF AC coupled input	
5	RF_O1	O	RF AC coupled output	
6	RFV_{CC}	P	RF block power supply	
7	J	I	I/V converted RF signal input	
8	I		I/V converted RF signal input	

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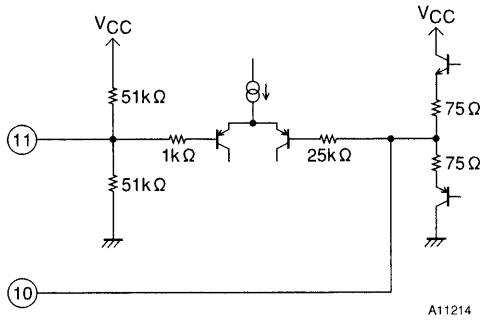
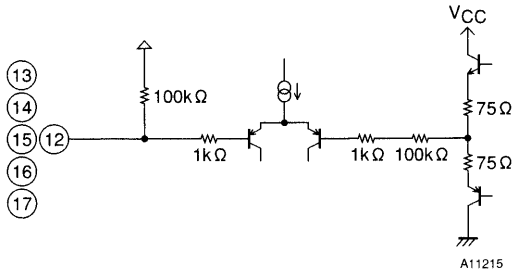
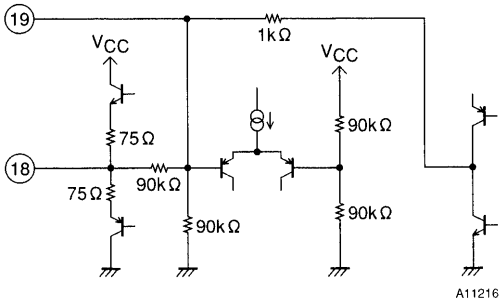
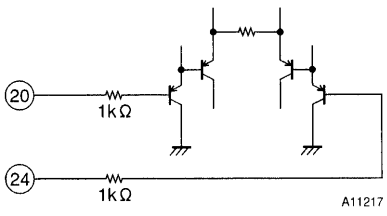
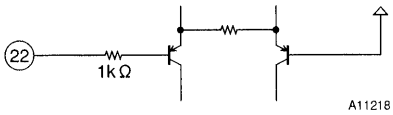
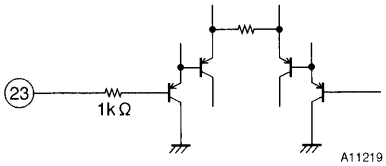
Pin No.	Pin	I/O	Function	Equivalent circuit
9	V_{CC}	P	Matrix block power supply	
10	V_C	O	1/2 V_{CC} output (reference voltage)	
11	V_R	I	1/2 V_{CC} input	
12 13	F E	I	Side beam signal inputs	
14 15 16 17	D C B A		Main beam signal inputs	
18	LD_D	O	APC output	
19	LD_D–	I	APC phase compensation capacitor connection	
20	LD_S	I	I/V converted laser optical intensity input	
24	LD_{REF}		Laser power setting input	
21	V_{EE}	P	Matrix block ground	
22	T_{BAL}	I	Tracking error signal balance adjustment voltage input	
23	SGC		V_{CA} gain control voltage input (ground reference)	

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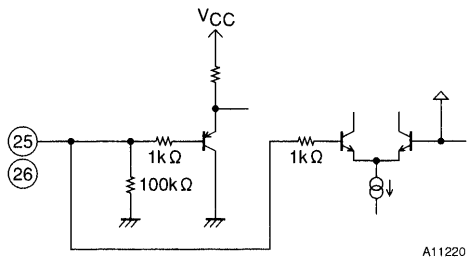
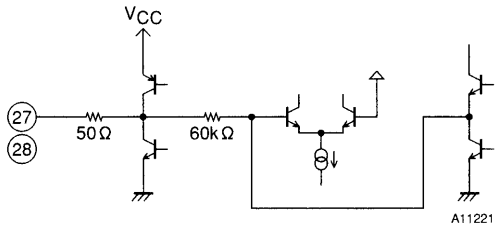
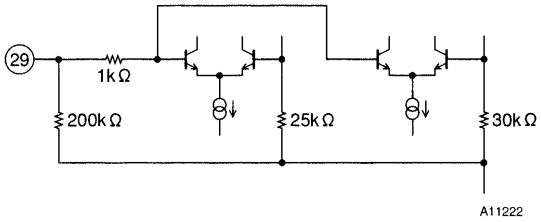
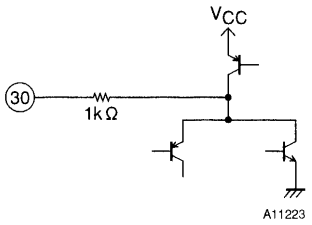
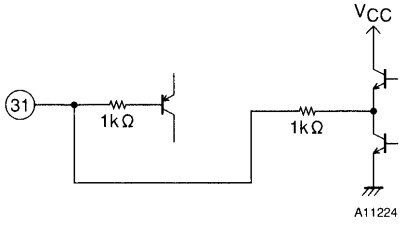
Pin No.	Pin	I/O	Function	Equivalent circuit
25	DSW0	I	Disc mode switching signal input, laser off input High: Low reflectance disc Low: High reflectance disc If both DSW0 and DSW1 are low, the laser is off.	
26	DSW1		Disc mode switching signal input, laser off input High: Tracking is over a pit Low: Tracking is over a groove If both DSW0 and DSW1 are low, the laser is off.	
27	FE	O	Focus error signal output	
28	TE		Tracking error signal output	
29	CC_I	I	Defect peak hold signal AC coupled input	
30	CP_O	O	Defect peak hold signal output	
31	C_{DP}	O	Defect peak hold capacitor connection	
32	V_{CC}	P	ADIP block power supply	

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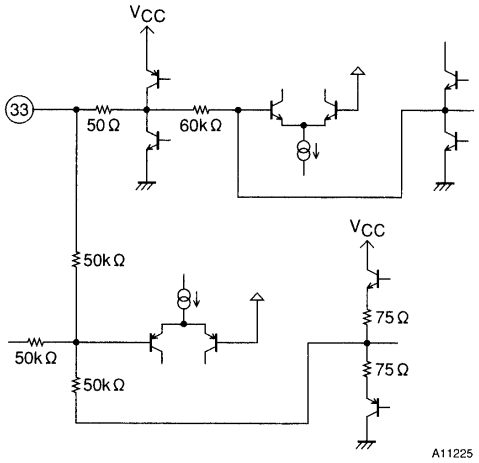
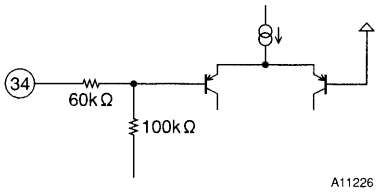
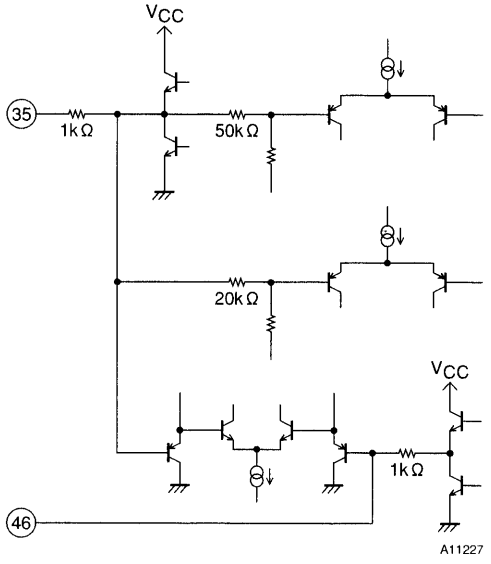
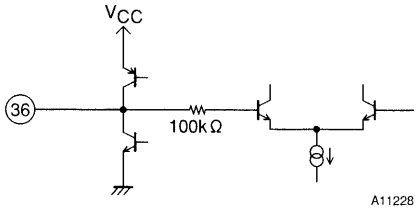
Pin No.	Pin	I/O	Function	Equivalent circuit
33	ABCD	O	Main beam optical intensity signal output	
34	HFL_{IN}	I	HFL detection optical intensity signal AC coupled input used in groove mode	
35	RF_{ENV}	O	RF envelope signal output	
46	C_{HFL}		Mirror peak hold capacitor connection	
36	HFL	O	HFL signal (tracking on/off signal) output	

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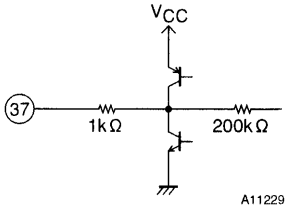
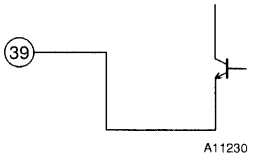
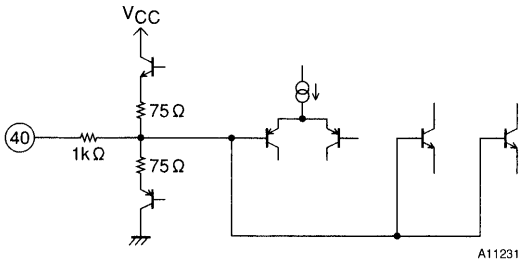
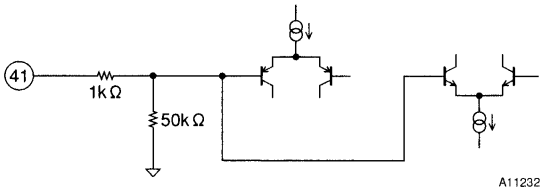
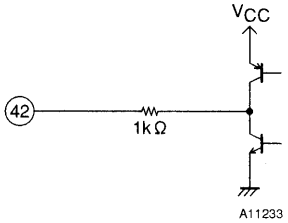
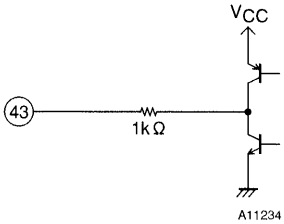
Pin No.	Pin	I/O	Function	Equivalent circuit
37	$ADIP_{CR}$	O	ADIP carrier output	
38	NC	—	No connection	
39	SETR	I	Bandpass filter fo setting	
40	WO_O	O	Wobble signal output	
41	WO_I	I	Wobble signal AC coupled input	
42	DF_O	O	Defect detection signal output	
43	PPIT	O	Pit/groove	
44	V_{EE}	P	ADIP block ground	

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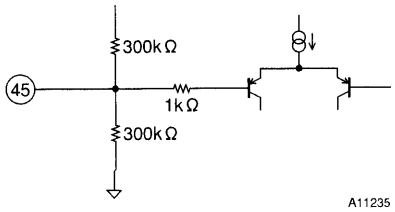
Pin No.	Pin	I/O	Function	Equivalent circuit
45	CAD	—	Wobble DC cut capacitor connection	
47	RFV_{EE}	P	RF block ground	
48	RF_I2	I	RF signal input